

DISSERTATION

Miniaturization Problems in CMOS Technology: Investigation of Doping Profiles and Reliability

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Kurzfassung

Die Leistungsfähigkeit eines MOS-Transistors wird sowohl durch die Kanallänge als auch durch die Transporteigenschaften des Kanalmaterials bestimmt. Um durch Bauelementskalierung auch weiterhin einen entsprechend großen Leistungsgewinn erzielen zu können, werden neuartige Materialien mit einer höheren Beweglichkeit benötigt als etwa mit herstellungsbedingt verspanntem Silizium erzielt werden kann. Stickstoff wird in sehr dünne Gateoxide beigemischt um parasitäre Effekte zu eliminieren. In dieser Doktorarbeit werden Dotierprofile in Materialien mit hoher Beweglichkeit untersucht und die NBTI-Zuverlässigkeit für eine CMOS-Technologie mit nitridiertem Gateoxid analysiert.

Die Ionenimplantation wird auch weiterhin das wichtigste Verfahren zur Einbringung von Dotierstoffen in Halbleiterwafern sein, um Bauelemente und integrierte Schaltungen (ICs) herzustellen. Die Gründe dafür liegen in der Flexibilität bei der Auswahl der Dotierspezies und des Einbauortes im Bauelement sowie in der genauen Anzahl der implantierten Dotieratome. Die anhaltende Verkleinerung der Sperrschichttiefen und lateralen Abmessungen von MOS-Transistoren haben zu einer Zunahme der Applikationen für die Ionenimplantation in der CMOS-Herstellungstechnik geführt. Ein Beispiel dafür ist die Notwendigkeit von sogenannten Halo-Dotierprofilen zur Unterdrückung des Kurzkanaleffekts. Der physikalische Implantationsprozess kann effektiv am Computer modelliert werden. Genaue Simulationen ermöglichen die Optimierung von Dotierprofilen und eine Verkürzung der Entwicklungszeit für eine neue CMOS-Technologie.

Die Untersuchung von Dotierprofilen für fortgeschrittene CMOS-Applikationen erfolgte mit Hilfe eines Monte-Carlo-Ionenimplantationssimulators, der im Rahmen von mehreren Dissertationen entwickelt wurde. Der dreidimensionale Simulator MCIMPL-II basiert auf der physikalischen BCA-Methode und verwendet das 'universelle' ZBL-Potential. Ein empirisches Modell wird für die elektronische Abbremsung der Ionen verwendet, und die erzeugten Punktdefekte werden mit einem modifizierten Kinchin-Pease-Modell berechnet. Im Rahmen dieser Arbeit wurde der Simulator verbessert und von kristallinem Silizium auf fortschrittliche Targetmaterialien auf der Basis von experimentellen Ergebnissen erweitert. Bor und Arsen wurden in biaxial verspanntes Silizium, SiGe-Schichten mit unterschiedlicher Zusammensetzung, und Germanium innerhalb des Energiebereiches von etwa 1keV bis 60keV implantiert. Die erfolgreiche Kalibrierung des Simulators für diese Materialien wird durch einen Vergleich der vorausgesagten Dotierprofile mit SIMS-Messungen gezeigt. Die Monte Carlo Simulation von Ionenbahnen kann zur Analyse der Auswirkung von Materialeigenschaften und physikalischen Effekten wie Akkumulation von Defekten und Channeling auf die Profile eingesetzt werden. Die wichtigsten Ergebnisse der Untersuchung sind eine Verschiebung zu seichteren Profilen mit zunehmendem Germaniumgehalt in SiGe-Legierungen, die erzeugten Defekte sind in Germanium gegenüber Silizium signifikant reduziert, und die stressbedingte Volumsausdehnung in verspanntem Silizium wirkt sich kaum auf die Profile aus.

Es wird zunehmend schwieriger, die Zuverlässigkeit der mit jeder CMOS-Generation kleiner werdenden Transistoren sicherzustellen. Der NBTI-Effekt in p-MOSFETs, die auf nitridierten Gateoxiden basieren, hat sich als der dominante Degradierungsmechanismus für fortgeschrittene CMOS-Technologien herausgestellt. Als ein weiterer Teil dieser Arbeit wurde eine experimentelle und simulationsbasierte Untersuchung über die durch NBTI hervorgerufene Degradierung der Transistorparameter für eine 90nm-Technologie durchgeführt.

Schließlich wird der verbesserte Monte-Carlo-Ionenimplantationssimulator für die Berechnung von Dotierstoffverteilungen in topologisch komplizierten dreidimensionalen Strukturen angewendet, die aus verspannten oder unverspannten Materialien mit erhöhten Beweglichkeiten bestehen. Die ausgewählten Beispiele demonstrieren das Leistungsvermögen des Simulationswerkzeuges zur Unterstützung der Herstellung von hochentwickelten Bauelementen. Darüber hinaus wird die Auswirkung der Speicherung von Zufallsbitfolgen auf die NBTI-Lebensdauer einer SRAM-Zelle mit Hilfe numerischer Simulationen analysiert. Alle präsentierten Applikationen wurden von der Industrie angefordert oder inspiriert.

Abstract

The MOS transistor performance depends on both the channel length and the carrier transport properties of the channel material. Novel materials with higher carrier mobilities beyond the achievable limits of process-induced strained silicon are required to facilitate continued commensurate device scaling. Nitrogen is incorporated into ultra-thin gate oxides to eliminate parasitic effects. In this thesis, doping profiles in high-mobility materials are investigated and the NBTI reliability is analyzed for a CMOS technology with nitrided gate oxide.

Ion implantation will continue to be the primary technology for introducing dopant atoms into semiconductor wafers to form devices and integrated circuits (ICs). The reason for this lies in the flexibility of this doping technique in selection of dopant species, spatial location within the device, and in the accuracy of the number of implanted dopant atoms. The continued reduction in junction depths and lateral dimensions of the MOS transistor has directly resulted in growth of ion implantation applications in CMOS process technology, e.g. halo doping profiles have become necessary to suppress the short-channel effect. The physical ion implantation process can be effectively modeled on computers. Accurate simulation capabilities allow to optimize the doping profiles and to reduce the development time for a new CMOS technology.

The investigation of doping profiles for advanced CMOS applications has been carried out with a Monte Carlo ion implantation simulator, developed in the scope of several PhD theses. The three-dimensional simulator MCIMPL-II is based on the physical BCA approach and uses the universal ZBL potential. An empirical model is used for the electronic stopping of ions and the generated point defects are calculated by a modified Kinchin-Pease model. As part of this work, the simulator has been improved and extended from crystalline silicon to advanced target materials on the basis of experimental results. Boron and arsenic were implanted into biaxially strained silicon, SiGe layers of different composition, and germanium within the energy range from about 1keV to 60keV. The successful calibration of the simulator for these materials is demonstrated by comparison of predicted doping profiles with SIMS measurements. The Monte Carlo simulation of ion trajectories is useful to analyze the impact of material properties and physical effects like damage accumulation and channeling on the profiles. The main results of the investigation are a shift to shallower profiles with increasing Ge content in SiGe alloys, the produced point defects are significantly reduced in germanium compared to silicon, and the stress-induced volume dilation in strained silicon has almost no influence on the profiles.

As transistors get smaller in each successive CMOS generation, ensuring their reliability becomes increasingly difficult. The negative bias temperature instability (NBTI) effect in p-MOSFETs based on nitrided gate oxides has emerged as the dominant degradation mechanism for advanced CMOS technologies. As another part of this work, an experimental and simulation study for NBTI induced device parameter degradation was performed for a 90nm technology.

Finally, the improved Monte Carlo ion implantation simulator is applied for the calculation of dopant distributions in topological complex three-dimensional structures, composed of strained or relaxed enhanced mobility materials. The selected examples demonstrate the capabilities of the simulation tool to facilitate the processing of advanced devices. Furthermore, the impact of storing random bit sequences on the NBTI lifetime of an SRAM cell is analyzed by numerical simulations. All presented applications were requested or inspired by industry.

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List of Abbreviations and Acronyms

AC	...	Alternating Current
API	...	Application Programming Interface
ASCII	...	American Standard Code for Information Interchange
BCA	...	Binary Collision Approximation
CM	...	Center of Mass
CMOS	...	Complementary MOS
CMP	...	Chemical Mechanical Polishing
CPU	...	Central Processing Unit
CVD	...	Chemical Vapor Deposition
DC	...	Direct Current
DFT	...	Density Functional Theory
DIBL	...	Drain-Induced Barrier Lowering
EOT	...	Equivalent Oxide Thickness
FCC	...	Face-Centered Cubic
Ge-on-Si	...	Germanium on Silicon
GIDL	...	Gate-Induced Drain Leakage
HCI	...	Hot Carrier Injection
IBM	...	International Business Machines Inc.
IC	...	Integrated Circuit
IRW	...	Integrated Reliability Workshop
IT	...	Information Technology
ITRS	...	International Technology Roadmap for Semiconductors
LAT	...	Large Angle Tilt
LDD	...	Lightly Doped Drain
MOS	...	Metal Oxide Semiconductor
MOSFET	...	MOS Field-Effect Transistor
MPI	...	Message Passing Interface
n-MOS	...	n-Channel MOS Transistor
NAND	...	Not AND
NBT	...	Negative Bias Temperature
NBTI	...	Negative Bias Temperature Instability
NIR	...	Near Infrared

LIST OF ACRONYMS

OpenMP	...	Open Multi Processing
PC	...	Personal Computer
p-MOS	...	p-Channel MOS Transistor
PhD	...	Doctor of Philosophy
PVD	...	Physical vapor deposition
R-D	...	Reaction-Diffusion
RTA	...	Rapid Thermal Annealing
SiGe	...	Silicon-Germanium
SoC	...	System on a Chip
SILC	...	Stress-Induced Leakage Current
SIMS	...	Secondary Ion Mass Spectrometry
SIMOX	...	Separation by Implantation of Oxygen
SNM	...	Static Noise Margin
SOI	...	Silicon on Insulator
SRAM	...	Static Random-Access Memory
STI	...	Shallow Trench Isolation
TCAD	...	Technology Computer-Aided Design
ULSI	...	Ultra Large Scale Integration
WSS	...	Wafer State Server
ZBL	...	Ziegler Biersack Littmark

Chapter 1

Introduction

Information technology (IT) is one of the most important technologies, which has allowed to change the industrial society into an information and knowledge based society. The electronic industry is the largest industry in the world with a global sales volume of over 1 trillion US\$ [1]. *Microelectronics* is the branch of electronics which deals with the miniaturization of integrated circuits (ICs). The evolution in microelectronics has resulted in complex System-on-a-Chip (SoC) devices which combine logic and memory units consisting of hundreds of millions of transistors packed on a single silicon chip. The production of ultralarge scale integrated (ULSI) circuits was only possible due to the CMOS (complementary metal oxide semiconductor) technology platform because of low-power and scaling properties.

The workhorse of integrated circuits is the MOSFET (metal-oxide-semiconductor field-effect transistor). This device is basically a switch where the electric current in the silicon between the *source* and *drain* electrodes is controlled by the potential of the *gate* electrode. For four decades, the semiconductor industry has achieved continuous performance enhancements by downscaling of the MOSFET device dimensions, as described by *Moore's Law*. That is, the number of transistors per chip doubles every eighteen months to two years. In the last three years it has become clear that the conventional transistor materials silicon and silicon dioxide have been pushed to fundamental material limits. The International Technology Roadmap for Semiconductors (ITRS) defines the current situation as *material-limited device scaling* [2] which requires the introduction of new materials. The incorporation of nitrogen into ultra-thin gate oxides to reduce the gate leakage current and the use of strain to enhance the carrier transport in silicon are two successful examples for the improvement of scaled bulk CMOS devices. In the next several years, either extensions of bulk CMOS technology or new approaches such as fully depleted SOI (silicon-on-insulator) and multi-gate devices must further reduce the cost-per-function and increase the performance of integrated circuits.

Technology Computer-Aided Design (TCAD) refers to the computer simulation of semiconductor process and device technologies. TCAD tools play a key role in the development of a new CMOS technology and they can help to reduce the development time and costs. The combination of process and device simulation tools in a TCAD framework enables analysis and optimization of the influence of process parameters on the electrical characteristics of a single device. Predictive modeling of a single process step in the IC manufacturing process requires to include the underlying physics of that step. An example of a very successful atomistic simulation approach

is the Monte Carlo modeling of the ion implantation process. Each ion trajectory is simulated separately in this approach. In this way, an accurate prediction of the doping profiles after ion implantation is achieved. For deep-submicron devices two- and three-dimensional process simulations can provide a better insight than measurement techniques and have become indispensable for the design of advanced CMOS devices. Rapid technology enhancements, introduction of new materials, and increasing reliability problems caused by more and more shrunk device dimensions have led to the situation that commercial TCAD tools cannot keep pace with numerous newer developments. This situation becomes more critical in the field of process simulation tools due to the existing diversity in the process steps.

1.1 Manufacturing of Integrated Circuits

The fabrication of a modern IC in the CMOS process involves hundreds of sequential steps and can last up to 30 days of processing time [3]. The following basic process steps are used:

- **Lithography:** A lithography step is used to transfer the layout information to the wafer. For instance, one photo mask can define the source/drain areas for n-MOS transistors. Ultraviolet light is typically applied to project the patterns defined by the mask to the photoresist layer which has been deposited on the wafer surface. The structure defined by the mask remains after the development process, if a positive photoresist is used.
- **Deposition:** Layers of various materials (semiconductors, metals, insulators, photoresist) are deposited on the wafer surface during the IC manufacturing process. Mainly two techniques are applied for deposition processes: *Physical Vapor Deposition (PVD)* and *Chemical Vapor Deposition (CVD)*.
- **Etching:** Etching processes are used either to remove complete material layers or to transfer the patterns in the photoresist layer (generated by a lithography step) into the underlying layer. Etching can be performed by a chemical attack (wet etching), by particles in a plasma chamber (dry etching), or by a combination of both.
- **Chemical Mechanical Polishing:** A non-planar surface is produced by process steps which modify the topography of the wafer (deposition, etching, oxidation). The planarization for the next step is performed by *Chemical Mechanical Polishing (CMP)*.
- **Oxidation:** Silicon dioxide is used for isolation purposes in devices and integrated circuits (e.g. shallow trench isolations between MOS transistors) and as mask or scattering layers for ion implantation processes. There are two silicon dioxide growth methods, dry and wet oxidation, depending on whether oxygen or water vapor is used.
- **Ion Implantation:** This is the primary technology in IC manufacturing to introduce impurities (dopant atoms) into semiconductors. An ion implanter is used to accelerate the dopant ions to high energies and to direct the beam of ions onto the wafer.
- **Diffusion:** Dopant diffusion occurs during any thermal processing step either as an intended or unwanted effect. Due to the requirement of very shallow junctions in advanced devices rapid thermal annealing (RTA) processes with very little diffusion (e.g. flash-assisted RTA or laser-anneal) are used to repair the ion implantation induced damage in the crystal.

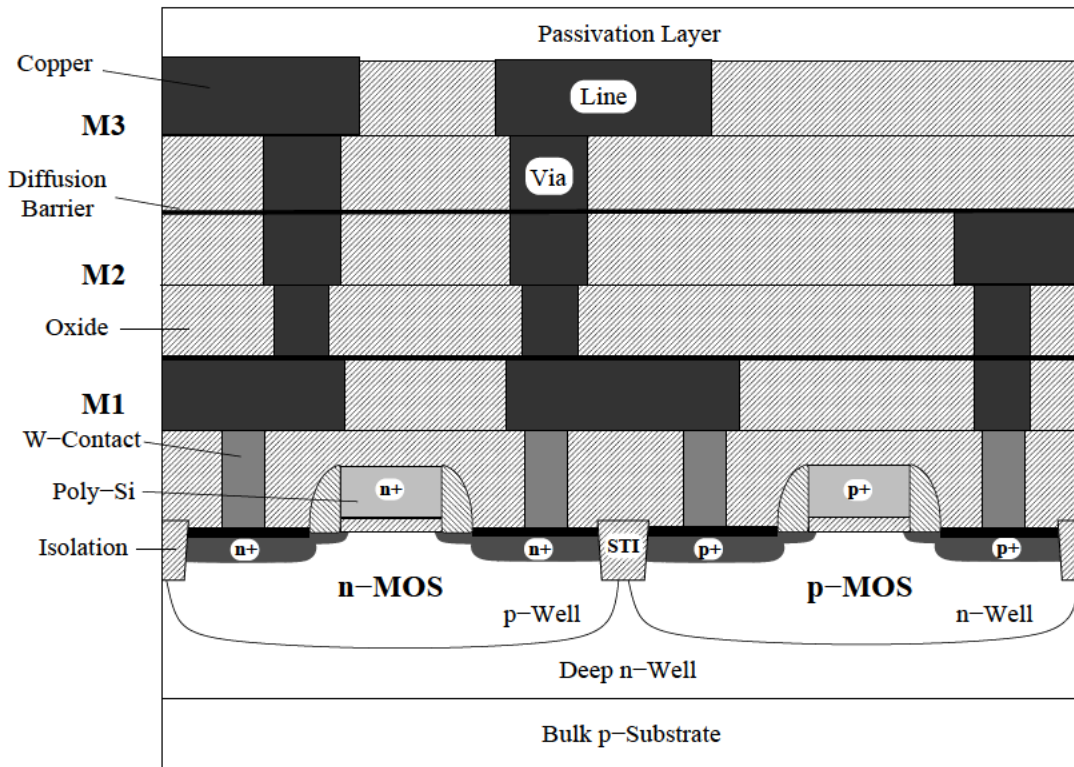


Figure 1.1: Schematic cross-section of a final CMOS integrated circuit with an interconnect structure of three metal layers (M1 – M3).

The CMOS process flow starts with a uniformly doped silicon wafer, and after processing, the wafer contains hundreds of identical rectangular chips. The IC fabrication can be subdivided into the following three major phases:

- The formation of the active devices close to the wafer surface (front-end processing).
- The generation of the interconnect structure above the active devices to form the integrated circuit (back-end processing).
- The chips on the wafer are electrically tested, separated, and packaged.

The final result of such a process flow is shown in Fig. 1.1. This modern bulk CMOS structure is fabricated using a *triple-well* and a *dual-polysilicon gate* process. Both MOS transistors are isolated by an oxide-filled *shallow trench isolation (STI)*. CMOS technology integrates n- and p-channel MOS devices on the same chip. An important characteristic of any CMOS circuit is that in either logic state, at least one device in the series path from the power supply to the ground is non-conductive. Therefore, the static power consumption of the CMOS inverter is given by the leakage current of the off device. A significant current flows only during the short transient period when both devices change their state. Due to the low power dissipation requirement in integrated circuits only the CMOS technology is currently used in advanced IC manufacturing. The NAND gate in Fig. 1.2 illustrates how additional n-MOS and p-MOS devices can be added to the inverter circuit to realize more complex logic functions. In the NAND circuit, the output

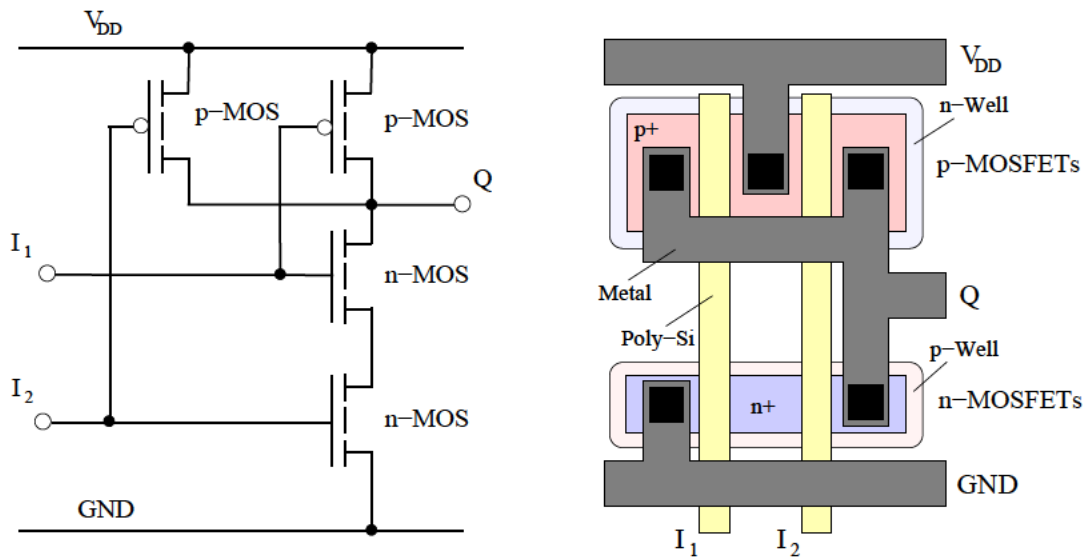


Figure 1.2: Schematic of a CMOS NAND-gate (left) and its layout (right) [4].

Q will be grounded through the two series n-MOS devices only, if both inputs I_1 and I_2 are high. The layout of the NAND-gate shows that the series connection of the two n-MOS devices can be performed easily by a shared n^+ -doped region, and the two p-MOS devices are connected by a shared p^+ region. It can be seen that the p-MOS device has a significantly larger area than the n-MOS device. At least double the width of the n-MOS device is used for the p-MOS due to the lower hole mobility in silicon. Finally, it should be noted that a complex IC circuit can contain over 10^9 transistors, and each of them must work correctly.

1.2 Critical Issues for Device Miniaturization

The shrinking of MOS transistor dimensions is typically performed by a scaling factor of 0.7 per each technology generation. It has been demonstrated by Intel that a gate length of 10nm is

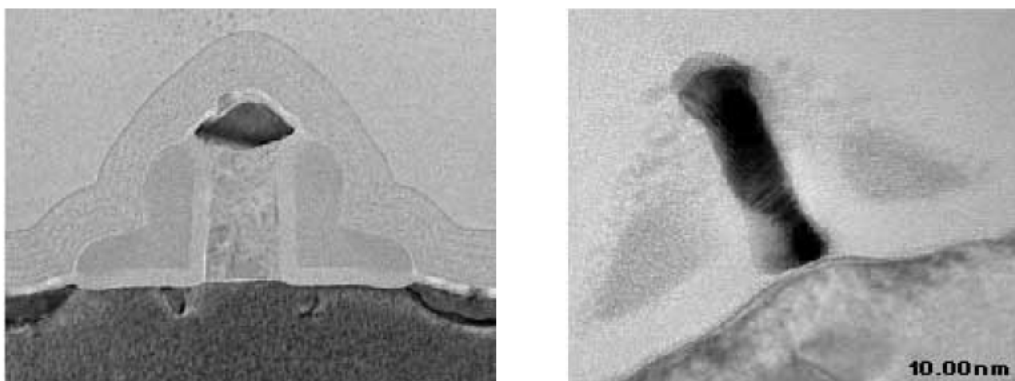


Figure 1.3: Small devices with a gate length of 60nm (left) and 10nm (right) [5, 6]. The gate dielectric thicknesses are 1.5nm and 0.8nm, respectively.

possible in experimental devices, as shown in Fig. 1.3. The ongoing downscaling trend leads to some limitations and issues in modern CMOS technology, mainly due to small-geometry effects. For instance, the punchthrough effect must be suppressed in short channel devices [7], or the application of ultra-thin gate dielectrics requires the incorporation of nitrogen into the oxide, which in turn worsens the interfacial properties [8]. The issue of ultra-shallow source/drain junctions and their increased parasitic resistance is discussed in Section 1.3.

1.2.1 Short-Channel Effects

An MOS transistor is considered *short* when the effective channel length L_{eff} is comparable to the source/drain junction depletion width [9]. In this case, the potential distribution in the channel depends on both the normal and the lateral electric field in the device. Experimentally, the short-channel effect is observed to degrade the subthreshold characteristics and to reduce the threshold voltage V_T with decreasing L_{eff} and increasing drain voltage V_D . When L_{eff} is further reduced, the drain current finally cannot be turned off and the gate has no control over the charge. The so-called *punchthrough effect* poses a severe problem for miniaturized devices. Measures which are taken to suppress this effect are retrograde wells and halo implants [7]. The purpose of these background doping profiles is to prevent the expansion of the drain depletion region into the lightly doped transistor channel when the device is switched on [10, 11].

For devices with very short channels an additional effect occurs which leads to increased leakage current. Due to the short distance between source and drain, the potential at the drain contact reduces the peak value of the energy barrier in the channel, which is called *drain-induced barrier lowering (DIBL)*. It leads to a decrease of the threshold voltage with reduced channel length.

The required high channel doping to control short channel effects degrades carrier mobility, lowers the drain current, and increases band-to-band tunneling across the junction and *gate-induced drain leakage (GIDL)* [2]. Moreover, statistical fluctuation of channel dopants in small area devices causes increasing variation of the V_T value, posing difficulty in circuit design while scaling the supply voltage.

1.2.2 Hot-Carrier Effects and Drain Engineering

As a consequence of the power-supply voltage being reduced much less proportionally to the channel length L_{eff} in practical scaling (deviation from constant-field scaling), the lateral electric field is increased in the device [9]. Carriers which move from the source to the drain in such a turned-on MOS transistor can get enough energy to cause impact ionization that generates electron-hole pairs in silicon and surmount the interfacial energy barrier. The carriers injected into a gate dielectric induce device degradation such as V_T shift and reduced drain current. Therefore, *hot carrier injection (HCI)* degradation significantly reduces the transistor lifetime. The n-MOS transistor is more sensitive to HCI than the p-MOS transistor, since electrons become hotter than holes due to their higher mobility and the energy barrier is lower for electrons compared to holes at the interface. This degradation effect was considered as the major reliability problem in former technology generations, in particular, if high electric fields were generated by constant-voltage scaling. However, to solve this issue, *drain engineering* is used to alleviate the peak of the lateral electric field located close to the drain edge by modifying the drain doping profile through the introduction of source/drain extension implants by a lower dose [7].

1.2.3 Gate-Dielectric Reliability

According to the CMOS scaling suggested in the ITRS roadmap [2], the gate dielectric thickness should be reduced with every new device generation. If the energy barrier between gate and semiconductor becomes too small, the quantum-mechanical *tunneling effect* comes into play [12]. One solution to this effect is to use dielectric materials which have a higher dielectric permittivity than silicon dioxide (SiO_2). These materials allow to achieve a high physical thickness together with a small *effective oxide thickness (EOT)*. The EOT is defined as the thickness of a SiO_2 layer with equal capacitance. Since none of the alternative dielectric materials forms a native oxide on silicon, a thin interfacial layer of SiO_2 can hardly be avoided. For a layer of SiO_2 and a high-k dielectric, the EOT of the stacked dielectric is

$$\text{EOT} = T_{\text{SiO}_2} + T_{\text{high-k}} \cdot \frac{k_{\text{SiO}_2}}{k_{\text{high-k}}}, \quad (1.1)$$

where T_{SiO_2} and $T_{\text{high-k}}$ denote the thickness of the SiO_2 and high-k layer, and k_{SiO_2} and $k_{\text{high-k}}$ are the respective permittivities, respectively. With *high-k dielectrics* it is possible to retain good control over the inversion charge even with physically thick dielectrics to block tunneling currents. However, only nitrided gate oxides (SiON) are currently used in state-of-the-art CMOS technologies because of critical reliability issues of high-k dielectrics. On the one hand side, the incorporation of nitrogen into the oxide reduces gate leakage, avoids boron penetration into the dielectric, and improves HCI, and on the other hand side, it increases the *negative bias temperature instability (NBTI)* effect [13]. The NBTI mechanism leads to a rapid shift of the transistor parameters (V_T , $I_{D\text{sat}}$) due to the buildup of charged interface traps during operation. The NBTI reliability will be investigated for a 90nm technology node in Section 5. CMOS scaling beyond the 45nm node requires the reduction of the gate dielectric thickness down to an EOT of $\sim 1\text{nm}$ which will either be realized with SiON or high-k dielectrics.

1.3 Trends in Doping Profiles for CMOS Technology

The ongoing scaling of device dimensions to increase packing density, to increase operating speed, and to reduce power consumption has posed difficult challenges for the doping of MOS transistors. As the channel length is reduced in a scaled device the threshold voltage decreases with the channel length (threshold voltage roll-off). The short channel effect can be minimized if the source/drain junction depth is reduced too. Table 1.1 shows the trend to very shallow junctions

Year of introduction	2005	2007	2010
Technology node (nm)	90	65	45
Channel doping concentration (cm^{-3})	$3.7 \cdot 10^{18}$	$5.4 \cdot 10^{18}$	$8.9 \cdot 10^{18}$
Sidewall spacer thickness t_{sp} (nm)	35.2	27.5	19.8
Extension junction depth X_j (nm)	11	7.5	6.5
Extension lateral abruptness (nm/decade)	3.5	2.8	2.0
Contact junction depth X_{jc} (nm)	35.2	27.5	19.8

Table 1.1: Doping requirements from the 2005 ITRS roadmap [2].

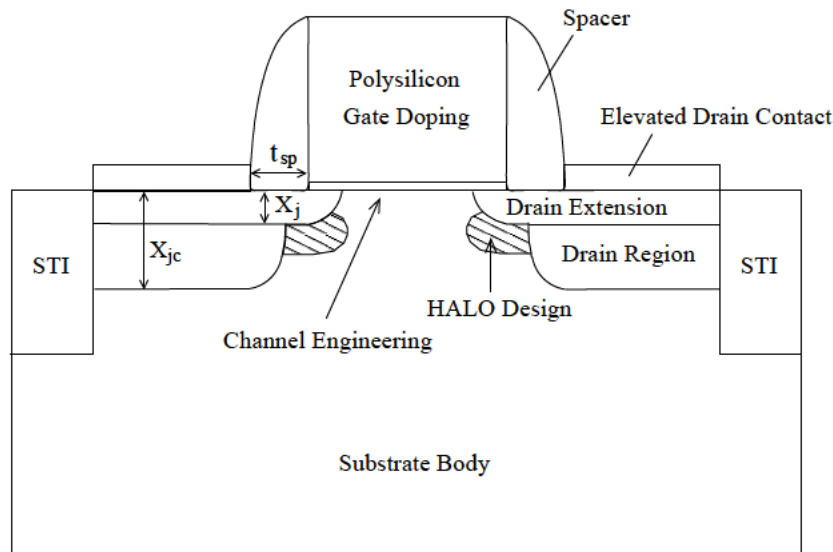


Figure 1.4: Doping problems in extremely scaled MOS transistors.

in future CMOS technology nodes. Shallower junctions require the introduction and activation of higher dopant concentrations to keep the resistance of the source and drain regions small so that the drive current is maximized. Table 1.1 also states that steeper lateral doping gradients of the source/drain extension regions under the gate are necessary to increase the device performance. Fig. 1.4 shows some major doping issues required to form an advanced MOS structure. Scaling of the contact area, junction depth, and contact silicide thickness leads to an increase in parasitic resistance. A possible solution is to use elevated source/drain contacts by selectively deposited silicon or germanium in the contact region to make more silicon available for the silicide formation process. In the polysilicon gate electrode the doping concentration has to be pushed beyond known limits in order to limit the depletion layer thickness [2]. Halo implants (also known as punchthrough suppression or “pocket” implants) avoid the punch-through between the source and drain through the bulk substrate in short-channel devices. This implantation places the dopants just below the active channel, adjacent to the source and drain regions, to precisely tailor the well background doping there (see Fig. 1.4). Operating frequencies above 1GHz have become possible for MOS transistors only due to the successful introduction of halo implants [4]. Finally, channel engineering with the doping profile of a modulated retrograde well structure will become increasingly important for the optimization of various device parameters (e.g. channel mobility, threshold voltage, source/drain junction capacitance, hot carrier control, substrate current, soft error control) in future CMOS technologies [7].

Virtually all doping profiles required for advanced CMOS processing are accomplished by ion implantation. The reasons that ion implantation has become the dominant doping technology in modern IC manufacturing are the flexibility in selecting the dopant species, spatial location, and amount of introduced dopant atoms within the device. This process provides a very precise control and reproducibility for the desired dopant distributions. Furthermore, the ion implantation process can be effectively modeled on computers. The accurate simulation of implanted dopant distributions in one-, two-, or three-dimensional structures requires only a few input parameters and can reduce the development time and costs for a new CMOS technology.

1.4 Overview of Ion Implantation Simulation Tools

The three-dimensional ion implantation simulator MCIMPL-II (**Monte Carlo Implantation**) [14] was used throughout this work for the investigation of implanted doping profiles in silicon and non-silicon materials. The simulator MCIMPL-II is based on a binary collision approximation (BCA) [15] and will be described in detail in Section 3. Beside MCIMPL-II, there are several ion implantation simulators available on the market today, both commercial and academic ones. Due to the high complexity inherent in BCA modeling, commercial ion implantation simulators are often based on academic simulation codes. An analytical ion implantation module is mostly used additionally to a Monte Carlo module to allow a fast simulation of implantation profiles.

TRIM

The Monte Carlo program TRIM (**T**ransport of **I**ons in **M**atter) was developed by Ziegler, Biersack and Littmark in 1985 [16], and then rewritten to run on PCs [17]. This BCA program simulates the slowing down and scattering of energetic ions in amorphous targets. The projectile trajectory is statistically followed by randomly selecting a target atom, an impact parameter, and a distance (mean free-flight-path). It was developed for determining ion range and damage distributions as well as angular and energy distributions of backscattered and transmitted ions.

MARLOWE and UT-MARLOWE

The development of the MARLOWE simulator has been started in 1974 by Robinson and co-workers [18, 19]. The program uses a BCA technique and considers crystalline target materials. The nuclear scattering is treated in a precise manner by numerically evaluating the classical scattering integral for realistic interatomic potentials. This calculation could be run only on a mainframe computer because of the tremendous computational effort. UT-MARLOWE is a highly modified MARLOWE code which was developed at the University of Texas at Austin [20, 21]. Recently, an interpolation scheme of scattering events was developed to allow the implantation simulation of an arbitrary species into crystalline silicon [22].

Crystal-TRIM

The program Crystal-TRIM was developed at the Forschungszentrum Rossendorf at Dresden [23], based on the MARLOWE and TRIM codes. The current version 04/1D simulates ion implantation into crystalline silicon, germanium and diamond with up to 10 amorphous overlayers of arbitrary composition [24]. Not only atomic ions but also molecular ions may be considered. Dynamic simulation of damage accumulation in crystalline substrates and the formation of amorphous layers are possible. The simulator can be used to calculate implanted range and damage distributions as function of depth. An efficient splitting algorithm is employed in order to enhance the statistical accuracy of the simulation results without considerable increase of computing time. It is particularly useful, if channeling tails are of interest. Other versions of Crystal-TRIM (for calculating two- and three-dimensional range and damage profiles) were part of the process simulators TESIM, DIOS and FLOOPS, which were distributed by ISE Integrated Systems Engineering AG, Zürich. Now some of these simulators are part of the TCAD software of Synopsys.

1.5 Outline of the Dissertation

New materials have become more and more important in the development and implementation of advanced CMOS technologies. Process-induced strained silicon is currently used in the 65nm technology to enhance the drive current. Biaxially strained silicon, silicon-germanium (SiGe) alloys with high Ge concentrations or pure germanium offer larger intrinsic carrier mobilities compared to process-induced strain, which can be exploited for channel engineering.

The purpose of **Chapter 2** is to provide a brief overview on semiconductor doping technology. The first part of the chapter explains the theoretical background of semiconductor doping and its impact on the electrical material properties. The ion implantation technique for introducing dopant atoms into semiconductors is presented in the second part.

Ion implantation is an extremely physical process, since the incoming dopant ions make way for themselves by knocking the target atoms out of their lattice sites. **Chapter 3** starts with the description of the fundamental physical models required for the Monte Carlo calculation of ion implantation distributions. The following section of the chapter is focused on the Monte Carlo ion implantation simulator MCIMPL-II [14]. The process simulation environment, the principle of operation, and the models used for the trajectory calculation are described. Atomistic simulation provides a better insight into the ion implantation process, for instance, single ion trajectories can be visualized or the implantation induced vacancy and interstitial concentration profiles are available. The improvement of the simulation results by an advanced smoothing procedure is analyzed, and the accomplishment of a three-dimensional application is demonstrated.

In **Chapter 4** the implantation of boron and arsenic is studied in novel crystalline materials such as SiGe alloys, germanium, and silicon-based heterostructures as a replacement for bulk silicon. For this purpose, the ion implantation simulator has been extended from silicon to these target materials on the basis of experimental results. For the simulation of a new material, the crystalline partner selection model has to be modified, the empirical electronic stopping model has to be calibrated, and the displacement energy for the damage generation has to be adapted. The investigations are focused on the influence of strain, the germanium content in SiGe alloys, the damage accumulation, and the channeling effect on the obtained doping profiles.

Negative bias temperature instability (NBTI) has emerged as a major reliability concern for newer CMOS technologies [25]. In **Chapter 5**, the impact of NBTI-driven degradation of transistor parameters on the lifetime of a high-performance p-MOSFET is investigated. Experiments for different gate voltages, frequencies, and duty cycles were performed to analyze the degradation behavior for the key device parameters, V_T and I_{Dsat} . The presently leading reaction-diffusion (R-D) model is used for the numerical simulation of interface trap generation based on the diffusion and accumulation of released hydrogen in the gate oxide.

In **Chapter 6**, several simulation applications are presented. MCIMPL-II is used for the three-dimensional simulation of ion implantation applications for processing advanced MOS transistors and a high-speed photodetector. The applicability of enhanced mobility materials for processing of improved MOS devices with existing ion implantation equipment is shown. A calibrated reaction-diffusion model is used to investigate the impact of NBTI-induced transistor parameter degradation on the lifetime of a state-of-the-art SRAM cell by numerical simulations.

Finally, **Chapter 7** summarizes the thesis with some conclusions.

Chapter 2

Semiconductor Doping Technology

Without exaggeration almost all of the basic MOSFET parameters are affected by the distribution of dopants in the device. Doping refers to the process of introducing impurity atoms into a semiconductor region in a controllable manner in order to define the electrical properties of this region. The doping with donors and acceptors allows to modify the electron and hole concentration in silicon in a very large range from 10^{13}cm^{-3} up to 10^{21}cm^{-3} . The carrier concentration can also be varied spatially quite accurately which is used to produce pn-junctions and built-in electric fields. All electronic and optical semiconductor devices incorporate dopants as a crucial ingredient of their device structure.

Ion implantation is the primary technology to introduce doping atoms into a semiconductor wafer to form devices and integrated circuits [7, 17]. This low-temperature process uses ionized dopants which are accelerated by electric fields to high energies and are shot into the wafer. The main reason in applying this technique is the precision with which the amount and position of the doping can be controlled. Dopant ions can be masked by any material which is thick enough to stop the implant as well as by existing device structures, which is referred to as self-aligned implants. After the implantation process the crystal structure of the semiconductor is damaged by the implanted particles and the dopants are electrically inactive, because in the majority of cases, they are not part of the crystal lattice. A subsequent thermal annealing process is required to activate the dopants and to eliminate the produced crystal damage.

Continuous growth and dominance of CMOS technology has directly resulted in the growth of ion implantation applications [17]. Leading edge CMOS processes which are used to fabricate a modern microprocessor require up to twenty ion implants per wafer. The doping requirements span several orders of magnitudes in both, energy and dose, for a wide range of dopant masses. An important implantation application for CMOS processing is, for instance, to form the source/drain regions in the substrate. Downscaling of MOS transistor dimensions requires the reduction of the source/drain junction depth to compensate the influence of the shorter channel length on the threshold voltage [7]. The subsequent application of an enhanced annealing process step like the flash-assist RTA (rapid thermal annealing) technique leads to a very limited diffusion which barely changes the as-implanted doping profiles and junction depth [26]. The distribution of dopants in the final device is therefore mainly determined by the ion implantation step, whereby channeling of implanted ions, which results from the regular arrangement of atoms in the silicon crystal structure, plays a major role.

2.1 Fundamentals of Semiconductor Doping

The starting material used for the fabrication of semiconductor devices is monocrystalline silicon. Silicon wafers are produced either by the Czochralski crystal pull method or by the floating-zone crystal growth technique [27]. Dopants are added to the silicon during the growth process in order to set the resistivity of the wafer in the range from $1\text{m}\Omega\text{cm}$ – $30\Omega\text{cm}$ [4]. Defects in the silicon crystal become much more severe for smaller device dimensions. Today, silicon wafers with a (100) surface plane are commonly used in semiconductor manufacturing [28], because the lowest defect density at the Si/SiO₂ interface can be achieved by thermal oxidation of (100) silicon. In this work we consider crystalline substrates of silicon, silicon-germanium, and germanium. At zero temperature the conductivity in a pure semiconductor crystal is zero, because the vacant conduction band is separated by an energy gap E_g from the filled valence band. As the temperature is increased, electrons are thermally excited from the valence band to the conduction band. Both the electrons in the conduction band and the vacant orbitals or holes left behind in the valence band contribute to the electrical conductivity.

2.1.1 Intrinsic Semiconductor

An intrinsic semiconductor is one that contains a negligibly small amount of impurities compared with thermally generated electrons and holes. The energy distribution of electrons in solids is given by the Fermi-Dirac statistics [29]. The probability that an electronic state at energy E is occupied by an electron in thermal equilibrium is given by the Fermi-Dirac distribution

$$f(E) = \frac{1}{1 + \exp\left(\frac{E - E_F}{k_B T}\right)}. \quad (2.1)$$

In Fig. 2.1 the Fermi-Dirac distribution function $f(E)$ versus energy ($E - E_F$) is presented for different temperatures. The Fermi energy E_F is the energy at which the probability of

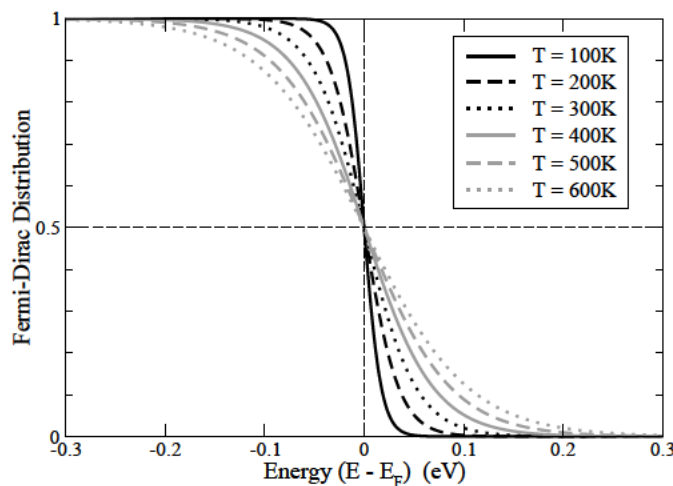


Figure 2.1: Fermi-Dirac distribution function for various temperatures.

occupation by an electron is exactly one-half. The probability of not finding an electron at energy E , $1 - f(E)$, is the probability of finding a hole there. At absolute zero temperature, $T = 0\text{K}$, all the states below the Fermi level are filled, $f(E) = 1$ for $E < E_F$, and all the states above the Fermi level are empty $f(E) = 0$ for $E > E_F$. At finite temperatures, continuous thermal agitation exists, which results in excitation of electrons from the valence band to the conduction band and an equal number of holes are left in the valence band. This process is balanced by recombination of the electrons in the conduction band with holes in the valence band. The width of the transition from one to zero of the probability distribution $f(E)$ increases with the thermal energy $k_B T$. Note that $f(E)$ is symmetrical around the Fermi level E_F . For energies that are $3k_B T$ above or below the Fermi energy, the exponential term in (2.1) becomes larger than 20 or smaller than 0.05, respectively. The Fermi-Dirac distribution can thus be approximated by simpler expressions according to

$$f(E) \doteq \exp\left(-\frac{E - E_F}{k_B T}\right) \quad \text{for } (E - E_F) > 3k_B T, \quad (2.2)$$

$$f(E) \doteq 1 - \exp\left(\frac{E - E_F}{k_B T}\right) \quad \text{for } (E - E_F) < -3k_B T. \quad (2.3)$$

The electron and hole concentrations in an intrinsic semiconductor under thermal equilibrium condition depend on the density of states $N(E)$, that is, the number of allowed energy states per unit energy per unit volume and is given by [29]

$$N(E) = 4\pi \left(\frac{2m_{e,h}}{h^2}\right)^{\frac{3}{2}} E^{\frac{1}{2}}. \quad (2.4)$$

The electron concentration n in the conduction band is given by integrating the product of the density of states $N(E)$ and the probability of occupying an energy level $f(E)$ according to

$$n = \int_{E_C}^{\infty} f(E) N(E) dE, \quad (2.5)$$

where E_C is the energy at the bottom of the conduction band. Substituting (2.2) and (2.4) into (2.5) and solving the integral results in

$$n = N_C \exp\left(-\frac{E_C - E_F}{k_B T}\right), \quad N_C \equiv 2 \left(\frac{2\pi m_e k_B T}{h^2}\right)^{\frac{3}{2}}, \quad (2.6)$$

where N_C is the effective density of states in the conduction band [29]. In a similar way the hole concentration in the valence band can be obtained according to

$$p = \int_{-\infty}^{E_V} [1 - f(E)] N(E) dE, \quad (2.7)$$

where E_V is the energy at the top of the valence band. Substituting (2.3) and (2.4) into (2.7) and solving the integral yields

$$p = N_V \exp\left(-\frac{E_F - E_V}{k_B T}\right), \quad N_V \equiv 2 \left(\frac{2\pi m_h k_B T}{h^2}\right)^{\frac{3}{2}}, \quad (2.8)$$

where N_V is the effective density of states in the valence band [29].

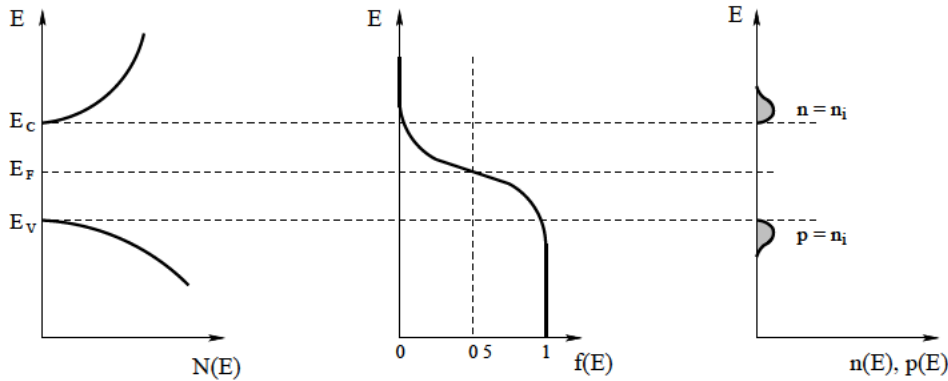


Figure 2.2: Density of states, probability distribution, and resulting electron and hole concentration in an intrinsic semiconductor [29].

For an intrinsic semiconductor the number of electrons in the conduction band is equal to the number of holes in the valence band, that is, $n = p = n_i$ where n_i is the intrinsic carrier concentration. In Fig. 2.2 the intrinsic electron and hole concentrations are obtained graphically from the product of $N(E)$ and $f(E)$. The Fermi level for an intrinsic semiconductor is obtained by equating (2.6) and (2.8) which yields

$$E_F = E_i = \frac{E_C + E_V}{2} + \frac{k_B T}{2} \ln \left(\frac{N_V}{N_C} \right). \quad (2.9)$$

The intrinsic Fermi level E_i lies very close to the middle of the bandgap $E_g \equiv E_C - E_V$, because the second term in (2.9) is much smaller than the bandgap at room temperature.

The intrinsic carrier concentration can be calculated from equations (2.6), (2.8), and (2.9) according to

$$np = n_i^2, \quad (2.10)$$

$$n_i = \sqrt{N_C N_V} \exp \left(-\frac{E_g}{2 k_B T} \right). \quad (2.11)$$

The intrinsic carrier concentration is largely controlled by $E_g/k_B T$, the ratio of the band gap and the temperature. When this ratio is large, the conductivity will be low. Table 2.1 summarizes these key values for germanium, silicon, and gallium arsenide at room temperature and Fig. 2.3 shows the temperature dependence of n_i for these semiconductors.

Material	E_g (eV)	n_i (cm ⁻³)
Ge	0.66	$2.4 \cdot 10^{13}$
Si	1.12	$9.65 \cdot 10^9$
GaAs	1.42	$2.25 \cdot 10^6$

Table 2.1: Bandgap and intrinsic carrier concentration at 300K for three common semiconductors [30].

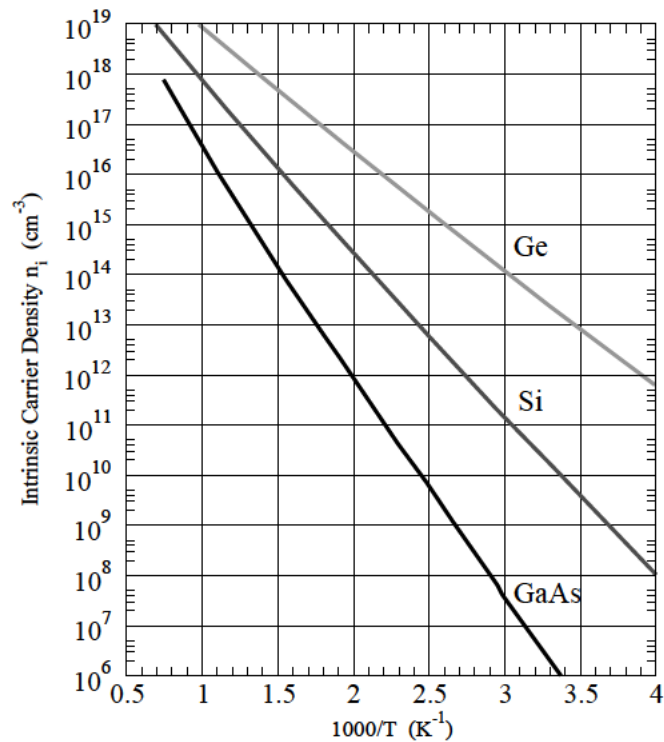


Figure 2.3: Intrinsic carrier densities of Ge, Si, and GaAs as a function of reciprocal temperature [30].

2.1.2 Donors and Acceptors

In processing of modern semiconductor devices, doping refers to the process of introducing impurity atoms into a semiconductor wafer by ion implantation. The purpose of semiconductor doping is to define the number and the type of free charges in a crystal region that can be moved by applying an external voltage. The electrical properties of a doped semiconductor can either be described by using the “bond” model or the “band” model. When a semiconductor is doped with impurities, the semiconductor becomes extrinsic and impurity energy levels are introduced. In Fig. 2.4 the bond model is used to show that a tetravalent silicon atom (group IV element) can be replaced either by a pentavalent arsenic atom (group V) or a trivalent boron atom (group III). When arsenic is added to silicon, an arsenic atom with its five valence electrons forms covalent bonds with its four neighboring silicon atoms. The fifth valence electron has a relatively small binding energy to its arsenic host atom and can become a conduction electron at moderate temperature. The arsenic atom is called a donor and a donor-doped material is referred to as an n-type semiconductor. Such a semiconductor has a defined surplus of electrons in the conduction band which are the majority carriers, while the holes in the valence band, being few in number, are the minority carriers. In a similar way, Fig. 2.4 demonstrates the behavior, if a boron atom with its three valence electrons replaces a silicon atom, an additional electron is “accepted” to form four covalent bonds around the boron, and a hole carrier is thus created in the valence band. Boron is referred to as an acceptor impurity and doping with boron forms a p-type semiconductor. The dopant impurities used in controlling the conductivity type

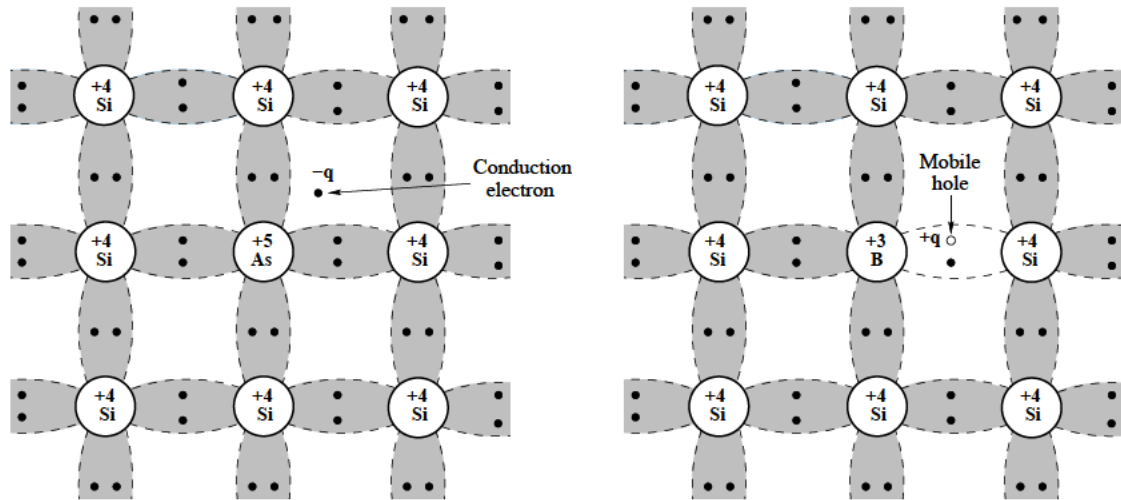


Figure 2.4: Schematic bond representation for n-type silicon doped with arsenic and p-type silicon doped with boron.

of a semiconductor usually have very small ionization energies, and hence, these impurities are often referred to as shallow impurities. The energy required to remove an electron from a shallow donor impurity such as arsenic, phosphorus, and antimony can be estimated based on the Bohr model of the hydrogen atom [30, 31]. The ionization energy of hydrogen is given by

$$E_H = \frac{m_0 q^4}{8 \epsilon_0^2 h^2} , \quad (2.12)$$

where m_0 is the free electron mass, q is the elementary charge, ϵ_0 is the dielectric constant, and h is the Planck constant. The evaluation of (2.12) results in 13.6 eV for the ionization energy E_H of the free hydrogen atom. The hydrogen atom model may be modified to take into account the dielectric constant of the semiconductor and the effective mass of an electron in the periodic potential of the crystal. Thus, the donor ionization energy is obtained by replacing q^2 with q^2/ϵ and m_0 by the effective mass m_e according to

$$E_D = \frac{m_e q^4}{8 \epsilon^2 \epsilon_0^2 h^2} \equiv \frac{m_e}{m_0 \epsilon^2} E_H . \quad (2.13)$$

The Bohr radius of the donor can also be derived from the hydrogen atom model according to

$$a_D = \frac{\epsilon \epsilon_0 h^2}{m_e q^2 \pi} . \quad (2.14)$$

The applicability to silicon and germanium is complicated due to the anisotropic effective mass of the conduction electrons. To obtain a first order approximation of the impurity levels we use $m_e \approx 0.2 m_0$ for electrons in silicon and $m_e \approx 0.1 m_0$ in germanium. Then the ionization energy for donors E_D , measured from the conduction band edge, can be calculated from (2.13), and is 20 meV for silicon and 5 meV for germanium. Calculations using the correct anisotropic mass

tensor predict 29.8 meV for silicon and 9.05 meV for germanium. According to (2.14), the Bohr radius a_D for donors is 30 Å in silicon and 80 Å in germanium, which is much larger than the Bohr radius of 0.53 Å for the hydrogen atom. Therefore, the average distance a_D between the electron and the positive charged donor ion is also much larger than the inter-atomic spacing of the semiconductor crystal. These large radii of the donor orbits overlap at relatively low donor concentrations in the crystal and an “impurity band” is formed from the donor states, which enables electron hopping from donor to donor.

Shallow acceptor impurities in silicon and germanium are boron, aluminium, gallium, and indium. An acceptor is ionized by thermal energy and a mobile hole is generated. On the energy band diagram, an electron rises when it gains energy, whereas a hole sinks in gaining energy. The calculation of the ionization energy for acceptors is similar to that for donors, it can be thought that a hole is located in the central force field of a negative charged acceptor. The calculated ionization energy for acceptors, measured from the valence band edge, is 50 meV in silicon and 15 meV in germanium. The used approach for the calculation of the ionization energy is based on a hydrogen-like model and the effective mass theory. This approach does not consider all influences on the ionization energy, in particular it cannot predict the ionization energy for deep impurities. However, the calculated values do predict the correct order of magnitude of the true ionization energies for shallow impurities. The ionization energy for shallow impurities can also be calculated by means of the density functional theory (DFT). In [32] both approaches are compared to experimental data. The results obtained by the DFT calculation are only for some impurities slightly more accurate than the simple approach. Table 2.2 presents the measured ionization energies for various donor and acceptor impurities in silicon and germanium.

Material	As	P	Sb	B	Al	Ga	In
Si	49.0	45.0	39.0	45.0	57.0	65.0	157.0
Ge	12.7	12.0	9.6	10.4	10.2	10.8	11.2

Table 2.2: Ionization energies of shallow impurities in silicon and germanium, in meV.

For shallow donors, it can be assumed that all donor impurities are ionized at room temperature. A donor atom which has released an electron becomes a positive fixed charge. The electron concentration under complete ionization is given by

$$n = N_D, \quad (2.15)$$

where N_D is the donor concentration. From (2.6) and (2.15), we obtain the distance of the Fermi level from the conduction band edge according to

$$E_C - E_F = k_B T \ln \left(\frac{N_C}{N_D} \right). \quad (2.16)$$

Under complete ionization, the hole concentration is equal to the acceptor concentration N_A ,

$$p = N_A. \quad (2.17)$$

In a similar way we obtain the distance of the Fermi level from the top of the valence band,

$$E_F - E_V = k_B T \ln \left(\frac{N_V}{N_A} \right). \quad (2.18)$$

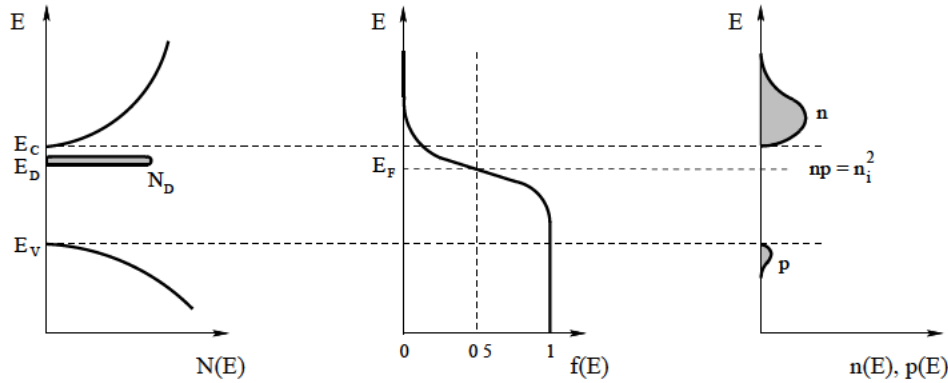


Figure 2.5: Density of states, probability distribution, and carrier concentration in an n-type semiconductor.

Equation (2.16) states that the higher the donor concentration, the smaller the energy difference ($E_C - E_F$), which means that the Fermi level will move up closer to the conduction band edge. On the other hand side, for a higher acceptor concentration, the Fermi level will move closer to the top of the valence band according to (2.18). According to the implanted impurity type, either n- or p-type carriers will dominate, but the product of n and p is equal to n_i^2 . Note that this result is equal to the intrinsic case, Equation (2.10), which is called the mass action law. Fig. 2.5 shows the graphic procedure for obtaining the carrier concentrations in an n-type semiconductor under thermal equilibrium.

If donor and acceptor impurities are introduced together, the impurity present in a higher concentration determines the type of conductivity in the semiconductor. The Fermi level must adjust itself to preserve charge neutrality. Overall charge neutrality requires that the negative charges (electrons and ionized acceptors) must be equal to the total positive charges (holes and ionized donors):

$$n + N_A = p + N_D. \quad (2.19)$$

Combining (2.10) and (2.19) results in the equilibrium electron and hole concentrations in an n-type semiconductor:

$$n_n = \frac{1}{2} \left[N_D - N_A + \sqrt{(N_D - N_A)^2 + 4n_i^2} \right], \quad (2.20)$$

$$p_n = \frac{n_i^2}{n_n}. \quad (2.21)$$

The index n refers to the n-type semiconductor. In a similar way the holes and electrons can be calculated in a p-type semiconductor:

$$p_p = \frac{1}{2} \left[N_A - N_D + \sqrt{(N_D - N_A)^2 + 4n_i^2} \right], \quad (2.22)$$

$$n_p = \frac{n_i^2}{p_p}. \quad (2.23)$$

The index p indicates the majority carrier type being holes.

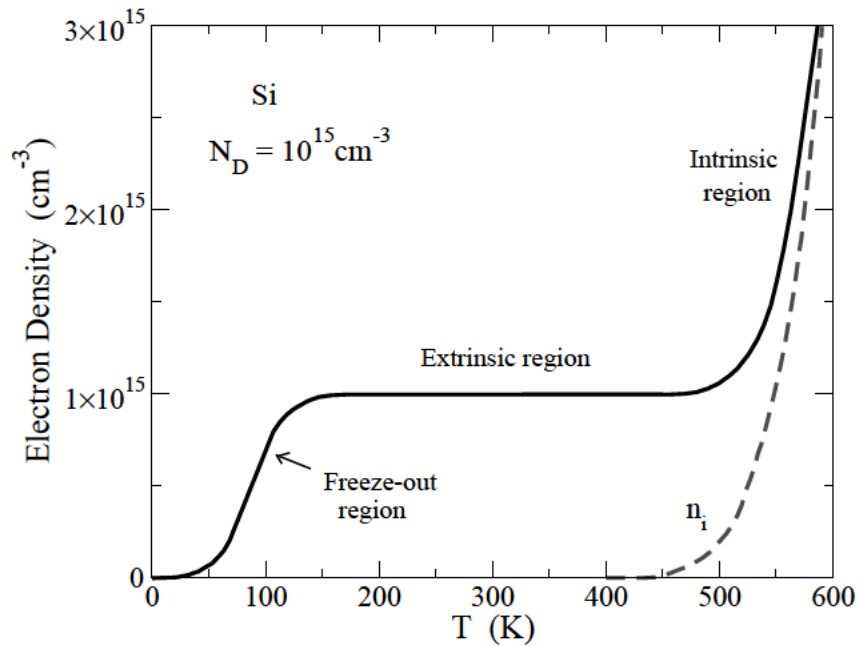


Figure 2.6: Electron density as a function of temperature for a Si sample with a donor concentration of 10^{15} cm^{-3} .

Generally, the magnitude of the net impurity concentration $|N_D - N_A|$ is larger than the intrinsic carrier concentration n_i and the relationships for n_n and p_p can be simplified to

$$n_n \approx N_D - N_A \quad \text{if} \quad N_D > N_A, \quad (2.24)$$

$$p_p \approx N_A - N_D \quad \text{if} \quad N_A > N_D. \quad (2.25)$$

Fig. 2.6 shows the electron concentration in doped silicon with $N_D = 10^{15} \text{ cm}^{-3}$ as a function of the temperature [29]. At low temperatures the thermal energy in the crystal is not sufficient to ionize all available impurities. Some electrons are “frozen” at the donor level and the electron concentration is less than the donor concentration. As the temperature is increased, the condition of complete ionization is reached, $n_n = N_D$. As the temperature is further increased, the electron concentration remains essentially the same over a wide temperature range. This region is called extrinsic. As the temperature is increased further, we reach a point where the intrinsic carrier concentration becomes comparable to the donor concentration. Beyond this point the semiconductor becomes intrinsic. The temperature at which the semiconductor becomes intrinsic depends on the impurity concentration and the bandgap value. It can be obtained from Fig. 2.3 by setting the impurity concentration equal to n_i .

2.2 Ion Implantation Technology

Ion implantation is a process whereby a focused beam of ions is directed towards a target wafer. Ionized particles are used in this process, because they can be accelerated by electric fields and separated by magnetic fields in an easy way in order to obtain an ion beam of high purity and well-defined energy. The ions have enough kinetic energy that they can penetrate into the wafer upon impact. The basic features of an ion implanter for doping semiconductors and the need to anneal the implant were patented by Shockley in 1957 [33]. The accelerators developed for nuclear physics research and isotope separation provided the technology from which ion implanters have been developed and the specific requirements of the semiconductor industry defined the evolution of the architecture of these small accelerators [34]. The next section describes some key elements of a modern ion implanter like the ion source and the beam transport system as well as a technique to achieve uniform doping over large wafers. The wafers are processed one at a time or in batches and are moved in and out of the vacuum by automated handling systems. The productivity of an ion implanter is of economic importance and there is continuing need to increase the usable beam current especially at low energies.

2.2.1 Ion Implantation Equipment

Commercial ion implanters are linear accelerators (linacs) that accelerate ions up to an energy of several MeV. Early machines of the 1970s typically used cold cathode ion sources, which were able to produce ion currents of up to $200\mu\text{A}$. In 1978, the first true high current ion implanter was introduced, which used a Freeman ion source and produced 10mA of ion current at energies up to 80keV [7]. The rapid change in manufacturing process has led to new and improved implanters being developed almost on a yearly basis. The wafer size is now 300mm and has increased seven times since 50mm wafers in 1970. Each size change obsoleted the previous generation of implanters. The changes needed were not only related to wafer handling, but the increase in area of 36 times meant that to maintain equivalent wafer throughput, the beam current needed to be increased correspondingly and as a result effects such as wafer heating, wafer charging, space charge and contamination became quite significant problems [34].

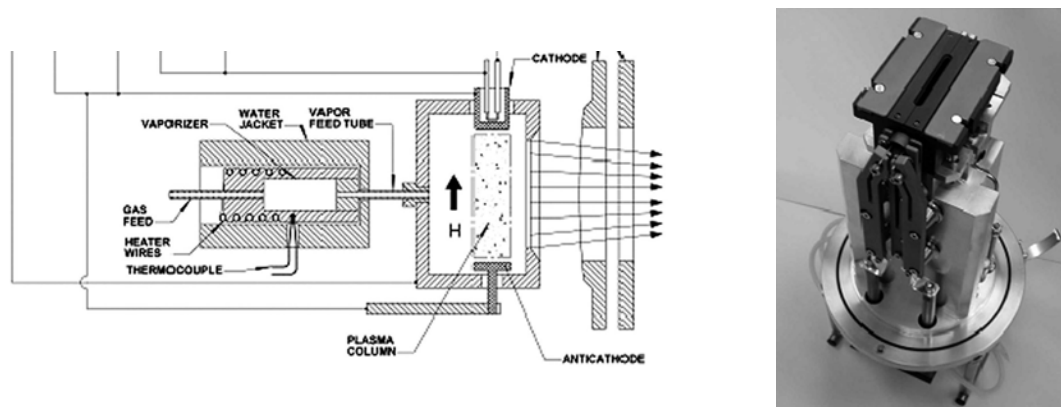


Figure 2.7: Cross-sectional schematic of a Bernas ion source with indirectly heated cathode and vaporizer (left) and corresponding photo (right) [34].

The ion source in an implanter must be capable of producing stable beams of the common dopants such as boron, phosphorus, arsenic, antimony, and indium. A beam current of up to 30mA and a lifetime of more than 100h before failure are required for cost effective productivity [34]. Among several different sources that have been developed the Bernas source with an indirectly heated cathode has become the source of choice for almost all implanters built today, and each manufacturer has developed a specialized design for their equipment [35]. Fig. 2.7 shows a typical example of this ion source. The ionizing electrons oscillate between the indirectly heated cathode and an anticathode and are confined by the magnetic field of a small electromagnet. The plasma density and the shape of the exit aperture of the ion source in combination with the extraction electrodes are important elements in the beam line since the quality and density of the ion beam entering the analyzing magnet system are determined in this region. A detailed discussion of extraction geometries can be found in a review by Hollinger [36], and of the beam transport system by Rose and Ryding [34].

When ion implantation was first adopted for doping semiconductors it was not realized what a large range of capabilities would ultimately be needed. Today, different machine types are used to cover the entire range of both energies and beam currents required for semiconductor fabrication. The machines can be grouped in medium current, high current, high energy implanters, and specialized implanters, for example, the oxygen implanter for SIMOX (separation by implantation of oxygen) technology [38].

Almost all the medium-current implanters which deliver beam currents in the range of a few mA incorporate the concept of hybrid scanning by combining a beam scan and a one-axis mechanical wafer scan. Fig. 2.8 shows an example of a modern medium-current implanter from Nissin Corp. for 300mm wafers which can be employed for the 45nm technology and beyond [37]. The ion beam is generated in the ion source, mass analyzed at the analyzing magnet, accelerated or decelerated at the acceleration column, energy filtered at the final energy magnet, swept by the beam sweep magnet, and then collimated through the collimator magnet. This implanter uses a one-dimensional hybrid scan, where the ion beam is scanned and collimated by magnetic

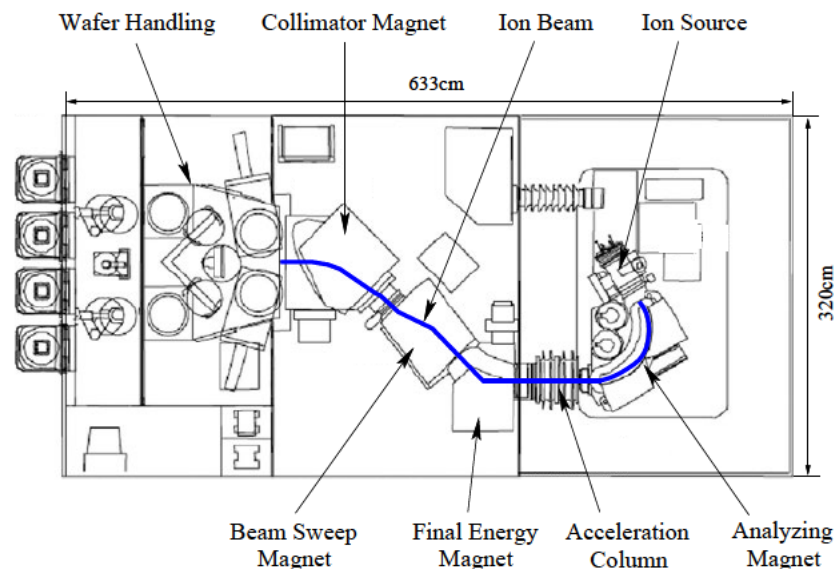


Figure 2.8: Schematics of the medium-current implanter EXCEED3000AH [37].

fields in horizontal direction and the wafer is then mechanically scanned in vertical direction. The typical energy range covered is between about 3keV and 250keV for singly charged ions. Using double or triple charged ions extends the energy range to approximately 750keV. Several manufacturers produce machines of this type and they are widely employed, because they satisfy many of the lower doping requirements for devices, they have a wide energy range and wafer throughputs as high as 450 wafers/h can be achieved [37].

When source/drain implants requiring doses of 10^{16} ions/cm² became important, high-current implanters capable of beam currents larger than 10mA were developed to allow fast processing of wafers. The decreasing junction depth is creating a challenge for high-current implanters because below a few keV it is difficult to obtain reasonably high beam currents [34].

2.2.2 Crystallographic Considerations

Channeling of implanted ions results from the regular arrangement of silicon atoms in rows and planes in crystalline silicon. The silicon crystal has a diamond structure, where each silicon atom is covalently bonded to four other silicon atoms in a tetrahedral arrangement. This configuration belongs to the face-centered cubic (FCC) crystal system with silicon atoms in all corners of a cube, in the center of each cube face, and at four interstitial positions within the cube, as shown in Fig. 2.9. The unit cell of the silicon crystal with its lattice constant a of 5.4307Å at 25°C defines the channels in silicon, where complex channeling behavior can arise from this relatively simple arrangement of atoms.

The Miller indices are commonly used to define planes of atoms and directions in the crystal [17, 39]. The Miller indices (hkl) of a particular plane are a set of three integers which are derived arithmetically from the intercepts x_1, y_1, z_1 of that plane with the coordinate axes X, Y, Z . The length of the intercepts is a related quantity which is specified in multiples of the lattice constant a . The Miller indices (hkl) are defined as

$$h = \frac{s_1}{x_1}, \quad k = \frac{s_1}{y_1}, \quad l = \frac{s_1}{z_1}, \quad (2.26)$$

where the factor s_1 is the lowest common multiple (LCM) of the three intercepts x_1, y_1, z_1 . This is illustrated in Fig. 2.9, which shows the Miller indices for three of the major planes in

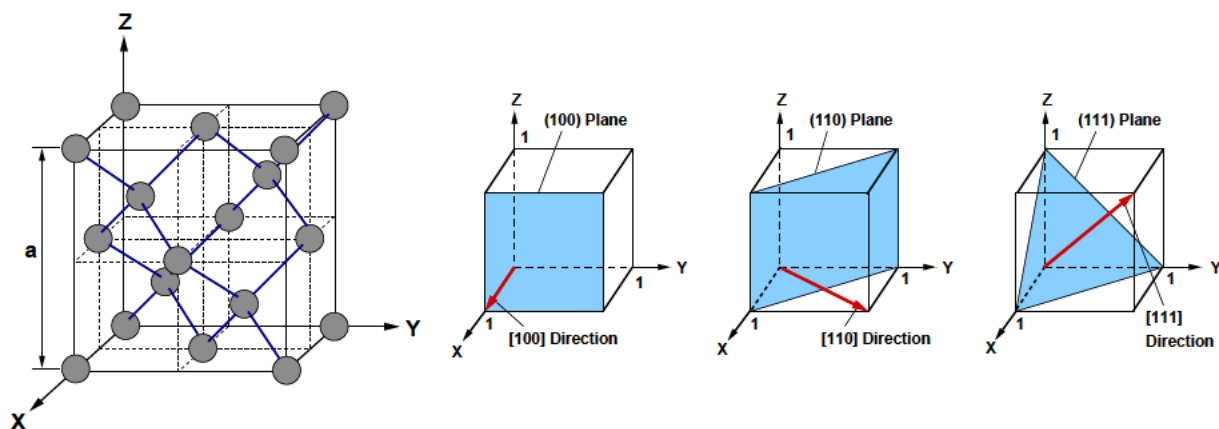


Figure 2.9: Illustration of the silicon crystal structure and Miller index notation.

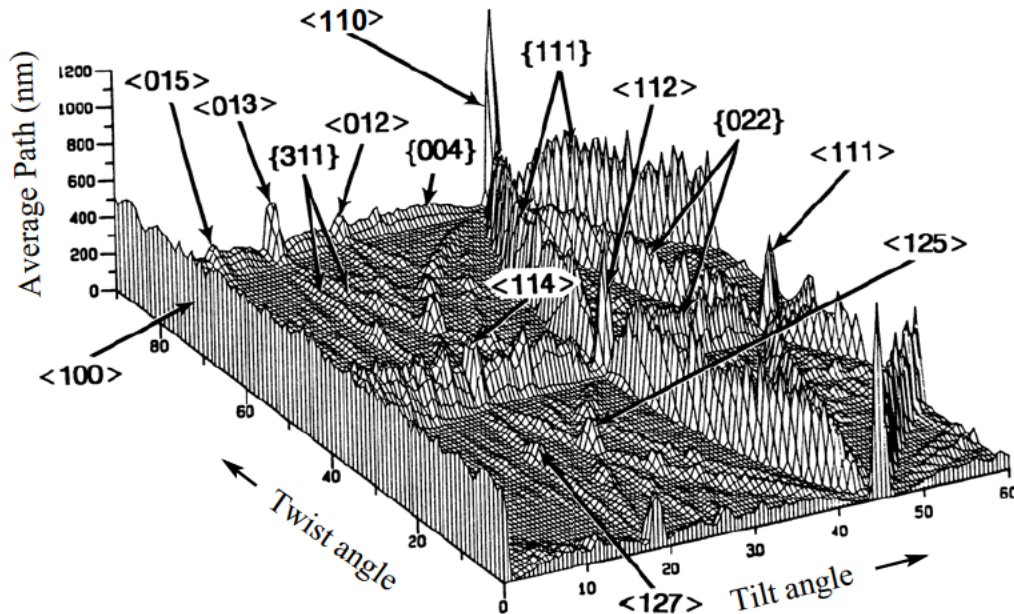


Figure 2.10: Simulated average path lengths of boron ions which are implanted with an energy of 100keV (Lever and Brannon [40]).

the silicon lattice. If a plane has a negative intercept value, this is indicated with a bar over the corresponding Miller index. For example, a plane with the intercepts 1, -1, 2 is designated as $(2\bar{1}1)$ plane.

There are some additional important points concerning the Miller index notation. In the FCC crystal structure, a direction that has the same h , k , l values in its Miller indices as a plane is perpendicular to that plane. Thus, $[100]$, $[110]$, and $[111]$ directions are perpendicular to (100) , (110) , and (111) planes, as demonstrated in Fig. 2.9. There are directions and planes that are identical with respect to physical properties like channeling. For example, the directions $[100]$, $[010]$, $[001]$, $[\bar{1}00]$, etc. are all equivalent and referred to as $\langle 100 \rangle$ directions, while the corresponding group of equivalent planes is designated as $\{100\}$ planes.

Channels exhibit a lower stopping power for the incoming ions since the atomic and electronic densities in the channels are considerably lower than elsewhere in the crystal. This means that ions which are moving along a channel have longer ranges than ions which are traveling in non-channeling directions. Channeling arises not only by the lower stopping power in the center of the channel but also by a focusing effect due to the atoms at the edges of the channel [41]. Lever and Brannon have performed comprehensive investigations of boron channeling in silicon in the region $0^\circ - 60^\circ$ tilt from the $\langle 100 \rangle$ axis in order to identify the major axial and planar channels [40]. The strongest channeling occurs due to the $\langle 110 \rangle$ axial channel which produces the two peaks at 45° tilt, 0° twist and at 45° tilt, 90° twist in Fig. 2.10. Other major channels appear in the $\langle 111 \rangle$ direction (planar channel), and in $\langle 100 \rangle$ direction (axial channel). It can also be observed that the effect of tilt angle is much stronger than that of the twist angle. For instance, a tilt of 7° and a twist of 22° can be used to minimize the channeling of ions.

Channeling is a significant phenomenon for implantation energies from 1keV up to several MeV. In the lower energy regime a larger deflection of an ion occurs even when the ion is traveling near the center of the channel [40]. This behavior is a direct consequence of the fact that the effective radius of silicon atoms along the channel increases as the ion energy is reduced. At a low enough energy the effective radii of the silicon atoms defining the channel become large enough to block that channel. Channeling can be reduced by a screening layer or by pre-amorphization. An amorphous layer, preferable silicon dioxide, can be deposited on the crystalline substrate to scatter the implanted ions. The pre-amorphization implant is performed before the desired implant in order to destroy the crystal structure of the substrate. Preferred ion species are silicon, germanium, or xenon. Both methods were investigated by simulation studies in [42].

2.2.3 Process Parameters for Ion Implantation

The ion implantation process is mainly determined by the following five process parameters:

- dopant species,
- ion beam energy,
- implantation dose,
- and tilt and twist angles.

The simplest semiconductor device is the pn-junction diode which can be easily formed by ion implantation. Fig. 2.11 illustrates a typical n^+/p -doping profile which is formed by a p-well implant followed by the n^+ -implant with its maximum concentration near the surface.

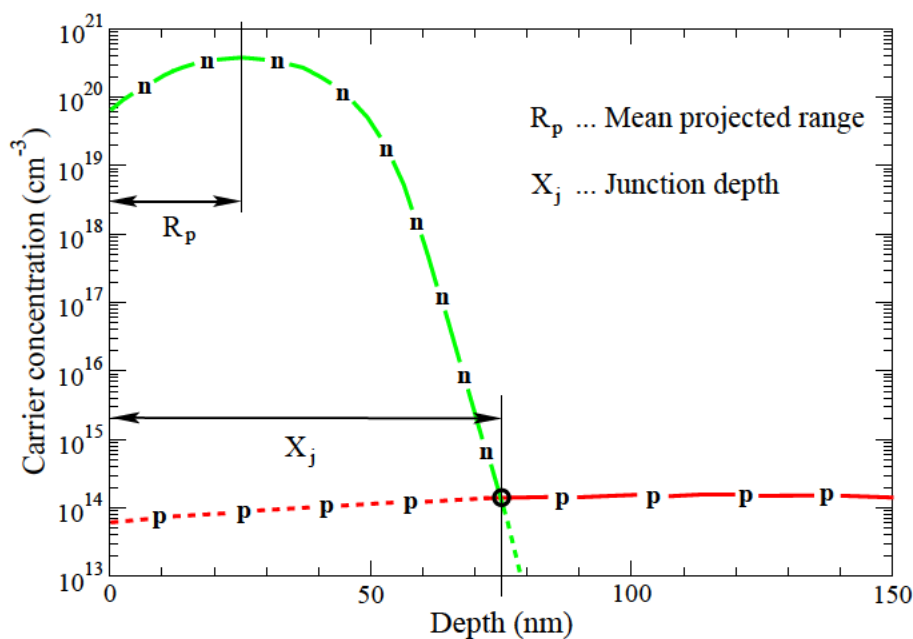


Figure 2.11: Typical implant doping profiles for pn-junction formation.

Species	Type	Atomic number	Mass (amu)	Comment
Antimony	n	51	120.904	Small diffusion coefficient
Arsenic	n	33	74.922	Box-like profiles
Boron	p	5	11.009	Strong channeling effect
Germanium	–	32	71.922	Bandgap engineering
Phosphorus	n	15	30.974	Well formation
Silicon	–	14	27.977	Pre-amorphization
Xenon	–	54	131.3	Pre-amorphization

Table 2.3: Physical properties of common impurities in silicon.

Ion implantation is a random process, because each ion follows an individual trajectory which is determined by the interactions with the atoms and electrons of the target material. The final position of an implanted ion is reached where it has lost its kinetic energy. The average depth of the dopant distribution is referred to as the mean projected range R_p . The junction depth X_j is the point where the donor and acceptor concentrations are equal, as shown in Fig. 2.11.

Dopant Species

Several dopant species are used for ion implantation applications. Table 2.3 summarizes some properties of the most important dopants for CMOS technology. Arsenic, phosphorus, and sometimes antimony are used for n-type doping, while the common p-type dopant is boron. The distribution of these dopants are compared in Fig. 2.12, using equal implantation dose and energy. The profiles were simulated with the ion implantation simulator MCIMPL-II [14]. If

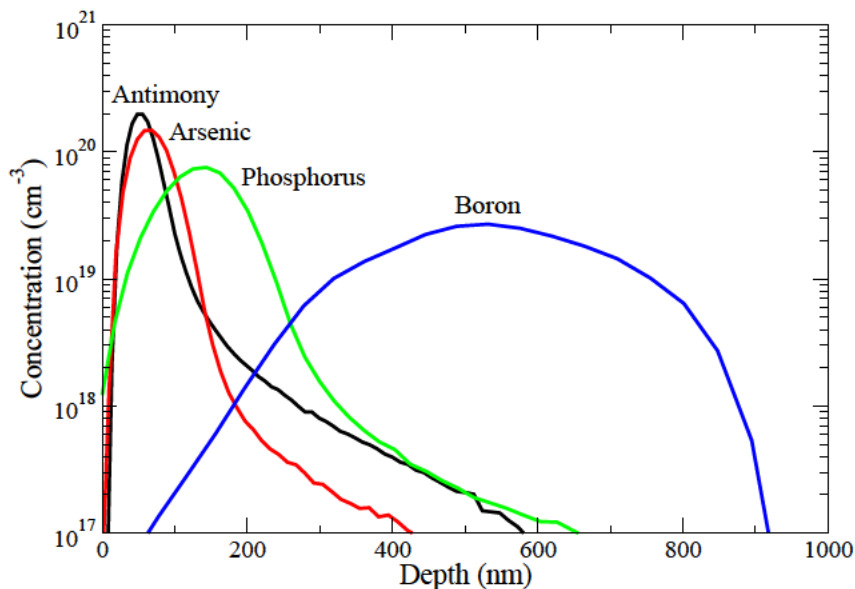


Figure 2.12: Simulated distribution of dopant ions implanted in crystalline silicon with an energy of 100keV and a dose of 10^{15} cm^{-2} .

different ions are implanted with the same energy, heavy ions like antimony stop at a shallower depth than the light ions. The very light boron atom has the largest projected range R_p and the broadest distribution, since a deeper penetration gives rise for more random collision events. Sometimes electrically inactive species like silicon or germanium are implanted before the boron implant to form an amorphous layer beneath the surface which suppresses the channeling effect for boron. Amorphizing pre-implants by germanium facilitate the forming of ultra-shallow junctions for the p-MOSFET, not only by controlling channeling, since germanium also reduces significantly the boron diffusion during the subsequent RTA annealing step. Shallower boron profiles can also be obtained by implanting molecular ion species like BF_2 or $\text{B}_{10}\text{H}_{14}$. The disadvantage of the molecular ion implantation is that additional impurities are introduced.

Ion Energy and Dose

The ion energy controls mainly the penetration depth of ions, and the amount of implanted ions is given by the dose, expressed in ions/cm². In modern semiconductor technology, the energy ranges from 100eV to 3MeV, and the dose from 10^{11} to 10^{16} ions/cm². Energies below a few keV at a high dose are used for the formation of ultra-shallow junctions. Energies in the medium range are applied for poly doping or for channel engineering like threshold voltage adjust or halo implant. Higher energies are required for some low dose applications like retrograde wells. Within the energy range for each doping application, lower mass species are typical implanted at lower energies than heavier species. The dose of the application depends on device design requirements and is independent of the dopant species. The process parameters energy and dose can be controlled very accurately by electrical measurements. A modern implanter guarantees a deviation in energy below 1%. The beam current is a measure of the flow of charged particles, whereby $1\mu\text{A}$ beam current corresponds to $6.25 \cdot 10^{12}$ ions/s. The ion beam is turned off by the dose integrator when it has counted the desired number of ions.

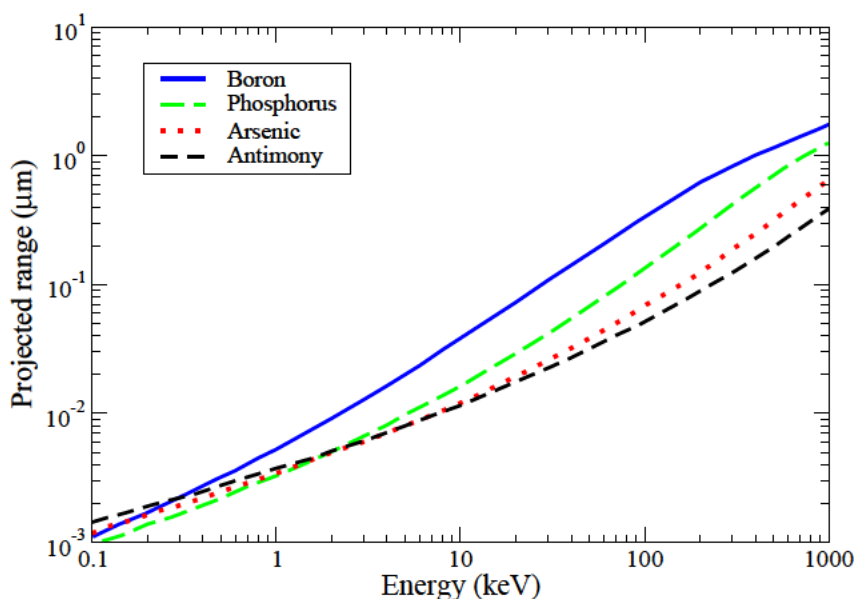


Figure 2.13: Projected range R_p for dopant atoms in amorphous silicon versus energy.

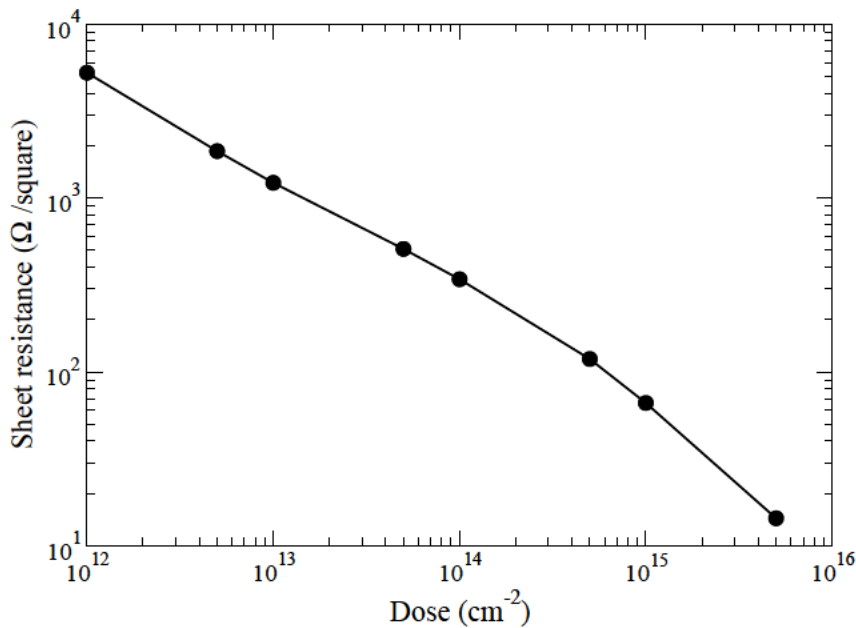


Figure 2.14: The sheet resistance was measured by Cypress Semiconductor for RTA annealed wafers using the Prometrix four-point probe.

Fig. 2.13 shows the experimentally determined mean projected range R_p of the most important dopant species as a function of the implantation energy [16, 43–45]. The R_p values are extracted from profiles measured by secondary ion mass spectrometry (SIMS). Note that the R_p data are averaged since SIMS data exhibit a wide variation in results and only amorphous target materials are commonly used to identify the R_p versus energy dependence. In Fig. 2.13 it can be observed that the projected range of an ion is larger for lower mass species. Therefore, boron has the largest projected range of all investigated dopants, while antimony has the shortest projected range. An exception of this rule can be observed for arsenic and antimony at lower energies. This effect arises because the stopping power is dominated by nuclear stopping in the low energy regime, while it is dominated by electronic stopping in the high energy regime (as described in Section 3.1.3). Antimony has the maximum position of the nuclear stopping power at a slightly higher energy than arsenic which results in a lower stopping power below 5keV (inverse region) and a larger R_p , respectively.

The total dose Q can be calculated by numerical integration of the dopant concentration profile $C(z)$ from the wafer surface to at least the junction depth X_j ,

$$Q = \int_0^{\infty} C(z) dz \approx \int_0^{X_j} C(z) dz . \quad (2.27)$$

Fig. 2.14 shows the sheet resistance R_s versus dose ($R_s \propto \frac{1}{Q}$). The concept of sheet resistance is often used to characterize doped layers. The resistance R of a rectangular block of uniformly doped material with resistivity ρ , length L , width W , and thickness T_{Si} can be written as

$$R = R_s \cdot \frac{L}{W} , \quad \text{with} \quad R_s = \frac{\rho}{T_{Si}} . \quad (2.28)$$

However, to avoid confusion between R and R_s , the sheet resistance is specified in the unit of “Ohm per square” (Ω/\square). The L/W ratio, defined by the unmasked implantation area, can be thought of as the number of unit squares of material in the ion implanted resistor. The maximum reasonable dose around 10^{16} cm^{-2} for the formation of highly conductive regions is determined by the solid solubility of the dopant species in the semiconductor material. At dopant concentrations higher than the solid solubility a part of the dopants cannot be activated, because they precipitate and form immobile clusters during the subsequent RTA annealing process.

Tilt and Twist Angle

The direction of incidence of the ion beam with respect to the wafer crystal orientation is defined by the tilt and twist angle, as shown in Fig. 2.15. The tilt is the angle between the ion beam and the normal to the wafer surface. Wafer rotation or twist is defined as the angle between the plane containing the beam and the wafer normal, and the plane perpendicular to the primary flat of the wafer containing the wafer normal. The primary flat defines the orientation of the silicon crystal, which is aligned to a [011] direction in a (100) oriented wafer. The Miller index notation for describing directions and planes in the crystal lattice system is explained in Section 2.2.2. An appropriate tilt and twist can be used to minimize the channeling effect. Large tilt angles are required in some implantation applications, for instance, in halo implants.

There are two silicon crystal orientations that are used in IC manufacturing, (100) and (111) silicon [28], which means that the crystal terminates at the wafer surface on {100} or {111} planes, respectively. Primarily because of the superior electrical properties of the (100) Si/SiO₂ interface, (100) wafers are dominant in manufacturing today.

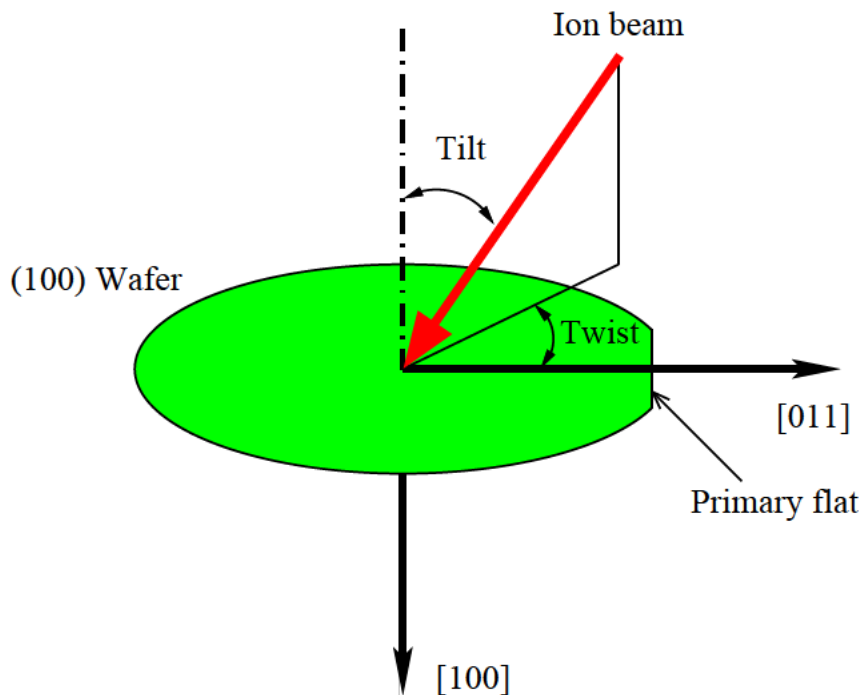


Figure 2.15: Definition of tilt and twist angle for the ion beam [17].

Chapter 3

Simulation of Ion Implantation

There are two methods, the analytical and the Monte Carlo method, which are commonly used in modern TCAD tools for the simulation of ion implantation processes. Mainly increasing accuracy requirements due to the continued downscaling of device dimensions necessitate the transition from the simple analytical simulation of ion implantation to the particle-based Monte Carlo simulation for more and more applications. This chapter outlines fundamental modeling concepts required for the physically based simulation of doping profiles.

The basic idea of the analytical approach is that the doping profile can be approximated by a statistical distribution function [42, 45–47]. This function depends on a set of parameters which can be expressed by characteristic parameters of the implanted dopant distribution, for instance, the mean projected range R_p . The characteristic parameters, the so-called moments, can be extracted from Monte Carlo calculation results or from measured doping profiles. One-dimensional distribution functions can be combined to multi-dimensional profiles by a convolution method which takes a dose matching rule and numerical scaling into account. The analytical simulation of profiles requires relatively little CPU-time, even in two and three dimensions.

Due to the simplicity of the underlying concept, analytical implantation tools cannot accurately predict doping profiles for complex targets, for instance, multilayer targets or advanced devices with junction depths in the range of a few nanometers. In a compound target like SiGe, range predictions will be still worse, because the doping profiles additionally depend on the germanium fraction of the alloy. In contrast to that, the physics-based Monte Carlo method uses an atomistic approach and, therefore, is able to simulate the channeling effect and the accumulation of point defects during the implantation process in crystalline targets, as well as, e.g., shadowing effects arising from mask edges [15, 17, 42]. The Monte Carlo method imitates the implantation process by computing a large number of individual ion trajectories in the target. The three-dimensional device structures can be complex, with the only limitation being the computer memory size which must hold all the interaction details of the target. The underlying physical models are applicable for a wide range of implantation conditions without the need for an additional calibration.

One drawback of the Monte Carlo method are long computing times, which is the main reason why the use of Monte Carlo implantation tools is usually avoided in technology optimization. However, the capability of accurately predicting doping profiles can significantly reduce the development time for a new CMOS technology. In particular next generation technology nodes in the deep sub-100nm regime will put high demands on the accuracy of TCAD tools.

3.1 Physical Models

This chapter outlines the fundamental physics associated with the penetration of energetic ions into solids. The moving ions lose energy to the solid, create point defects, and after stopping they produce the final distribution in the target. The Monte Carlo modeling of ion implantation allows the incorporation of arbitrarily complex physical models at an atomic level.

3.1.1 Stopping of Ions in Solids

An ion which penetrates into a target loses energy constantly to the sea of electrons. It may go many atomic layers, before there is a collision with a target atom which is hard enough to displace that atom and create an interstitial and vacancy pair. The energy required to push a target atom just far enough from its lattice site so that it cannot pop back into its empty site is the *displacement energy* E_d , which is approximately 15eV in silicon. Fig. 3.1 shows different scenarios which can arise for ions shot into a crystalline target material.

Assume an incident ion with atomic number Z_1 and energy E has a collision with a target atom of atomic number Z_2 . After the collision the incident atom has energy E_1 and the struck atom has energy E_2 . A *displacement* occurs if $E_2 > E_d$, so that the atom Z_2 has enough energy to leave the site. A *vacancy* occurs if both $E_1 > E_d$ and $E_2 > E_d$. Both atoms then become moving atoms of the cascade. If $E_2 < E_d$, then the atom Z_2 does not have enough energy and it will vibrate back to its site releasing E_2 as *phonons*. If $E_1 < E_d$, $E_2 > E_d$, and $Z_1 = Z_2$, then the incoming atom remain at the site and the collision is called a *replacement collision* with E_1 released as phonons. This type of collision is common in single element targets with large recoil cascades. If $E_1 < E_d$, $E_2 > E_d$, and $Z_1 \neq Z_2$, then Z_1 becomes an *interstitial atom*.

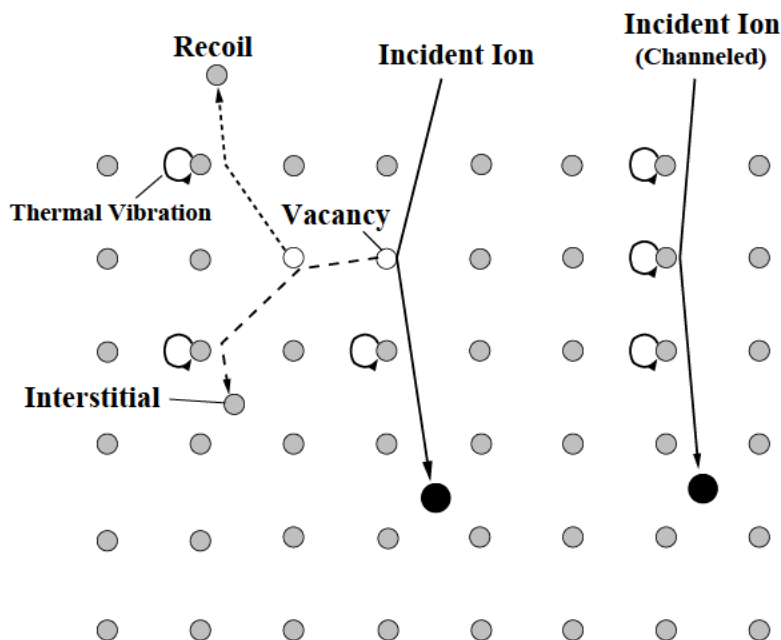


Figure 3.1: The incident ions 'make way' for themselves by knocking the target atoms out of their lattice sites, whereas recoil cascades are generated.

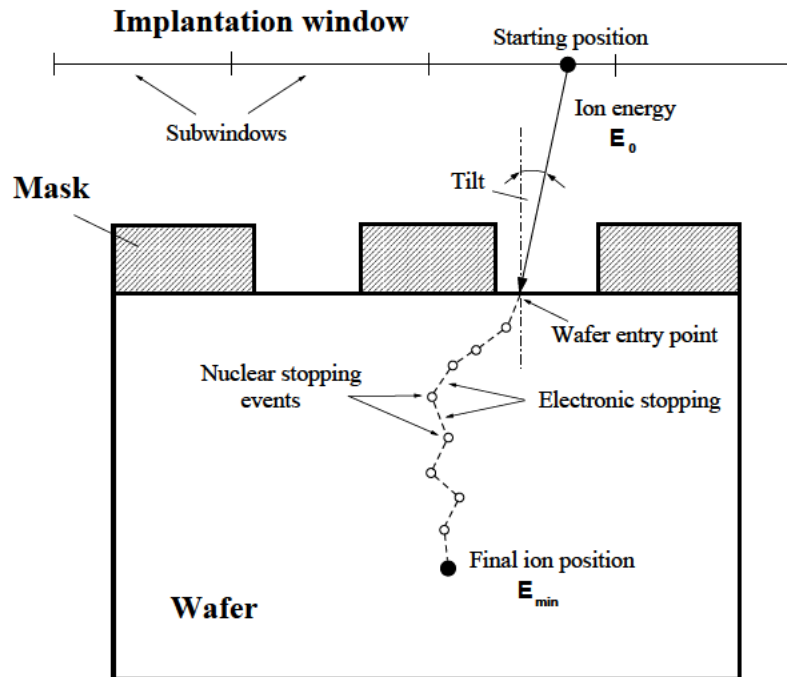


Figure 3.2: Principle of the Monte Carlo simulation method.

Ziegler et al. have demonstrated in [16] that the Monte Carlo calculation of ion trajectories is a very feasible way for accurately simulating the final ion distribution in crystalline silicon. Typically, Monte Carlo programs calculate a large number of individual particle trajectories in a target. Each particle history begins with a random starting position within the implantation window, a given direction, and an ion beam energy E_0 . Fig. 3.2 depicts that a particle changes its direction as a result of nuclear collision events and moves in straight free-flight-paths between collisions. The kinetic energy of the particle is reduced as a result of nuclear and electronic energy losses, and the history is terminated either when the energy drops below a specified value E_{min} or when the particle leaves the simulation domain. The rate at which an ion loses energy depends on the target atom density N_T (in cm^{-3}) and on the nuclear and electronic stopping powers $S_n(E)$ and $S_e(E)$ (in eVcm^2),

$$\frac{dE}{dx} = -N_T [S_n(E) + S_e(E)] . \quad (3.1)$$

The nuclear and electronic stopping powers are assumed to be independent and both are in general functions of energy.

3.1.2 Binary Collision Approximation

The interaction of the moving ion with an atomic nucleus of the target (nuclear stopping) can be treated as an elastic collision process, whereas the interaction with the electrons can be treated as an inelastic process without any scattering effects (electronic stopping). The binary collision approximation (BCA) assumes that only two charged particles, the moving ion (atomic number

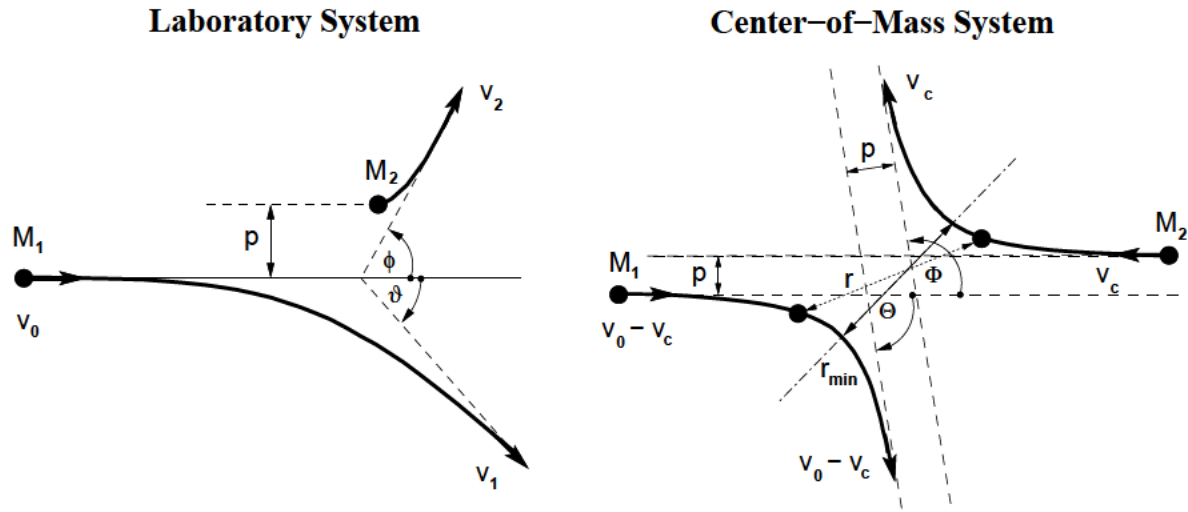


Figure 3.3: Classical two particle scattering process in the laboratory system and in the center-of-mass system.

Z_1 , mass M_1 , kinetic energy E_0) and one target atom (atomic number Z_2 , mass M_2) are involved in one scattering process. While the moving particle M_1 passes and is deflected, the stationary particle M_2 recoils or at least activates thermal lattice vibrations. The distance between the incident direction and the stationary particle is the impact parameter p . Fig. 3.3 shows the scattering variables in a two-body collision. The unknown velocities v_1 , v_2 and directions ϑ , ϕ from the incident direction after the collision event can be found from the conservation of energy (3.2) and momentum (3.3), (3.4) in the laboratory system.

$$\frac{1}{2} M_1 v_0^2 = \frac{1}{2} M_1 v_1^2 + \frac{1}{2} M_2 v_2^2, \quad (3.2)$$

$$M_1 v_0 = M_1 v_1 \cos \vartheta + M_2 v_2 \cos \phi, \quad (3.3)$$

$$0 = M_1 v_1 \sin \vartheta + M_2 v_2 \sin \phi. \quad (3.4)$$

For solving this two-body problem it is convenient to transform the scattering process from the laboratory coordinates to the center-of-mass coordinate (CM) system of ion and target atom. In Fig. 3.3, the CM system moves with constant velocity v_c to the right. Equation (3.5) defines v_c in such a way that the total momentum of the CM system becomes zero. The basic reason for this transformation is that the CM system reduces any two-body problem to a one-body problem, because the total momentum of the particles is always zero and the paths of the two particles are symmetric as shown in Fig. 3.3. The single particle has the initial kinetic energy E_c (3.6) and moves with a reduced mass M_c (3.7) and velocity v_c in a stationary potential $V(r)$ which is centered at the origin of the CM coordinates.

$$M_1 v_0 = (M_1 + M_2) \cdot v_c, \quad (3.5)$$

$$E_c = \frac{M_2}{M_1 + M_2} \cdot E_0, \quad (3.6)$$

$$M_c = \frac{M_1 M_2}{M_1 + M_2}. \quad (3.7)$$

Ziegler derives the particle scattering path by using Lagrangian mechanics in polar coordinates in [17]. The result is the famous “scattering integral” (3.8) which allows to evaluate the scattering angle Θ in the CM system. The angle Θ depends on the energy E_c , the interatomic potential $V(r)$, and the impact parameter p . The distance of minimum approach between the two particles is denoted as r_{min} (see Fig. 3.3), which is determined by the real root of the denominator in (3.8).

$$\Theta(p, E_c) = \pi - 2p \int_{r_{min}}^{\infty} \frac{dr}{r^2 \sqrt{1 - \frac{V(r)}{E_c} - \frac{p^2}{r^2}}} . \quad (3.8)$$

The inverse transformation leads to the scattering angle ϑ of the ion (3.9), the angle ϕ of the recoil (3.10), and the loss in energy of the ion, ΔE , which is equal to the recoil energy (3.11).

$$\tan \vartheta = \frac{\sin \Theta}{\frac{M_1}{M_2} + \cos \Theta} , \quad (3.9)$$

$$\cos \phi = \sin \frac{\Theta}{2} , \quad (3.10)$$

$$\Delta E = \frac{4 M_1 M_2}{(M_1 + M_2)^2} \cdot \sin^2 \frac{\Theta}{2} \cdot E_0 . \quad (3.11)$$

The scattering integral (3.8) cannot be calculated analytically for interatomic screening potentials and a numerical integration would be too time-consuming, since a simulated ion undergoes typically 100 to 1000 collisions. Solutions to this problem are to use an analytical approximation formula or a lookup table method. The used method is of critical importance in terms of accuracy and efficiency for the Monte Carlo calculation.

Interatomic Potential

The only non-trivial quantity in equation (3.8) is the interaction potential $V(r)$ between the ion and the target atom. The potential $V(r)$ is a repulsive Coulomb potential between the two positively charged nuclei, which is screened by surrounding electrons. The effect of the electrons is described by a dimensionless screening function $\Phi(r)$ which is less than one.

$$V(r) = \frac{Z_1 Z_2 q^2}{4 \pi \epsilon_0 r} \cdot \Phi(r) . \quad (3.12)$$

Z_1 and Z_2 are the atomic numbers of the involved particles, q is the elementary charge, and ϵ_0 is the dielectric constant. Well-known older screening functions are the Bohr potential [48], the Thomas-Fermi potential [49], the Moliere [50], and the Lenz-Jensen approximation [51]. Ziegler, Biersack, and Littmark performed the calculation of the interatomic potentials for 522 atom pairs. Based on these calculations they could derive the *universal screening potential* which is suitable for arbitrary atom pairs [17].

$$\Phi(x) = 0.1818 e^{-3.2x} + 0.5099 e^{0.9423x} + 0.2802 e^{-0.4029x} + 0.02817 e^{-0.2016x} , \quad (3.13)$$

$$x = \frac{r}{a_U} \quad \text{with} \quad a_U = 0.8854 \frac{a_0}{Z_1^{0.23} + Z_2^{0.23}} \quad (\text{\AA}) . \quad (3.14)$$

The equation (3.13) for the universal screening function $\Phi(x)$ consists of four fitted exponential terms and uses the scaled radius x as its argument. Ziegler, Biersack, and Littmark introduced

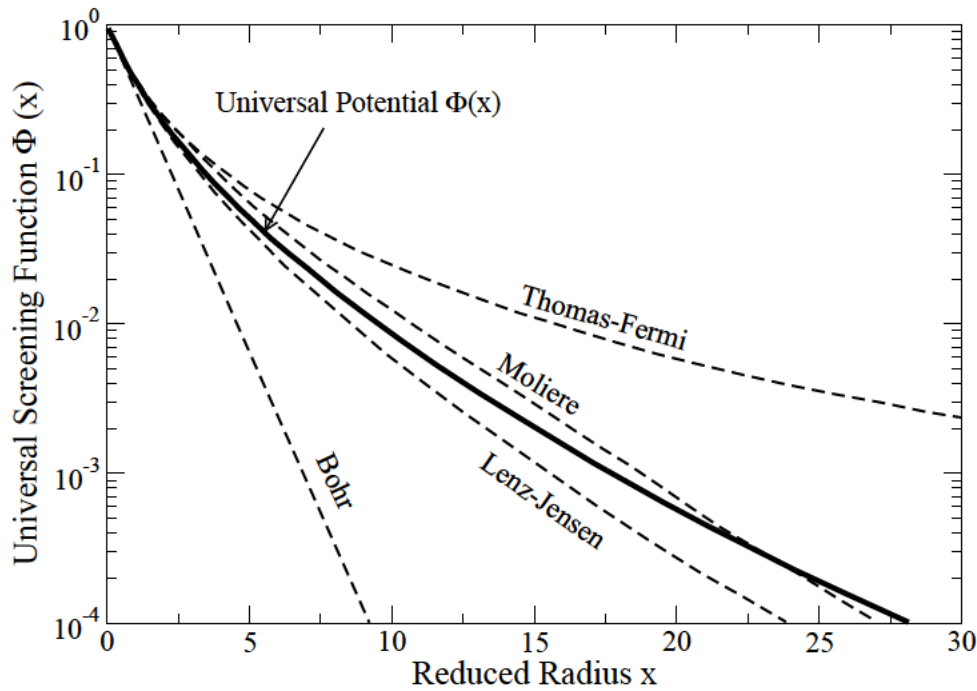


Figure 3.4: Universal screening potential and other approximations.

the scaled radius x according to (3.14), where r is the real radius, a_U is the universal screening length, and $a_0 = 0.529\text{\AA}$ is the Bohr radius. In the literature the universal potential is known as Ziegler-Biersack-Littmark (ZBL) potential.

Lattice Vibrations

Thermal vibrations displace the lattice atoms from their ideal lattice positions and they have been identified as source of the dechanneling mechanism, unless the crystalline target contains considerable damage [52, 53]. The approximation of a spherically symmetric Gaussian distribution $f(\Delta x, \Delta y, \Delta z)$ can be used to describe the displacement of atoms from their rest position.

$$f(\Delta x, \Delta y, \Delta z) = \frac{1}{\sqrt[3]{2\pi\sigma^2}} \cdot \exp\left(-\frac{\Delta x^2 + \Delta y^2 + \Delta z^2}{2\sigma^2}\right). \quad (3.15)$$

The standard deviation σ of the atomic displacement $\sqrt{\Delta x^2 + \Delta y^2 + \Delta z^2}$ from the rest position can be adjusted according to the *Debye theory* [54], which is in good agreement with X-ray diffraction experiments [55]. This theory uses an empirical parameter, the Debye temperature

Method	Θ_D (K)	σ (Å) at 300K
Specific heat	645	0.065
Channeling experiment	490	0.083
Simulation of ion implantation	450	0.090

Table 3.1: Debye temperature Θ_D and corresponding average vibration amplitude σ .

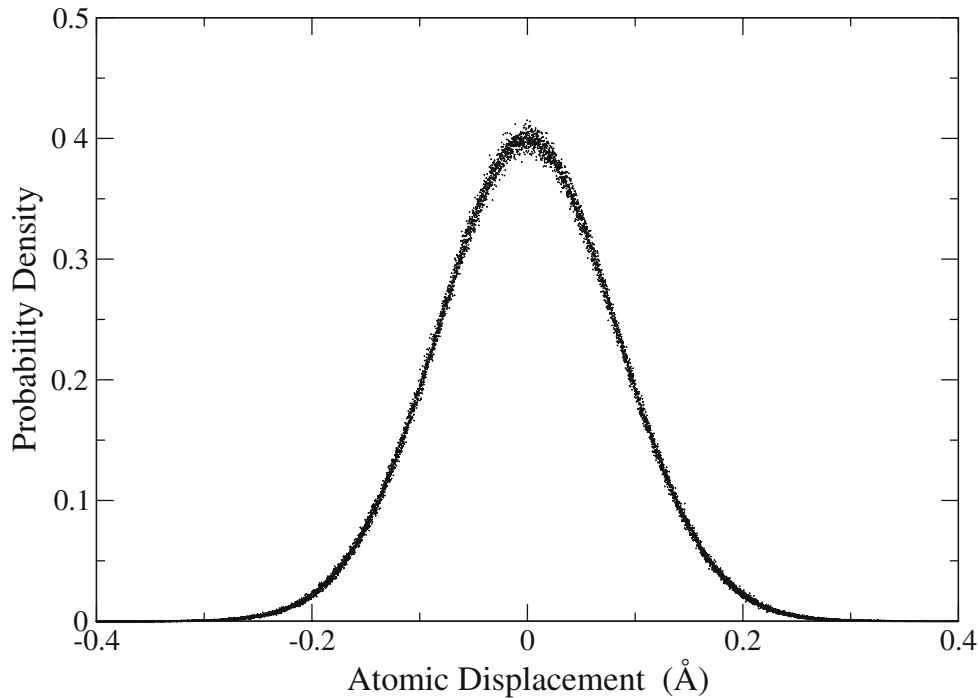


Figure 3.5: Gaussian distribution of the atom vibration amplitudes in MCIMPL-II.

Θ_D , which can be determined with the aid of specific heat measurements [56], by channeling experiments [57], or by comparison of simulated profiles with SIMS data [58], as summarized in Table 3.1 for silicon at a wafer temperature of 300K.

Fig. 3.5 shows a sample size of 10000 atom vibration amplitudes which are used for the Monte Carlo calculation of ion trajectories in MCIMPL-II. The simulator uses an average vibration amplitude $\sigma = 0.083\text{\AA}$ according to a Debye temperature of 490K to model the motion of the atoms in silicon. Note that the random variates from the Gaussian distribution presented in Fig. 3.5 are derived from a random-number generator which produces uniformly distributed random variates in the interval $[0, 1]$. The fast *polar method* is used to generate originally random variates in pairs from the normal distribution contained in the interval $[-\infty, \infty]$ with mean $\mu = 0$ and standard deviation $\sigma = 1$, as described in [59].

3.1.3 Electronic Stopping Power

The electronic stopping power of the target is complicated and not fully understood up to now, since several physical processes contribute to the electronic energy loss [16]:

- Direct kinetic energy transfer to target electrons, mainly due to electron–electron collisions.
- Excitation of band- or conduction-electrons (effect on weakly bound or non-localized target electrons).
- Excitation or ionization of target atoms (effect on localized electrons).
- Excitation, ionization, or electron-capture of the projectile.

The electronic stopping models used for Monte Carlo implantations into silicon can be classified as non-local or local. While non-local models assume that the electronic energy loss is independent of the relative positions of the ion and the target atoms [16, 60], local models take such a dependence into account, using either the impact parameter of the collisions [61] or the local electron concentration along the ion path [62]. Hobler et al. proposed an empirical electronic stopping model for the implantation into crystalline silicon [63], which is based on the Lindhard electronic stopping model and an impact parameter approach.

In the Hobler model the total electronic energy loss ΔE is composed of a non-local part which dominates in the case of large impact parameters (channeling ions) and a local part which is considered at every collision.

$$\Delta E = \Delta E_{nl} + \Delta E_{loc} . \quad (3.16)$$

The non-local part ΔE_{nl} is proportional to the the path length ΔR traveled by the ion between two nuclear collision events in a target material with atomic density N .

$$\Delta E_{nl} = N S_e \Delta R \cdot \left[x_{nl} + x_{loc} \left(1 + \frac{p_{max}}{a} \right) \exp \left(-\frac{p_{max}}{a} \right) \right] . \quad (3.17)$$

The local part ΔE_{loc} is exponentially proportional to the impact parameter as proposed by Oen and Robinson in [61].

$$\Delta E_{loc} = x_{loc} \frac{S_e}{2 \pi a^2} \exp \left(-\frac{p}{a} \right) . \quad (3.18)$$

The term in equation (3.17) containing x_{loc} approximates the local electronic energy loss due to collisions with impact parameters larger than p_{max} . The electronic stopping power S_e is assumed to be velocity proportional in (3.19). Lindhard et al. proposed the expression (3.20) for the coefficient k [60], which considers the properties of the ion species and the target material.

$$S_e = k_{corr} k \sqrt{E} , \quad (3.19)$$

$$k = 8 \pi \hbar a_0 \sqrt{2} \cdot \frac{Z_1^{\frac{7}{6}} Z_2}{\left(Z_1^{\frac{2}{3}} + Z_2^{\frac{2}{3}} \right)^{\frac{3}{2}} \sqrt{M_1}} . \quad (3.20)$$

Z_1 and M_1 are the charge and the mass of the implanted particle, Z_2 is the atomic charge in single-element targets, a_0 is the Bohr radius, and E the kinetic energy of the particle. The *Lindhard correction factor* k_{corr} is used to empirically adjust the strength of the electronic stopping. The *screening length* a is expressed by the value $\frac{a_U}{0.3}$ in [61], where a_U is the screening length used for the interatomic screening potential in (3.14). Hobler et al. multiplied the length by a *screening pre-factor* f according to

$$a = f \cdot \frac{a_U}{0.3} . \quad (3.21)$$

The parameters x_{nl} and x_{loc} are the non-local and the local fraction of the total electronic stopping power which requires the relation (3.22) to hold.

$$x_{nl} + x_{loc} = 1 . \quad (3.22)$$

Dopant species	Energy limit (MeV)
Arsenic	194.1
Boron	2.2
Phosphorus	28.0

Table 3.2: Energy limits for the velocity proportional electronic stopping power [42].

The non-local fraction x_{nl} depends on the energy E and can be modeled by a power law,

$$x_{nl} = y_{nl} \cdot E^q, \quad (3.23)$$

where the empirical parameters y_{nl} and q are the *non-local pre-factor* and *non-local power*. Lindhard indicated that the electronic stopping power S_e is only proportional to the ion velocity up to a maximal energy which is shown for some important ion species in Table 3.2.

The drawback of the empirical Hobler model is that many parameters have to be fitted, in particular for crystalline materials. Hobler has demonstrated for boron implantations in crystalline silicon [64] that the accuracy of the empirical model is better than that of the purely electron-density-based model. The Hobler model requires less additional computational effort since the impact parameter which is used by the BCA algorithm to determine the nuclear energy loss can be applied to calculate the electronic energy loss. Both the nuclear and the electronic stopping powers depend on the energy and contribute to the total stopping. Fig. 3.6 demonstrates the slowing down of boron ions with an initial energy of 40keV. Note that the nuclear stopping has its maximum at 3keV and the electronic stopping dominates for higher energies.

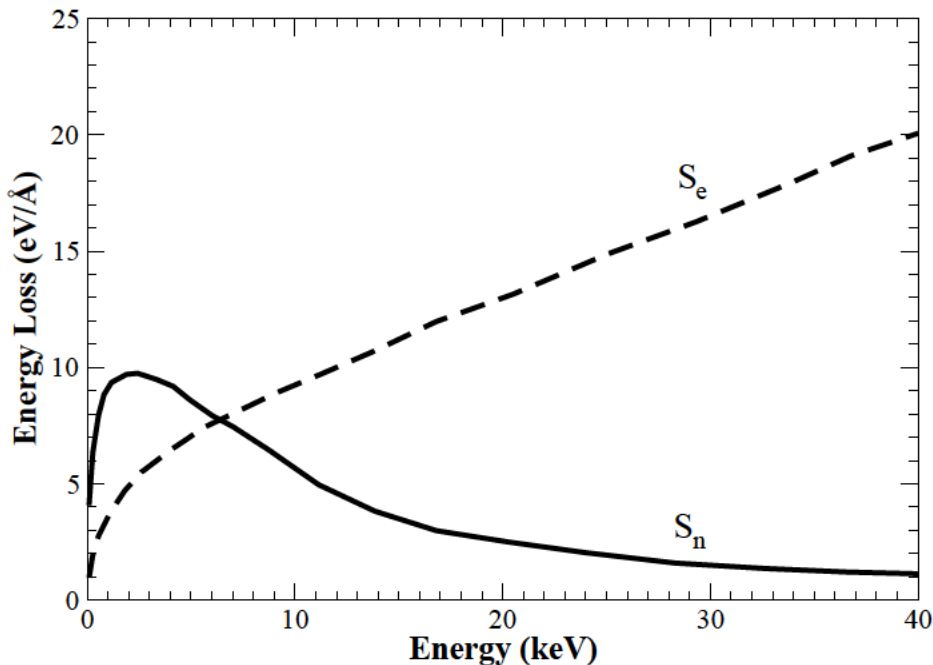


Figure 3.6: Average nuclear and electronic stopping powers $S_n(E)$ and $S_e(E)$ for a 40keV boron implantation into silicon, analyzed with MCIMPL-II.

Summarizing, it can be said that the electronic stopping is dominant for higher energies, lighter ions, and under channeling conditions.

3.1.4 Damage Generation

The nuclear stopping process of energetic ions in crystalline targets displaces atoms from their lattice sites. If the ion implantation dose is high enough, a continuous amorphous layer can be formed in a silicon wafer beneath the surface. A so-called *Frenkel pair* or *Frenkel defect* is formed when a displaced target atom forms an interstitial and leaves a vacancy behind at its original lattice site [29]. The point defects in the target accumulate during the implantation process and influence the trajectories of subsequently implanted ions. In addition, the generated point defects cause a transient enhanced diffusion (TED) effect of dopant atoms during the RTA annealing process. Due to the fact that it is difficult to measure damage concentrations in crystals, the simulation of implantation induced point defects as well as the identification of amorphized regions in the device are very beneficial for modern CMOS process engineering.

The generation of point defects can be modeled by the analytical *modified Kinchin-Pease model* or by the computationally intensive *Follow-Each-Recoil method*.

Modified Kinchin-Pease Model

The modified Kinchin-Pease model assumes that the number of displaced atoms (Frenkel pairs) in a collision cascade is a function of the transferred energy ΔE from the ion to the primary recoil atom [65, 66]. In this theory, the defect producing energy E_ν is obtained from the kinetic energy of the primary knock-on recoil, reduced for the electronic loss by all recoils comprising the cascade. The recoils themselves are not individually followed in this computationally fast approach. It was found in [63] that experimental results can be well described by the modified Kinchin-Pease model together with a model for point defect recombination. The defect recombination which takes place in a recoil cascade can be modeled empirically by using the local point defect concentration.

The electronic energy loss is calculated according to Lindhard's theory [67] using the analytical approximation of Robinson [68] to the universal function $g(\varepsilon_d)$. The "damage energy" E_ν is calculated from the initial energy ΔE of the primary recoil by

$$E_\nu = \frac{\Delta E}{1 + k_d \cdot g(\varepsilon_d)}, \quad (3.24)$$

$$k_d = 0.133745 \cdot \frac{Z^{\frac{2}{3}}}{M^{\frac{1}{2}}}, \quad (3.25)$$

$$g(\varepsilon_d) = 3.4008 \varepsilon_d^{\frac{1}{6}} + 0.40244 \varepsilon_d^{\frac{3}{4}} + \varepsilon_d, \quad (3.26)$$

$$\varepsilon_d = 0.0115 (\text{eV})^{-1} \cdot Z^{-\frac{7}{3}} \cdot \Delta E, \quad (3.27)$$

where Z and M are the atomic number and mass of the recoil atoms, and the reduced energy ε_d is a dimensionless quantity. The number of generated Frenkel pairs ν_{gen} in a recoil cascade can be calculated from the energy E_ν using a constant displacement efficiency $\kappa = 0.8$ in the

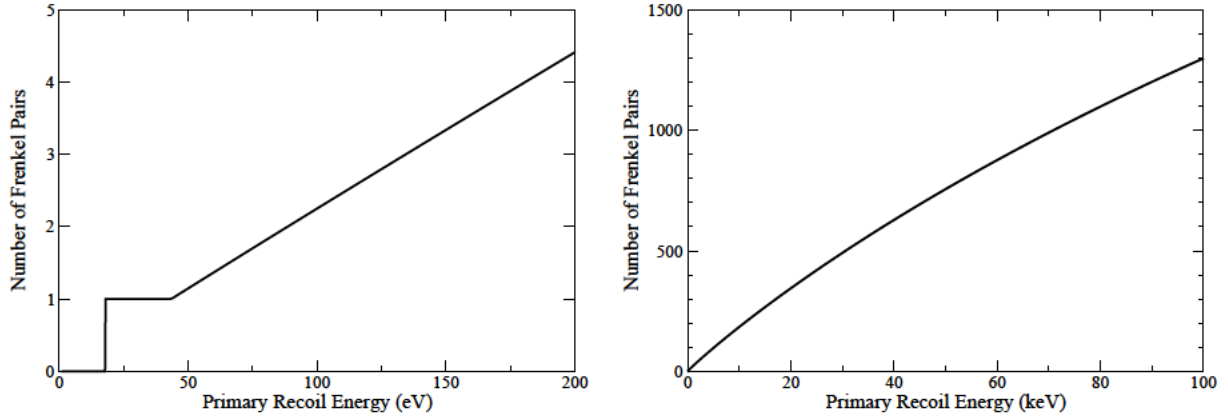


Figure 3.7: Number of Frenkel pairs generated by a primary knock-on atom in silicon assuming $E_d = 15\text{eV}$, plotted for two different energy ranges.

modified Kinchin-Pease damage generation formula, given by

$$\nu_{gen} = 0 \quad \text{for } E_\nu < E_d, \quad (3.28)$$

$$\nu_{gen} = 1 \quad \text{for } E_d \leq E_\nu < 2.5 \cdot E_d, \quad (3.29)$$

$$\nu_{gen} = \frac{\kappa E_\nu}{2 E_d} \quad \text{for } E_\nu \geq 2.5 \cdot E_d. \quad (3.30)$$

The primary recoil atom produces only lattice vibrations if the damage energy E_ν is below the displacement energy E_d . The curves in Fig. 3.7 show the number of produced point defects ν_{gen} for damage cascades in silicon as a function of the transferred energy ΔE without considering pre-existing point defects, as calculated by the modified Kinchin-Pease model.

The recombination between interstitials and vacancies has to be taken into account in order to realistically calculate the produced amount of point defects [63]. The recombination within a collision cascade can be described by a constant fraction f_{rec} of Frenkel pairs surviving the spontaneous self-annealing process due to beam-induced heating of the wafer. If ν_{gen} is the number of point defects generated in a recoil cascade, then the average number of point defects surviving recombination within the cascade is given by $\nu_{gen} \cdot f_{rec}$. The correction parameter f_{rec} depends on the ion species since heavy ions produce damage more efficiently by overlapping of large cascades than lighter ions. A light ion produces typically small cascades due to small transfer energies, where recombination becomes more likely. The recombination with point defects of previously generated damage cascades can be included by an additional factor f_{pre} which depends on the recombination probability p_{rec} defined in (3.33). The average number of stable point defects ν_{st} is linked to the number of generated point defects ν_{gen} according to

$$\nu_{st} = \nu_{gen} \cdot f_{rec} \cdot f_{pre}, \quad (3.31)$$

$$f_{pre} = (-1)p_{rec}^2 + (+1)(1 - p_{rec})^2 = 1 - 2p_{rec}, \quad (3.32)$$

$$p_{rec} = \frac{N_V + N_I}{4 N_{sat}}. \quad (3.33)$$

The factor f_{pre} is obtained by considering the four possible cases for a Frenkel pair having survived recombination within the recoil cascade. In the first case, the generated Frenkel pair (both components) recombines with a pre-existing Frenkel pair, which reduces the total number of Frenkel pairs by one. The probability for this process is p_{rec}^2 . In the second case, which occurs with the probability $(1 - p_{rec})^2$, the generated Frenkel pair survives, resulting in an additional Frenkel pair. In the third and fourth case either the interstitial or the vacancy survives while the other one recombines, resulting in no change of the total Frenkel pair number. Adding these changes with their probabilities yields $(1 - 2p_{rec})$ as the net average fraction of point defects surviving recombination with previously generated point defects. The recombination probability p_{rec} is proportional to the concentration of already existing vacancies and interstitials and it has a species dependent saturation level N_{sat} as given in (3.33). Assuming equal local concentrations of vacancies and interstitials, $N_V = N_I$, the probability p_{rec} has to be equal to the probability of survival $(1 - p_{rec})$ at the saturation concentration, leading to $p_{rec} = 0.5$ for $N_V = N_{sat}$. Substituting (3.32) and (3.33) into (3.31) and assuming $N_V = N_I$, the number of stable point defects ν_{st} are finally obtained by

$$\nu_{st} = \nu_{gen} \cdot f_{rec} \cdot \left(1 - \frac{N_V}{N_{sat}}\right). \quad (3.34)$$

In principle, the displaced atoms can be placed on tetrahedral interstitial sites (tetrahedral interstitial model) [69], on random positions (random model) [70], or on random positions within spheres around the tetrahedral interstitial sites. In [63], Hobler et al. placed the silicon interstitials on random positions within the maximum impact parameter p_{max} from the ion path in the plane perpendicular to the ion's direction of motion. From the comparison of simulations and experiments they found that the silicon interstitials are rather randomly distributed in the crystal lattice than located at tetrahedral interstitial sites.

Follow-Each-Recoil Method

The modified Kinchin-Pease model can only estimate the number of vacancies produced in a collision cascade and, therefore, this damage model assumes the same local concentration for the interstitials. There is a small offset between the local vacancy and interstitial concentrations, since a vacancy stays at the position where the recoil has been generated whereas an interstitial typically comes to rest somewhere slightly deeper in the target. This results in an interstitial profile with its peak at a slightly deeper position than the peak of the corresponding vacancies. The Follow-Each-Recoil method calculates the trajectories of all recoiling atoms in a collision cascade. In the full cascade simulation, the nuclear and electronic loss of a recoil is calculated in the same way as for an implanted ion just with different physical properties. This approach requires a tremendous computational effort, since a cascade can be in the range of thousand displaced atoms in silicon, as demonstrated for high energies of the primary recoil in the right plot of Fig. 3.7. The advantage of the Follow-Each-Recoil method is that the location of the interstitials can be accurately calculated as well as pollution effects can be estimated. A pollution occurs in a semiconductor device, for instance, if implanted ions push oxygen atoms from an isolation layer into the active area of the device [71].

3.2 Monte Carlo Implantation with MCIMPL-II

For a rigorous study of doping profiles for advanced semiconductor devices it is mandatory to consider crystalline materials and arbitrary three-dimensional geometries. The Monte Carlo ion implantation simulator MCIMPL-II was used for the simulation of doping profiles throughout this thesis. Therefore, a brief description of the simulator is presented in this section. The simulator has been developed on the basis of MCIMPL [15] at the Institute for Microelectronics. In contrast to its predecessor, MCIMPL-II has a flexible object-oriented architecture and uses the functionality of the Wafer-State-Server library [72]. MCIMPL-II can be easier extended to new materials, while MCIMPL was originally just designed for the implantation into silicon. Hobler started the project in 1986 by implementing the fundamental physical models and by calibrating the models for the most important dopant species used in silicon technology [73]. Stippel extended the simulator to three dimensions [74] and Bohmayr implemented the Trajectory-Split method [75]. Hössinger included the Follow-Each-Recoil method in MCIMPL [42]. When he designed MCIMPL-II, he replaced the simple data management of MCIMPL by a better handling of the simulation data for a fast point location in heavily non-planar device structures [76]. In the scope of this work, the postprocessing of raw Monte Carlo data in MCIMPL-II was improved, and a grid-generator was implemented to allow a fast simulation of one-dimensional doping profiles which is particularly necessary for calibration purposes.

3.2.1 Basic Features and Principle of Operation

The current status is that MCIMPL-II can be used for one- and three-dimensional implantation applications. Two-dimensional applications can be modeled by using two-and-a-half dimensional device geometries with a small depth dimension. The simulator can handle arbitrarily shaped device structures including overhang structures. The simulated structure can be composed of several amorphous and crystalline material segments. Various amorphous materials can be simulated, for instance, SiO_2 , Si_3N_4 , TiN, or TaN, which are typically used in CMOS processing. Several crystalline material segments can also be used in one simulation domain with the restriction that the crystal orientation has to be identical in all segments. In this work the simulator has been extended from crystalline silicon to $\text{Si}_{1-x}\text{Ge}_x$ alloys of arbitrary germanium content in the range from silicon to germanium. Polycrystalline materials are treated as amorphous materials in which the crystalline structure of the grains is neglected. This is not really a restriction, since low-resistivity polysilicon for gates or interconnects is usually processed by deposition of amorphous silicon, followed by high-dose ion implantation doping, and finishing annealing.

The Monte Carlo calculation of ion trajectories in crystalline targets uses substantially only two random processes. The first one is applied to achieve equally distributed starting points of ion trajectories within the implantation window and the second one is used to imitate the thermal vibrations of the target atoms. While the simulated ion moves through the target the simulator uses locally either a crystalline or an amorphous model for searching the next collision partner of the ion. The application of the amorphous model in crystalline targets is performed with a certain probability which depends on the amount of already generated damage in the crystal. Thus the transition from the crystalline to the amorphous state of a region is taken into account, which is caused by the accumulation of point defects during the implantation process. Note that the Monte Carlo simulation of ion implantation without consideration of

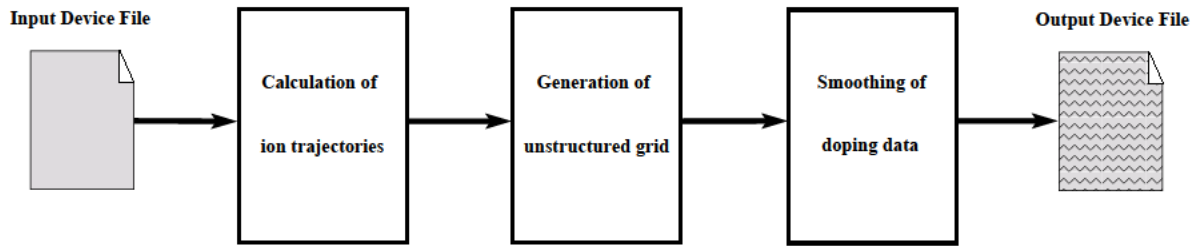


Figure 3.8: Schematic diagram of the Monte Carlo simulation with MCIMPL-II.

damage is a static problem where the passage of time plays no role. In consideration of damage accumulation over time the Monte Carlo simulation becomes dynamic. In order to improve the performance, the simulator uses histogram cells aligned on an orthogonal grid to count the number of implanted ions and of generated point defects. The doping or damage concentration within a cell is obtained by the number of particles contained in the cell divided by the volume of the cell. However, the ion implantation process is accurately simulated by computing a large number of individual ion trajectories in the target. Being based on appropriately scaled random numbers, the results obtained with the Monte Carlo method are never exact, but they converge to the characteristics of the underlying physical models by increasing the number N of simulated ions. The statistical error of Monte Carlo results vanishes for a sample size $N \rightarrow \infty$.

The principle of simulator operation can be grouped into the following three sections:

- Initialization of the internal data structures
- Physical Monte Carlo simulation of ion trajectories
- Transfer of the doping data to an unstructured grid

The input device structure for implantation is provided as a file in the WSS (Wafer State Server) format [77], which contains all geometry and material information of the simulation domain. Thereby the dimension of the simulation is specified by the input WSS file. Additionally, the input file can contain implantation data from previous implantation steps. The implantation conditions and simulation parameters, for instance, the desired number of simulated ions are specified by user defined command-line parameters. A description of the simulator command-line interface is provided in [42]. Fig. 3.8 shows schematically the simplified simulation data flow from the input file to the output file. The simulation is started by initializing the histogram for the Monte Carlo simulation. When histogram cells are set up, they are initialized with data from previous implantation steps and they are continuously updated when damage is generated by an ion. Thereby damage accumulation from several ion implantation steps is automatically considered as well as damage accumulation within a single implantation step. The incoming dopant ions are slowed down due to the nuclear and electronic stopping power of the target material. The final position of an implanted ion is reached where it has lost its kinetic energy. After performing the Monte Carlo calculation of all ion trajectories, the dopants, vacancies and interstitials are stored in histograms. A sophisticated smoothing algorithm based on the Bernstein polynomial approximation [78] is applied in order to reduce the statistical fluctuation of raw Monte Carlo results. The smoothed data are then translated from the internal orthogonal

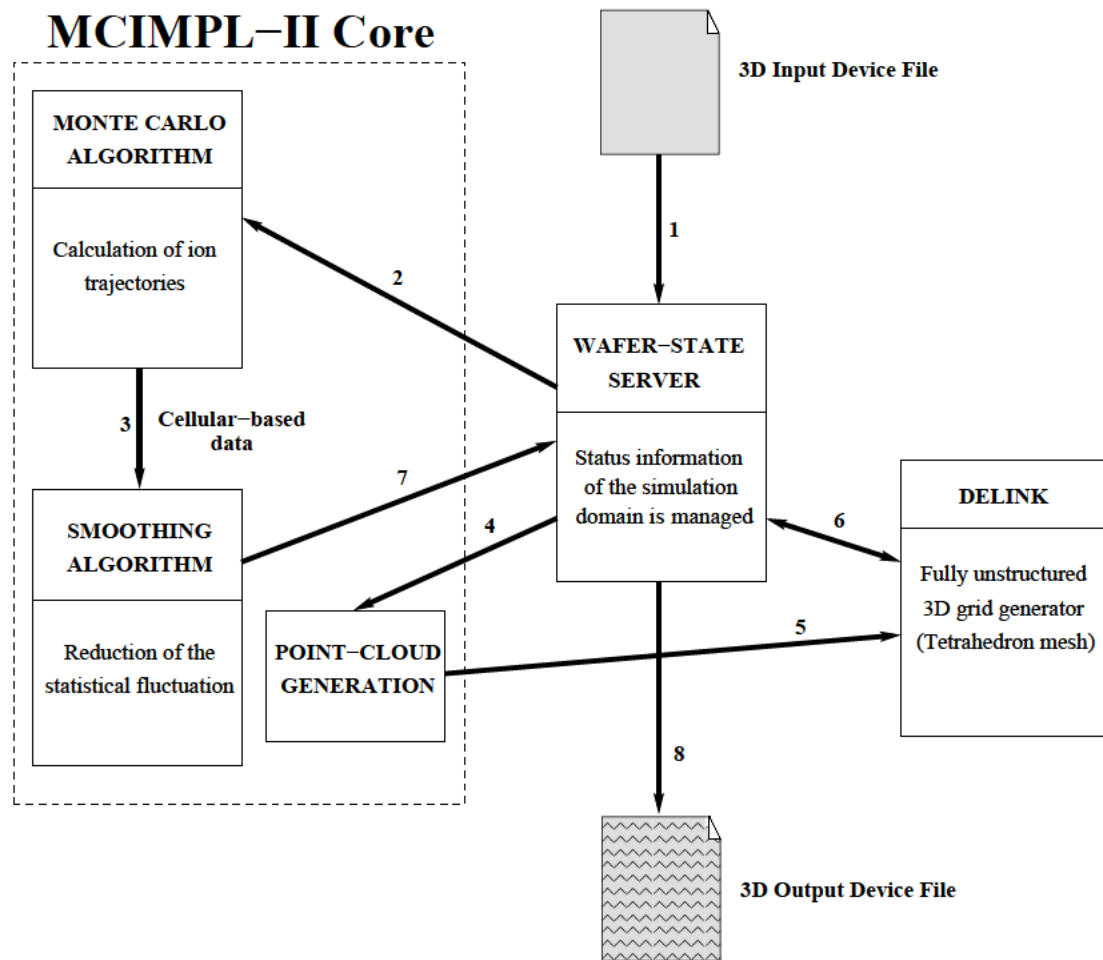


Figure 3.9: Flow of data between the linked software components of MCIMPL-II, consisting of MCIMPL-II Core, Wafer-State-Server, and DELINK.

grid to an unstructured destination grid. The resulting output file contains the smoothed doping and damage profiles which include the implantation results of all already performed implantation steps. This WSS file can then be visualized for analysis purposes and/or it can be used as input file for the subsequent simulation of annealing processes.

The simulator makes use of the Wafer-State-Server functionality not only for reading a WSS file (geometry and attributes request) or WSS file writing (attributes update), but there is also a continuous interaction during the simulation. When an ion moves through the simulation domain, the simulator requires the material type information at the current position of the ion in order to select the appropriate model for the next collision event. The Wafer-State-Server performs a point location and delivers the desired information to the simulator core unit. Lastly, the Wafer-State-Server provides a gridder interface to integrate different grid generators with the simulator. Fig. 3.9 shows the data flow during the three-dimensional simulation of ion implantation in a more detailed way including the Wafer-State-Server and the three-dimensional unstructured grid generator DELINK [79]. A brief description of the Wafer-State-Server based simulation environment and the WSS file format is provided in Appendix A.

3.2.2 Calculation of Ion Trajectories

The core of the simulator performs the calculation of ion trajectories in a three-dimensional manner independent of the dimension of the simulated device structure. An ion trajectory is simulated by successively applying nuclear and electronic stopping processes that slow down the ion motion (as described in Section 3.1). Therefore it is necessary to locate atomic nuclei of the target which collide with the ion projectile. After finding the location of the next collision partner, the parameters of the nuclear and electronic stopping models are determined. The partner dependent parameters for the stopping models are the mass and charge of the target atom, the impact parameter, and the free flight path length between two nuclear collisions. Several physical and numerical models are involved in the trajectory calculation. Each material segment of the simulation domain has assigned its own set of models.

A model set consists primarily of four models selected from the following model classes:

- Partner selection model
- Nuclear scattering model
- Electronic stopping model
- Damage generation model

Initial Conditions

The starting points of the ions are equally distributed within a rectangular implantation window lying in a plane somewhat above the surface of the simulation domain. But instead of selecting the starting points completely randomly, the implantation window is divided into equally sized subwindows and one ion starts from each subwindow. The position of the ion within the subwindow is randomly chosen. This procedure for determining the starting points provides a better statistical equidistribution of the points. Another advantage is that this procedure allows to define a time step for a transient simulation in a very convenient way, which is required for the parallelization of the trajectory calculation. The calculation of the ion trajectories for all subwindows is performed within one time step.

The initial momentum of an ion is determined by the implantation conditions *energy*, and *tilt and twist angles*. In addition a *divergence of the ion beam* can be specified. When a three-dimensional simulation is performed, the simulator assumes that the wafer rotation (twist angle) of 0° is parallel to the x-axis, which means according to the definition of the tilt and twist angle (see Section 2.2.3) that the y-axis is parallel to the primary flat of the wafer.

Selection of Collision Partners

Two different selection strategies exist for crystalline and amorphous materials. In crystalline materials the atoms are placed around their crystal lattice sites due to thermal vibrations. The selection of the target atom which takes part in the next nuclear scattering process is depicted in the left sketch of Fig. 3.10. The ion is located at the beginning of the free flight path L . The actual collision partner among the potential atoms in the direction of motion is that atom which

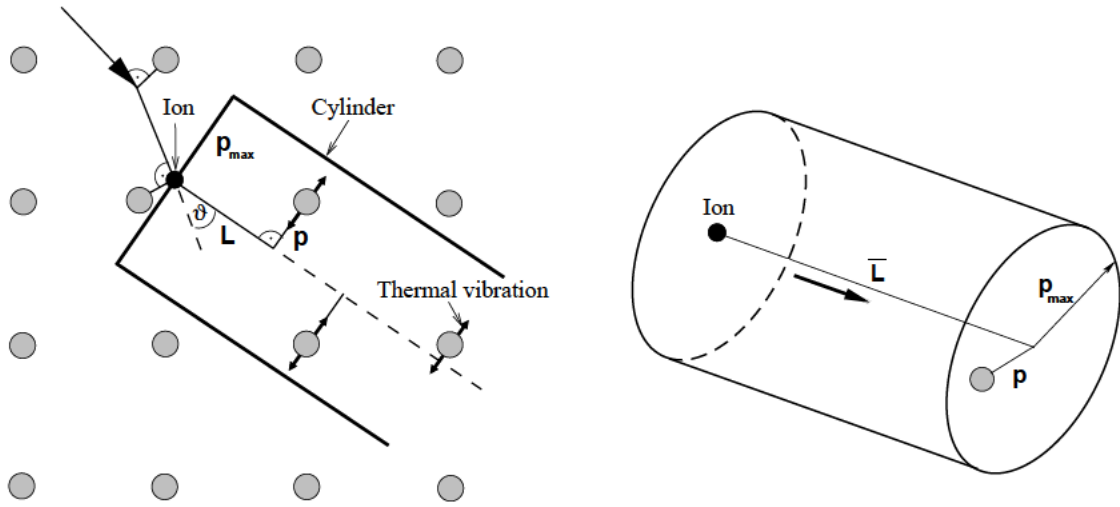


Figure 3.10: Searching for the next collision partners in crystalline materials (left) and cylinder which determines the partner in amorphous targets (right).

leads to the smallest positive free flight path length with an impact parameter p smaller than p_{max} . The maximum impact parameter p_{max} is in the order of magnitude of half of the lattice constant. If two collision partners would lead to almost the same free flight path lengths, the two partners are treated simultaneously based on the BCA method. In this multiple collision the sum of the momenta transferred to the target atoms in individual binary collisions with neighboring atoms is assumed to be the total momentum transferred to the crystal.

The amorphous partner selection model is based on the fact that the atoms in amorphous materials are approximately equally distributed. Therefore only the material density has to be considered by a cylinder with a radius of the maximum impact parameter p_{max} and a length of the average free flight path \bar{L} (as shown in Fig. 3.10) which contains one target atom. The average free flight path is defined according to

$$p_{max}^2 \cdot \pi \cdot \bar{L} = \frac{1}{N_T}, \quad (3.35)$$

where N_T is the atom density in the target. This model uses a constant flight path length \bar{L} and the collision partner is placed in a circular area with the radius p_{max} on a plane perpendicular to the direction of motion with the distance \bar{L} from the actual ion position. The actual amorphous impact parameter p is calculated by using the realization X_i from the set of uniformly distributed random numbers X_1, \dots, X_n in the interval $[0, 1]$ according to

$$p = p_{max} \cdot \sqrt{X_i}. \quad (3.36)$$

The maximum impact parameter p_{max} is determined only by the target atom density:

$$p_{max} = \frac{1}{\sqrt[3]{N_T}}. \quad (3.37)$$

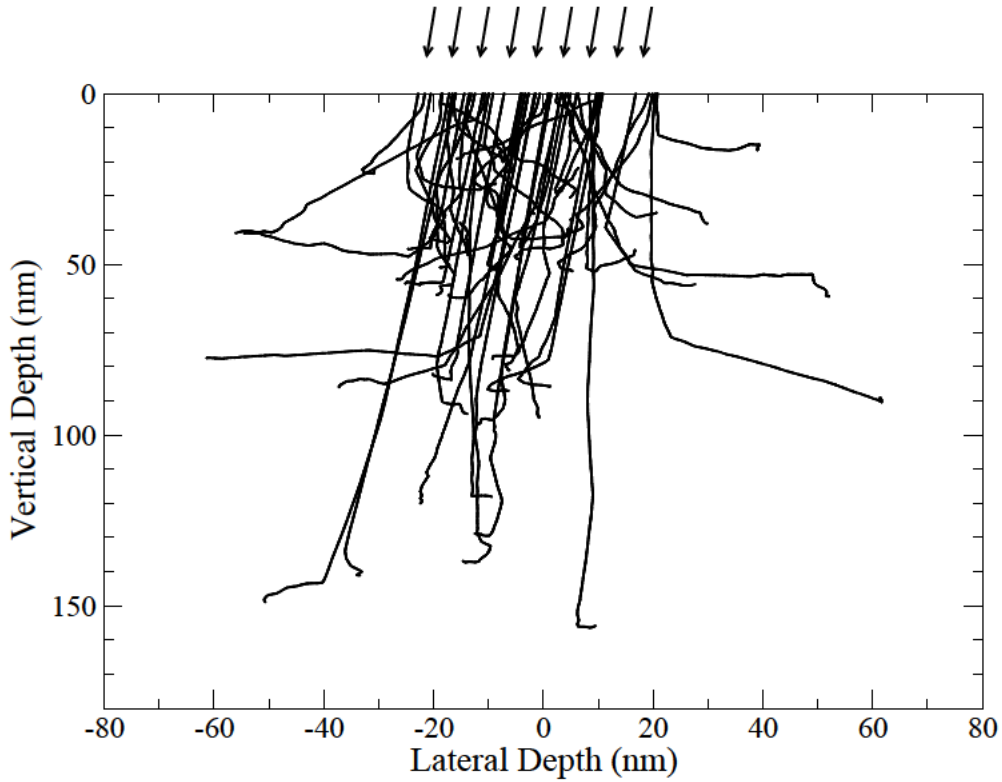


Figure 3.11: Monte Carlo simulation of 50 boron trajectories in crystalline silicon using an energy of 10keV and a tilt of 7°.

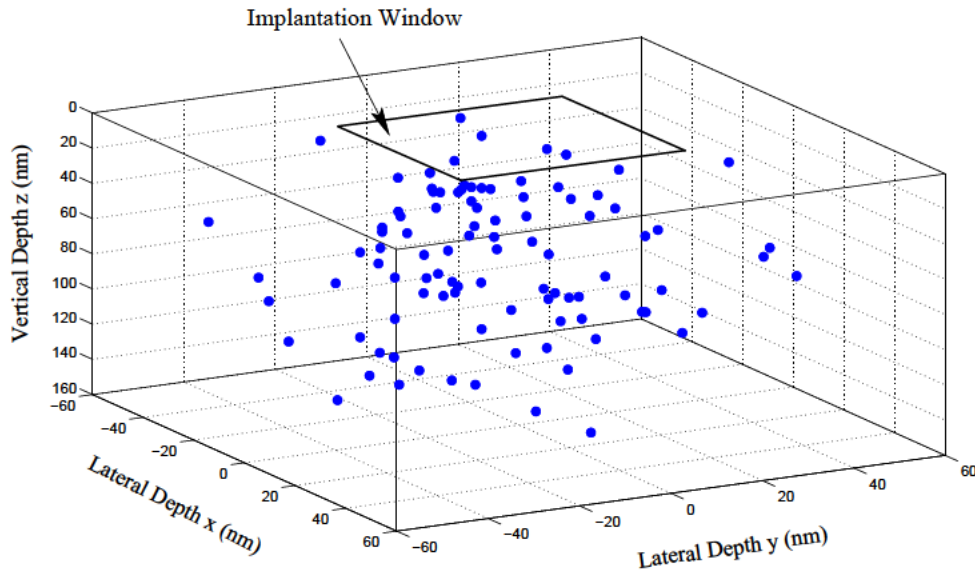


Figure 3.12: Final position of 100 boron atoms implanted with 10keV into silicon.

Nuclear Stopping Process

The nuclear stopping process is simulated with the physical BCA model which is based on the universal ZBL potential (as described in Section 3.1.2). The BCA model contains no tunable parameters and can be applied to all materials. The elastic two-particle scattering process is approximated by its asymptotic behavior and the ion is placed at the closest distance to the collision partner (which is equal to the impact parameter) before the nuclear scattering event. The center-of-mass scattering angle Θ is obtained from a lookup table as a function of the reduced impact parameter \tilde{p} and the reduced energy \tilde{E} which are defined as

$$\tilde{p} = \frac{p}{a_U}, \quad (3.38)$$

$$\tilde{E} = \frac{a_U}{Z_1 Z_2 e^2} \cdot E_c, \quad (3.39)$$

where the universal screening length a_U (3.14) and the transformed energy E_c (3.6) are used. The calculated ion trajectories presented in Fig. 3.11 show the change of the flight direction of ions due to heavy ion-atom collisions (small impact parameter) as well as the retention of the flight direction as ions travel along crystalline channels. The atomic-scale distances between nuclear collision events produce continuously plotted trajectories (every trajectory point

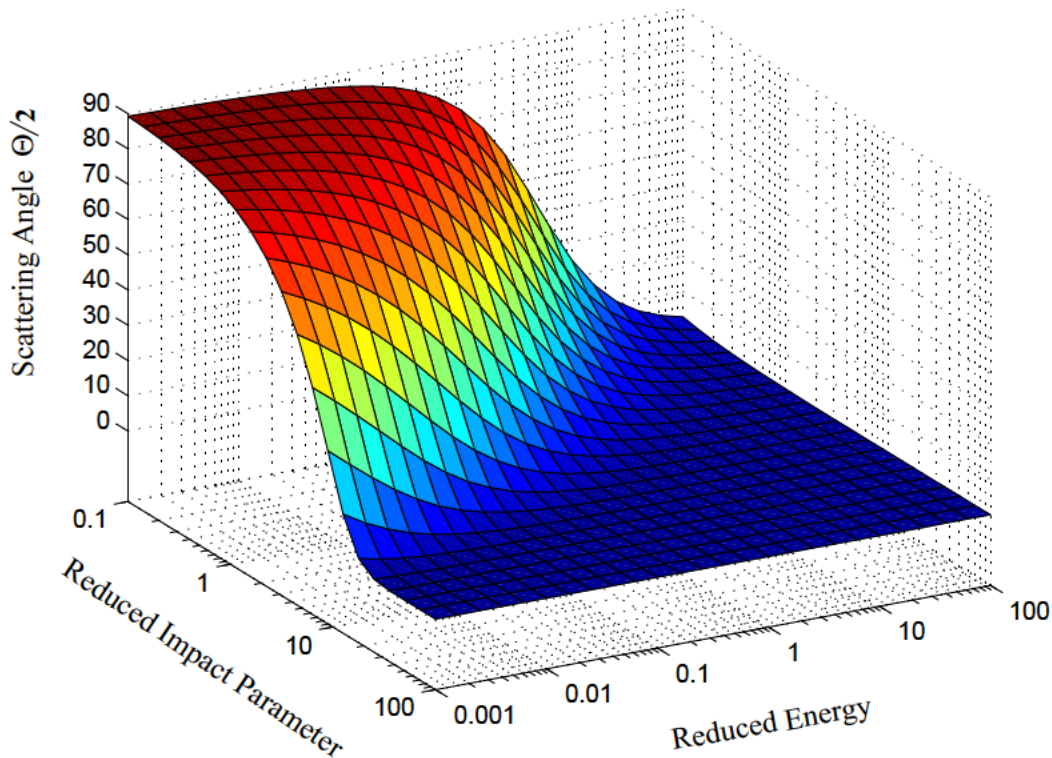


Figure 3.13: Tabulated scattering angle as a function of the scaled quantities impact parameter and energy.

corresponds to a single collision event). Fig. 3.12 shows the simulated distribution of 100 boron atoms in crystalline silicon which are implanted from the implantation window using the same implantation conditions as for the visualized trajectories in Fig. 3.11. The three-dimensional visualization of the tabulated scattering angle is presented in Fig. 3.13 by using a bicubic spline interpolation. The table values of the scattering angle are stored in a data file for 28 energy values and 17 impact parameter values. The surface plot $\Theta(\tilde{p}, \tilde{E})$ revealed that a small impact parameter \tilde{p} and a low energy \tilde{E} of the ion produces strong nuclear scattering ($\Theta/2 \approx 90^\circ$) for a binary collision event while channeling of ions occurs at large impact parameters or at high energies ($\Theta \approx 0^\circ$). The scattering angles of the ion and of the recoil in the laboratory system are calculated from the center-of-mass scattering angle Θ by (3.9) and (3.10), and the transferred energy to the primary recoil atom of a collision cascade is obtained by (3.11).

Electronic Stopping Process

The electronic stopping process is calculated by using the Hobler model described in Section 3.1.3. The only physical parameter required for this electronic stopping model is the impact parameter which is determined in the BCA model when selecting a collision partner. The model requires for every crystalline material a set of four parameters k_{corr} , a_U , y_{nl} , and q for each ion species (Table 3.3). In contrast to MCIMPL, where there is only one set of parameters per ion species for one target material available (since MCIMPL was originally just designed for the implantation into silicon), the model parameters can be independently calibrated for each ion-target combination in MCIMPL-II. Therefore, different crystalline material segments can be used in one simulation domain. Due to the fact that the model implies a dependence on the charge and the mass of the atoms of the target material, the electronic stopping power is averaged in the case of a compound material like SiGe. The contribution of each atom species is considered according to the stoichiometry of the material. In addition, a special treatment is applied for multiple collisions. While the non-local part of the electronic stopping model is considered only once, the local contribution to the electronic stopping process is calculated once for each binary collision which is part of the multiple collision event.

Ion species	Charge	Mass	k_{corr}	a_U	y_{nl}	q
Boron	5	11.009	1.75	0.450	0.050	0.230
Nitrogen	7	14.006	1.6861	0.4364	0.3177	0.1101
Oxygen	8	15.994	1.55	0.099	3.193E-5	0.97
Fluorine	9	18.998	0.9	0.6586	0.08	0.0
Silicon	14	27.977	1.4	0.4	0.12	0.1
Phosphorus	15	30.994	1.2674	0.4212	0.1447	0.0253
Germanium	32	72.59	1.15	0.3	0.3	0.0
Arsenic	33	74.92	1.1316	0.3056	0.2991	0.0243
Indium	49	114.82	1.1	0.3	0.5	0.0
Antimony	51	120.9	1.1	0.3	0.5	0.0
Xenon	54	131.3	1.1	0.3	0.5	0.0

Table 3.3: Empirical parameters for the electronic stopping process in silicon.

Ion species	f_{rec}	N_{sat} (cm^{-3})
Boron	0.139	$4 \cdot 10^{21}$
Phosphorus	1.0	$2 \cdot 10^{22}$
Arsenic	2.1	$5 \cdot 10^{22}$

Table 3.4: Recombination model parameters for different dopant species in silicon.

Calculation of Damage Production

The calculation of implantation induced point defects in crystalline materials is performed with the computationally efficient modified Kinchin-Pease damage model in combination with the Hobler recombination model as described in Section 3.1.4. The ion species dependent parameters of the empirical recombination model (Table 3.4) are stored in common with the parameters of the electronic stopping model in an ASCII data file. This file contains one data record for each combination of ion species and target material which holds all empirical parameters including the atomic number and atomic mass of the ion species.

Fig. 3.14 compares simulated boron profiles for 20keV channeling implantations in (100) silicon (shown by continuous lines) to SIMS measurements for the doses of 10^{13} , 10^{14} , and 10^{15}cm^{-2} . The one-dimensional profiles were obtained with one million simulated particles using an ion

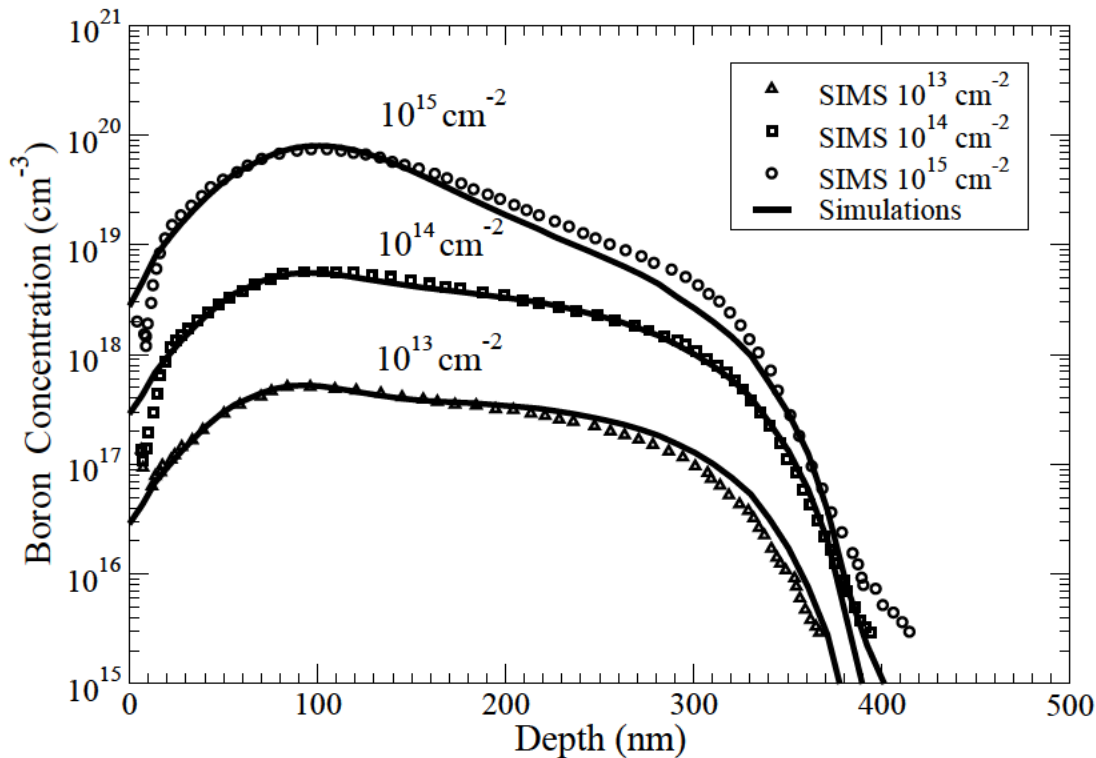


Figure 3.14: Illustration of the dose dependence for boron profiles using an energy of 20keV and a tilt of 0° , simulated with the Kinchin-Pease model.

beam divergence of $\pm 1^\circ$ in the simulations. It can be observed that the shape of the boron profiles is significantly influenced by the produced crystal damage. The accumulation of point defects with increasing implantation dose is well reproduced by the combined damage modeling approach based on the generation and recombination of point defects. It should be noted that the assumption of a native oxide film of 1nm thickness on the wafer surface is necessary to obtain a good agreement between boron simulation results and experimental data.

3.2.3 Speed-up Algorithms

The atomic-scale simulation of ion implantation processes using a Monte Carlo method is one of the most time-consuming computational tasks in semiconductor process simulation. On the one hand side, dramatically shrunk geometries of advanced devices require highly accurate simulation results by computing a very large number of ion trajectories and, on the other hand side, applications with higher implantation energies produce long trajectories in large-volume simulation domains. Three speed-up methods can be employed for the trajectory calculation in three-dimensional applications to get shorter simulation runtimes without losing accuracy:

- Trajectory-Split method
- Trajectory-Reuse method
- Parallelization of trajectory calculation

Trajectory-Split Method

The simulation of ion implantation produces a statistical distribution of the implanted dopant ions (in initial ion direction and lateral), where most of the simulated ions come to rest at a penetration depth close to the projected range in the target. For instance, regions with a dopant concentration of three orders of magnitudes smaller than the maximum concentration are reached just by one of thousand implanted ions. The statistical accuracy of simulation results becomes even worse in regions with lower dopant concentrations, since a reasonable simulation result includes three to five orders of the dopant concentration. At least some implanted particles have to be counted even in histogram cells located in peripheral regions with a very low concentration level of dopants, since no significant information can be derived from a histogram cell which contains only one implanted particle.

The basic idea of the Trajectory-Split method is to increase the number of ion trajectories that end up in regions with a bad statistical representation of dopants by splitting a particle trajectory [42, 80]. The splitting of a particle produces several particles with the same physical properties as the original particle but with a reduced weighting factor. The increase in the number of dopants, vacancies, and interstitials caused by a splitted particle are multiplied with the weighting factor before they are stored in the corresponding histogram. While the simulation of a molecular ion is performed with a weighting factor larger than one to account for statistical identical particles of the same atom species in the molecule [81], the weighting factor has to be below one for a splitted elemental ion to conserve the total implantation dose. The build-up of a trajectory tree is implemented by the full calculation of a primary trajectory and determining of the split points along this trajectory according to various rules. Afterwards a new trajectory

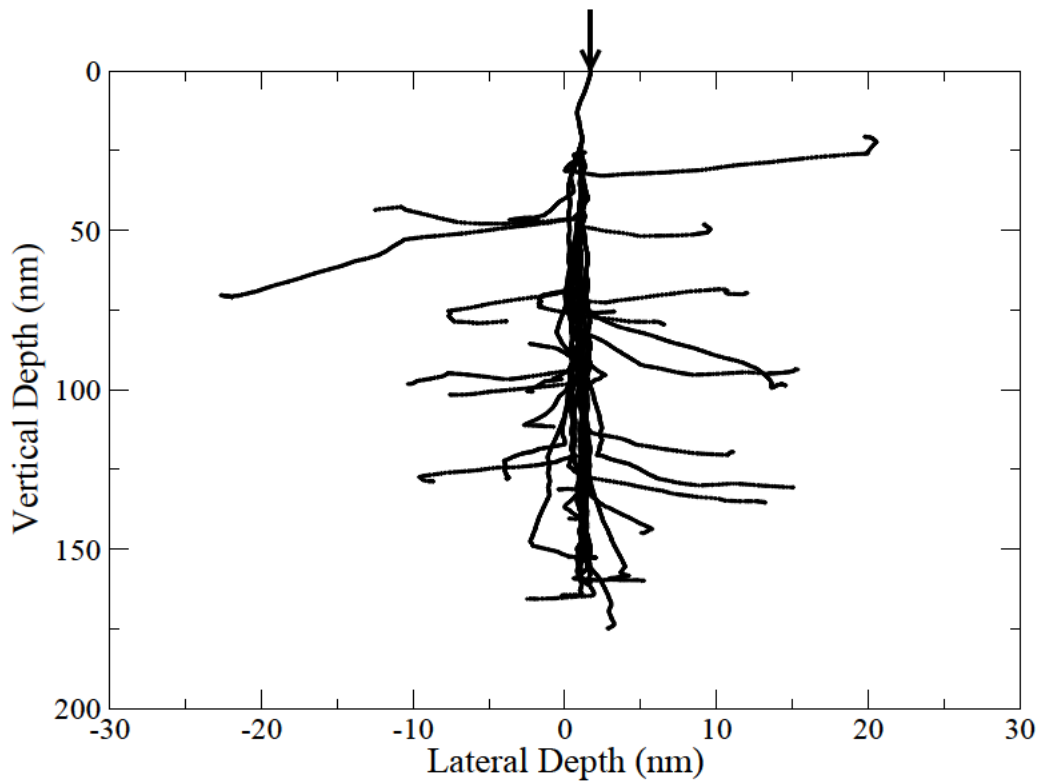


Figure 3.15: Monte Carlo simulation of a boron trajectory tree with a split depth value of 5, an energy of 10keV, and a tilt of 0° in crystalline silicon.

is calculated from every split point up to the end point. In crystalline materials the vibration of the lattice atoms guarantees that two branches of a trajectory tree are not identical after a split point despite equal initial conditions at the split point. The effect of the Trajectory-Split method is that one implanted particle delivers several effective ions which share the same initial part of the trajectory. Therefore less initial ions are required to get a simulation result with the same statistical accuracy. The sharing of parts of a trajectory reduces the average calculation time for trajectories of effective ions. The visualized boron trajectory tree, shown in Fig. 3.15, has a split depth of five, which corresponds to 2^5 trajectories with a particle weight of 2^{-5} . Finally, it should be noted that the Trajectory-Split method is typically applied for crystalline materials to reduce long computation times and to improve the statistical accuracy of doping profiles in the channeling tail region.

Trajectory-Reuse Method

The basic idea of the Trajectory-Reuse method is to use the fact that different regions of the simulation domain behave identical with respect to the trajectory calculation [42]. Therefore it is possible to calculate a trajectory only once and to copy it to other regions. The copying of trajectories can be interpreted as spreading one-dimensional simulation results over a two- or three-dimensional simulation domain as far as possible. In terms of trajectory calculation two

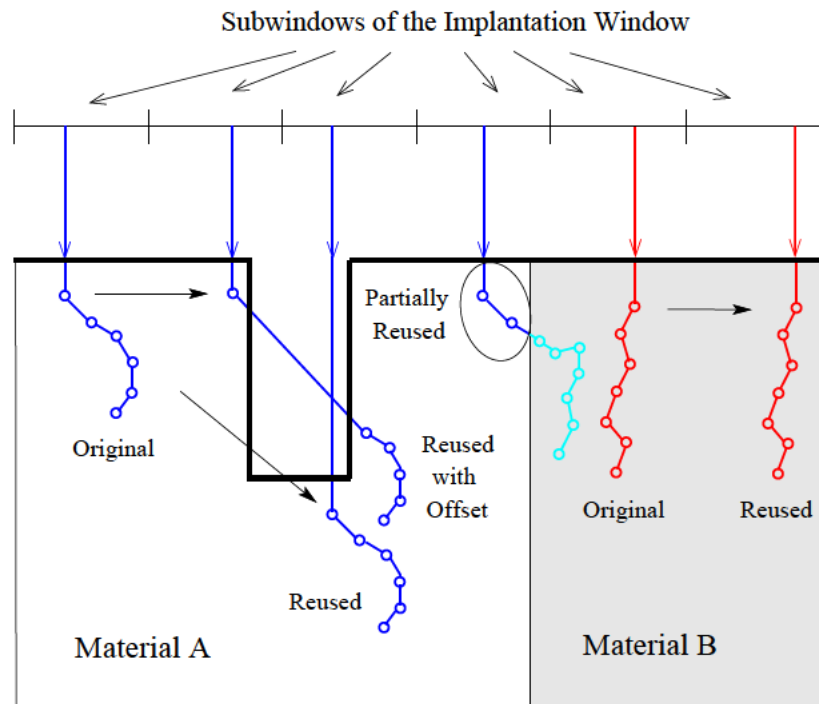


Figure 3.16: Illustration of the Trajectory-Reuse method for two different materials.

regions are considered identical, if all material properties that influence the particle motion are equal along the complete trajectory. In the case of amorphous materials only the density and composition of the material are considered in the simulation, while in the case of crystalline materials the trajectory is also influenced by the damage distribution in the material. Therefore the Trajectory-Reuse method can only be applied to amorphous materials, because regions with an exactly identical damage distribution along the complete trajectory are very improbable. They exist only for an initially undamaged crystal structure.

Fig. 3.16 demonstrates how the Trajectory-Reuse method works for a trench structure and for crossing the boundary between two amorphous materials A and B. As described in Section 3.2.2 the implantation window is subdivided into subwindows and one ion is started from each subwindow during every time step. The Trajectory-Reuse algorithm splits a calculated trajectory which goes through different materials into several sub-trajectories, one for each amorphous material, and stores the obtained sub-trajectories in a list. All parts of a calculated trajectory in crystalline materials are neglected. When the next ion is started, the algorithm searches through the stored trajectory list. The target material of a stored trajectory must be identical to the entrance material of the ion and the ion energy must be less than the energy loss ΔE along a stored trajectory. A new trajectory is calculated and added to the trajectory list, if no suitable trajectory is available in the list.

The Trajectory-Reuse method improves significantly the simulation speed for three-dimensional implantation applications, since large regions of MOS transistor structures are typically composed of amorphous materials. Finally, it should be noted that the performance gain of this method increases with decreasing subwindow size.

Parallelization of Trajectory Calculation

The three-dimensional Monte Carlo simulation of ion implantation requires fairly long simulation run-times to achieve accurate simulation results in complex target structures, which can be in the order of several days on a modern computing environment. The simulation performance can be significantly improved by parallelization of the trajectory calculation. Two parallelization strategies can be used in principle for the trajectory calculation:

- Parallel computing on a cluster of workstations
- Parallel computing on a shared-memory multiprocessor system

A parallelization method based on the Message Passing Interface (MPI) was implemented in MCIMPL [82]. The intention was to perform a distributed simulation on a cluster of workstations which are connected over a slow network. The simulation domain was geometrically distributed among several workstations which have to exchange only a small amount of data during the simulation. Due to the distribution of the memory requirement among several workstations, small workstations could be used for three-dimensional simulations.

However, the current status of the object-oriented simulator MCIMPL-II is that the trajectory calculation is implemented only in a sequential manner. For future work, a powerful parallelization of the simulator can be achieved by using OpenMP based parallel computing on a shared-memory multiprocessor architecture [83]. The OpenMP standard provides a portable standard parallel API specifically for programming shared-memory multiprocessor systems. This standard supports also an *incremental parallelization* by adding compiler directives to the source code. The execution of the simulation program on one multiprocessor workstation ensures a more reliable operation for longer simulation runs compared to a network based MPI solution. The damage accumulation during the simulation has to be considered for parallel computing of trajectories. Only a small error occurs, if the trajectories for all subwindows of the implantation window are computed in parallel using the initial damage distribution of the current time step. At the end of the time step, it has to be ensured that the newly generated damage is updated in the shared internal data structures before proceeding with the next time step.

3.2.4 Postprocessing of Monte Carlo Results

After the calculation of the desired number of ion trajectories, the doping information is stored in histogram cells aligned on an orthogonal grid. Each histogram cell contains a certain number of implanted ions, and the doping concentration within a cell is given by the number of ions divided by the volume of the cell. The statistical nature of the Monte Carlo implantation process produces a statistical fluctuation in the obtained raw cellular doping information. In particular, three-dimensional Monte Carlo implantation results have inherently large variances in the peripheral regions. An advanced smoothing technique based on a Bernstein polynomial approximation has been developed [14, 84–86] in order to transfer the cellular data to an unstructured destination grid which is suitable for the subsequent process simulation step. Finite element simulations are used in the next simulation step to imitate thermal annealing processes which are required to activate the dopants and to eliminate the substrate damage. On the one hand side, the postprocessing procedure performs the necessary interpolation operation, and on the other hand side, it reduces the statistical noise of the obtained doping and damage data.

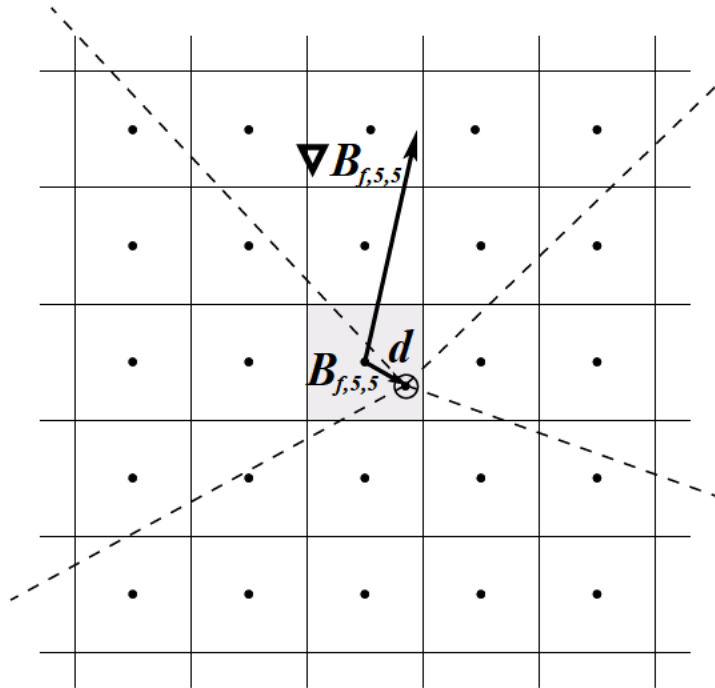


Figure 3.17: Illustration of the smoothing operation performed for one point of the new unstructured grid in a two-dimensional example. The orthogonal lines confine the cells of the internal grid. The four dashed lines denote the unstructured grid, where the new point is marked by a small circle. In the first step the 5^2 sample points are used to calculate the concentration $B_{f,5,5}$ at the middle of the central grey cell. Then the scalar product of the gradient $\nabla B_{f,5,5}$ and the offset vector \mathbf{d} is calculated to estimate a value for the delta concentration.

Advanced Smoothing Algorithm

The postprocessing procedure starts by invoking the mesh generator DELINK [79] and passing over a point cloud in common with all interfaces and surfaces present on the Wafer-State-Server to discretize the doping distribution. As a result, the mesh generator produces a tetrahedral mesh which is approximately aligned to the surface and which is fine enough to resolve the doping profile. This mesh is handed over to the Wafer-State-Server where the doping information is added to the points (Fig. 3.9). Therefore, the Wafer-State-Server calls the Bernstein approximation operation provided by the MCIMPL-II core module for each point of the new mesh.

The smoothing of the Monte Carlo result is performed by approximating the doping concentration value for a grid point of the unstructured grid by means of Bernstein polynomials defined in a cubical surrounding space [85]. The Bernstein polynomial $B_{f,n,n,n}(x_1, x_2, x_3)$ approximates a function f of 3 variables, where $n \in \mathbf{N}$ are the concentration sample points in each dimension. The Bernstein approximation $B_{f,n,n,n}$ is specified by n^3 sample points, whereby $B_{f,n,n,n}$ does not run through the sample points, but each of them affects the approximated function. The sample points are also referred to as control points, since they enforce the progression of the

multivariate function. A critical issue is that the calculation of the Bernstein approximation requires a reasonable information in all sample points. In order to fulfill this requirement, the concentration value of a cell which contains no doping information (empty cell) is determined by averaging over the values of non-empty neighboring cells. Due to the fact that the evaluation of the Bernstein polynomial at an arbitrary point is computationally very expensive, the polynomial is only calculated for the middle point $(\frac{1}{2}, \frac{1}{2}, \frac{1}{2})$ of the domain $[0, 1]^3$. For that special point the Bernstein polynomial can be significantly simplified according to the formula given in (3.40) which enables a fast computation of the approximated value.

$$B_{f,n,n,n} \left(\frac{1}{2}, \frac{1}{2}, \frac{1}{2} \right) = \sum_{k_1=0}^n \sum_{k_2=0}^n \sum_{k_3=0}^n f_{k_1,k_2,k_3} \binom{n}{k_1} \binom{n}{k_2} \binom{n}{k_3} \left(\frac{1}{2} \right)^{3n}. \quad (3.40)$$

The drawback of this simplification method is that the obtained approximated value is independent of the given point position somewhere in the cell. This drawback is eliminated by also calculating the derivative of the Bernstein polynomial at the center of the cell and modifying the approximated value according to this local gradient as shown in Fig. 3.17. Therefore, the concentration difference $\Delta B_{f,n,n,n}$ between the new point and the cell middle point is calculated by the system of equations (3.41), (3.42) and (3.43) and added to the approximated value $B_{f,n,n,n}$ at the cell middle point. Equation (3.43) points out that it is possible to calculate the required three partial derivatives in a fast way too.

$$\Delta B_{f,n,n,n} = \nabla B_{f,n,n,n} \cdot \mathbf{d}, \quad (3.41)$$

$$\nabla B_{f,n,n,n} = \frac{\partial}{\partial x_1} B_{f,n,n,n} \mathbf{e}_1 + \frac{\partial}{\partial x_2} B_{f,n,n,n} \mathbf{e}_2 + \frac{\partial}{\partial x_3} B_{f,n,n,n} \mathbf{e}_3, \quad (3.42)$$

$$\frac{\partial}{\partial x_i} B_{f,n,n,n} \Big|_{\left(\frac{1}{2}, \frac{1}{2}, \frac{1}{2}\right)} = \sum_{k_1=0}^n \sum_{k_2=0}^n \sum_{k_3=0}^n f_{k_1,k_2,k_3} \binom{n}{k_1} \binom{n}{k_2} \binom{n}{k_3} \cdot \left(\frac{1}{2} \right)^{3n} (4k_i - 2n). \quad (3.43)$$

Analysis of the Smoothed Simulation Result

For the analysis of the implemented smoothing algorithm, numerical experiments were performed with the simulator MCIMPL-II on a three-dimensional structure equivalent to a one-dimensional problem. It is assumed that all simulated ions are statistically independent. Fig. 3.18 shows the three-dimensional phosphorus implantation result in a crystalline silicon substrate for $N = 4 \cdot 10^6$ simulated ions. The corresponding statistical fluctuation of the phosphorus concentration as a function of the penetration depth z is visualized in Fig. 3.19 for the unstructured grid. Each sample consists of the concentration values C_1, C_2, \dots, C_n located in a horizontal plane $z = \text{const}$. The one-dimensional doping profile is derived by calculating the mean concentration value $\bar{C}(n) \Big|_{z = \text{const}}$ for each sample. The standard deviation $S(n)$ of a sample defined by the values of n grid points in a plane $z = \text{const}$ is given by (3.44). The relative standard deviation σ of the dopant concentration in a horizontal plane according to (3.45) is a measure for the simulation error of three-dimensional results compared to one-dimensional results.

$$S(n) \Big|_{z = \text{const}} = \sqrt{\frac{1}{n-1} \sum_{i=1}^n [C_i - \bar{C}(n)]^2}, \quad (3.44)$$

$$\sigma \Big|_{z = \text{const}} = \frac{S(n)}{\bar{C}(n)}. \quad (3.45)$$

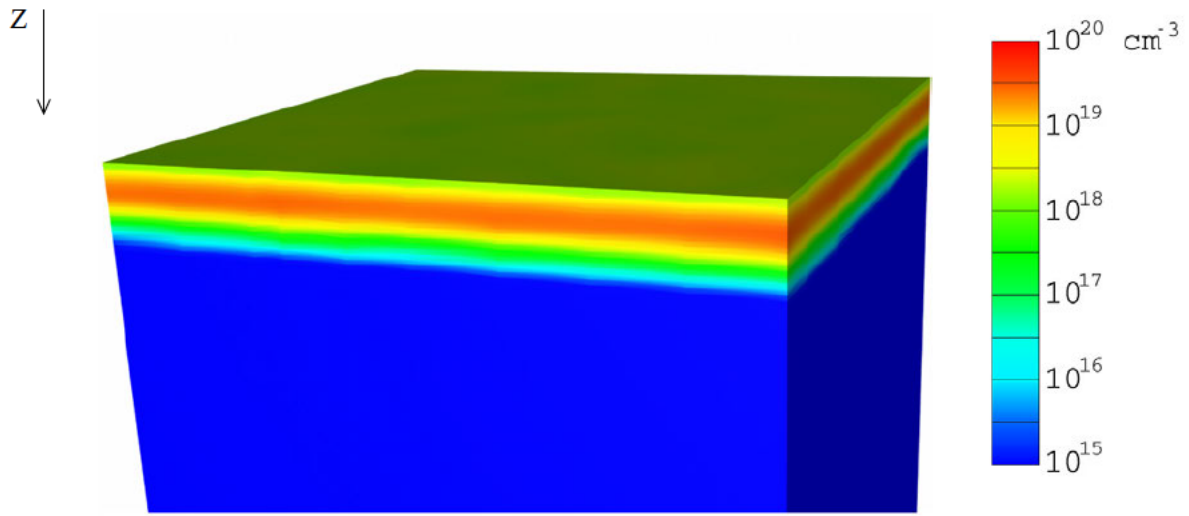


Figure 3.18: Smoothed result of a phosphorus Monte Carlo implantation in silicon, using $4 \cdot 10^6$ simulated ions, an energy of 25keV, and a dose of 10^{14} cm^{-2} .

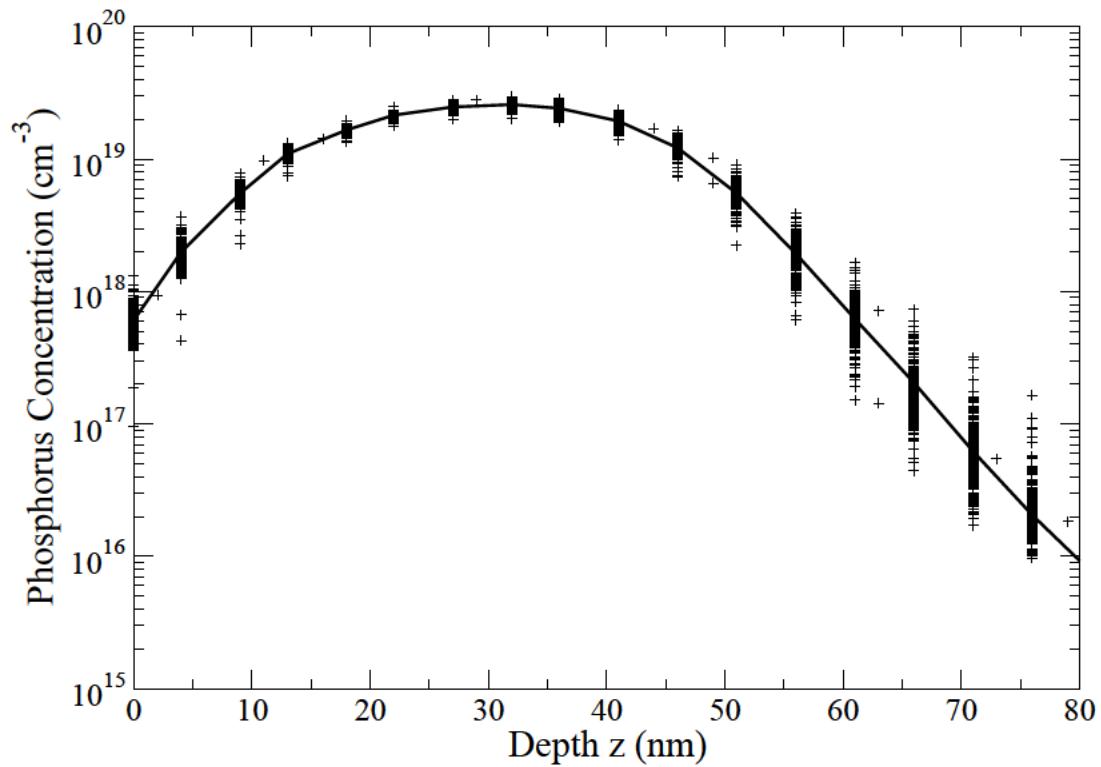


Figure 3.19: Fluctuation of the smoothed three-dimensional dopant distribution and the corresponding one-dimensional doping profile.

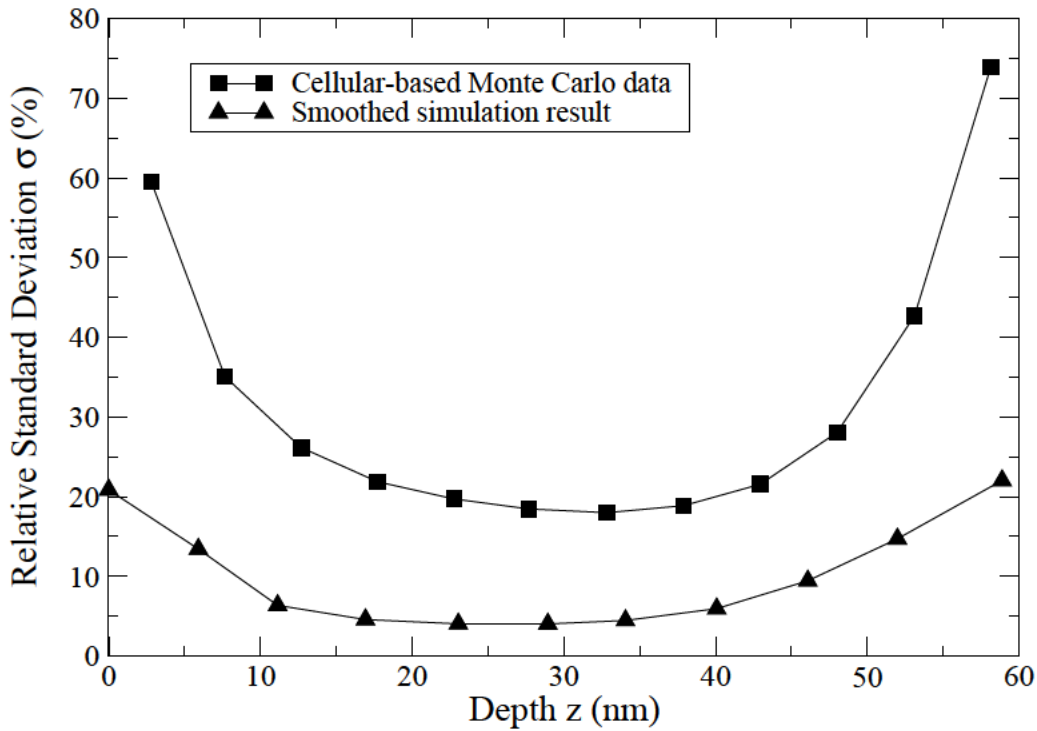


Figure 3.20: Improvement of the simulation accuracy by the smoothing procedure.

Fig. 3.19 depicts that the sample variance becomes minimal around the projected range R_p , since most of the ions come to rest there. For the evaluation of the postprocessing improvement the ratio of the maximal standard deviation σ_{\max} within the range $2 \cdot \Delta R_p$ (twice the straggling at the mean projected range) of the doping profile, after and before smoothing, can be used. As shown in Fig. 3.20, $\sigma_{\max, \text{after}} / \sigma_{\max, \text{before}} \approx \frac{1}{4}$ within $2 \cdot \Delta R_p = 22 \text{nm}$ at $R_p = 30 \text{nm}$.

$$\sigma_{\max} \propto \frac{1}{\sqrt{N}}. \quad (3.46)$$

The theoretical simulation error σ_{\max} of the Monte Carlo method follows from the Central Limit Theorem [59]. Equation (3.46) has been expectedly verified by simulation experiments with different N . In order to reduce σ_{\max} by $\frac{1}{4}$, one has to increase N by a factor of 16. But as shown in Fig. 3.20, a significant improvement of the statistical accuracy can also be achieved by sophisticated postprocessing, in particular through the filtering effect of the Bernstein polynomials, which eliminates high-frequency fluctuations from the original Monte Carlo data.

The linear approximation of the delta concentration value $\Delta B_{f,n,n,n}$ between the grid point of the unstructured grid and the cell middle point reduces the effect of the cell discretization. The left diagram of Fig. 3.21 shows the smoothed doping profile generated by the Bernstein approximation without using the additional gradient-based approximation step. The internal cell dimension of 5nm produces equal concentration values for the first two samples. The right diagram shows the doping profile obtained by using the advanced smoothing technique. The advanced algorithm produces a smoother and therefore a more realistic doping profile. Longer simulation run times or worse statistics would arise, if the cell dimension of the simulator is further reduced to enhance the internal resolution. In contrast to that, the used smoothing

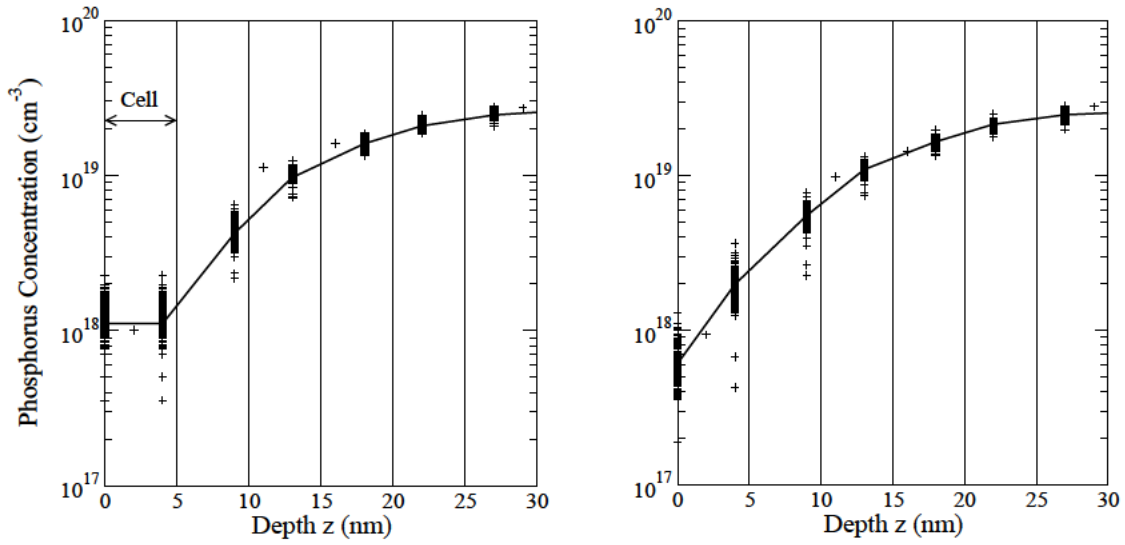


Figure 3.21: Smoothing without (left) and with (right) linear approximation step.

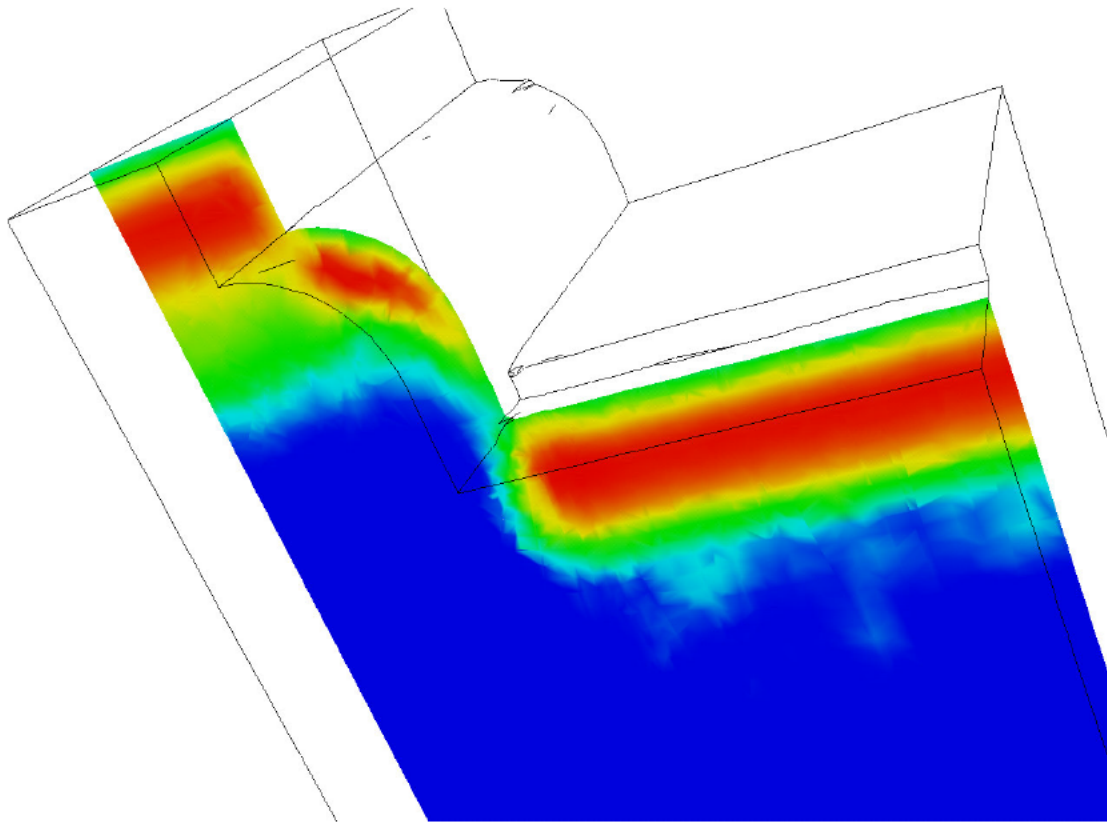


Figure 3.22: Implantation of arsenic ions into a complex device structure with an energy of 70keV and a dose of $3 \cdot 10^{15} \text{ cm}^{-2}$.

technique improves the accuracy of three-dimensional Monte Carlo implantation results in a computationally efficient way.

Being based on random numbers, the results obtained with the Monte Carlo technique are never exact, but rigorous in a statistical sense. Therefore, a confidence interval can be constructed for the one-dimensional doping profile shown in Fig. 3.19 in order to estimate the error of the mean in a plane $z = \text{const}$ [59]. The relationship (3.46) can also be used to estimate the number of initial ions N required to obtain a specific precision in a Monte Carlo simulation study. For the calculation of the required number N as a function of the desired maximum standard deviation σ_{\max} , a parameter γ is used which takes the dopant species and the implantation energy into account. The following formula can be used to estimate the number N for an implantation window size A and a desired precision σ_{\max} :

$$N = \gamma \frac{A}{A_0} \frac{1}{\sigma_{\max}^2}, \quad (3.47)$$

where $A_0 = 0.455 \mu\text{m}^2$ is the investigated top surface area of the simulation domain shown in Fig. 3.18, and the parameter $\gamma = 15992$ for a phosphorus implantation with an ion energy of 25keV [86]. Note that the computational effort of three-dimensional implantation applications grows proportionally to the implantation window size in order to maintain a certain statistical accuracy of the simulation results.

Fig. 3.22 shows the smoothed Monte Carlo implantation result. The arsenic source/drain implantation was performed with an energy of 70keV and a dose of $3 \cdot 10^{15} \text{cm}^{-2}$ into a modern MOS transistor structure. The simulation was carried out with 2000000 initial ions and the default split-depth of five to demonstrate the fluctuation of the resulting dopant distribution. It is recommended to use at least 2000000 ions/ μm^2 , otherwise the simulation result is inacceptably inaccurate due to statistical fluctuations.

3.2.5 Three-Dimensional Demonstration Example

The presented simulation example explains the accomplishment of three-dimensional implantation applications with the simulator MCIMPL-II in principle. For complex targets it is advantageous to add the desired unstructured output grid for the implantation result already to the input structure used for the ion implantation simulation rather than to generate the output grid on-the-fly as shown in Fig. 3.8. This approach allows to manually adjust the grid refinement for a specific application. A simulation application typically includes the following steps:

- Generation of the device geometry in the WSS format
- Addition of the unstructured grid to the geometry
- Simulation of the ion implantation step (with the option *reuse grid*)

Fig. 3.23 shows the non-planar oxide mask and the unstructured grid used in the implantation example. The two-segment geometry consisting of *silicon* and *oxide* was generated with the three-dimensional solid modeler LAYGRID [87]. LAYGRID reads its input from a text file which contains the geometric structure represented by layers and polygons, and some properties of the used materials. Each layer is defined by a two-dimensional mask and a layer thickness.

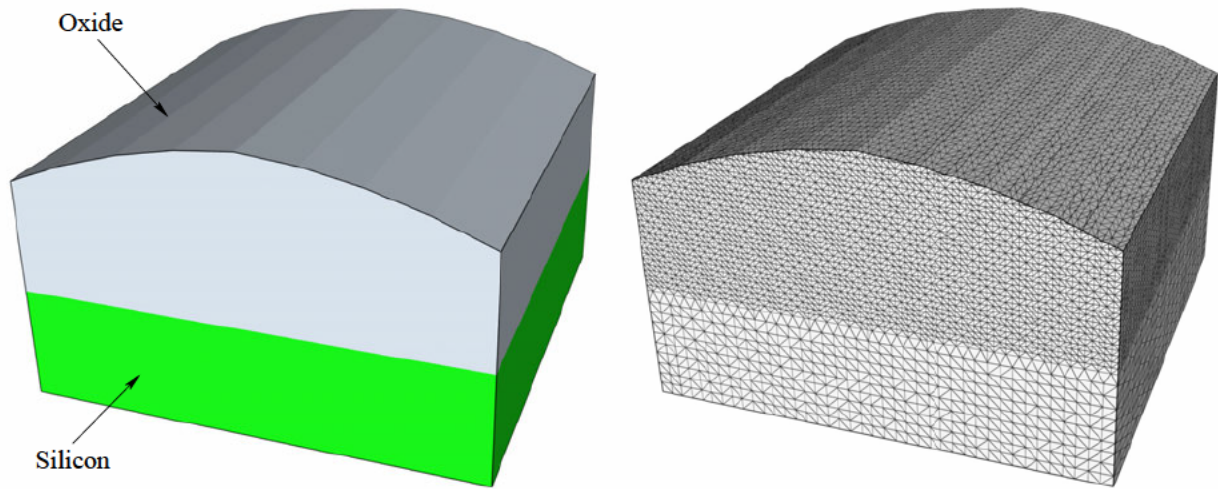


Figure 3.23: Non-planar two-segment structure (left) and unstructured grid (right).

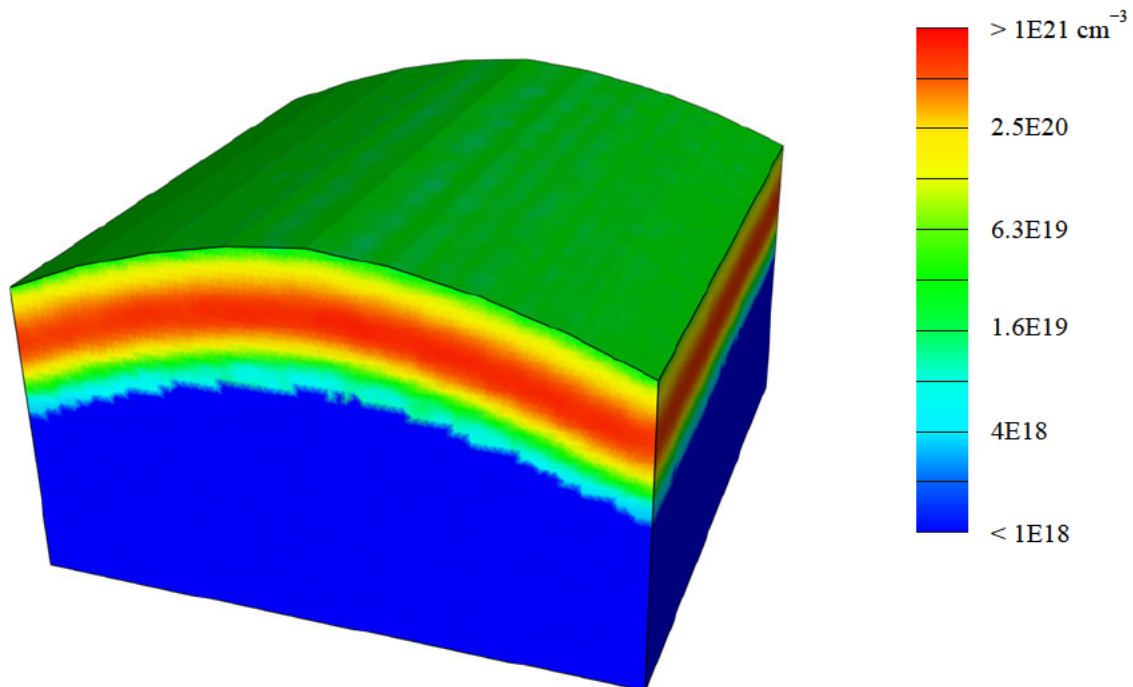


Figure 3.24: Boron implantation result in the non-planar oxide mask performed with an energy of 20keV and a dose of $5 \cdot 10^{15} \text{ cm}^{-2}$.

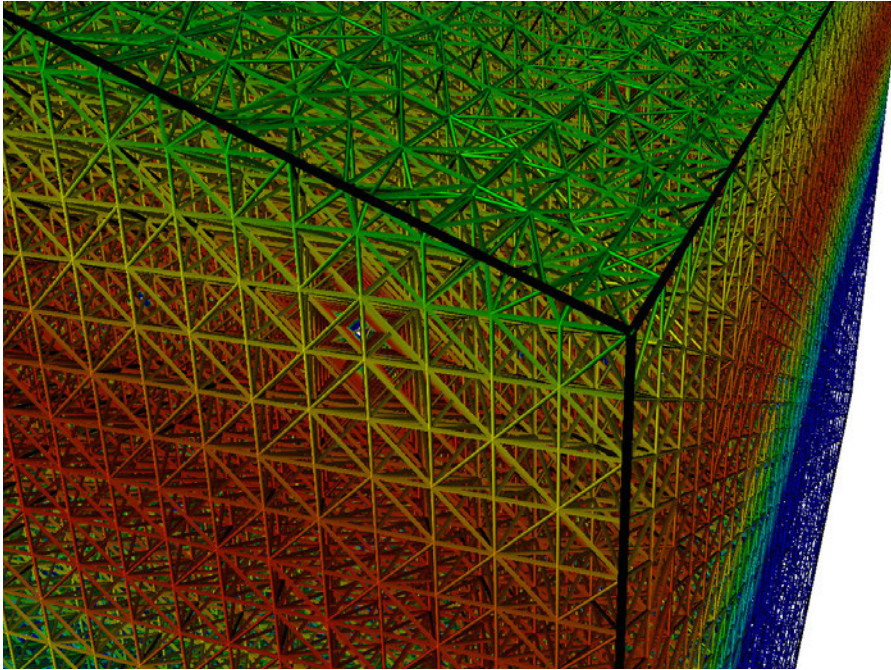


Figure 3.25: Visualization of the boron result and the grid lines in a geometry corner.

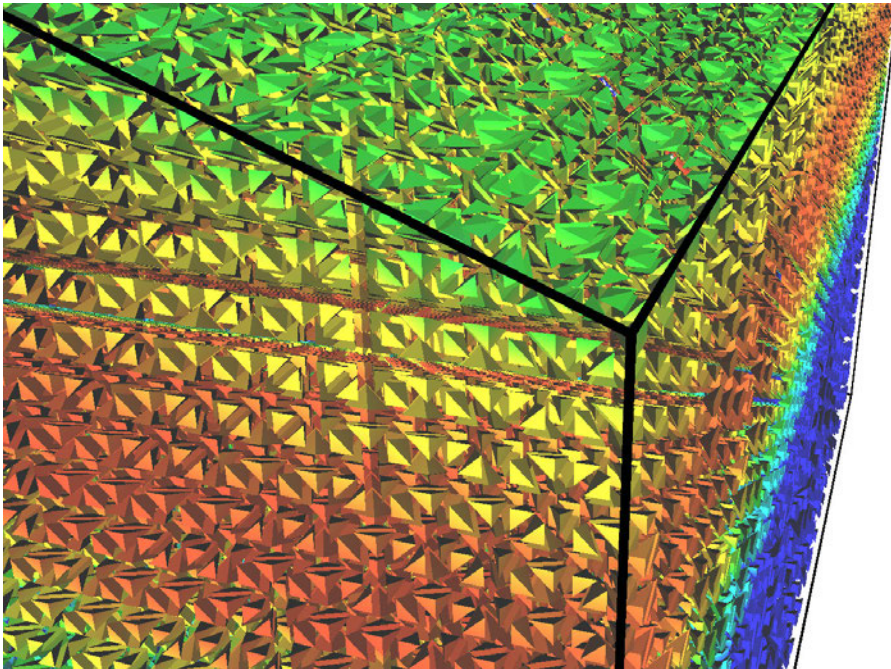


Figure 3.26: Visualization of the boron result and the tetrahedral elements which are shrunk to 40% of their original size.

The thickness is always constant for ideally planarized structures and for non-planar layers it is necessary to define a three-dimensional surface area. A layer mask definition contains the geometry information and material references of all included material segments. The resulting geometry is then written to a WSS file. The visualized grid in Fig. 3.23 has been added to the WSS file by the mesh generator DELINK with the *box refinement method*. This method allows to control approximately the distance of the grid points in the x , y , and z direction within a specified box-shaped container. A finer grid resolution is used up to the expected maximum penetration depth of the boron distribution. Fig. 3.24 shows the implanted boron distribution in the oxide mask which has been produced by 25 million simulated ions without using the splitting of trajectories. In this application, the implantation window of approximately $0.7\mu\text{m}^2$ is divided into 36 subwindows which requires to start 694445 ions per subwindow. An internal histogram resolution of 10nm was used to discretize a cuboid region (internal simulation domain) of the input geometry. The upper limit of the discretization cuboid is determined by the highest position of the oxide mask surface and the lower limit is derived by the estimated maximum penetration depth of 400nm from the lowest oxide mask surface position. Fig. 3.25 shows the grid lines and Fig. 3.26 the tetrahedral elements located in the zoomed-in right upper corner on the front side of the geometry. For the final boron result, 99754 grid points and 564887 tetrahedrons are used.

Chapter 4

Doping of Group-IV-Based Materials

While the first transistor was developed in 1947 by using germanium as the semiconductor material and GaAs devices have demonstrated high switching speed, it is silicon which completely dominates the present semiconductor market. This development has arisen due to the low cost of silicon CMOS technology. The fabrication processes and the device performance rely heavily on a number of natural properties of silicon, for instance, the availability of a good oxide. For alternative semiconductor materials much more expensive fabrication processes must be used, whereby the phenomenal yields achievable on a silicon CMOS line cannot be reached. One drawback of silicon is its relatively small carrier mobility. Since the device speed depends on how fast the carriers can be transported through the device channel under sustainable low operating voltages, silicon can be regarded as a relatively slow semiconductor. Today, it is commonly believed that a further improvement in the channel mobility beyond those that can be achieved with process-induced strain will be required in order to maintain continued commensurate device scaling. The higher carrier mobility offered by group-IV materials like SiGe compounds, germanium, and various heterostructures, for instance, biaxially strained silicon on relaxed SiGe, are required as new channel materials for bulk and on-insulator implementations [88–90].

While ion-implanted doping profiles are well studied in silicon for various dopant species and implantation conditions, such doping profiles are scarce in SiGe alloys as well as in pure Ge. An accurate and multi-dimensional simulation of ion implantation processes is required to optimize the doping profiles in these semiconductor materials for high-performance CMOS applications and optoelectronic devices. Since quantitatively predictive capabilities are a must for a Monte Carlo ion implantation simulator, the used models for implantations into silicon have been evaluated to extend the simulator to this wide class of materials on the basis of experimental results. For calibration purposes, a set of specifically selected experiments for arsenic and boron implantations into SiGe virtual substrates with different Ge content has been developed and carried out. Additional experimental results from other research groups obtained by arsenic and boron implantations into strained Si, relaxed SiGe layers with high Ge contents, and into Ge wafers have been included. The doping profiles in the investigated non-silicon materials are always compared to a reference doping profile in silicon, implanted under the same conditions. On the basis of these experiments various effects which influence the dopant distribution (e.g. Ge content in the alloy, damage accumulation, channeling effect) can be analyzed independently. The extended simulator is able to accurately predict the doping profiles in germanium and in SiGe alloys of arbitrary Ge content, and to estimate the produced point defects.

4.1 Silicon-Germanium Alloys

Silicon-germanium (SiGe) is a IV-IV compound semiconductor which offers enhanced carrier mobility and a higher dopant solubility compared to pure silicon. The remarkable potential of the SiGe material arises from the possibility to modify its properties by altering the composition. For instance, the band gap decreases from 1.12eV (pure silicon) to 0.66eV (pure germanium) at room temperature. The lattice parameter of the germanium crystal is 4.2% larger than that of silicon. Relaxed SiGe has a lattice parameter value which lies between those of the endpoint elements silicon and germanium depending on the Ge content in the alloy. Crystalline SiGe can be grouped into the two categories relaxed and strained. Strain engineering is used to enhance the carrier mobility for MOS transistors. By building different kinds of Si-SiGe heterostructures various properties for device design can be optimized. When silicon is epitaxially grown on SiGe, silicon forms a strained layer configuration up to a certain critical thickness. A strained SiGe layer can be grown on silicon in a similar way. A strained-Si/relaxed-SiGe structure produces tensile strain which primarily improves the electron mobility, while compressive strain obtained by a strained-SiGe/relaxed-Si structure boosts the hole mobility. Although the quality of SiGe virtual substrates or bulk wafers has steadily improved over the last years, the defect density is still too large to guarantee a reasonable yield in CMOS processing at present time [91].

4.1.1 Modeling of Ion Implantation in SiGe Alloys

The simulation of ion implantation in silicon with MCIMPL-II is based on general physical models which are explained in Section 3. Nevertheless, some of the models used for the trajectory calculation have to be extended or the change of an empirical parameter value is sometimes required in order to extend the simulation capabilities to SiGe alloys [92–94]. Precise material data and many SIMS profiles are used for the investigation of ion implantation.

Crystalline Partner Selection Model

Silicon and germanium, which both crystallize in the diamond lattice structure, are completely miscible forming $\text{Si}_{1-x}\text{Ge}_x$ solids with x ranging from 0 to 1. The most precise and comprehensive investigation of bulk lattice parameters and densities for $\text{Si}_{1-x}\text{Ge}_x$ alloys for x from 0 to 1 with Ge intervals of 5% has been carried out by Dismukes et al. [95]. We extended the target materials of the simulator MCIMPL-II from crystalline silicon to the class of $\text{Si}_{1-x}\text{Ge}_x$ alloys and germanium by adjusting the lattice parameter $a(x)$ of the crystalline model by

$$a(x) = 0.02733 x^2 + 0.1992 x + 5.431 \quad (\text{\AA}) \quad \text{for} \quad 0 \leq x \leq 1. \quad (4.1)$$

While Vegard's law determines the $\text{Si}_{1-x}\text{Ge}_x$ lattice parameter only by a linear interpolation between the lattice parameters of the endpoint elements silicon and germanium, equation (4.1) takes the small departure from Vegard's law into account [96]. The parabolic relation (4.1) for the lattice parameter as a function of the Ge content x is derived from measurement values in [95] and approximates the experimental data with a maximum deviation of about 10^{-3}\AA . The deviation from Vegard's law has been confirmed in a recent study on SiGe epitaxial layers on (100) silicon substrates analyzed by X-ray diffraction and Rutherford backscattering [97].

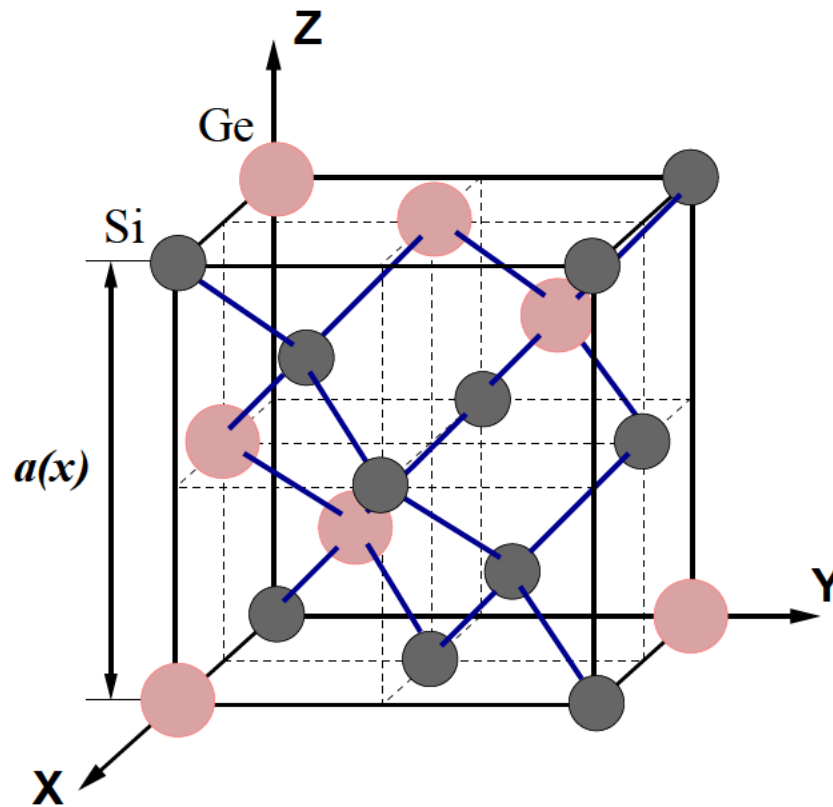


Figure 4.1: Local crystal model used for the simulation of ion implantation in Si, $\text{Si}_{1-x}\text{Ge}_x$ alloys of arbitrary Ge content, and pure Ge ($0 \leq x \leq 1$).

While the ion moves through the simulation domain, a local crystal model (as shown in Fig. 4.1) is built up around the actual ion position for searching the next collision partner. The selection of the target atom species for a collision event in $\text{Si}_{1-x}\text{Ge}_x$ targets is performed by probability x for germanium and $1 - x$ for silicon, respectively. This random choice of the atom species in the crystalline model is acceptable, because no ordering has been observed in bulk SiGe crystals and ordering mechanisms in epitaxial grown SiGe layers are still under investigation.

Table 4.1 summarizes some important physical properties relevant for ion implantation in silicon, germanium, and $\text{Si}_{1-x}\text{Ge}_x$ alloys with $x = 0.25$, $x = 0.5$, and $x = 0.75$. A linear interpolation between the endpoint elements silicon and germanium is used to derive the values for

Properties	Si	$\text{Si}_{0.75}\text{Ge}_{0.25}$	$\text{Si}_{0.5}\text{Ge}_{0.5}$	$\text{Si}_{0.25}\text{Ge}_{0.75}$	Ge
Mass (amu)	28.09	39.2175	50.345	61.4725	72.6
Atomic density (cm^{-3})	$5.02 \cdot 10^{22}$	$4.855 \cdot 10^{22}$	$4.712 \cdot 10^{22}$	$4.566 \cdot 10^{22}$	$4.418 \cdot 10^{22}$
Density (kg/m^3)	2329.11	3161.85	3939.23	4661.86	5326.69
Lattice constant (\AA)	5.431	5.4825	5.5374	5.5958	5.6575
Debye temperature (K)	640	573.5	507	440.5	374

Table 4.1: Approximation of SiGe material properties at 300K for ion implantation.

the average atomic mass and the Debye temperature in SiGe for different compositions. The values of the SiGe lattice parameter were calculated by using the quadratic approximation (4.1). The lattice parameter at a Ge concentration x , $a(x)$, determines the atomic density $N(x)$ for $\text{Si}_{1-x}\text{Ge}_x$ according to (4.2). Finally, the $\text{Si}_{1-x}\text{Ge}_x$ material density $\rho(x)$ is obtained by inserting equation (4.2) into equation (4.3) and by proportionately averaging over the atomic weights of silicon and germanium, M_{Si} and M_{Ge} .

For the simulation with MCIMPL-II the properties of an arbitrary SiGe material segment can be uniquely defined in the input WSS file by specifying the three quantities *molecular formula (composition)*, *material density*, and *crystal orientation*.

$$N(x) = \left(\frac{2}{a(x)} \right)^3 \cdot 10^{24} \quad (\text{Atoms/cm}^3), \quad (4.2)$$

$$\rho(x) = N(x) \left[(1-x) M_{\text{Si}} + x M_{\text{Ge}} \right] \cdot \text{amu} \cdot 10^6 \quad (\text{kg/m}^3). \quad (4.3)$$

Thermal lattice vibrations in silicon are considered in the crystalline partner selection model by using the Debye model with a Debye temperature value of 490K, as described in Section 3.1.2. Table 4.1 shows that germanium has a smaller Debye temperature value of 374K which corresponds to a smaller average vibration amplitude of the 2.6 times heavier germanium atom. We found by a comparison of simulated and measured implanted profiles that the model parameter value of 490K used for the simulation of silicon can also be applied for SiGe targets of arbitrary composition and pure germanium. Note that the used parameter value of 490K is close to the average value of the theoretical Debye temperatures in silicon and in germanium.

Nuclear and Electronic Stopping Power

The total stopping process of the ions in the target solid is modeled as a sequence of alternating nuclear and electronic stopping processes, as explained in Section 3.1.2 and in Section 3.1.3. The inverse transformation of the scattering integral (3.8) leads, amongst others, to (4.4) which determines the scattering angle ϑ of the ion in the laboratory system. The scattering angle ϑ depends on the scattering angle Θ in the center-of-mass coordinate system, on the mass M_1 of the ion, and on the mass M_2 of the involved atomic nucleus of the SiGe target.

$$\tan \vartheta = \frac{\sin \Theta}{\frac{M_1}{M_2} + \cos \Theta}. \quad (4.4)$$

From (4.4) it can be derived that if the ion is heavier than the target atom ($M_1 > M_2$), a maximal scattering angle $\vartheta_{\max} < 90^\circ$ exists according to

$$\sin \vartheta_{\max} = \frac{M_2}{M_1}. \quad (4.5)$$

For instance, if an arsenic ion hits a silicon atom then $\vartheta_{\max} = 22^\circ$, and if the arsenic ion hits the heavier germanium atom, a larger maximal scattering angle $\vartheta_{\max} = 69^\circ$ is possible. Due to the fact that the angles of subsequent collisions have to be added up for a turn around from the incident direction, the backscattering probability for dopant ions increases with the germanium content in the alloy.

The electronic stopping process is calculated with the empirical Hobler model. The only physical parameter required for this model is the impact parameter which is determined when selecting a collision partner. Due to the fact that the model implies a dependence on the charge and the mass of the atoms of the target material, the electronic stopping power is averaged in the case of a compound material like SiGe. The electronic stopping power of SiGe is larger compared with silicon, which is caused by the higher electron density due to the electron-rich germanium atom [98]. The calibration of the model for $\text{Si}_{1-x}\text{Ge}_x$ targets was performed by arranging the Lindhard correction parameter k_{corr} as a linearly rising function of the germanium fraction x . For the other three parameters of the model the values from crystalline silicon could be applied. We found the relations (4.6) and (4.7) by comparing simulated profiles with SIMS profiles, which determine the parameters $k_{As}(x)$ for arsenic and $k_B(x)$ for boron.

$$k_{As}(x) = 1.132 + 1.736 x , \quad (4.6)$$

$$k_B(x) = 1.75 + 0.375 x . \quad (4.7)$$

It is difficult to calibrate the electronic stopping model based on SIMS depth profiles for a couple of reasons. First of all, ion implantation experiments from different research groups exhibit a wide variation in results. Ziegler compared 48 papers on the range distributions of boron implantations in silicon and found a factor of about 2 for the variation in experimental results [17]. With sputter-profiling techniques, the first 10–20nm of the dopant concentration profile cannot be measured correctly due to transient sputtering effects such as preferential sputtering and implantation of the incident ions, which changes the total sputtering yield and distorts the profiles somewhat. Furthermore, it is fundamentally difficult to measure arsenic profiles in SiGe due to the presence of a severe mass interference at ^{75}As by ^{74}GeH [99]. Therefore, it is not possible to characterize arsenic profiles in SiGe by SIMS analysis with a resolution larger than about three orders-of-magnitudes below the maximum arsenic concentration.

4.1.2 Simulation Results and Discussion

We have studied the implantation of arsenic as an n-type and boron as a p-type dopant in crystalline SiGe layers with different germanium content. Fig. 4.2 shows simulated and measured arsenic implant profiles in $\text{Si}_{1-x}\text{Ge}_x$ layers with a thickness of 150nm on a silicon substrate. All implantations were performed with an energy of 60 keV, a dose of 10^{11} cm^{-2} , a tilt of 7° , and a twist of 15° . Two effects of the germanium content on the dopant profiles can be observed. Firstly, with increasing germanium fraction there is a shift towards shallower profiles. Secondly, the germanium content produces a stronger decline of the dopant concentration compared to silicon. It has been pointed out by interpretation of (4.5) that the heavier germanium atom produces an increased backscattering probability for the ions. The electronic stopping power of $\text{Si}_{1-x}\text{Ge}_x$ increases with the germanium fraction x and, therefore, causes a stronger decline of the concentration profiles. Fig. 4.3 demonstrates the successful calibration of the simulator for 38keV and 60keV arsenic implantations in $\text{Si}_{0.65}\text{Ge}_{0.35}$, using otherwise the same implantation conditions. The implanted boron profiles in SiGe layers with 53%, 63%, and 86% germanium content are very similar. Fig. 4.4 shows the simulated and measured result for a 20keV boron implantation into $\text{Si}_{0.47}\text{Ge}_{0.53}$. A native oxide of 1nm on the wafer surface was taken into account. Fig. 4.5 demonstrates again the effect of the germanium content on 5keV boron profiles. SiGe facilitates the forming of shallow junctions, but the trend to shallower profiles is non-linear.

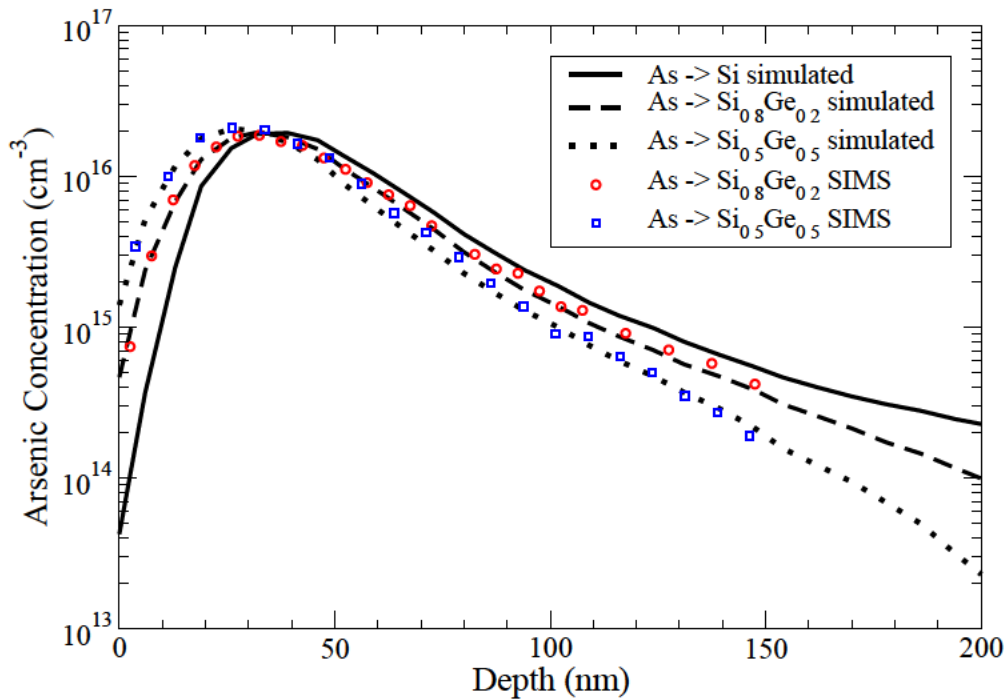


Figure 4.2: Simulated 60keV arsenic concentration profiles in (100) Si_{1-x}Ge_x layers with $x = 0, 20\%, 50\%$ compared to smoothed SIMS data.

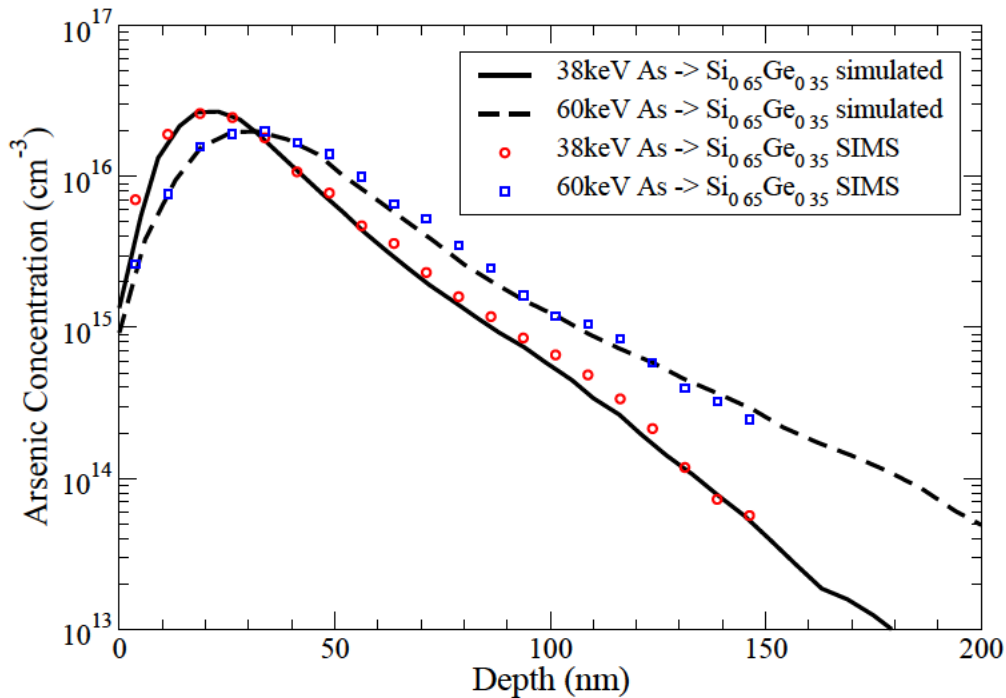


Figure 4.3: Simulated 38keV and 60keV arsenic profiles in (100) Si_{0.65}Ge_{0.35} layers compared to smoothed SIMS data.

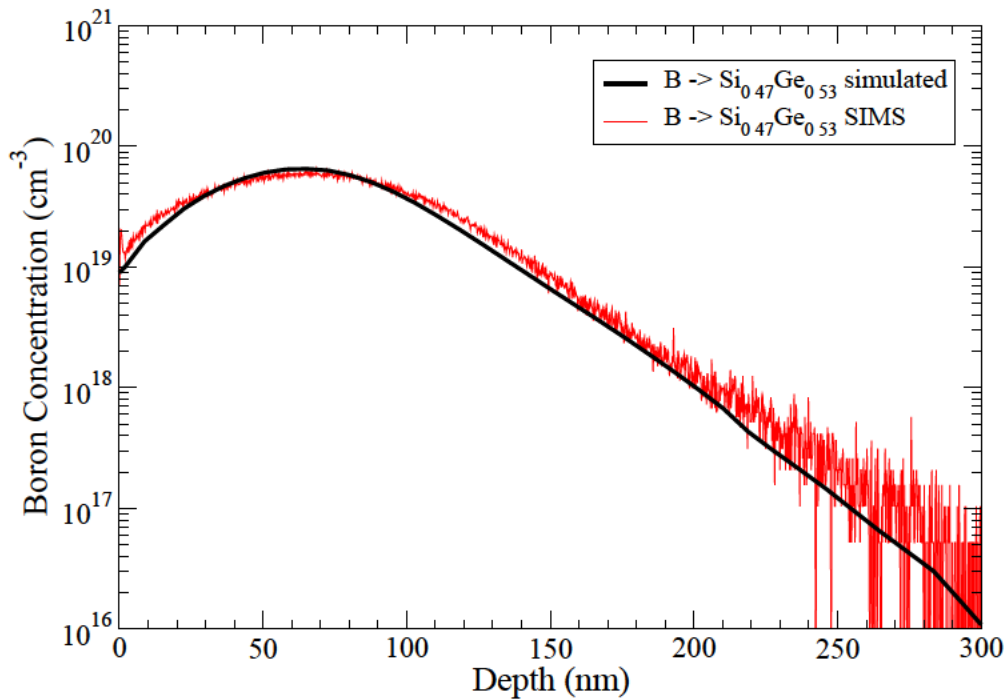


Figure 4.4: Simulated 20keV boron implant profile in (100) $\text{Si}_{0.47}\text{Ge}_{0.53}$ using a dose of $6 \cdot 10^{14} \text{cm}^{-2}$ and a tilt of 7° compared to SIMS.

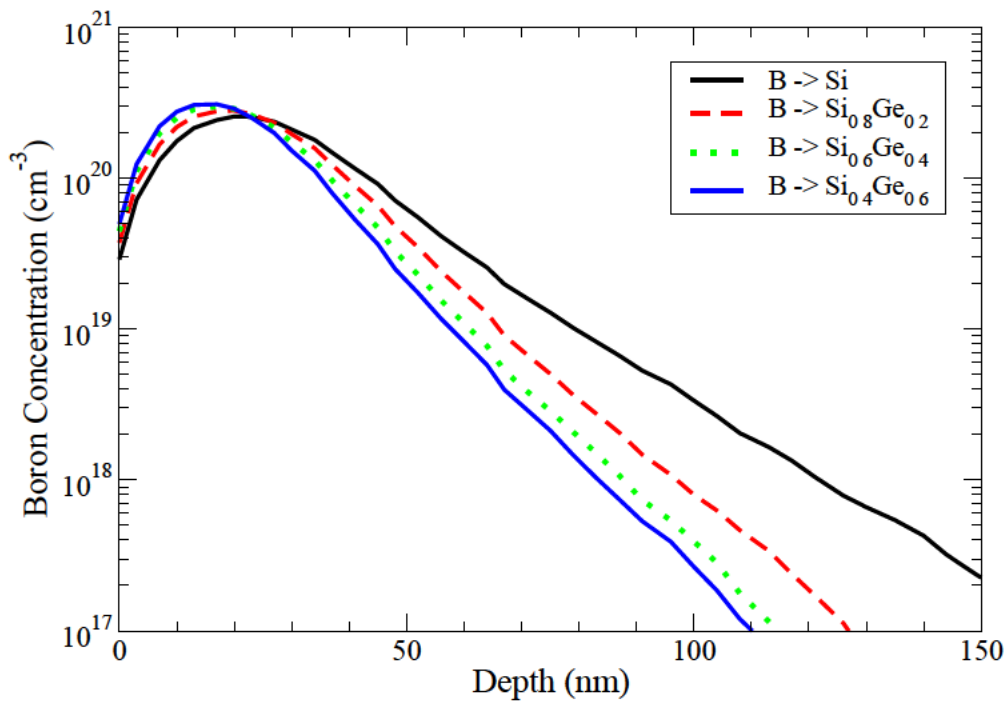


Figure 4.5: Simulated 5keV boron profiles in (100) $\text{Si}_{1-x}\text{Ge}_x$ with $x = 0, 20\%, 40\%, 60\%$ using a dose of 10^{15}cm^{-2} and a tilt of 7° .

4.2 Strained-Si/SiGe Heterostructure

Despite scaling the channel lengths into the sub-50nm regime, carrier mobility continues to be a critical parameter in scaled MOS devices and carrier transport remains far from ballistic [90]. This is partly because the mobility is degraded by increased channel doping (as predicted by the ITRS roadmap in Table 1.1 in Section 1.3). Strained silicon provides an attractive platform for building high-performance CMOS applications due to mobility enhancements compared to unstrained silicon. It turned out that strain-induced enhancements persist even at high channel doping levels, studied up to a dopant concentration of $6 \cdot 10^{18} \text{cm}^{-3}$ [100]. There are two dominant methods, global and local stress, for introducing strain in the silicon surface channel. Both methods produce changes in the silicon bandstructure due to breaking of the crystal symmetry, and hence alter carrier scattering and effective masses. Global stress techniques employ epitaxial technology to generate a thin layer of strained silicon on a thick relaxed $\text{Si}_{1-x}\text{Ge}_x$ layer. Local stress relies on process techniques such as modifications to shallow trench isolation, high-stress nitride-capping layers around the gate, and selective epitaxial $\text{Si}_{1-x}\text{Ge}_x$ in the sources/drain regions [101]. These techniques are effective in small device geometries where it is possible to induce uniaxial strain in the channel by stressing the regions around the channel. However, it turned out that the improvement in electron mobility using biaxially tensile strained silicon on relaxed $\text{Si}_{1-x}\text{Ge}_x$ is larger than that obtained for local stress techniques [88].

Fig. 4.6 shows the strained-Si/relaxed-SiGe heterostructure which is used to investigate the impact of strain on ion implantation. Relaxed SiGe layers are epitaxially grown on (100) silicon substrates using a grading technique to obtain the desired Ge composition. Next a constant composition layer is grown to spatially separate the subsequently grown strained silicon layer from the misfit dislocations contained in the graded SiGe layer. When silicon is grown on SiGe, the lattice mismatch between the two materials can be accommodated by uniform lattice strain

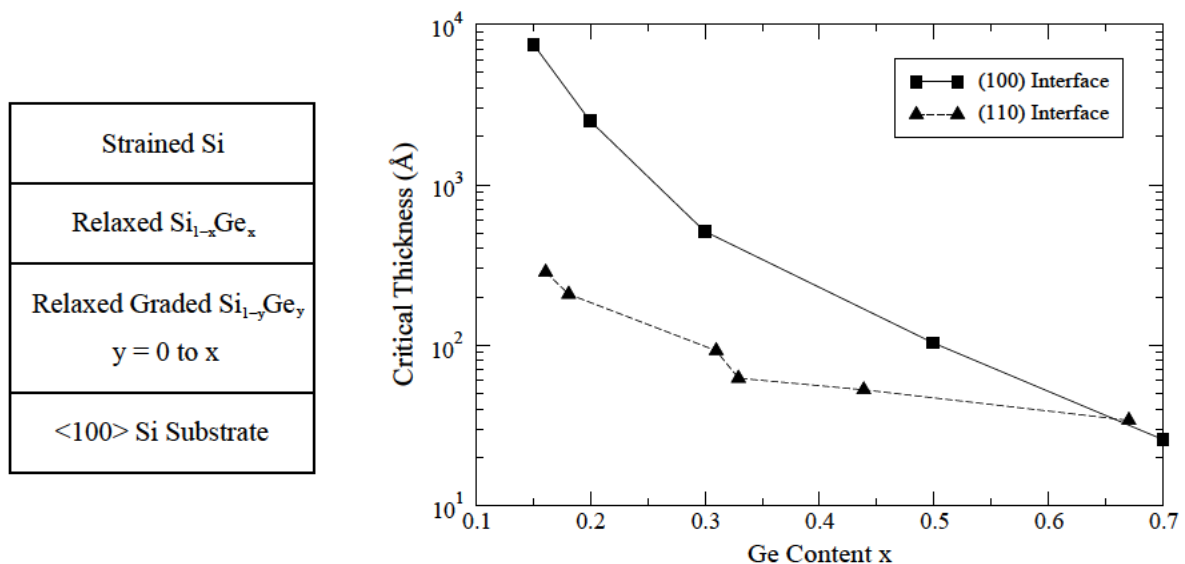


Figure 4.6: Schematic illustration of the strained Si/relaxed $\text{Si}_{1-x}\text{Ge}_x$ system (left) and experimental data for the critical thickness of strained silicon (right).

in sufficiently thin silicon layers [102]. If silicon is grown beyond its critical thickness, the strained crystal relaxes to its natural size and a high concentration of dislocations is introduced. Fig. 4.6 shows also typical experimental data for the critical layer thickness which depends on growth rates, growth temperature, SiGe surface orientation, and mostly on the Ge concentration [96].

4.2.1 Modeling of Biaxially Strained Silicon

A strained silicon channel is formed by a silicon layer with a thickness smaller than the critical thickness, epitaxially grown on the (100) surface of a relaxed $\text{Si}_{1-x}\text{Ge}_x$ buffer layer. The silicon layer is under biaxial tensile strain and the so-called *pseudomorphic interface* is characterized by an in-plane lattice constant a_{\parallel} which remains the same throughout the heterostructure. By using the empirically determined parabolic relation (4.1) for the $\text{Si}_{1-x}\text{Ge}_x$ lattice parameter as a function of the Ge fraction x we obtain for strained silicon

$$a_{\parallel}(x) = 0.02733 x^2 + 0.1992 x + 5.431 \quad (\text{\AA}) . \quad (4.8)$$

The out-of-plane silicon lattice constant a_{\perp} , in the direction perpendicular to the interface plane, is reduced according to the continuum elastic theory [103],

$$a_{\perp}(x) = a_{\text{Si}} \left[1 - \frac{2C_{12}}{C_{11}} \left(\frac{a_{\parallel}(x)}{a_{\text{Si}}} - 1 \right) \right] \quad (\text{\AA}) , \quad (4.9)$$

where a_{Si} denotes the lattice constant of unstrained silicon, and C_{11} , C_{12} are the elastic constants of silicon ($C_{11} = 1.675$ Mbar, $C_{12} = 0.650$ Mbar at room temperature after [102]).

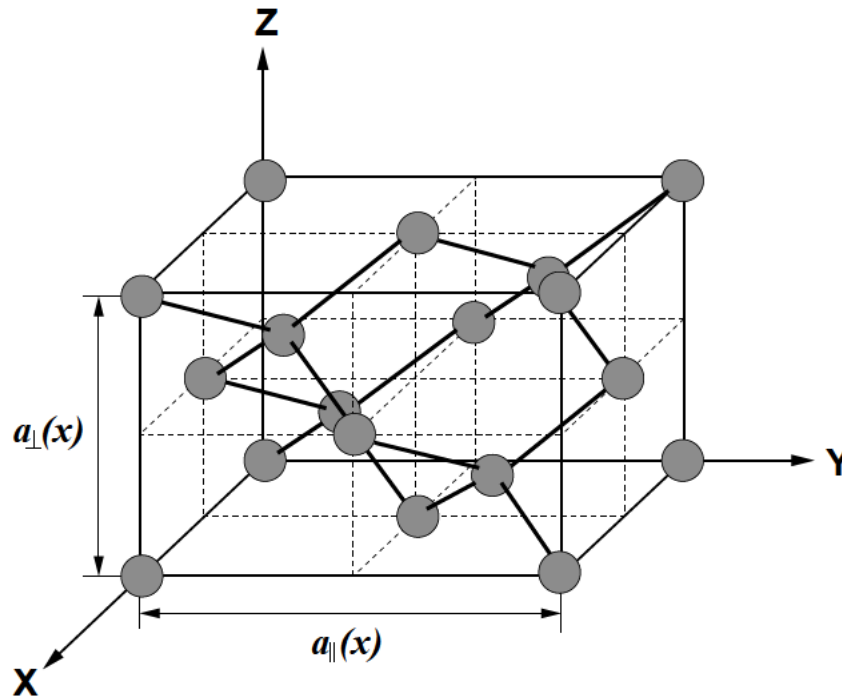


Figure 4.7: Crystal model for biaxially tensile strained silicon layers.

The constraints for the two lattice parameters in strained silicon are given by

$$a_{\perp}(x) < a_{\text{Si}} < a_{\parallel}(x) \quad \text{for} \quad 0 < x < 1. \quad (4.10)$$

The strain components parallel and perpendicular to the interface plane are then defined by

$$\varepsilon_{\parallel}(x) = \frac{a_{\parallel}(x) - a_{\text{Si}}}{a_{\text{Si}}} \quad \text{and} \quad \varepsilon_{\perp}(x) = \frac{a_{\perp}(x) - a_{\text{Si}}}{a_{\text{Si}}}. \quad (4.11)$$

Fig. 4.7 shows the strained unit cell with the edge lengths a_{\parallel} and a_{\perp} , which can be used for the Monte Carlo simulation of ion implantation in strained silicon targets [104]. While the simulated ion moves through a strained silicon region, the strained crystal model from Fig. 4.7 is built up around the actual ion position for searching the next collision partner. The displacement energy of 15eV used for bulk silicon can be applied for strained silicon too. Due to the fact that the strained silicon lattice system is coherently aligned to the $\text{Si}_{1-x}\text{Ge}_x$ virtual substrate lattice, channeling ions can pass the interface between these two crystalline layers without being interrupted. While the implantation profiles in strained and unstrained silicon show only a very small difference at a given implantation energy, the penetration depth of ion-implanted dopants in relaxed $\text{Si}_{1-x}\text{Ge}_x$ is significantly reduced with increasing Ge fraction x , as demonstrated in Section 4.1. Thus the underlying $\text{Si}_{1-x}\text{Ge}_x$ layer helps to reduce the tail region of source/drain doping profiles in this heterostructure.

4.2.2 Ultra-Shallow Junction Formation

We study the implantation of boron as a p-type and arsenic as an n-type dopant in a silicon cap layer with a thickness of 12nm on a thick $\text{Si}_{0.8}\text{Ge}_{0.2}$ layer. Fig. 4.8 shows the simulated and experimental doping profile of a boron implantation with an energy of 400eV and a dose of 10^{15}cm^{-2} . Fig. 4.9 shows the arsenic implantation result, performed with an energy of 2keV and the same dose. The presented doping profiles demonstrate highly doped source/drain extension implants for a typical 65nm CMOS technology under the sidewall spacer, where lightly doped drain (LDD) structures used to be in previous technology generations.

Fig. 4.8 shows that the simulated boron profiles in strained and unstrained silicon are almost identically distributed, and the simulation result agrees well with the SIMS data. It is not possible to characterize arsenic concentration profiles in $\text{Si}_{1-x}\text{Ge}_x$ by SIMS analysis with a resolution larger than about three orders-of-magnitude due to similar atomic masses of arsenic and germanium [99]. As shown in Fig. 4.9 the Monte Carlo simulation can help to get a realistic continuation of the doping profile below the arsenic detection limit. The discrepancy between the predicted and measured doping profiles near the wafer surface may arise from a measurement error in this region. Feedback from industry revealed that this error can be eliminated by the deposition of amorphous silicon on the wafer before the SIMS measurement. Using this procedure, SIMS profiles show an increase in the near-surface region too. However, the simulation results in Fig. 4.9 demonstrate that the arsenic distribution in strained silicon has a slightly deeper penetration compared to unstrained silicon, which can be explained by a stress-induced volume dilation of the material. Strained silicon on $\text{Si}_{0.8}\text{Ge}_{0.2}$ has a strain $\varepsilon_{\parallel}(0.2) \approx 0.75\%$ and approximately 99% of the atomic density of unstrained silicon.

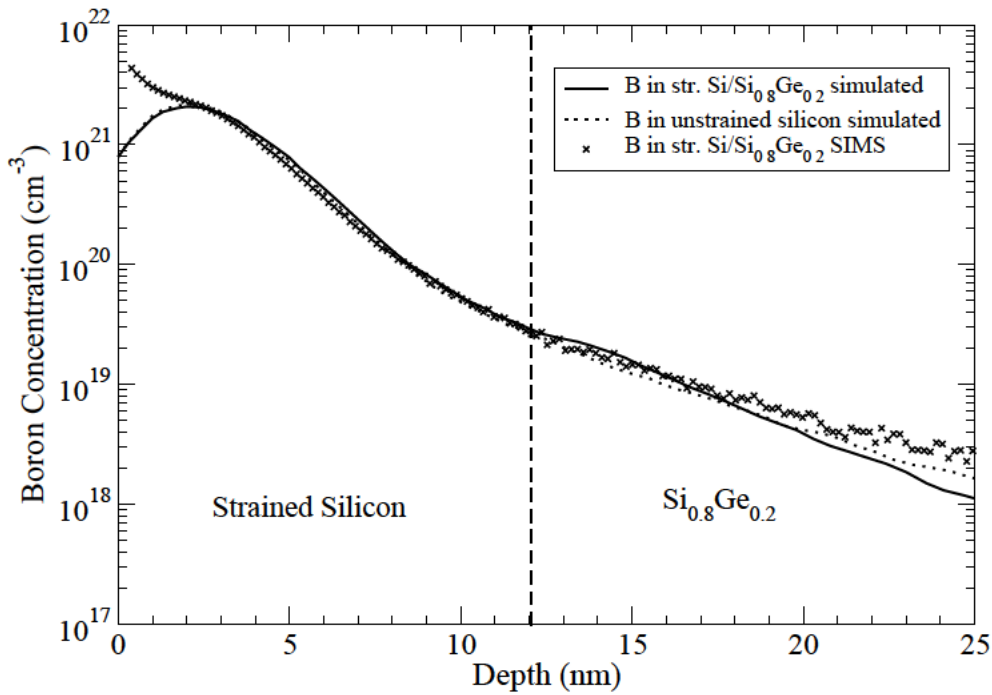


Figure 4.8: Simulated 400eV boron implant profile in a 12nm thick strained silicon layer compared to SIMS measurement.

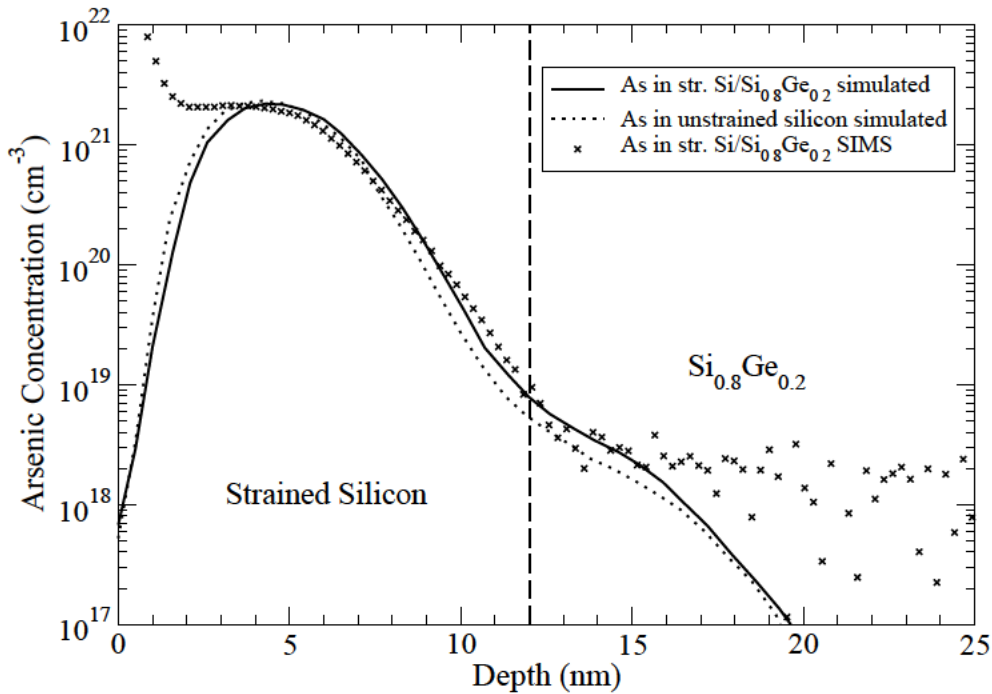


Figure 4.9: Simulated 2keV arsenic implant profile in strained silicon compared to SIMS data.

4.3 Germanium

Germanium has regained attention in the semiconductor industry for future silicon-compatible optoelectronic and advanced CMOS device applications. The carriers have lower effective masses and the intrinsic mobility is about two times higher for electrons and four times higher for holes in germanium compared to silicon, as shown in Table 4.2. Therefore, germanium offers the highest performance enhancement potential for channel engineering compared to bulk SiGe or strained silicon. On the one hand, the smaller band gap of germanium is advantageous to build photodetectors and, on the other hand, junctions made in a smaller band gap material will typically exhibit larger leakage currents.

In recent years, deep-submicron germanium MOS transistors have been processed in a silicon-like process flow by using either germanium oxynitride (GeO_xN_y) [105] or Hafnium oxide (HfO_2) based high-k dielectrics [106, 107] as the gate insulator. The diffusion of the p-type dopant boron is suppressed while the diffusion of the n-type dopants phosphorus, arsenic, and antimony is increased in SiGe and germanium compared with silicon [108]. Thus, the formation of ultra-shallow junctions in germanium is facilitated for p-MOS transistors, while it becomes more challenging for n-MOS devices. It was found in [107] that the junction leakage is about four decades higher for germanium at a chip temperature of 110°C compared with silicon. The reduction of the relatively large leakage current will be a key issue for Ge-CMOS technology to obtain devices with reasonably low I_{off} current. It is reported in [105], that the leakage current of boron implanted p^+/n junctions in germanium can be reduced down to the order of $10^{-4}\text{A}/\text{cm}^2$ with annealing at 400°C , which is considered acceptable for device operation. Ge-rich $\text{Si}_{1-x}\text{Ge}_x$ alloys ($x > 80\%$) and germanium have been recognized as promising materials for photodetectors in fibre-optical transmission systems due to the high optical absorption coefficient for an operation at a wavelength of $1.3\mu\text{m}$ in the near infrared (NIR) regime [109, 110]. The use of epitaxial Ge-on-Si technology allows the integration of germanium pin-photodiodes with CMOS circuits on a silicon chip to build optical communication receivers with low fabrication costs. Optical chip-to-chip communication solutions and even optical on-chip interconnects will be required to meet the challenges of differentiated, high-performance systems in the future.

Ion implantation is a crucial step for processing these device structures. An experimental and simulation study for introducing boron ions into (100) germanium wafers in the energy range from 5 to 40keV is presented in this section [112]. The successful calibration of the simulator MCIMPL-II for germanium is demonstrated by comparing the predicted boron profiles with SIMS data. A doping profile in germanium is shallower than in silicon for any given energy due to the larger nuclear and electronic stopping power. We found also that the produced crystal damage is significantly reduced in germanium, which is consistent with former experimental observations [113] indicating that boron-implanted germanium remains essentially crystalline.

Properties	Germanium	Silicon
Band gap (eV)	0.66	1.12
Electron mobility ($\text{cm}^2/\text{V}\cdot\text{s}$)	3900	1500
Hole mobility ($\text{cm}^2/\text{V}\cdot\text{s}$)	1900	450

Table 4.2: Important electronic properties of germanium vs. silicon at 300K [111].

4.3.1 Modeling of Ion Implantation in Germanium

The extended crystalline simulation model presented in Fig. 4.1 can be applied to germanium by using the maximum lattice parameter value $a(1) = 5.6575\text{\AA}$ and a probability of 100% for meeting a germanium atom at the next collision event. In a screened Coulomb collision the energy loss of the ion, ΔE , is equal to the transferred energy to the recoil atom,

$$\Delta E = \frac{4 M_1 M_2}{(M_1 + M_2)^2} \cdot \sin^2 \frac{\Theta}{2} \cdot E_0, \quad (4.12)$$

where M_1 and M_2 are the masses of ion and target atom, Θ is the transformed scattering angle in the center-of-mass coordinates, and E_0 is the kinetic energy of the ion before the collision event. From this equation it can be derived that a smaller energy loss ΔE occurs in nuclear collisions in germanium due to the different masses between ion and atom. The transferred energy ΔE from a boron ion to a germanium atom is approximately the half (0.568-fold) compared to ΔE in silicon at a given scattering angle. Note that the difference in masses between boron and germanium leads also to a strong backscattering effect for the light boron ions.

An advantage of the Monte Carlo simulation is that the used Kinchin-Pease model (as described in Section 3.1.4) allows to estimate the produced vacancies in the germanium crystal. Note that equal local concentrations of vacancies and interstitials are assumed, since the recoils themselves are not individually followed in our computationally fast simulation approach. However, a critical model parameter is the threshold displacement energy required for the ion to displace a target

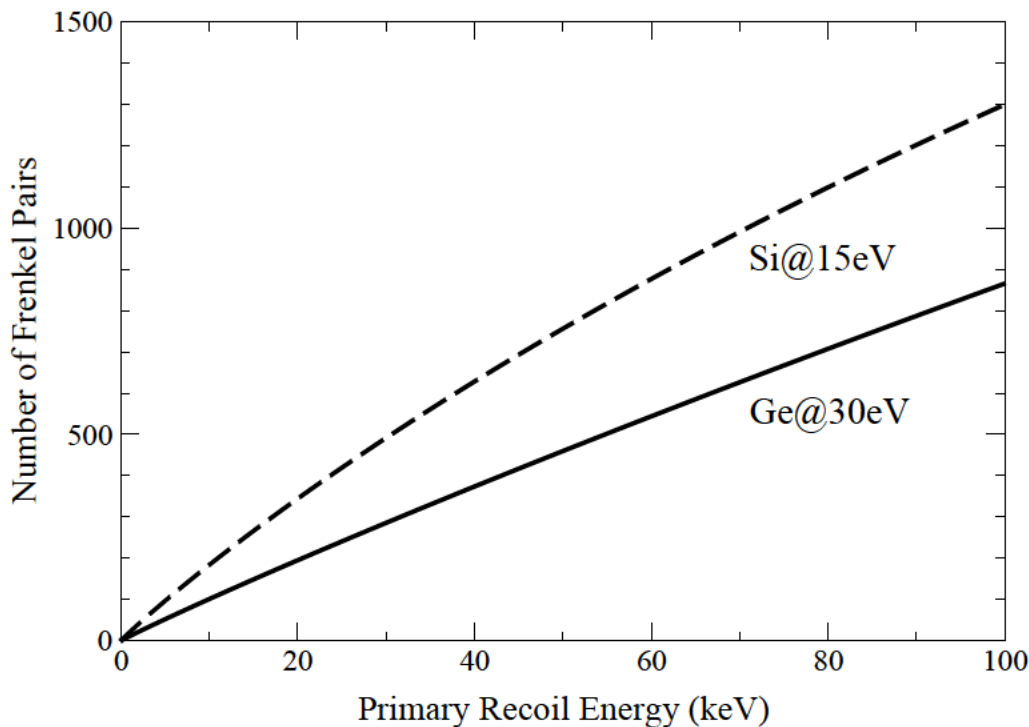


Figure 4.10: Number of Frenkel pairs generated by a primary knock-on atom in Si and in Ge, assuming a displacement energy of 15eV and 30eV.

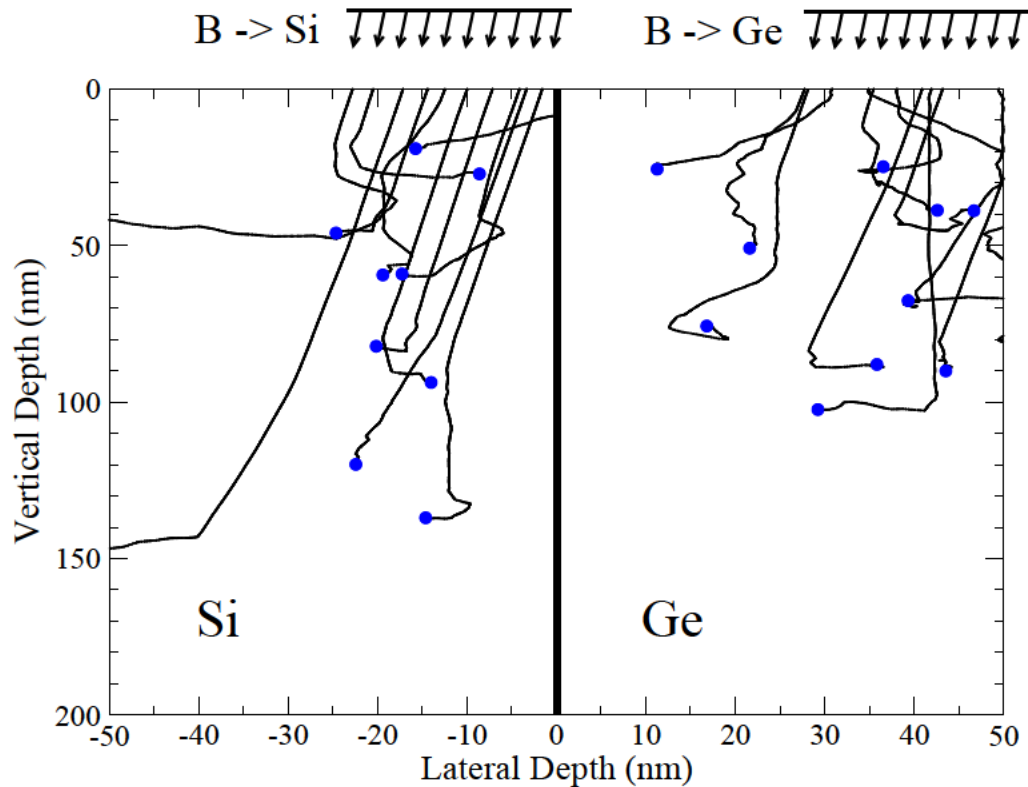


Figure 4.11: Comparison of the Monte Carlo simulation of ten boron trajectories in silicon and in germanium using an energy of 10keV and a tilt of 7° .

atom. A displacement energy E_d of 15eV has become widely accepted for silicon. We fitted a value of $E_d = 30\text{eV}$ for germanium by comparison of simulated boron profiles with SIMS measurements. Fig. 4.10 shows the number of produced point defects for a damage cascade, calculated with the modified Kinchin-Pease model. The used value for the displacement energy in germanium is in good agreement with $E_d = 31\text{eV}$ which was deduced by Mitchell in 1957 for germanium [114]. The larger E_d value is responsible for the generation of significantly fewer point defects by a boron ion in germanium compared with silicon for any amount of transferred energy ΔE to the primary knock-on atom of a cascade. The reduced damage production by ion implantation in crystalline germanium is consistent with former experimental observations [113].

The Lindhard correction parameter k_L of the empirical electronic stopping model, which is explained in Section 3.1.3, has been calibrated to adjust the strength of the electronic stopping power for boron ions in germanium. We increased the empirical parameter value from $k_L = 1.75$ for silicon to a value of 1.9 for germanium.

In the following simulation study, at least 10^6 trajectories were calculated for a one-dimensional boron profile. Fig. 4.11 shows the visualization of ten arbitrarily selected boron trajectories in silicon and in germanium. This comparison demonstrates that the larger nuclear and electronic stopping power of germanium, in particular the stronger backscattering of boron ions in germanium, typically reduces the trajectory length.

4.3.2 Simulation Results and Discussion

Germanium has a larger nuclear and electronic stopping power for incoming ions due to the heavier atomic mass and higher electron density. For this reason, an implanted dopant profile in germanium is significantly shallower than in silicon and SiGe for any given implantation energy. Fig. 4.12 shows that the calibrated simulator can accurately reproduce the measured 20keV boron concentration profiles implanted with a dose of $6 \cdot 10^{14} \text{cm}^{-2}$ in amorphous and in crystalline germanium targets. The amorphization of germanium was performed by the implantation of ^{72}Ge ions with an energy of 200keV and a dose of 10^{15}cm^{-2} . A channeling tail can be observed for the profile in crystalline germanium. Fig. 4.13 demonstrates a good agreement between the simulated and measured boron profiles implanted with a lower energy of 5keV and a lower dose of $3 \cdot 10^{13} \text{cm}^{-2}$. Fig. 4.14 compares simulated 20keV boron profiles in silicon and in germanium. We found the projected range R_p of the boron distribution in $\text{Si}_{0.5}\text{Ge}_{0.5}$ at a depth of 65nm, which lies well within the boundaries defined by the projected ranges in germanium at 55nm and in silicon at 80nm. Table 4.3 summarizes simulated and measured R_p and σ_p parameters for boron implants in crystalline silicon, $\text{Si}_{0.5}\text{Ge}_{0.5}$, and germanium targets. The projected range R_p is read off at the maximum concentration of a boron distribution and the provided straggling σ_p is the average value of the left and right straggling values which are determined by 60% of the maximum boron concentration. The results in the table were obtained with an implantation dose of 10^{14}cm^{-2} and a tilt of 7° .

Fig. 4.15 compares the simulated vacancy concentration profiles in silicon and in germanium associated with the 20keV boron implantations shown in Fig. 4.14. The vacancy maximum is not at the wafer surface, since the electronic stopping process dominates at high initial energies of the ions, when they enter the crystal. A boron ion enters most likely a channel at the surface and despite of the tilted incident direction it can stay at least a short distance inside a channel. The higher displacement energy of 30eV, the stronger backscattering of boron ions in germanium, and the smaller energy transfer ΔE from the ion to the primary recoil of a cascade are mainly responsible for the significantly smaller damage production in germanium. Previous experimental boron implantation results in germanium [113] performed up to a dose of 10^{14}cm^{-2} within the energy range of 25–150keV revealed that 100% of the boron ions are immediately active after implantation without thermal annealing since boron-implanted germanium remains crystalline. This is a unique phenomenon, since an annealing step is required for every other dopant species implanted in silicon or germanium in order to activate a significant amount of dopants. Finally, Fig. 4.16 illustrates the dose dependence of 40keV boron profiles in germanium, which were simulated with the Kinchin-Pease model. It is obvious that the shape of the profiles is influenced by the damage accumulation in the crystal.

Cryst. Material	Si	$\text{Si}_{0.5}\text{Ge}_{0.5}$	Ge	Si	$\text{Si}_{0.5}\text{Ge}_{0.5}$	Ge
Energy (keV)	5	5	5	20	20	20
R_p (nm)	18.91	15.44	14.32	79.52	65.32	55.27
σ_p (nm)	14.16	12.56	12.16	37.42	36.33	39.38
SIMS R_p (nm)	-	-	16.23	-	67.11	56.99
SIMS σ_p (nm)	-	-	11.23	-	40.58	34.91

Table 4.3: Projected range and straggling parameters for boron distributions.

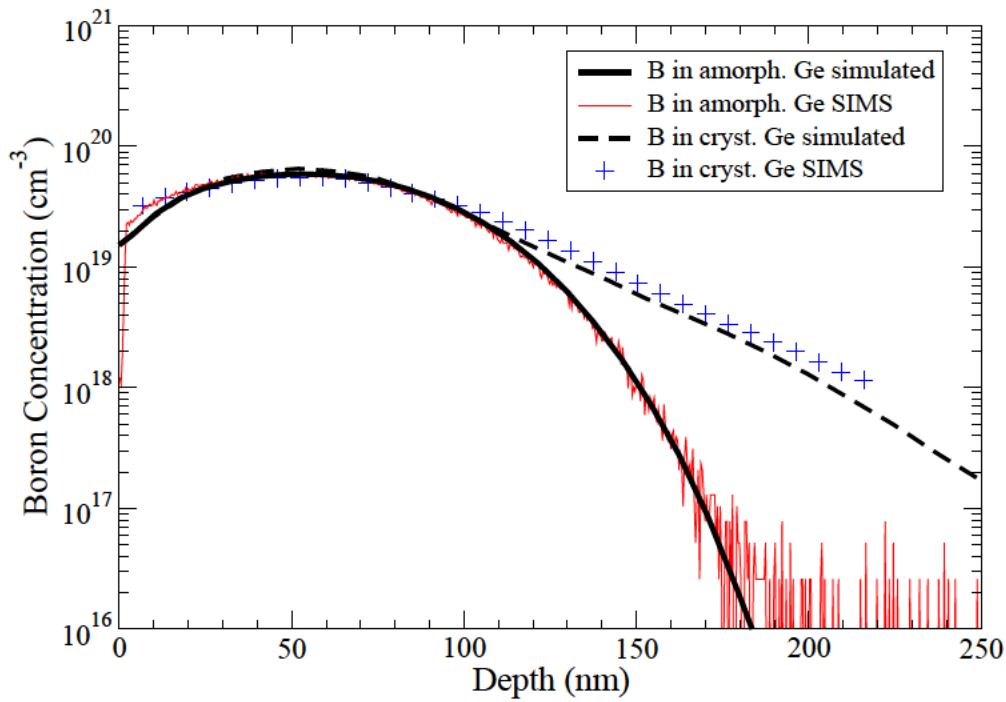


Figure 4.12: Simulated 20keV boron implantations in amorphous Ge and in (100) Ge using a dose of $6 \cdot 10^{14} \text{cm}^{-2}$ and a tilt of 7° compared to SIMS profiles.

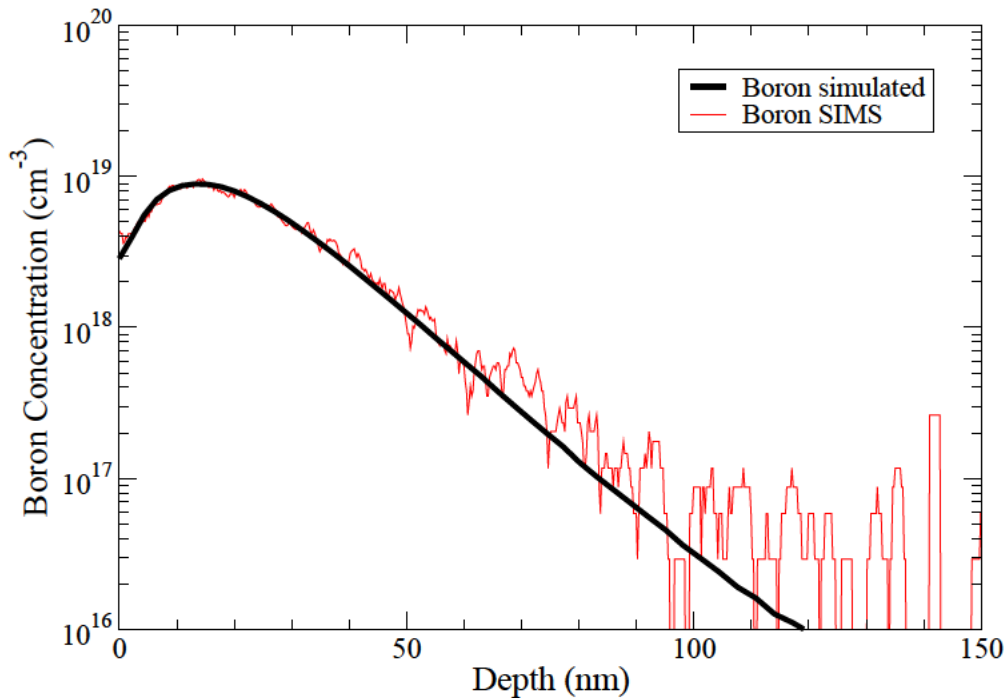


Figure 4.13: Simulated 5keV boron profile in (100) Ge using a dose of $3 \cdot 10^{13} \text{cm}^{-2}$ and a tilt of 7° compared to SIMS measurement.

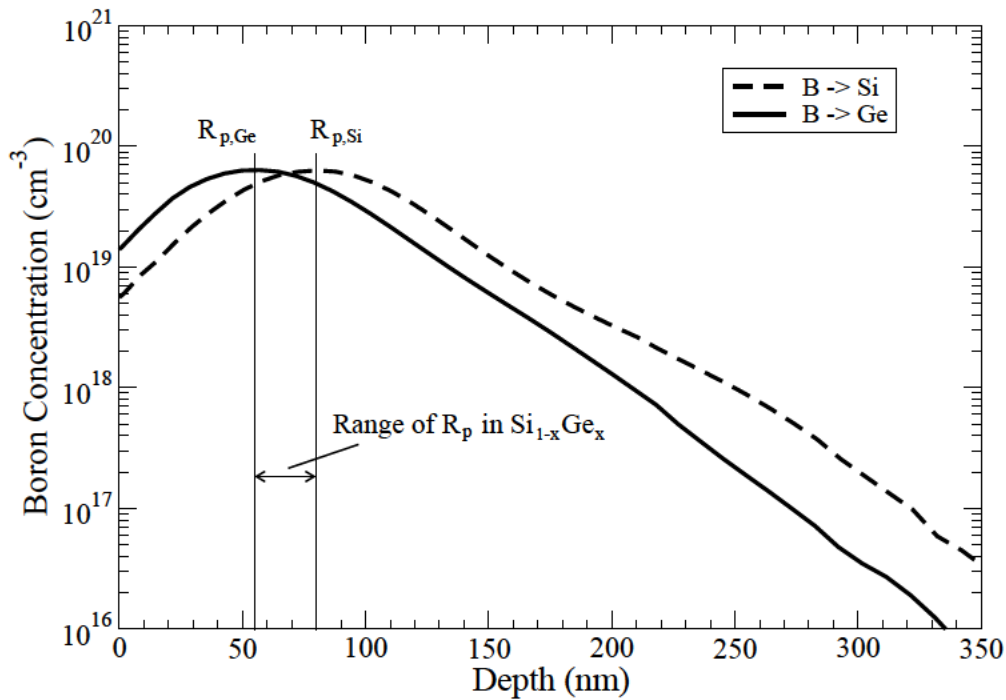


Figure 4.14: Comparison of simulated 20keV boron implant profiles in silicon and germanium using a dose of $6 \cdot 10^{14} \text{cm}^{-2}$ and a tilt of 7° .

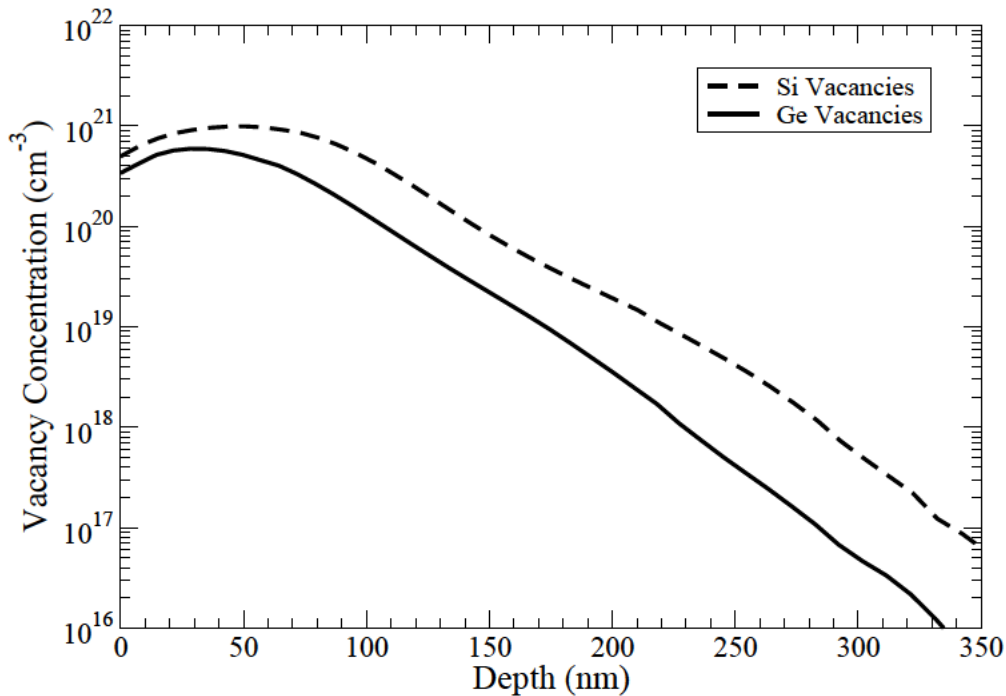


Figure 4.15: Comparison of produced vacancies for the 20keV boron implantations in silicon and germanium using a dose of $6 \cdot 10^{14} \text{cm}^{-2}$ and a tilt of 7° .

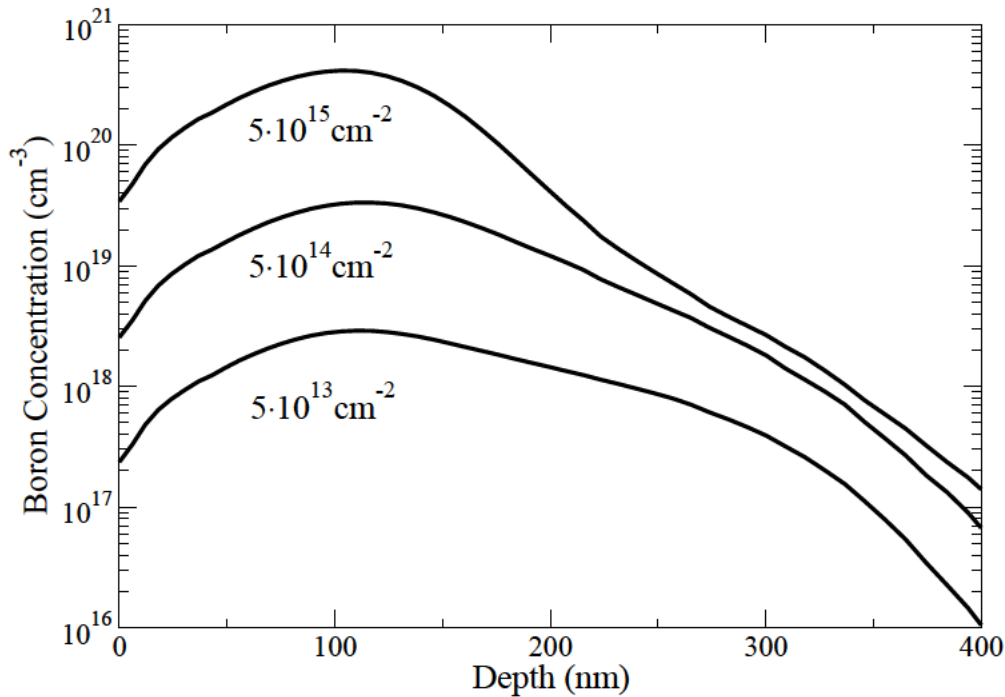


Figure 4.16: Simulated 40keV boron implants in (100) Ge at doses of $5 \cdot 10^{13}$, $5 \cdot 10^{14}$, and $5 \cdot 10^{15} \text{cm}^{-2}$ using a tilt of 7° .

The simulated point responses in crystalline silicon and germanium are shown in Fig. 4.17 and Fig. 4.18 to study quantitatively the lateral and vertical penetration of boron ions. The used two-and-a-half dimensional input geometry has a depth dimension of 40nm, and the slot width of the implantation window in an impenetrable mask is 8nm. A high-resolution mesh which consists of 33181 grid points and 144159 tetrahedrons is added to the input structure to resolve the implanted boron distribution. Boron is implanted with an energy of 10keV, a dose of $5 \cdot 10^{15} \text{cm}^{-2}$, and the ion beam is 7° tilted in such a way that the lateral component of the incident direction is parallel to the direction of view ($\langle 010 \rangle$ direction). Therefore, the presented point responses are symmetric. Approximately 420000 simulated boron ions of a total number of 50 million ions can enter the substrate at the mask opening and contribute to the Monte Carlo result represented by the internal histogram cells.

The visualization of single trajectories in silicon and in germanium (as shown in Fig. 4.11) and in particular the comparison of the point responses indicate that the boron distribution in germanium is significantly reduced in the vertical direction, while the lateral profile is quite similar in silicon and germanium. Additionally, it can be observed that the channeling tail is closely centered around the $\langle 100 \rangle$ axis in both cases. This demonstrates that in (100) silicon and in (100) germanium, axial channeling in the $\langle 100 \rangle$ direction dominates by far over channeling in other directions.

As demonstrated in this study, the used physics-based simulation approach in combination with experimental results allows to get a comprehensive understanding of implantation-related phenomena in germanium.

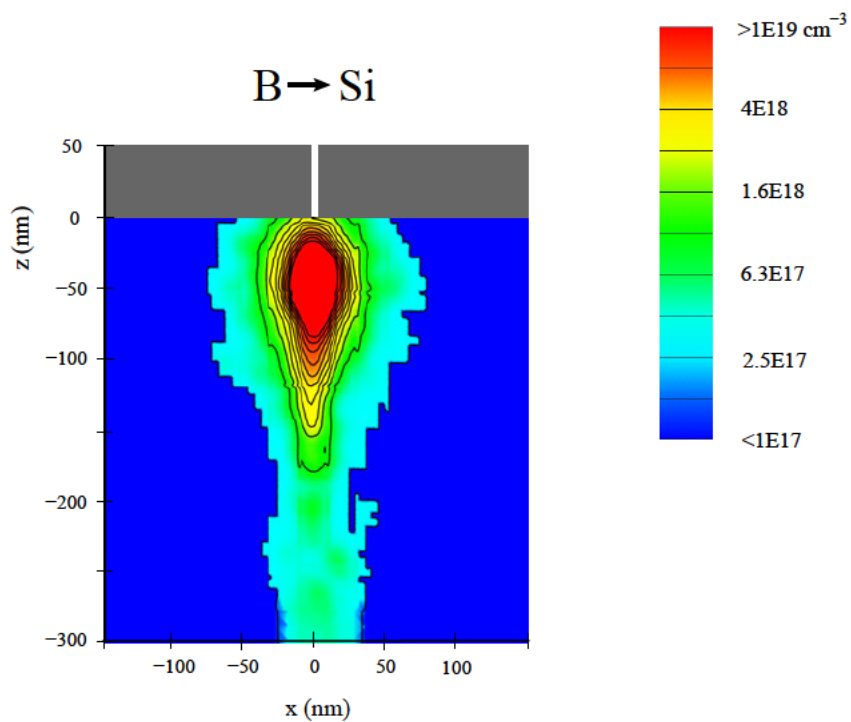


Figure 4.17: Simulated point response for a 10keV high-dose implantation of boron into crystalline silicon.

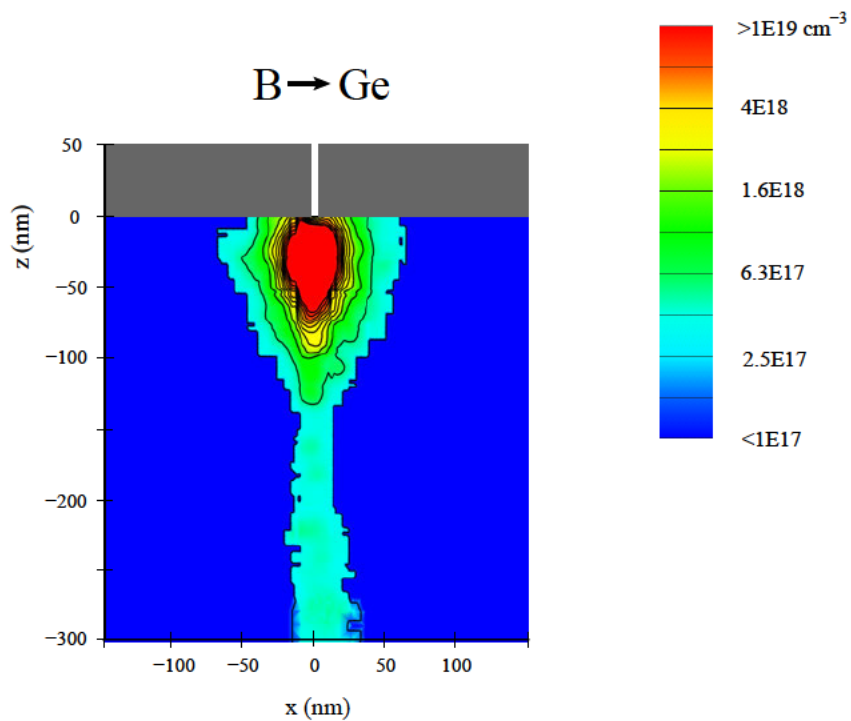


Figure 4.18: Simulated point response for a 10keV high-dose implantation of boron into crystalline germanium.

Chapter 5

NBTI Reliability Analysis

While most of the miniaturization problems in CMOS technology are more or less related to doping issues, the continued reduction of the gate oxide thickness has necessitated the incorporation of nitrogen into silicon dioxide, which in turn has aggravated NBTI (negative bias temperature instability), especially, since we have entered the 90nm and 65nm technology nodes. As drive currents increase HCI reliability usually gets worse since the drive current directly determines the carriers generated by impact ionization. However, optimization of the drain extension doping profile reduces the electric field at the drain edge significantly. Therefore, the substrate current, which is a quantitative measure for impact ionization, is strongly reduced for advanced CMOS technologies [115]. Since HCI has lost on importance and NBTI is the leading reliability concern for current technology nodes, a detailed analysis of the degradation and relaxation behavior of the NBTI mechanism in a 90nm transistor is presented.

The key device parameters of the p-MOSFET such as threshold voltage and saturation current show a rapid shift under negative bias at an elevated temperature due to the build-up of positive interface charges. Since indirect measuring techniques have to be applied, it is difficult to correlate measurement results to NBTI induced degradation of the gate-dielectric/substrate interface associated with bond breaking and chemical species. While the exact nature of the complex NBTI mechanism is still unknown, it is widely accepted that interface traps are generated by breaking of hydrogen-passivated silicon bonds at the interface and subsequent diffusion of hydrogen [25, 116, 117]. Charge pumping and gate leakage current measurements revealed that NBTI under moderate oxide fields is purely due to interface traps N_{it} and the generated oxide traps N_{ot} can be neglected [118]. The NBTI induced interface charges cause a parameter degradation of the MOSFET firstly due to a reduction in inversion layer holes and secondly due to a mobility degradation by Coulomb scattering. Both the reduced gate overdrive ($V_G - V_T$) and the degraded mobility reduce the saturation current and the transconductance of the transistor.

Jeppson and Svensson studied the process of trap formation at the Si/SiO₂ interface during NBT stress in MOS capacitors in 1977 [119]. They found that the NBTI-driven shift of the threshold voltage in p-MOSFETs depends on the applied gate voltage, temperature, and stress time. It is commonly assumed that the generated interface states are dangling silicon bonds with an energy distribution within the silicon band gap. Holes can occupy these energy states under inversion condition and produce positive interface charges [116]. For advanced CMOS technologies, nitrogen is incorporated in thinner gate oxides mainly to reduce gate leakage current, to avoid

boron penetration into the dielectric, and to improve HCI reliability. However, it turned out that silicon dioxide-nitride compositions exhibit a significantly higher NBTI degradation compared to pure silicon dioxide for the same physical oxide thickness and voltage condition [13]. Experimental studies revealed that the thermal activation energy of interface trap generation decreases steadily with increasing nitrogen concentration at the interface [120, 121].

Under dynamic operation of the transistor the interface traps which are generated during the on-state are partially annealed in the off-state. Therefore the AC degradation is significantly lower than the DC degradation for any given stress time. The magnitude of the NBTI driven parameter shift over time is significantly reduced for higher frequencies [122] or smaller “on” duty cycles [123, 124]. In this section we analyze mainly the impact of an operation at higher frequencies in the MHz-range at slightly different supply voltages on the AC lifetime of a 90nm transistor. The NBTI transistor level degradation is closely linked to circuit and product level degradation, which will be analyzed for a typical 90nm-based SRAM memory cell in Section 6.4.

5.1 NBTI Experiments for a 90nm CMOS Technology

The investigated p-MOSFET device was fabricated in a 90nm bulk technology with shallow trench isolation (STI). The gate oxide was annealed in an NO_x gas ambient and has a physical oxide thickness of 2.4nm and an equivalent oxide thickness (EOT) of 2.05nm. A dual poly-gate CMOS configuration was used on top of the nitrated gate oxide. Source/drain extension implant profiles and halo implants for punchthrough suppression were created by ion implantation processes before a nitride spacer was deposited. The source/drain regions were implanted subsequently followed by a high temperature RTA annealing step to activate the dopants and to eliminate the crystal damage. The backend was completed by employing local interconnect as well as a triple-layer aluminum-metal process.

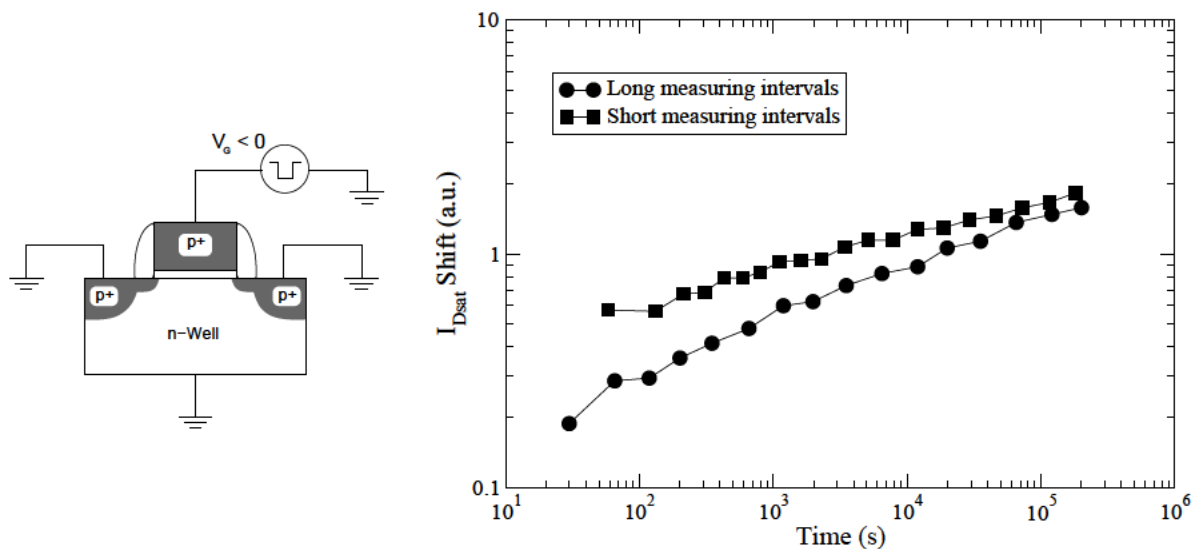


Figure 5.1: Configuration for NBTI experiments under DC and AC stress (left) and influence of relaxation during long measuring intervals on the slope of I_{Dsat} shift at a constant gate voltage stress $V_G = -1.5\text{V}$ (right).

The sketch on the left hand side of Fig. 5.1 shows the used configuration for NBTI experiments under DC and AC gate voltage stress conditions at a constant temperature of 125°C. The used amplitude for AC stress is identical to the negative DC voltage during the pulse “on” phase and zero Volt during the pulse “off” phase. The NBT stress was interrupted at certain times to measure the threshold voltage and drain saturation current. The threshold voltage V_T was extracted by using a linear extrapolation of $I_D - V_G$ data from the point of maximum transconductance, and the saturation current I_{Dsat} was determined at $V_G = -1.2V$ and $V_D = -1.2V$.

The measuring interval of the tester used for monitoring the key parameters of the MOSFET over the stress time should be kept as short as possible to minimize the influence of relaxation on measurement results. The diagram on the right hand side of Fig. 5.1 illustrates that the I_{Dsat} parameter shift is significantly reduced by stronger annealing of interface traps for longer relaxation phases. In the long stress time regime the influence of the relatively short measuring intervals plays a secondary role and the results of long and short intervals become comparable. The longer measuring interval lasts ten times longer than the shorter interval of 700ms.

The accomplishment of all presented NBTI measurements in this section were managed by Dr. Puchner at Cypress Semiconductor Corp. in San Jose. Different rectangular gate signals were used in order to analyze the gate voltage, duty cycle, and frequency dependence of the NBTI degradation behavior. Voltages were applied from -1.5V down to -2.7V to the gate of the transistor, frequencies were used in the range from DC to 1MHz, and “on” duty cycles in the range of 30% to 70%. The MOSFET parameters V_T and I_{Dsat} were monitored for a maximum stress time of $2 \cdot 10^5$ s. The experimental data were used to analyze the relationship between the I_{Dsat} shift and the V_T shift, to empirically investigate the gate voltage and frequency dependence of NBTI, and finally to calibrate the numerical simulations for the 90nm p-MOSFET device.

5.2 Reaction-Diffusion Model

Although several NBTI models have been developed to explain the physics of interface trap generation based on electrochemical reactions and activation energies, only the reaction-diffusion (R-D) model can explain to some extent the power-law time dependence of the NBTI degradation. Jeppson and Svensson developed the first model approach in 1977 [119], Ogawa and Shiono generalized the R-D model equations [125], Alam performed numerical simulations for newer CMOS technologies [25, 126], and finally Mahapatra verified the applicability of the model [118, 121]. Quite recently, Grasser et al. proposed a coupled modeling solution of the R-D model with the semiconductor current transport equations [127]. The R-D model states that the NBTI induced shift in p-MOSFET parameters is driven by breaking of hydrogen-passivated silicon bonds at the substrate interface and subsequent diffusion of hydrogen. The formation of interface traps is described by two coupled differential equations:

$$\frac{\partial N_{it}(t)}{\partial t} = k_f [N_0 - N_{it}(t)] - k_r N_{it}(t) C_H(x=0, t), \quad (5.1)$$

$$\frac{\partial N_{it}(t)}{\partial t} = -D \left. \frac{\partial C_H(x, t)}{\partial x} \right|_{x=0} + \frac{\delta}{2} \frac{\partial C_H(x, t)}{\partial t}. \quad (5.2)$$

Equation (5.1) states that the N_{it} generation is determined by a chemical hydrogen release reaction with a constant dissociation rate k_f , when the p-MOSFET is biased in inversion. When

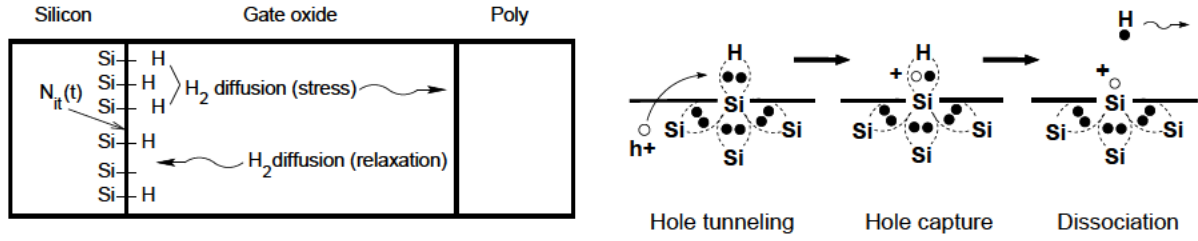


Figure 5.2: Schematic description of the R-D model (left) and possible mechanism for breaking interfacial Si-H bonds by inversion-layer holes (right).

the transistor is switched off, the forward rate k_f becomes zero and the reverse rate k_r stays unchanged. The parameter N_0 denotes the total Si-H bond density at the interface before stress. Equation (5.2) is obtained by integration of the standard diffusion equation across the silicon/oxide interface with a thickness δ . The diffusion coefficient D is the average diffusivity of the diffusing hydrogen species (atomic and molecular hydrogen). Note that the generated interface traps $N_{it}(t)$ are equal to the number of released hydrogen atoms at any given time t .

The left sketch in Fig. 5.2 shows that released hydrogen diffuses into the gate oxide during NBT stress and returns back to the interface when stress is removed. The active region of the NBTI mechanism is uniformly distributed over the channel according to a one-dimensional problem. The right sketch depicts that a hole can tunnel to a Si-H bond during inversion of the p-MOSFET and it can take one electron of the covalent bonding away. After that, the hydrogen atom diffuses away with its electron and leaves a positively charged interface trap behind.

The discretization of the differential equations (5.1) and (5.2) is based on a one-dimensional finite differences method. The simulation domain for the diffusing hydrogen is the gate oxide with the boundary condition of an adjustable reflecting and absorbing wall at the oxide/poly interface. The differential quotients are approximated with differences using the spatial and temporal increments h and Δt , respectively. Grid points (x_i, t_j) with resolution $m = \frac{T_{ox}}{h}$ are used for an oxide thickness T_{ox} , and $x_i = ih$ for $i = 0, 1, \dots, m$ and $t_j = j \Delta t$ for $j = 0, 1, \dots$. We are solving for the next time step $(n + 1)$ in order to calculate the hydrogen diffusion profile $C_{H,i}^j = C_H(x_i, t_j)$ and the interface trap concentration $N_{it}^j = N_{it}(t_j)$ at the next instant according to the following equations:

$$C_{H,0}^{n+1} = C_{H,0}^n + \frac{2 \Delta t \gamma^n}{\delta} + \frac{2 \lambda h}{\delta} (C_{H,1}^n - C_{H,0}^n), \quad (5.3)$$

$$N_{it}^{n+1} = N_{it}^n + \gamma^n \Delta t, \quad (5.4)$$

$$\gamma^n = k_f (N_0 - N_{it}^n) - k_r N_{it}^n C_{H,0}^n, \quad (5.5)$$

$$\lambda = \frac{D \Delta t}{h^2}. \quad (5.6)$$

The dimensionless parameter λ includes the ratio of the temporal and spatial discretization step, whereby stability and convergence is ensured for the interval $0 < \lambda \leq 0.5$ [128].

Fig. 5.3 compares the numerical solution of the calibrated R-D model for DC and AC operation to experimental data of the investigated 90nm p-MOSFET. The V_T degradation under static and dynamic NBT stress was simulated with the same model parameter set, which includes $k_f = 0.47 \text{ s}^{-1}$, $k_r = 2.8 \cdot 10^{-19} \text{ cm}^3 \text{ s}^{-1}$, $N_0 = 6.11 \cdot 10^{11} \text{ cm}^{-2}$, and $\delta = 0.2 \text{ nm}$.

Chakravarthi et al. found that the atomic hydrogen model exhibits the typical power-law time dependence $V_T \propto t^{0.25}$ whereas the molecular hydrogen model predicts a time dependence of $t^{0.165}$ [117]. We found a time exponent of 0.183 for our DC data, which supports that both atomic and molecular hydrogen is present. The hydrogen distribution is calculated in the gate oxide with a physical thickness $T_{ox} = 2.4\text{nm}$ for every time step. The final simulation result is the defect density N_{it} and the corresponding shift $\Delta V_T \propto N_{it}$. Fig. 5.4 demonstrates that the calibrated model can be used to study the evolution of the MOSFET parameter degradation over time under DC and symmetric AC operation. The dynamic NBTI effect guarantees, even for a very slow switching operation, that the NBTI lifetime is improved by at least a factor of 2.

The left diagram in Fig. 5.5 shows four snapshots of hydrogen profiles $C_H(x, t_i)$ during the first stress phase. After 400s the transistor is switched off. The right diagram shows the corresponding profiles during relaxation. When relaxation starts, the free hydrogen near the interface can rapidly anneal broken Si-H bonds. The consumption of hydrogen near the interface creates a diffusion hole. Fig. 5.6 shows the second stress-relaxation cycle. When stress is applied again, a rapid generation of interface traps starts. After the diffusion hole is filled the generation slows down due to diffusion limited transport. In the relaxation phase hydrogen moves back to the interface again. This forward and backward movement continues in subsequent cycles.

Interface traps are built up quickly during the first seconds of a stress phase (reaction-limited regime). With increasing time the hydrogen diffusion front moves towards the oxide-poly interface (diffusion-limited regime). After long times, free and bounded hydrogen densities at the silicon-oxide interface become very low, corresponding to a high level of generated interface defects. Recently, Tsujikawa and Yugami have investigated released hydrogen atoms from the substrate interface during NBT stress in a p-MOSFET with a 1.85nm thick nitrided gate dielectric [8]. Although it was expected that hydrogen can easily diffuse out in the case of ultra-thin gate dielectrics, it was found that much of the released hydrogen remains in the gate dielectric. The R-D model must take the accumulation of hydrogen in the gate oxide as well as the loss of hydrogen into the poly into account in order to predict the long-time degradation slope appropriately. We suggest to model the boundary condition at the oxide/poly interface with a more reflecting than absorbing wall. The simulated accumulation of hydrogen after 400s can be observed in the right diagram of Fig. 5.5, since the diffusion front has already reached the poly interface at $x = 2.4\text{nm}$ at this time.

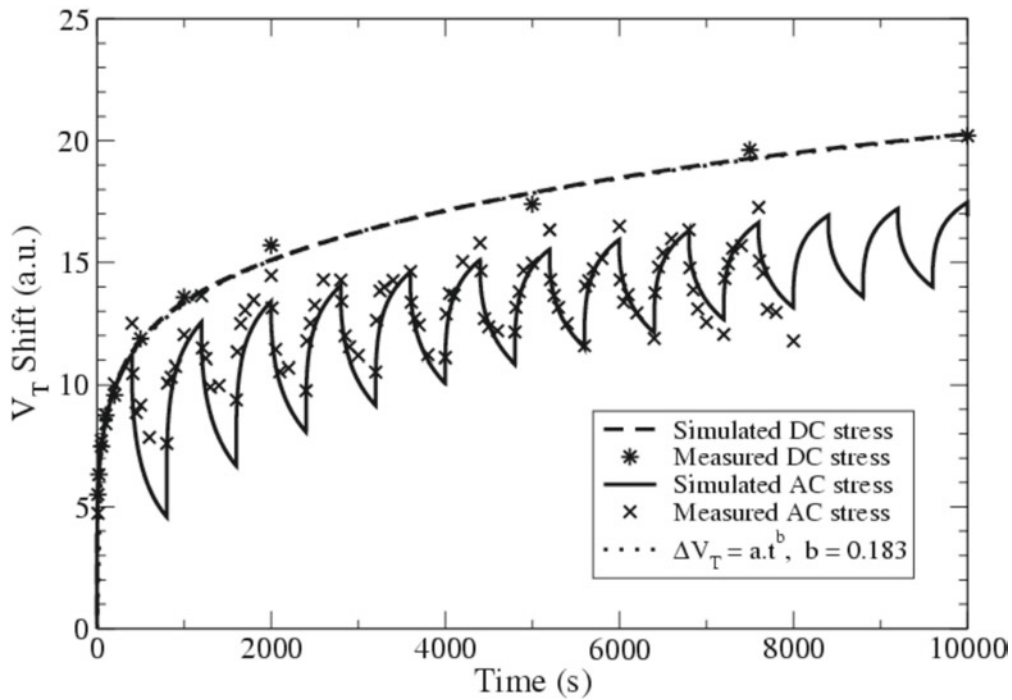


Figure 5.3: Comparison of the numerical solution of the calibrated R-D model to measured DC and AC data (stress: 400s, relaxation: 400s).

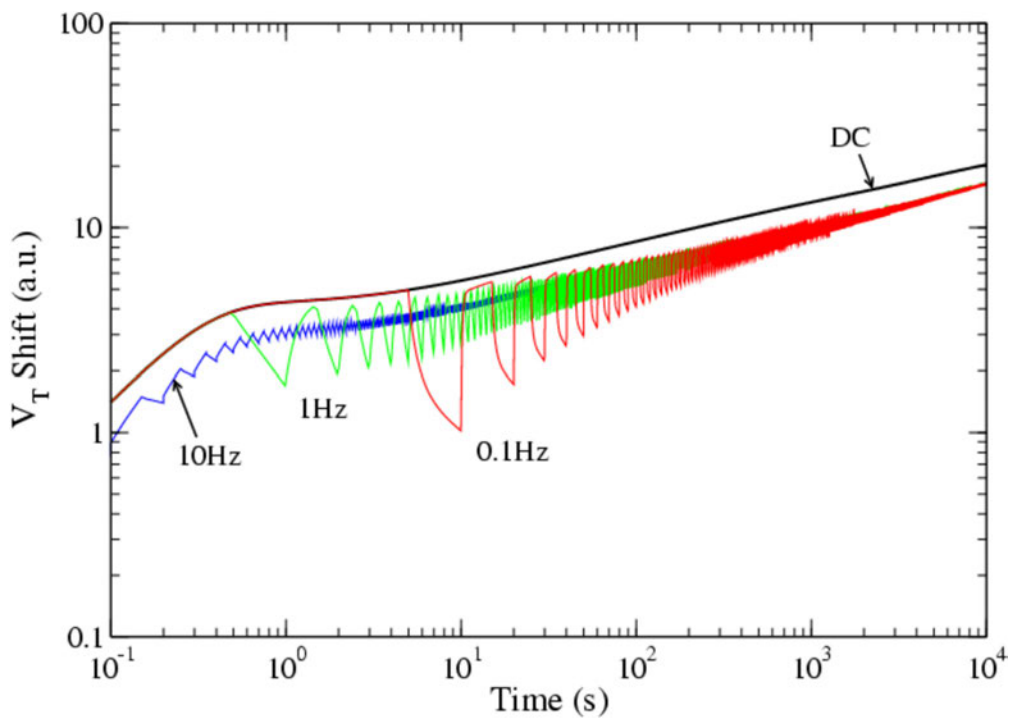


Figure 5.4: Simulated NBTI responses to rectangular gate signals in the frequency range from DC – 10Hz for the 90nm p-MOSFET.

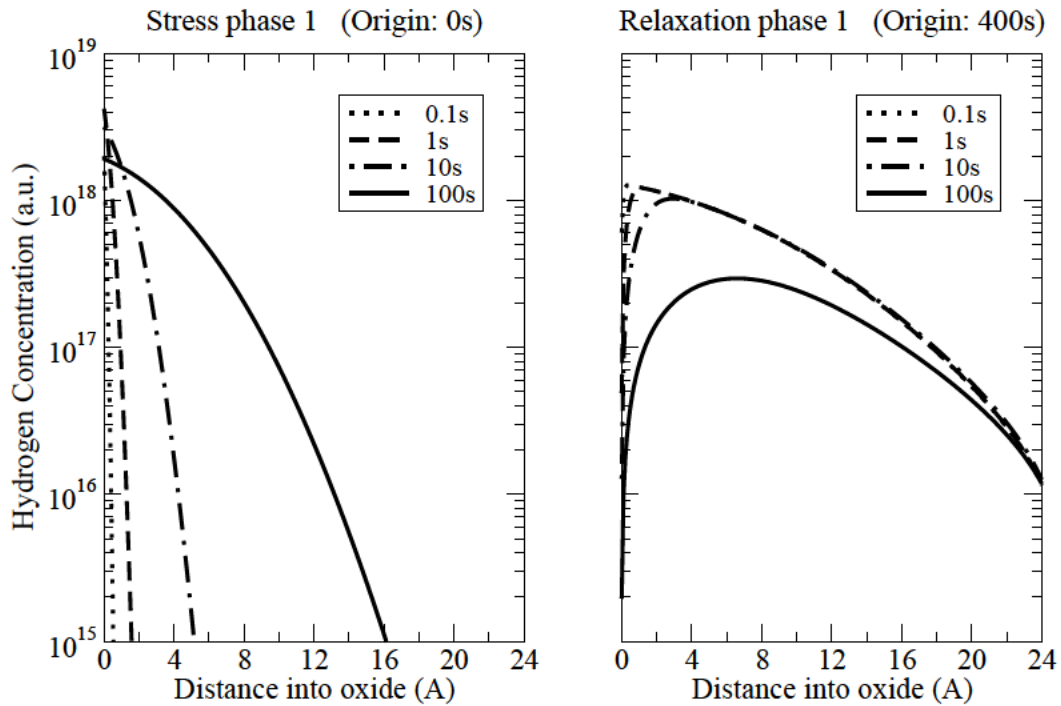


Figure 5.5: Snapshots of hydrogen diffusion profiles in the gate oxide during the first stress-relaxation cycle (stress: 400s, relaxation: 400s).

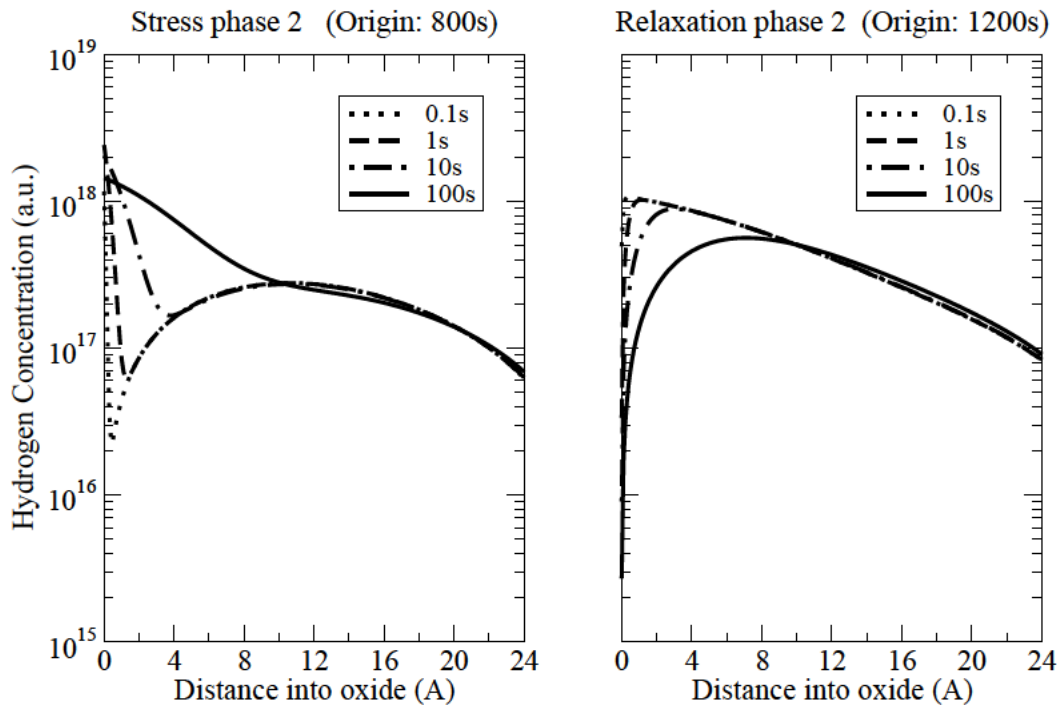


Figure 5.6: Simulated hydrogen distributions in the gate oxide during the second stress-relaxation cycle (stress: 400s, relaxation: 400s).

5.3 Effect of Interface Charge

The presence of donor-like interface states has three major effects on the characteristics of the degraded p-MOSFET. Firstly, the positively charged interface traps change the surface potential and hence reduce the inversion layer hole density. Secondly, the interface charge leads to a degradation in mobility due to the Coulomb scattering effect. Thirdly, the interface traps can act as generation-recombination centers, or assist in the tunneling process, and thus contribute to the gate leakage current [129].

5.3.1 Effect of Interface Charge on Surface Potential

For a MOS structure, the effect of interface charge can be described in terms of change in gate voltage which is necessary to restore the surface potential to that of zero interface charge. In other words, the interface charge density ($N_{it} \cdot q$) produces a threshold voltage shift ΔV_T which depends mainly on the oxide capacitance per unit area, C_{ox} , given by

$$\Delta V_T \approx - \frac{N_{it} \cdot q}{C_{ox}} . \quad (5.7)$$

The effect of an arbitrary space charge $\rho(x)$ distributed over an interface zone of thickness δ is equivalent to a virtual sheet charge σ_{equ} located at the silicon/oxide interface according to

$$\sigma_{equ} = \frac{1}{T_{ox}} \int_0^{\delta} x \rho(x) dx . \quad (5.8)$$

The R-D model can be used to calculate the interface trap density N_{it} of the device which arises under NBT stress for a certain stress time. The calculated N_{it} value can then be used as input quantity for the device simulator Minimos-NT in order to analyze the effect of the generated interface traps on the drain current [130]. The simulator allows to set an interface charge σ at the interface between the semiconductor and the gate dielectric, which leads to a discontinuity of the dielectric flux perpendicular to the interface εE_{\perp} according to

$$\varepsilon_1 E_{1\perp} - \varepsilon_2 E_{2\perp} = \sigma \quad (\text{As/cm}^2) . \quad (5.9)$$

The interface charge density $\sigma = N_{it} \cdot q$ can be interpreted as the number of holes trapped per cm^2 . Fig. 5.7 shows the Minimos-NT result for the degraded drain current of a p-MOSFET at the end of the device lifetime. The simulated device has a gate dielectric of pure SiO_2 with a thickness of $T_{ox} = 3\text{nm}$. Note that this first-order simulation considers only the electrostatic effect of the interface charge on the drain current and ignores the mobility degradation.

5.3.2 Effect of Interface Charge on Mobility Degradation

Coulomb scattering arises due to charged centers in the gate oxide, at the interface, and due to ionized impurities. Higher interface trap densities imply higher Coulomb scattering. This

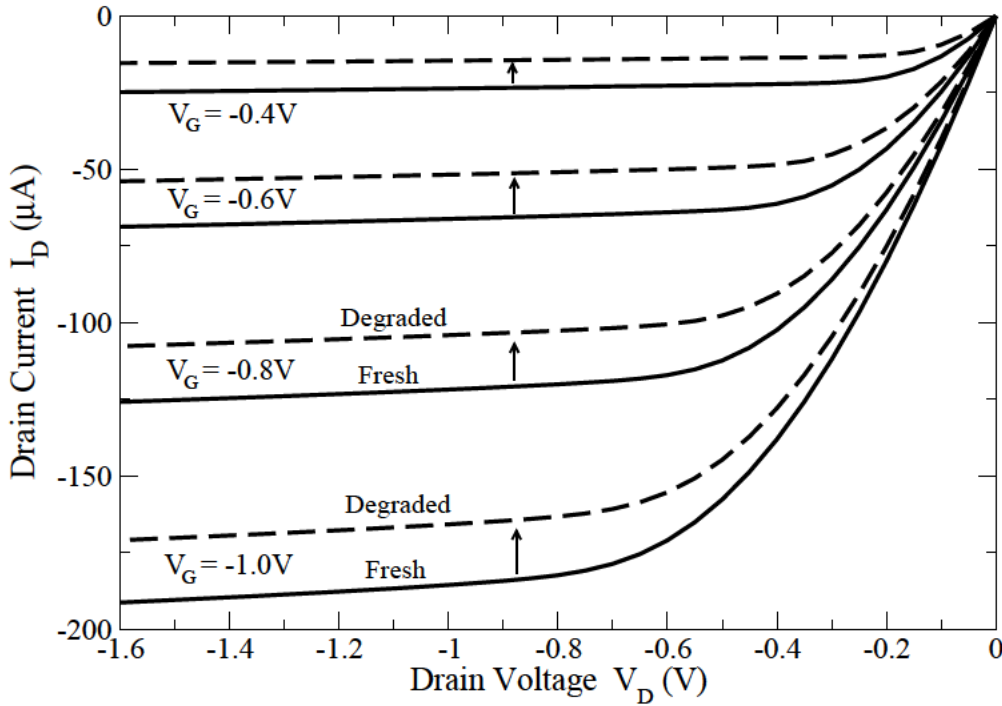


Figure 5.7: Simulated output characteristics of a p-MOSFET before and after NBTI degradation. A shift of $\Delta V_T = -60\text{mV}$ is produced by an interface trap density of $4.31 \cdot 10^{11}\text{cm}^{-2}$ at the end of the lifetime.

dissipative process causes a large mobility degradation for lightly inverted surfaces, but the degradation decreases at higher oxide fields due to increased inversion charge screening. The impact of NBTI on mobility was investigated for a 130nm CMOS technology in [131]. This group reported that the mobility degradation has a significant contribution of approximately 40% to the drain current degradation.

The mobility degradation is primarily large at gate voltages close to V_T and affects also the V_T shift of the device. A device model is used to derive the relationship between V_T shift and trap density N_{it} in a simplified manner [9]. In the following derivation, the absolute values of quantities are specified to describe the p-MOSFET and the subscript “0” denotes the initial value of a quantity before stress. The V_T shift caused by interface traps can be composed by an electrostatic part and a mobility degradation part:

$$\Delta V_T = \Delta V_{T,charge} + \Delta V_{T,Coulomb} . \quad (5.10)$$

The pre-stress drain current is given by the well-known expression for the linear MOSFET region

$$I_{D0} = \frac{W}{L} \mu_0 C_{ox} \left(V_G - V_T - \frac{V_D}{2} \right) V_D . \quad (5.11)$$

If uniformly distributed interface traps N_{it} are introduced, they will cause a drain current degradation firstly due to a loss in mobile charge and secondly due to a degradation in mobility,

which results in

$$I_D = \frac{W}{L} \mu \left[C_{ox} \left(V_G - V_T - \frac{V_D}{2} \right) - qN_{it} \right] V_D . \quad (5.12)$$

The mobility degradation caused by Coulomb scattering can be empirically modeled with a constant α according to

$$\mu = \frac{\mu_0}{1 + \alpha \cdot N_{it}} . \quad (5.13)$$

When the degradation of the transconductance g_m is relatively small, the relative degradation $\frac{\Delta g_m}{g_{m0}}$ can be approximated by

$$\frac{\Delta g_m}{g_{m0}} \approx \frac{\Delta g_m}{g_{m0} - \Delta g_m} = \alpha \cdot N_{it} , \quad (5.14)$$

The result $\alpha \cdot N_{it}$ in equation (5.14) is obtained by differentiating equation (5.11) and (5.12).

Since the threshold voltage V_T is defined for a fixed drain current I_T in this derivation, ΔV_T is the difference in the gate voltage after and before NBT stress. From (5.11) to (5.14) we obtain finally an extended relationship between ΔV_T and N_{it}

$$\Delta V_T = \left[\frac{q}{C_{ox}} + \frac{\alpha L I_T}{W \mu_0 C_{ox} V_D} \right] \cdot N_{it} , \quad (5.15)$$

where the first term accounts for the reduced inversion charge and the second term for the mobility degradation. The degraded p-MOSFET has a reduced transconductance, g_m , and hence a larger gate voltage V_G is required in order to reach the current level I_T which defines the threshold voltage. This results in a contribution by the mobility degradation, $\Delta V_{T,Coulomb} \propto \Delta g_m$, on the total V_T -shift ΔV_T .

5.4 Impact of NBTI Induced Degradation on the Lifetime

The NBTI driven device parameter shift (V_T , I_{Dsat}) over time depends significantly on the frequencies and “on” duty cycles which are used to drive the transistor gate. It will be shown that apart from the rectangular waveform characteristics of the gate signal the supply voltage tolerance of the chip plays also a major role for the transistor lifetime at a given temperature.

5.4.1 Analysis of Device Parameter Degradation

Throughout this work, the analysis of degradation trends for the parameters is based on numerical simulations with a calibrated R-D model. Extensions to the model were made by empirically gained relationships to allow the simulation of current degradation, as well as to include the gate voltage and frequency dependence of the NBTI effect.

Current Degradation

A relationship between the threshold voltage degradation and the current degradation is required in order to translate the calculated shift $\Delta V_T \propto N_{it}$ into the corresponding current reduction ΔI_{Dsat} . Cypress has measured four 90nm p-MOSFET devices at different gate voltages. Fig. 5.8 shows the found linear relationship between the I_{Dsat} shift and the V_T shift, which is caused by operating in a quite linear range of the $I_D - V_G$ transfer characteristic. Note that the spread for the pre-stress parameter I_{Dsat0} of the transistors is eliminated by relating the I_{Dsat} data on the corresponding I_{Dsat0} value. A factor $\vartheta \approx 1$ was found for the relationship between the relative current degradation and the relative V_T degradation given by

$$\frac{\Delta I_{Dsat}}{I_{Dsat0}} = \vartheta \cdot \frac{\Delta V_T}{V_{T0}} . \quad (5.16)$$

Fig. 5.9 shows the impact of AC operation on the drive current degradation of the transistor. Note that the 1 : 1 relation between the relative changes of V_T and I_{Dsat} parameters implies an equal relative degradation level for both parameters.

Behavior of NBTI under AC Conditions

NBTI degradation is independent of the frequency only in the low-frequency regime up to approximately 100Hz. As the frequency is increased further the NBTI degradation decreases significantly with increasing frequency. The effect of the frequency on the V_T parameter shift is demonstrated in Fig. 5.10 for a very low frequency operation. It can be observed that the amplitude of the AC response signals decreases with increasing frequency and all signals oscillate around a similar average degradation level. The reduction in device degradation during AC operation is mainly caused by the passivation of interface traps during the “off” state of the applied duty cycle of 50%. In contrast to that, Fig. 5.11 shows different average degradation levels for AC response signals at different “on” duty cycles. The R-D model assumes a hydrogen dissociation process with constant rate k_f which is switched on and off without a delay by the edges of the gate voltage signal. Therefore this first-order model predicts that the parameter

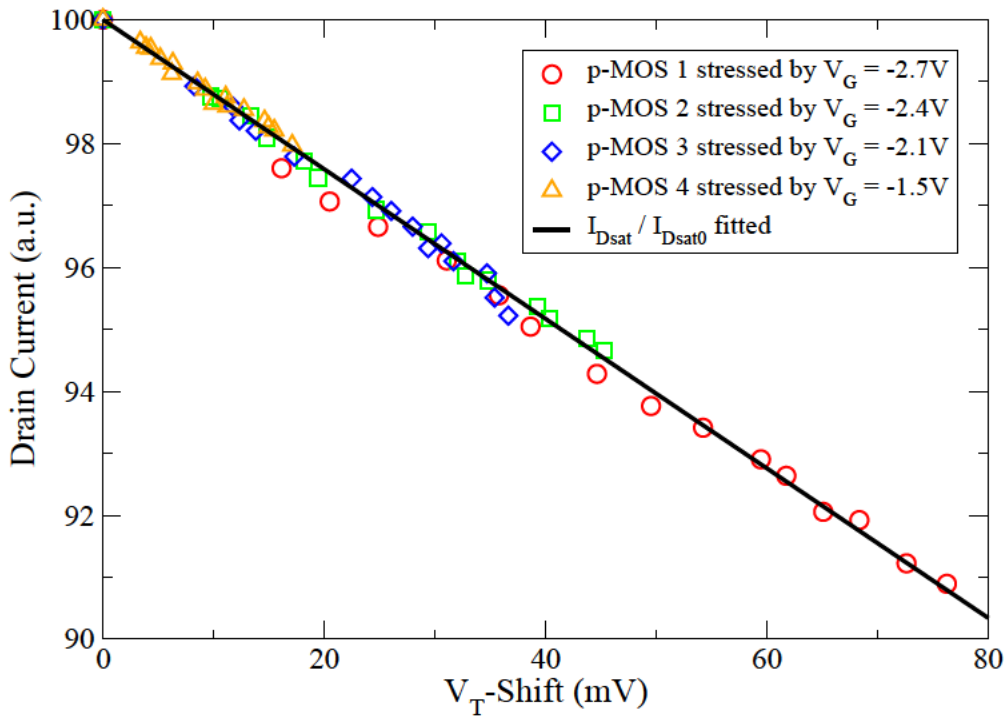


Figure 5.8: The data show a linear relationship between I_{Dsat} shift and V_T shift valid at least up to a 80mV-lifetime ($\approx 20\%$ change in threshold voltage).

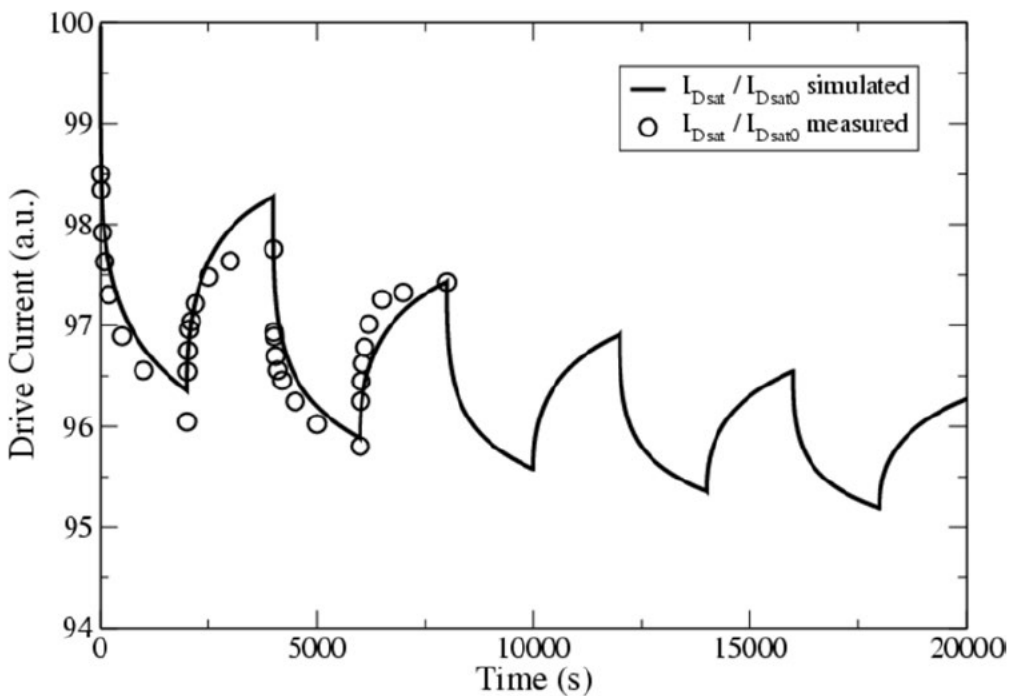


Figure 5.9: Comparison of simulated and measured drive current degradation I_{Dsat} under slow AC operation at 2.4V power supply.

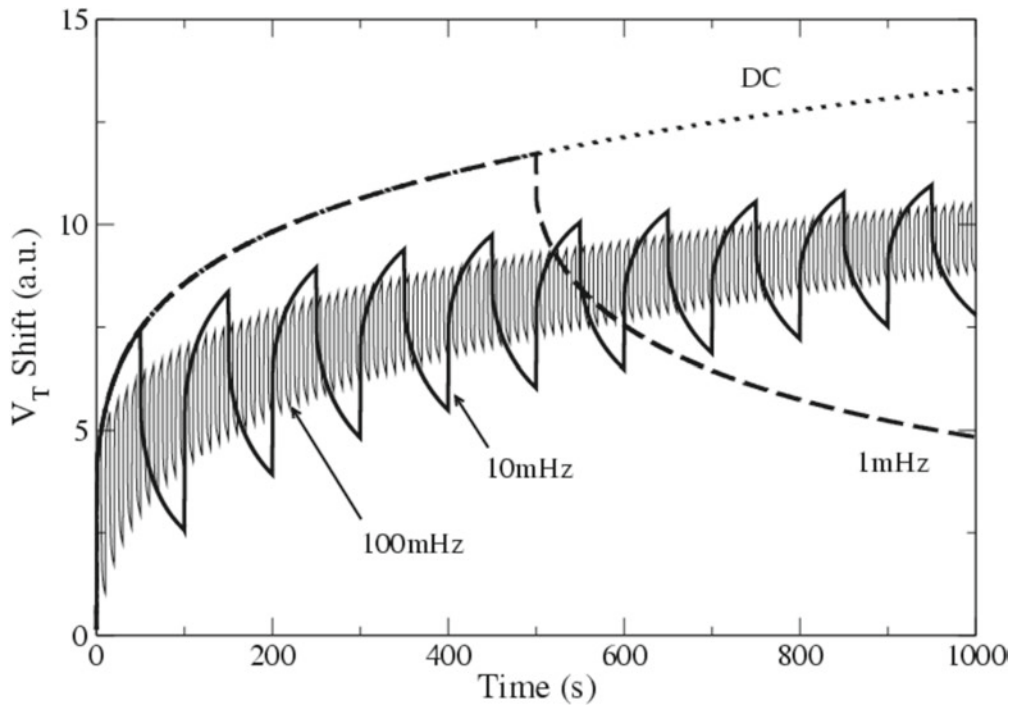


Figure 5.10: Simulation results for the V_T degradation during the first 1000 seconds under AC operation in the low frequency regime.

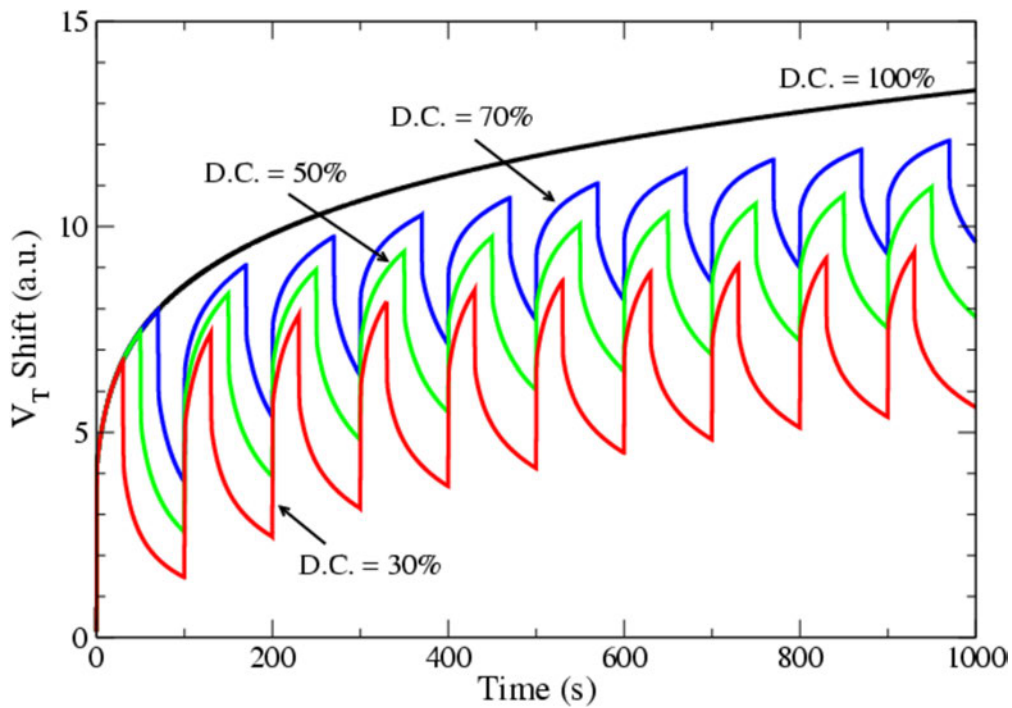


Figure 5.11: The simulations demonstrate the effect of the “on” duty cycle on the V_T degradation during the first 1000 seconds.

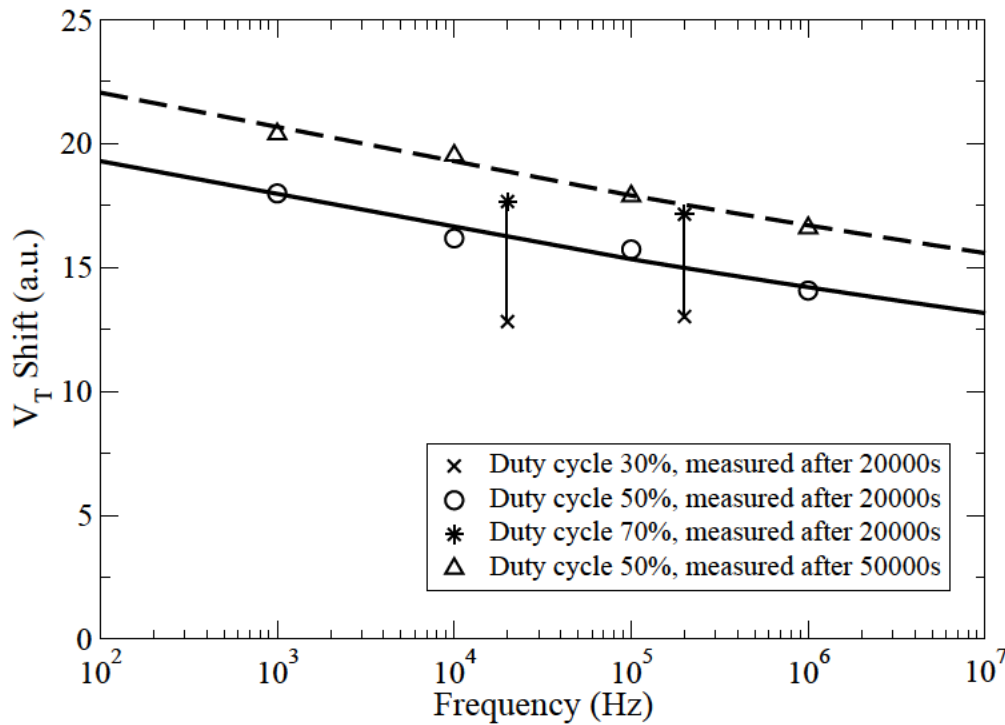


Figure 5.12: Measured V_T shift at different duty cycles as a function of frequency.

shift does not depend on the frequency (it depends only on the duty cycle of the gate signal). However, the measured frequency dependence of NBTI at higher frequencies indicates that there is an asymmetry of the delays between dissociation and annealing. It can be speculated that a short delay exists between the availability of holes and their capture by Si-H bonds. Therefore it can be assumed that the slower starting of the dissociation process is responsible for the reduced parameter shift in the higher frequency regime. The simulation of a higher frequency signal is performed at a low reference frequency f_0 and the result is corrected afterwards with the measured relative V_T shift as function of the frequency according to

$$V_T(f) = V_T(f_0) \left(\frac{f}{f_0} \right)^{-0.03323}. \quad (5.17)$$

Fig. 5.12 demonstrates that the NBTI induced V_T shift is significantly reduced for higher frequencies or smaller “on” duty cycles. Discussions at the IEEE Integrated Reliability Workshop (IRW) in 2005 revealed that the parameter degradation is further reduced above 100MHz.

Electric Field Dependence of NBTI Degradation

Devices of different gate oxide thickness T_{ox} show the same parameter degradation at the same oxide field E_{ox} . The dissociation rate k_f is determined by the available surface hole density p which is controlled by E_{ox} during inversion. Surface holes can tunnel to the Si-H bonds located in the SiO_x interface zone governed by the field E_{ox} . It can be speculated that the amount

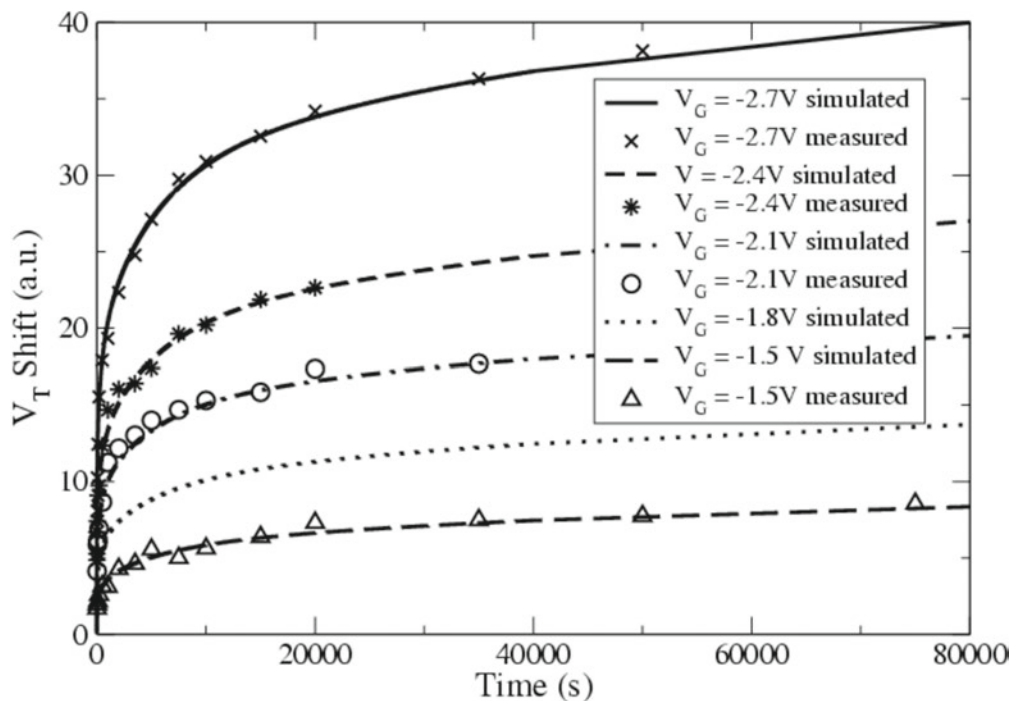


Figure 5.13: Simulated and measured V_T shift at different negative gate bias.

of Si-H bonds N_0 at the interface which can be reached by this stochastic tunneling process increases with the oxide field. Therefore the parameters k_f and N_0 of the R-D model depend on the gate voltage. It was found in [132] that the parameter degradation has a tendency to saturate with increasing stress time, but the saturation value becomes higher under higher stress voltage condition. Fig. 5.13 shows a good agreement between simulation results and experimental data in the whole measurement range from -1.5V up to -2.7V. The V_T degradation depends on the gate voltage in a nonlinear manner, in particular in the higher stress-voltage regime.

5.4.2 Analysis of NBTI Lifetime

Currently there is no clear specification for the characterization of NBTI lifetime across industry. Companies use various stress conditions for NBTI measurements as well as different electrical stability requirements for their lifetime projections. A reasonable failure criterion for the 90nm CMOS technology is, for instance, to tolerate a maximum shift of 10% for the key device parameters V_T and I_{Dsat} at 125°C. The maximum tolerable parameter shift is determined by process-related parameter fluctuations like random dopant fluctuations or circuit applications. Fig. 5.14 shows long-time simulations for the lifetime estimation at a supply voltage of 1.5V under DC and AC operation up to 10MHz. It can be observed that the diffusion-limited regime is reached rapidly which is characterized by a reduced slope of the V_T shift over time. Note that the worst-case is assumed for the degradation slope at large stress times where no significant further reduction in the slope occurs.

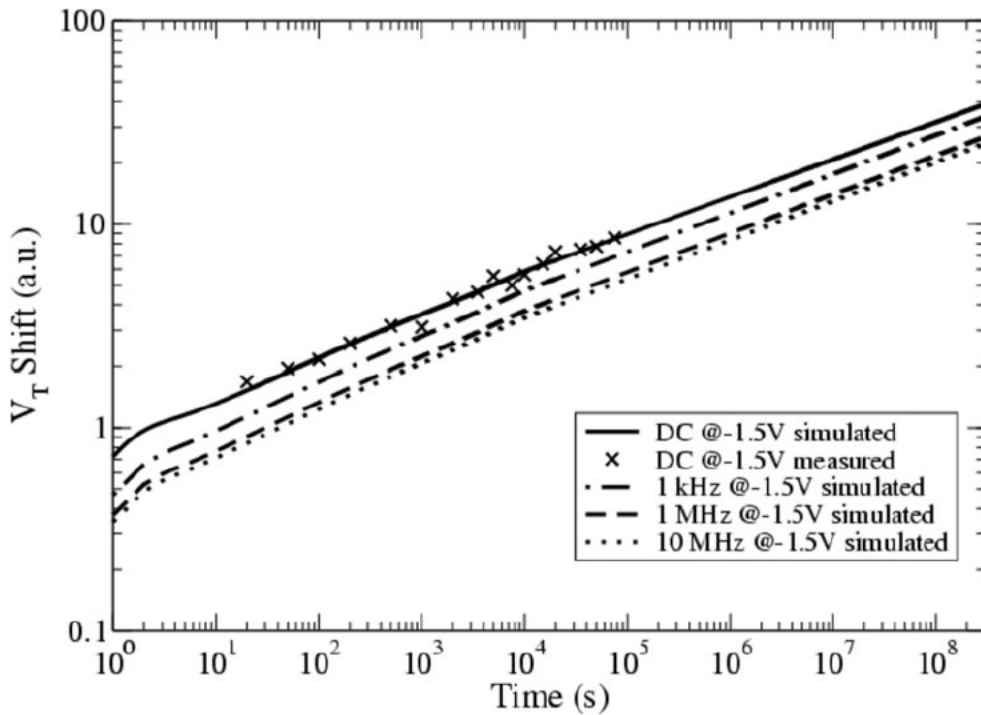


Figure 5.14: Long-time simulations for the V_T shift at chip operating frequencies in the MHz-range at a power supply of 1.5V.

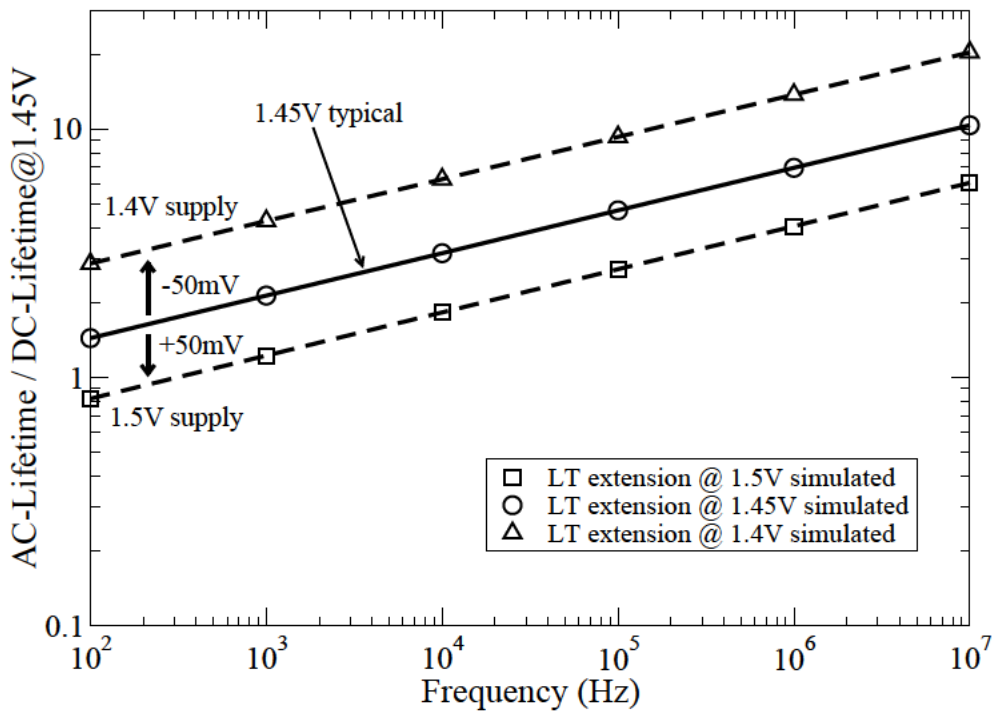


Figure 5.15: Simulated lifetime extension under AC operation for slightly different supply voltages of the chip.

The lifetime extension of the p-MOSFET under higher frequency operation is analyzed quantitatively in Fig. 5.15. The lifetime at a typical power supply of 1.45V and a frequency of 10MHz is ten times higher than the DC lifetime. Due to the high voltage sensitivity of NBTI the impact of a power supply tolerance of $\pm 50\text{mV}$ is investigated. The device lifetime is defined here by a V_T shift of 80mV. The simulation predicts that the AC lifetime at 10MHz lies between six times (for 1.5V supply) and twenty times (for 1.4V) of the DC lifetime at 1.45V operation. A remarkable result is also that the lowering of the 1.5V supply by only 50mV improves the NBTI lifetime by a factor of 1.8.

The NBTI mechanism was systematically investigated for a 90nm CMOS technology in this section. Experiments for different gate voltages, frequencies, and duty cycles were performed in cooperation with Cypress to analyze the device parameter degradation of the p-MOSFET. It turned out that the R-D model is well suited to explain static and dynamic experimental data. The gate voltage and frequency dependence of NBTI was included by means of an empirical relationship. All measured data could be well reproduced by the performed numerical simulations. The presented simulation approach allows, on a physically rigorous basis, to predict the p-MOSFET lifetime which depends strongly on the applied stress conditions.

Chapter 6

Applications

This chapter mainly presents three-dimensional simulation applications of ion implantation processes for the investigation of dopant distributions in topological complex targets. The strained or relaxed high-mobility materials employed in the modeled device structures will likely be introduced in leading-edge CMOS technology in the next several years. The simulation on computers is advantageous over experimentally obtained doping profiles. Firstly, it is faster and cheaper, and secondly, only one-dimensional doping profiles can be measured by the SIMS technique. Two- and three-dimensional simulation results provide a better insight into the implantation process than an indirect measurement like measuring the electrical conductivity after some process steps. The simulator MCIMPL-II has been ported to the operating system AIX since the simulation of large three-dimensional device geometries requires a huge amount of computer memory. Most of the three-dimensional applications in this chapter were performed on an IBM-AIX p655 cluster with 64 Gigabyte of main memory per node.

A special emphasis in the ion implantation applications is laid on the formation of ultra-shallow junctions, since this topic is one of the most important issues for processing heavily shrunk MOS devices. The simulation of low-energy source/drain and extension implants is an attractive example to demonstrate the simulation capabilities of a TCAD tool to analyze and optimize the resulting dopant distribution in the device after multiple implantation steps by tuning the process parameters of a single step. Furthermore, a three-dimensional simulation treatment allows to study shadowing effects which arise for large tilt-angle implantations by using self-aligned masking techniques. The most prominent representative of this application class is the halo implantation for punch-through suppression in advanced CMOS devices. However, an important point is that the underlying implantation process is compatible with contemporary CMOS process technology and it can be performed with existing ion implantation equipment.

The NBTI reliability must be investigated under DC and AC stress conditions for any high-performance CMOS technology that uses nitrated gate oxides. The calibrated NBTI model described in Section 5 is used to study NBTI degradation and lifetime for a full SRAM cell based on a 90nm technology. In the performed simulation study, the impact of storing random bit values on the NBTI lifetime of the memory cell is analyzed. We determine the lifetime extension related to the DC lifetime of the cell as function of the probability for storing a one bit between 100% and 50% every second.

6.1 Simulator Check on a Three-Dimensional Test Structure

The goal of the two presented three-dimensional simulation applications is to evaluate the simulator in terms of functioning and performance. A relatively simple structure is used in both implantation applications, which represents a portion of an STI-isolated MOS device.

6.1.1 Low-Energy Arsenic Implantation

Downscaling of MOS transistors requires the formation of very shallow source/drain junction depths which are estimated in Section 1.3 for future CMOS technologies. It is expected that ion implantation technology will continue to dominate the junction formation for advanced MOS devices. Shallow n-type source/drain regions can be easily formed by low-energy arsenic implantation supported by the rapid formation of a fully amorphous layer during the implantation process caused by the high mass of arsenic ions and high implantation doses.

The input structure and the mesh for the arsenic implantation are shown in Fig. 6.1, which has been generated in a similar manner as described in the demonstration example in Section 3.2.5. The MOS structure has a base area of 266 x 180nm and consists of four segments including the standard materials silicon, oxide, and polysilicon. A scattering oxide layer with a thickness of 5nm is used on top of the silicon substrate which is surrounded by STI isolation in the modeled structure. The mesh for the projected shallow implant has 19478 mesh points and 101406 tetrahedral elements. An anisotropic mesh refinement has been applied locally to optimize the mesh for the intended shallow doping and to keep the overall grid below 20 000 points. Arsenic ions have been implanted with an energy of 5keV, a dose of $5 \cdot 10^{14} \text{cm}^{-2}$, and a tilt of 7° . The

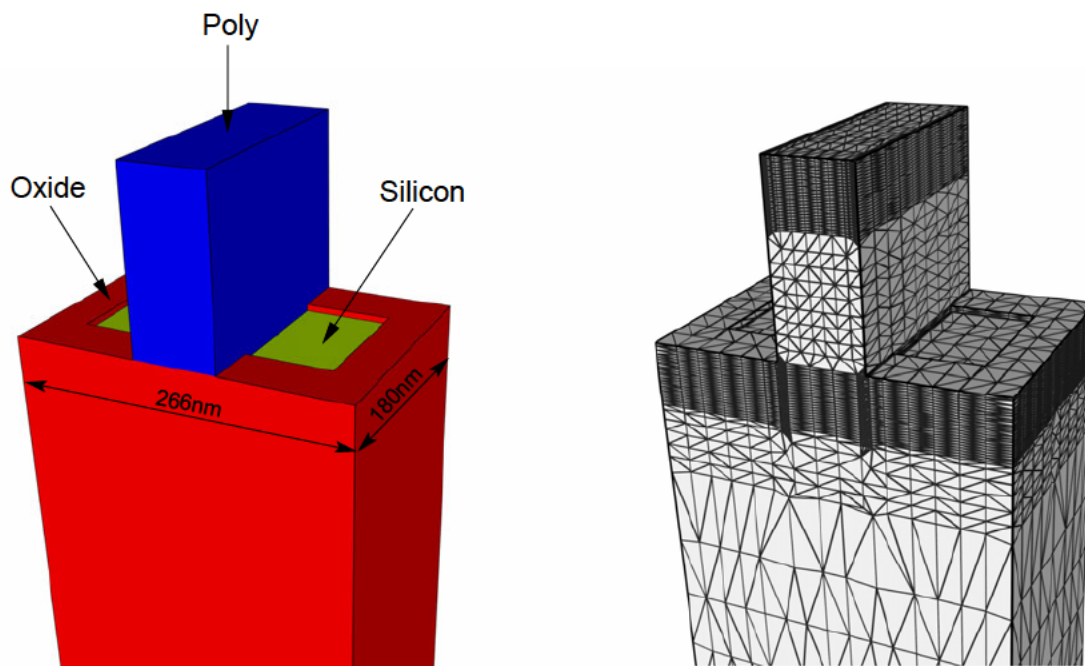


Figure 6.1: MOS structure (left) and mesh for the shallow arsenic implant (right).

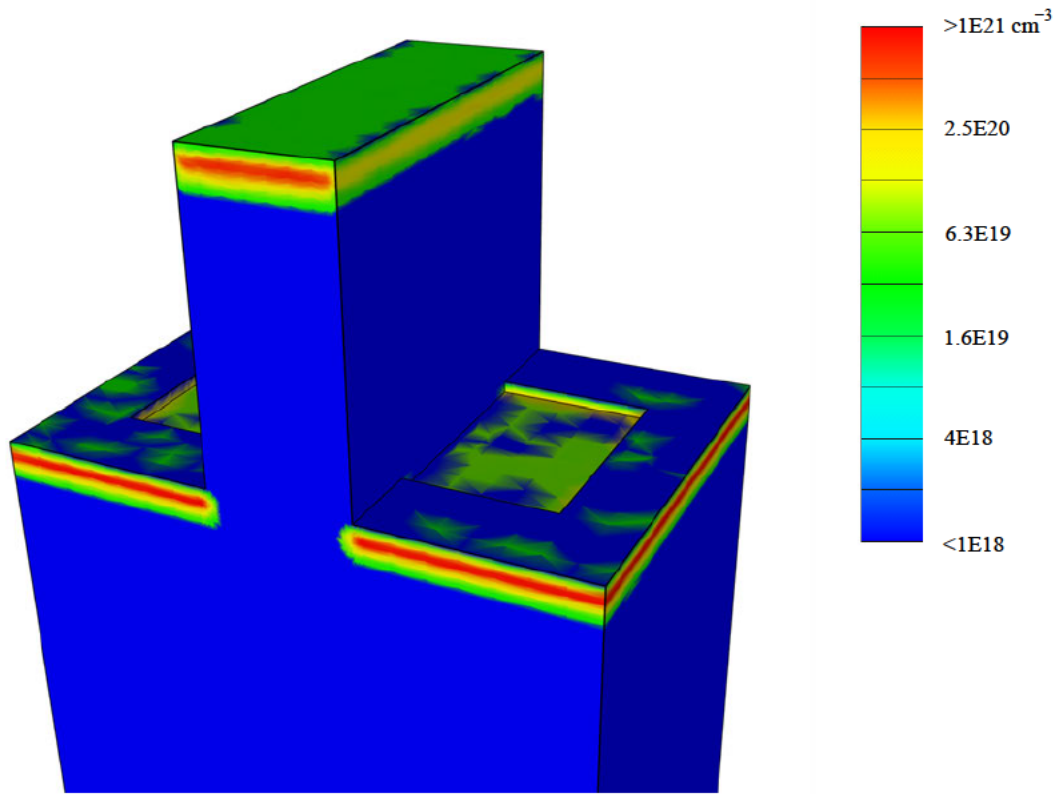


Figure 6.2: Shallow 5keV arsenic-implant distribution in the MOS structure.

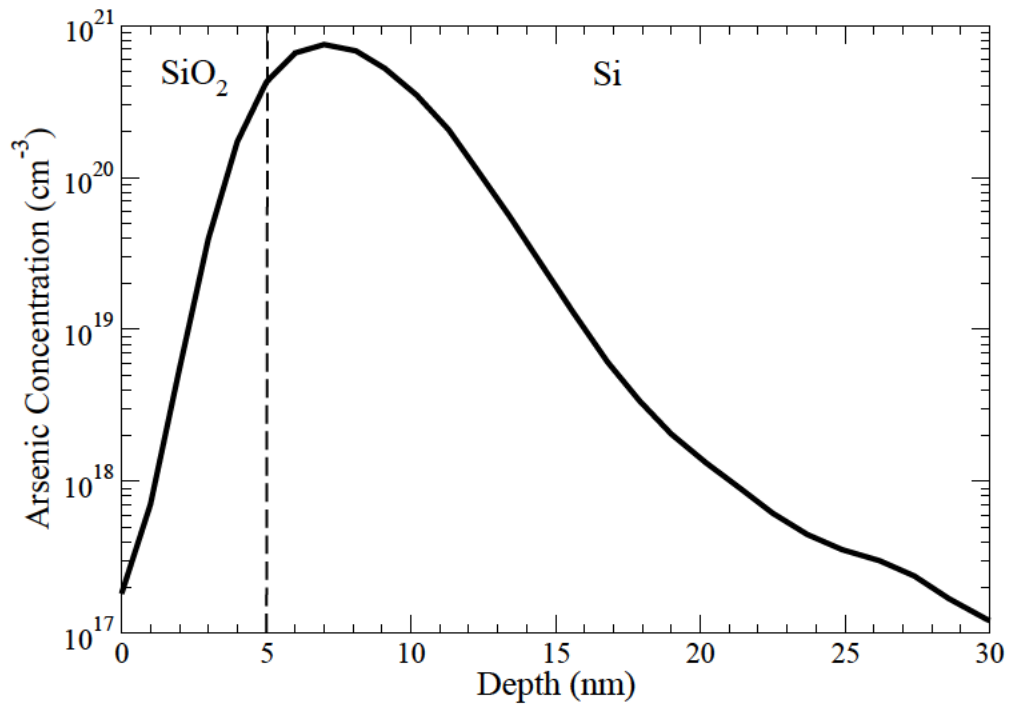


Figure 6.3: Simulated shallow 5keV arsenic implant profile in the substrate.

accurate Monte Carlo simulation with eight million ions resulted in the three-dimensional arsenic distribution presented in Fig. 6.2. The corresponding one-dimensional arsenic concentration profile in Fig. 6.3 was obtained by only $2 \cdot 10^5$ simulated ions. The doping profile reaches its peak concentration of almost 10^{21} atoms/cm³ at a depth of 2nm below the surface of the substrate and it is characterized by a steep rise and fall of the dopant concentration around the maximum.

6.1.2 Large-Tilt-Angle Boron Implantation With Quad Repositioning

The *LAT (large angle tilt) implantation technique* can be employed to achieve a larger lateral penetration of the dopants under a mask edge for processing optimized device structures required for advanced CMOS applications. This technique uses large tilt angles in combination with target wafer rotational repositioning during the implant processing sequence, without removing the wafer from the implant platen. The LAT implant technology is typically applied to form the halo implants (or “pocket” implants) for the punch-through suppression in shrunk MOS devices. A tilt of 30° is used for the simulated sequence of boron implantations which are performed by using a wafer rotation of 90° after each implantation step. The already used “Manhattan” structure is well suited to demonstrate the equality of the obtained boron distributions between the twist angles of 0° ↔ 180° and the symmetry between 90° ↔ 270°.

The structure and the generated mesh for the boron implantation are shown in Fig. 6.4. The created volume mesh consists of 8228 mesh points and 41266 tetrahedral elements of similar size. The simulated boron distributions are shown in Fig. 6.5, processed with an energy of 25keV, a dose of 10^{13} cm⁻², and a tilt of 30°. The Monte Carlo simulation was carried out with four million

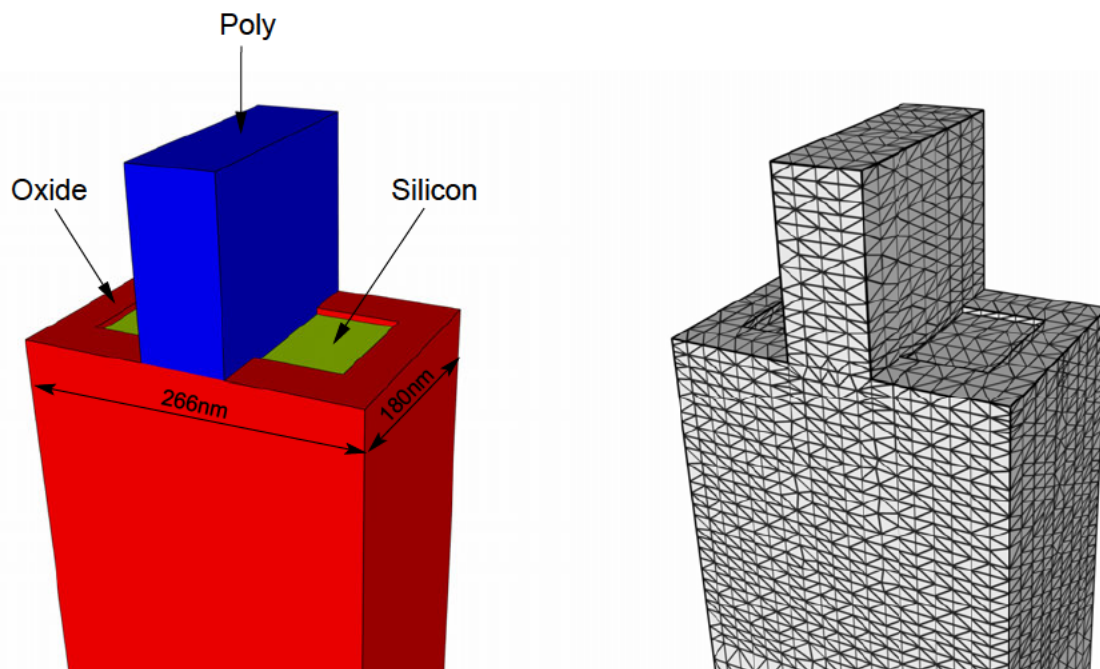


Figure 6.4: MOS structure (left) and mesh for the deep boron distribution (right).

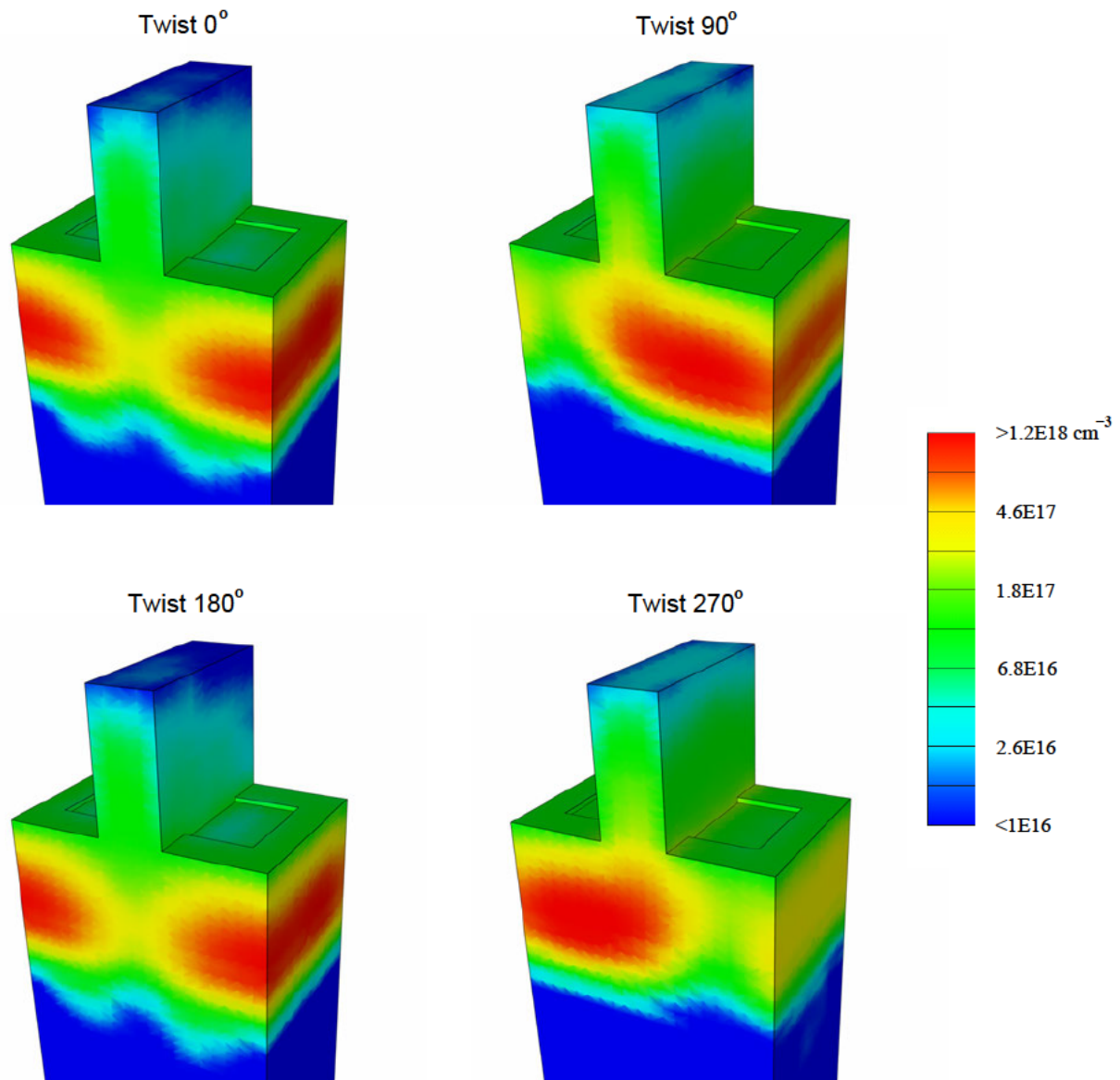


Figure 6.5: Sequence of four 25keV boron LAT implants with a tilt of 30° , processed by 90° rotational repositioning of the test structure.

particles for each implantation step. The simulation domain and the external implantation window were both expanded by about 50nm perpendicular to the front, back, left, and right boundaries of the input geometry to avoid any boundary influence for the dopant distribution at the surface of the device structure. Fig. 6.5 demonstrates the successfully performed symmetry check for the simulator MCIMPL-II. The three-dimensional results obtained at a twist of 0° and 180° are evidently equal, while the results at 90° and 270° are mirror-symmetric to each other.

The boron LAT implants in the one-dimensional SiO_2/Si layer structure were simulated with $2 \cdot 10^5$ ion trajectories by using the same implantation conditions as for the three-dimensional

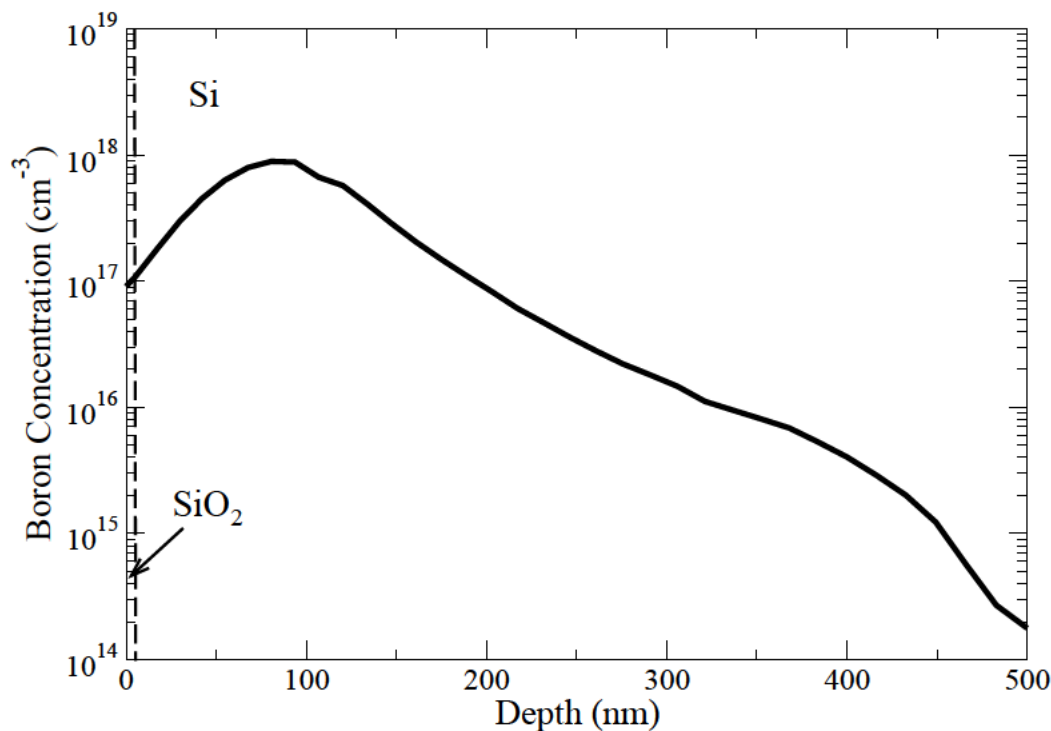


Figure 6.6: Simulated boron profiles for the twist angles of 0° , 90° , 180° , and 270° .

test structure. Fig. 6.6 demonstrates that all four boron implantations yield the same doping profile since the used ion beam directions are crystallographically identical.

6.2 Source/Drain Engineering for a Strained Silicon n-MOSFET

The formation of ultra-shallow source/drain and extension regions by two ion implantation steps is demonstrated for a 65nm gate-length n-MOS transistor, which is shown in Fig. 6.7. The modeled device structure has a 12nm thick strained silicon channel layer on top of a 620nm thick relaxed $\text{Si}_{0.8}\text{Ge}_{0.2}$ virtual substrate block with a base area of $170 \times 600\text{nm}$. The gate oxide has a thickness of 2nm and can be grown by thermal oxidation of strained silicon. The simulated high-performance n-MOS transistor is electrically isolated from other devices by using a chip-area saving shallow trench isolation (STI). The MOS structure can be used for processing strained silicon n- and p-MOSFETs depending on the implanted dopant species. Using scaling considerations, a source/drain vertical junction depth around 27.5nm is recommended by the ITRS roadmap for the fabrication of a 65nm technology node, as shown in Table 1.1.

In the first ion implantation step, the arsenic source/drain extensions were implanted with an energy of 2 keV and a dose of 10^{15}cm^{-2} . Fig. 6.8 shows the arsenic distribution in the device structure without sidewall spacer after smoothing of the Monte Carlo result and translating it to the destination mesh. For the ion implantation simulation of the source/drain extensions,

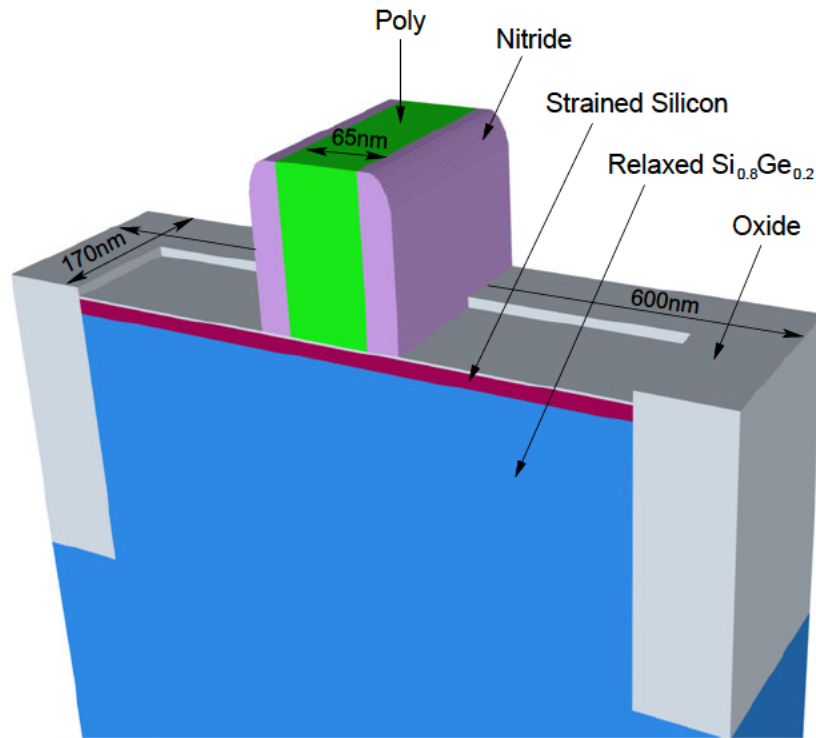


Figure 6.7: Modeled structure of the half of a high-performance strained-Si/Si_{0.8}Ge_{0.2} n-MOSFET with an STI isolation scheme.

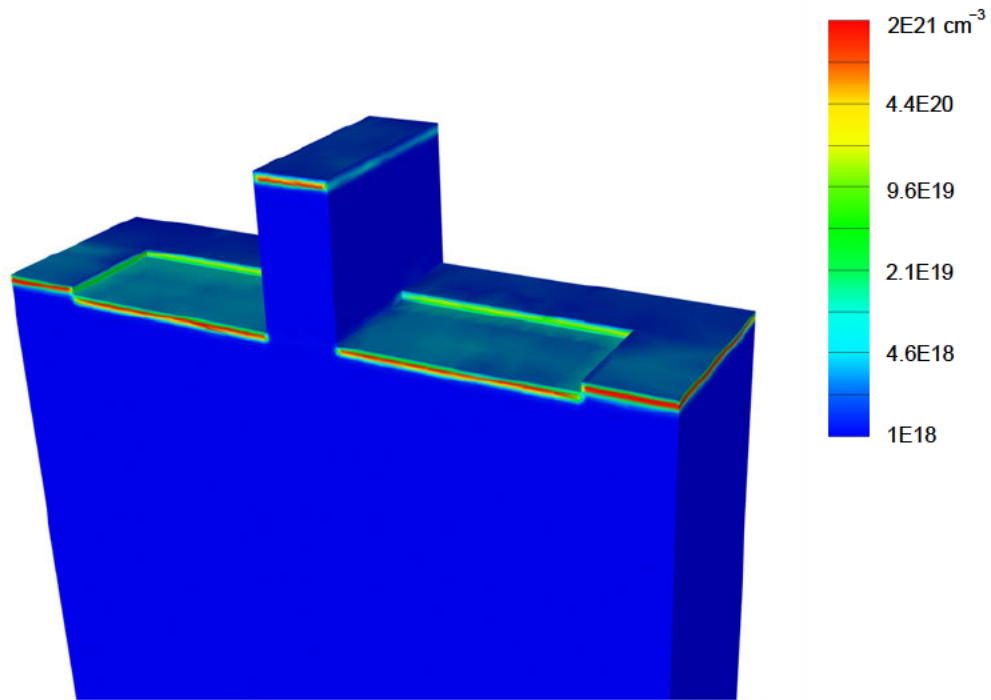


Figure 6.8: Simulated three-dimensional dopant distribution in the n-MOS structure after performing the 2keV arsenic source/drain extension implantation.

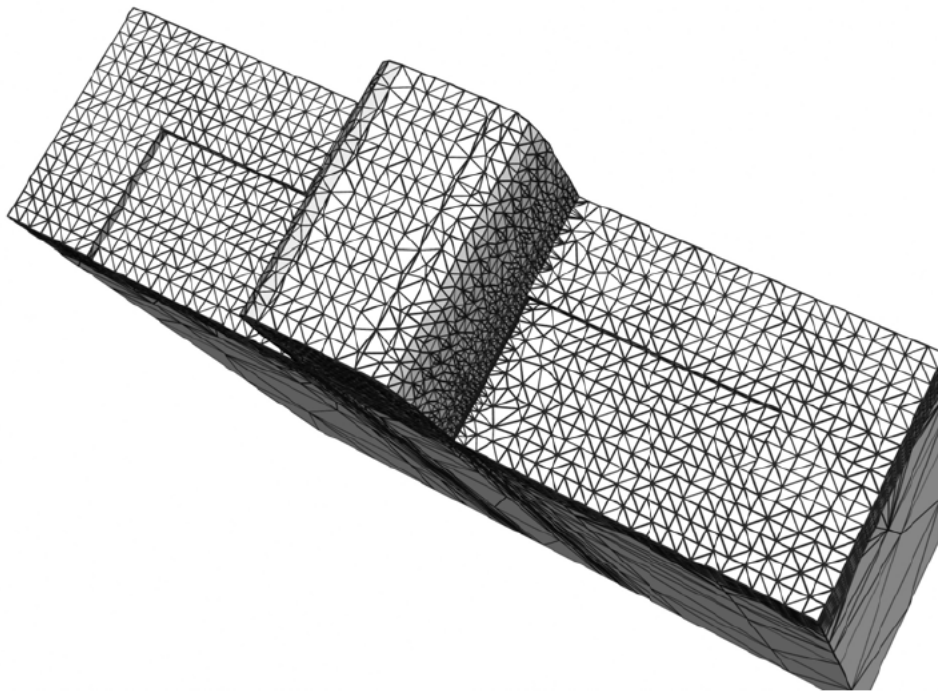


Figure 6.9: Top view of the meshed STI transistor structure with sidewall spacer.

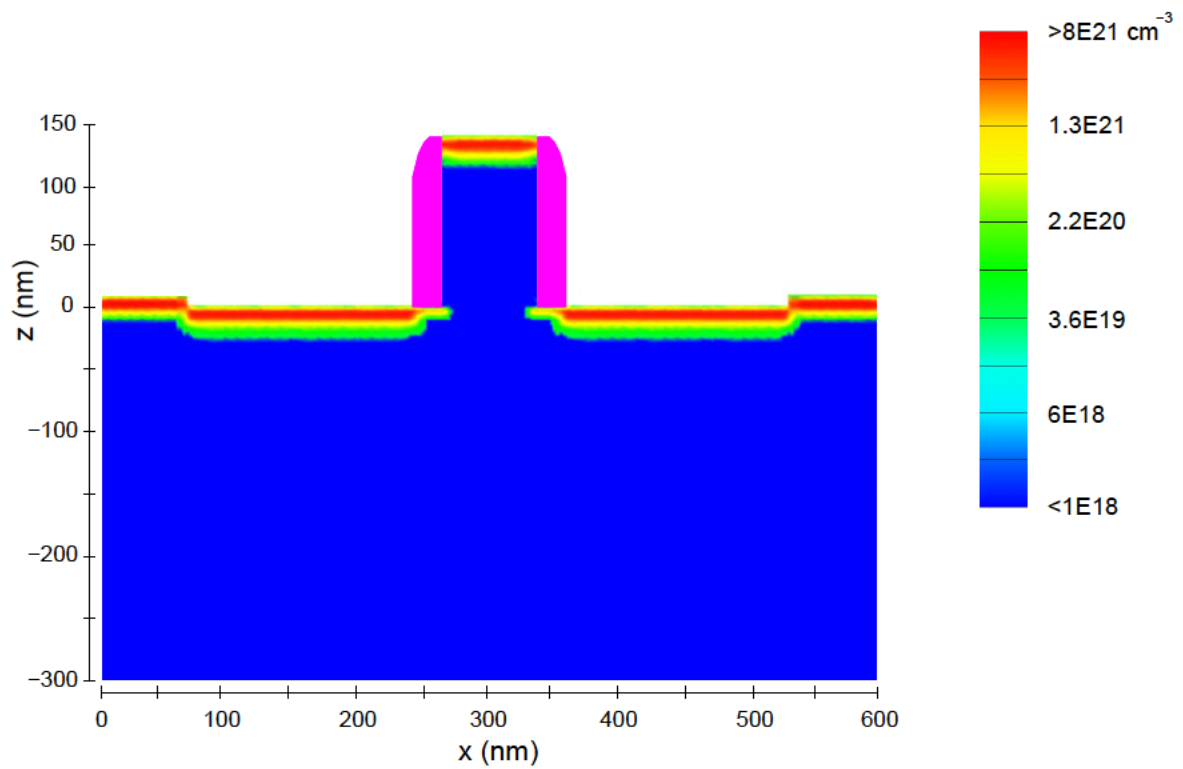


Figure 6.10: Final dopant distribution in the cross-section of the MOSFET along the channel after performing the 6keV arsenic source/drain implantation.

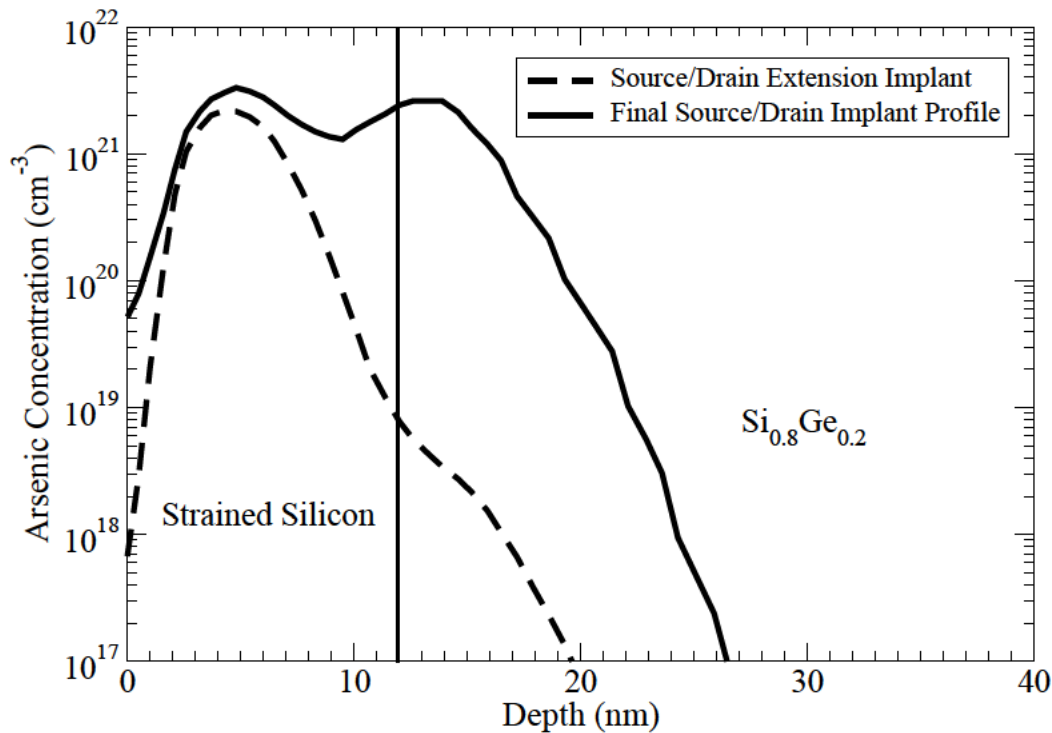


Figure 6.11: Final implanted source/drain doping profile of the strained n-MOSFET along a vertical line through the drain region.

the nitride spacer segment is cut off from the meshed transistor structure. Fig. 6.9 shows the meshed structure required to simulate the second implantation step in the two-step sequence. While no additional segments can be added to a final meshed device structure, any non-required segment of the structure can be removed.

In the second arsenic implantation step, the source/drain regions are formed using an energy of 6 keV and a dose of $5 \cdot 10^{15} \text{ cm}^{-2}$. Fig. 6.10 shows the simulated cross-section along the channel of the strained n-MOSFET after performing the source/drain implants. In this application the Monte Carlo simulation was carried out with $2 \cdot 10^7$ ion trajectories per implantation step to achieve a low statistical fluctuation of the predicted doping profiles.

The use of multiple ion implantation steps with different energies and doses allows to optimize the doping in the device for source/drain engineering problems. Fig. 6.11 compares the simulated one-dimensional doping profiles obtained after the first and after the second arsenic implantation step. The superposition of both implanted dopant distributions produces two peak concentrations in the final arsenic profile. The simulation analysis of a specific ion implantation sequence is very useful to determine the exact process parameters required for a desired doping profile. The shown arsenic profile in Fig. 6.11 reveals that the critical junction depth of 27.5nm is not exceeded for the 65nm n-MOS transistor in this implantation application. Finally, P. Kohli and R. Wise found that arsenic and boron dopants show very little diffusion in the strained-Si/Si_{0.8}Ge_{0.2} bilayer system by using a flash-assist RTA technique [26].

6.3 Formation of Interdigitated Germanium PIN-Photodiodes

In optical transmission systems, an operation at $1.3\mu\text{m}$ and $1.55\mu\text{m}$ wavelengths is preferred due to the low attenuation in fiber-optic cables. Germanium is an attractive candidate for high-speed photodetector applications due to its high electron mobility and high optical absorption coefficient in this wavelength range [133]. Recently, a bandwidth of 10GHz has been demonstrated at a wavelength of $1.3\mu\text{m}$ for a PIN-photodiode, fabricated in epitaxial Ge-on-Si technology [110]. The use of germanium is advantageous over III-V compound materials in terms of lower fabrication costs and feasible integration with silicon CMOS technology.

Compositionally graded SiGe layers are deposited on the silicon wafer to achieve a $1\mu\text{m}$ thick germanium layer with a low defect density. In this doping application, the interdigitated p^+ - and n^+ -finger regions of the photodetector are formed by ion implantation. For this purpose, photoresist masks are used to define the finger structure with a width of $1\mu\text{m}$ and a spacing of $2\mu\text{m}$. Fig. 6.12 shows the schematic top and cross-sectional views of the final PIN-photodiode. This large area photodetector consists of elementary photodiodes which are connected in parallel. An elementary photodiode can be defined as the three-dimensional region from the center of a p^+ -finger to the center of an n^+ -finger. In the first process step the p^+ -fingers are patterned and boron is implanted with an energy of 15keV and a dose of $2 \cdot 10^{15}\text{cm}^{-2}$. The three-dimensional boron distribution, as shown in Fig. 6.13, was obtained by using a 5nm thick oxide scattering layer on top of germanium. In the second process step the n^+ -fingers are formed by an implan-

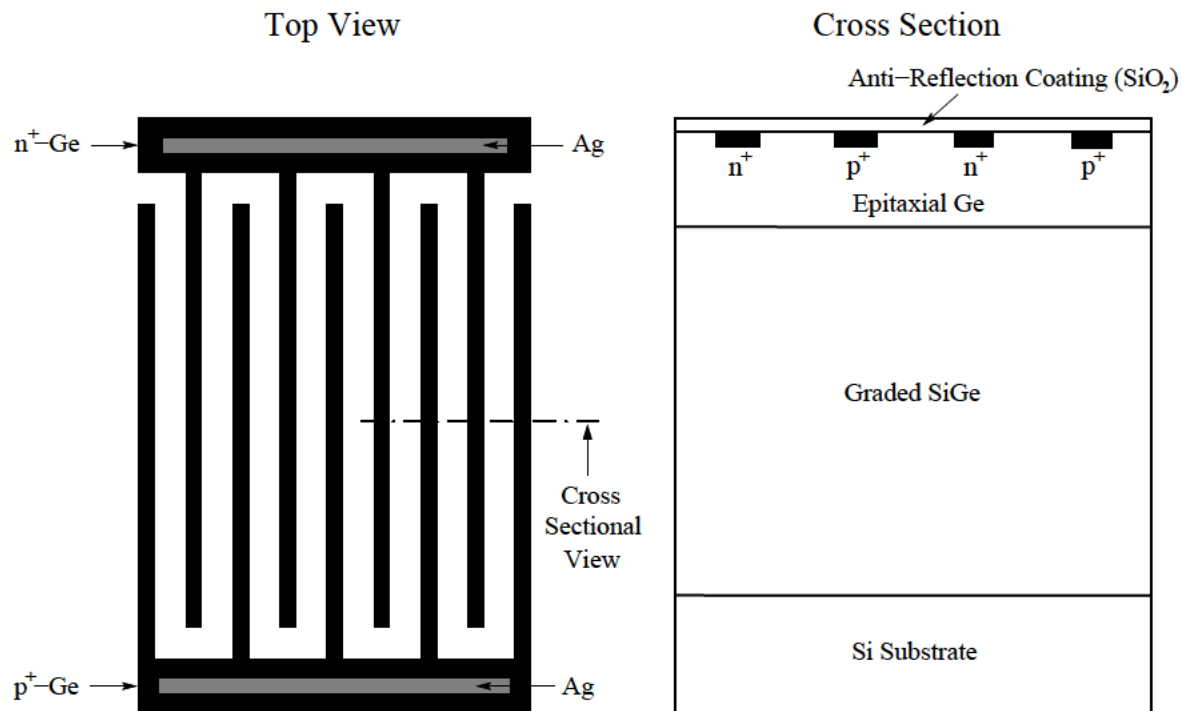


Figure 6.12: Layout (left) and cross-section (right) of a high-speed Ge-on-Si PIN photodetector with planar interdigitated p^+ - and n^+ -fingers.

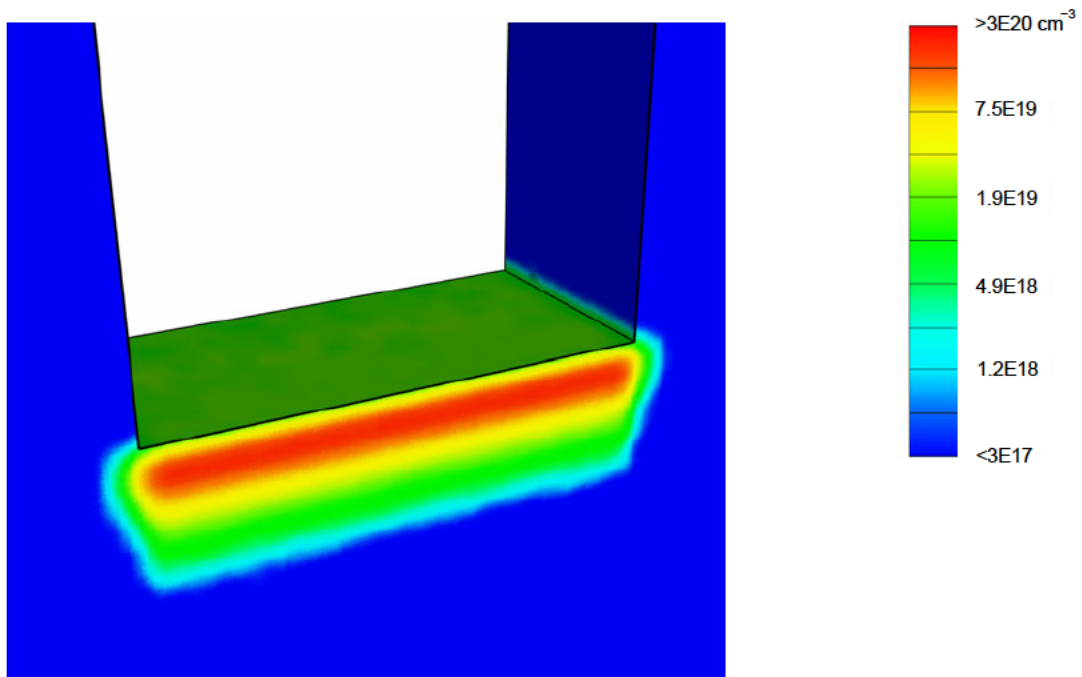


Figure 6.13: Simulated 15keV boron implantation step for the p^+ -finger formation in germanium using a photoresist mask.

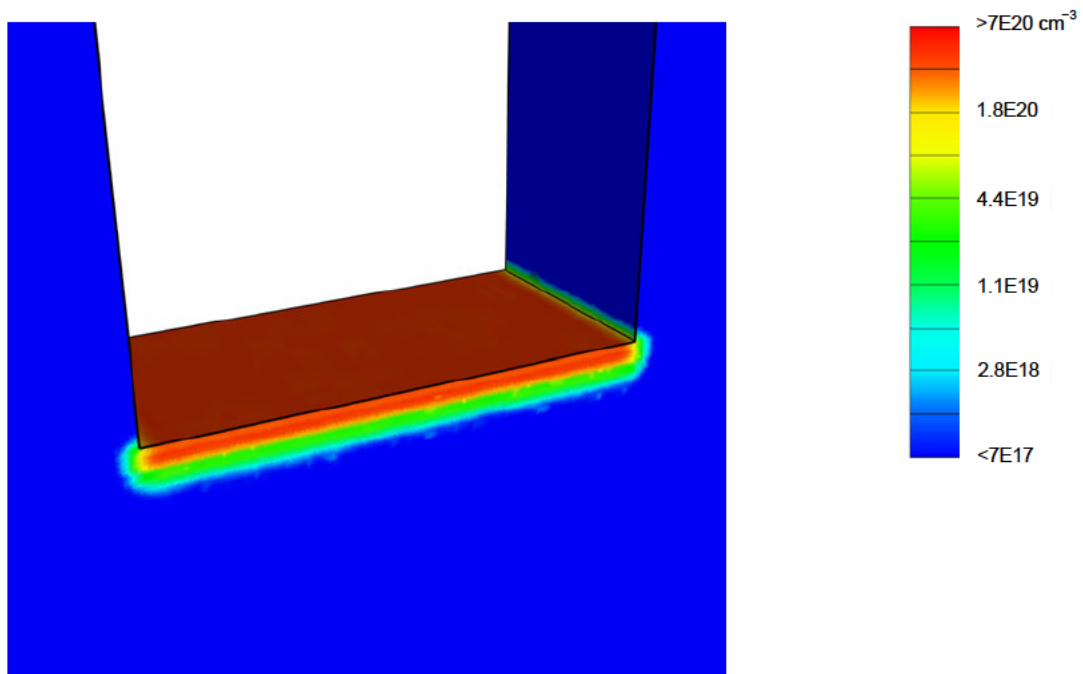


Figure 6.14: Simulated 60keV arsenic implantation step for the n^+ -finger formation in germanium using a photoresist mask.

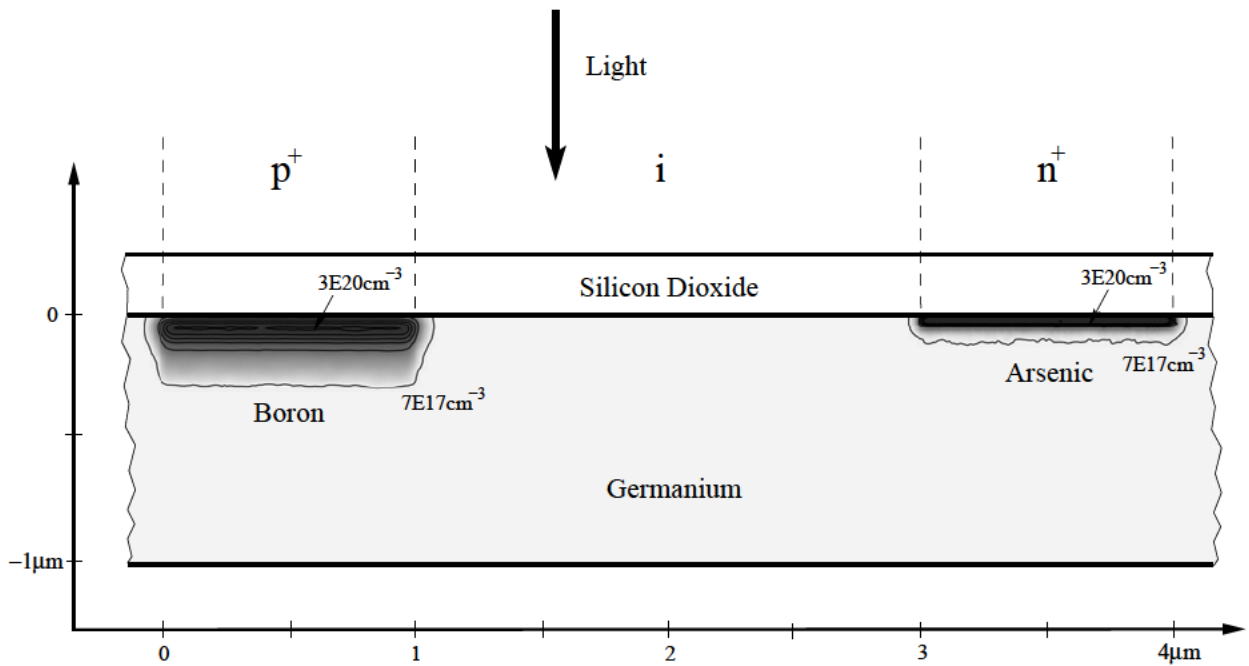


Figure 6.15: Simulated doping concentration isolines in the p⁺- and n⁺-fingers of an elementary PIN-photodiode of the detector in the cross-sectional view.

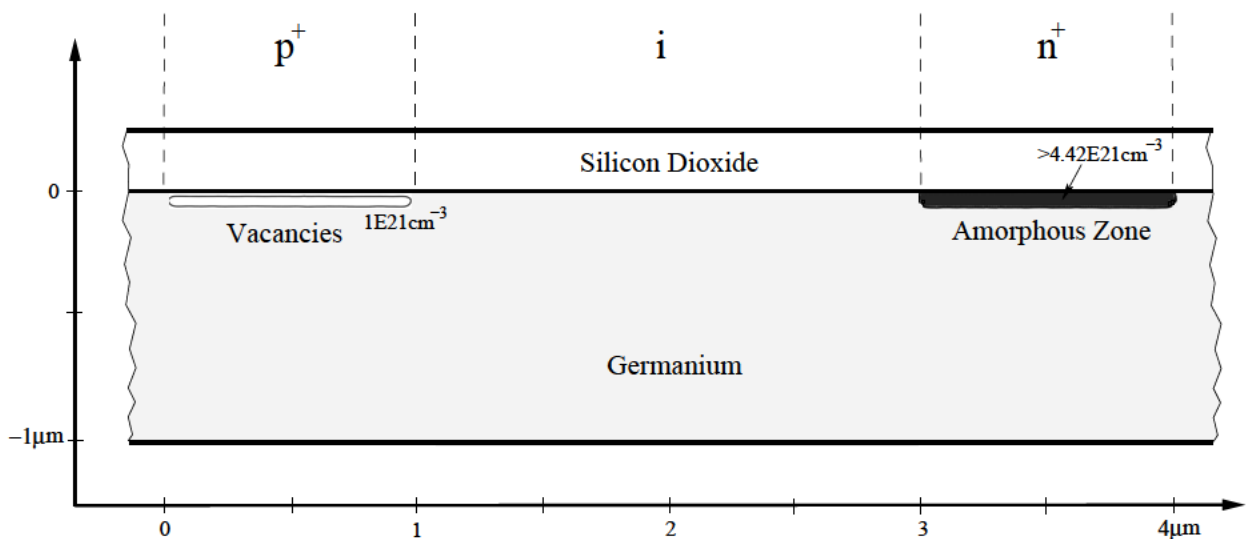


Figure 6.16: Simulated amorphization of germanium in the finger regions after the boron and arsenic implantations with a dose of $2 \cdot 10^{15} \text{cm}^{-2}$.

tation of arsenic with an energy of 60keV and same dose. The shallow arsenic distribution in the simulated device part is presented in Fig. 6.14. In spite of the lower implantation energy, boron ions can penetrate much deeper into the germanium layer than arsenic ions. Fig. 6.15 allows to compare the simulated boron and arsenic profiles in the PIN-photodiode by using equal doping concentration isolines. The reason for the large channeling tail of the boron profile lies mainly in the small amount of produced point defects in germanium. The critical level of point defects (Frenkel pairs) needed for amorphization of germanium is about $4.42 \cdot 10^{21} \text{cm}^{-3}$, one tenth of the germanium atomic density [134]. Fig. 6.16 demonstrates that the arsenic implantation has produced an amorphous zone, while the maximum defect concentration of the boron implantation is significantly lower than the amorphization level. The predicted damage results are consistent with experimental observations obtained by processing a PIN-photodiode on a germanium substrate under similar process conditions. In [135] it was found that the as-implanted resistance of the boron implant was $201 \Omega/\square$ at a dose of $2 \cdot 10^{15} \text{cm}^{-2}$, while that for the arsenic implant was not measurable. This fact strongly indicates that boron-implanted germanium remains crystalline at least up to the used dose, while arsenic-implanted germanium becomes amorphous.

6.4 NBTI Lifetime Analysis of a CMOS SRAM Cell

Conventional six-transistor CMOS SRAM cell structures are dominantly employed in today's cache memory blocks for advanced microprocessors. The long-term stability of such a CMOS memory cell is strongly affected by NBTI induced degradation of MOSFET parameters (e.g. threshold voltage) which leads to a reduction in the static noise margin (SNM) of the cell [136]. As explained in Section 5, negative bias temperature instability (NBTI) in p-MOSFETs with nitrated gate oxides has emerged as the dominant degradation mechanism for newer CMOS technologies. The AC degradation is significantly lower than the DC degradation for any given stress time, since the interface traps generated during the on-state of the MOSFET are partially annealed in the off-state (dynamic NBTI effect). While transistor degradation in CMOS-based NAND circuits depends on the AC operating conditions (e.g. clock frequency), in SRAM cells it is possible that a stored bit value does not change for a long time. On the other hand, it would be too strict to equate the lifetime of an SRAM transistor with its DC lifetime. The two p-MOSFETs employed in a 6T-SRAM cell are unsymmetrically NBT stressed by the stored bit values. The split of on-state times between the two devices (only either of them is "on") lies well within the boundaries of pure DC stress (100/0 stress-split) and symmetric AC stress (50/50 stress-split). Only a periodically flipping of the bit with comparable on-times would lead to equal parameter degradation of both devices and hence to the longest lifetime of the SRAM cell. The worst-case lifetime of an SRAM cell can be determined by storing a random bit sequence where the probability is, for instance, 90% for storing a "one" (or 90% for storing a "zero") which corresponds to a 90/10 NBT stress-split. In this simulation study, NBTI responses to random bit sequences are studied by using a calibrated reaction-diffusion model [137].

The investigated SRAM cell, shown in Fig. 6.17, was fabricated in a 90nm process technology. The cell consists of two cross-coupled CMOS inverters (T1, T2 and T3, T4) and the access transistors T5 and T6. While the p-MOSFETs T2 and T4 are affected by NBTI as long as the power is supplied to the cell (at least either of them), the parameter degradation of the

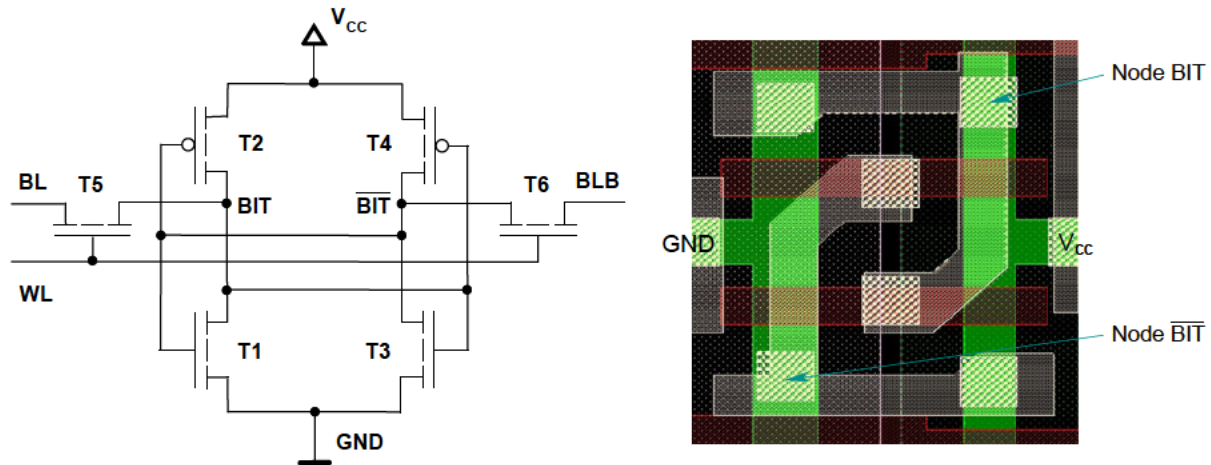


Figure 6.17: Schematic (left) and layout (right) of the investigated 6T-SRAM cell.

comprised n-MOSFETs is neglected in this study. In the high state of the flip-flop (node BIT is high), T2 is under NBTI stress, and in the other state (BIT low), T4 is stressed. The performed NBTI measurements for the 90nm p-MOSFET device are described in Section 5.

Fig. 6.18 shows the NBTI induced V_T parameter degradation of the MOSFET T2 for storing a bit value every second in the memory cell, whereby the probability is 90% for storing a “one”. The worst-case parameter degradation of T2/T4 lies always in the range between the envelope degradation curves under DC and under symmetric AC stress. Due to the high unsymmetry between the turn on and off times at a ratio of 90/10 for T2, the V_T degradation lies closer to the DC boundary than to the symmetric AC boundary. Fig. 6.19 shows the zoomed-in time diagram of the beginning phase from Fig. 6.18 (first 150 seconds), where the progression of the NBTI response of T2 and the corresponding random gate drive signal can be seen more clearly. The rectangular gate signal of the simulation was derived from a random-number generator which produces uniformly distributed random variates in the interval $[0, 1]$. In the simulation presented in Fig. 6.20, the overall stress time of T2 is further increased by storing a random bit sequence with a probability of 95% for a one. It can be observed that the NBTI response curve converges to the DC degradation envelope since the annealing of interface traps during the unfrequent “high” states of the gate signal is not sufficient to reduce the parameter degradation significantly from the degradation under DC stress. A data flipping technique for SRAM arrays is proposed in [136] to solve the problem of highly unsymmetrical NBTI induced degradation of p-MOSFET devices in SRAM cells. The periodic flipping of the contents of all SRAM cells, e.g. every 10^5 seconds, can be performed either by software or hardware.

Long-time simulations were performed at a supply voltage of 1.5V under DC and under symmetric AC stress with a 10Hz rectangular gate signal to determine the boundaries for the SRAM lifetime. Fig. 6.21 shows the lifetime extension of the cell due to the dynamic NBTI effect. The lifetime was defined here as a V_T shift of 40mV for the p-MOSFETs. The AC lifetime for a symmetric gate signal operation at 10Hz would be 1.7 times longer than the DC lifetime of the cell. The SRAM lifetime for storing a random bit sequence with a probability of 90% for storing a one bit (or 90% for a zero bit) is 1.14 times longer than the DC lifetime.

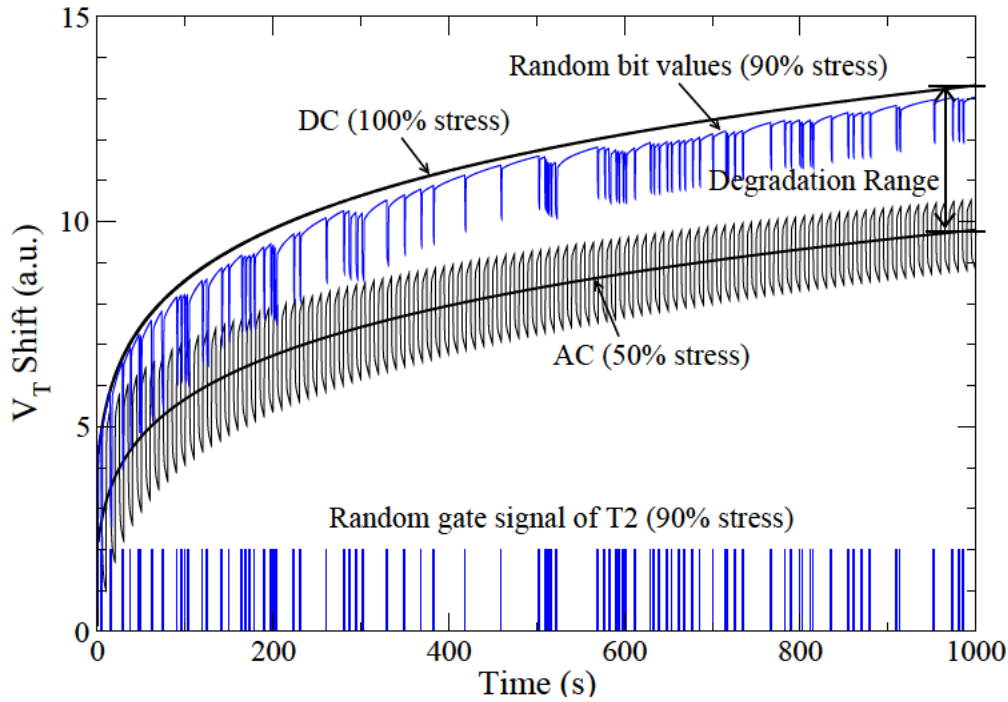


Figure 6.18: Comparison of storing random bit values every second in the cell with 90% probability for a one to DC and AC degradation of transistor T2.

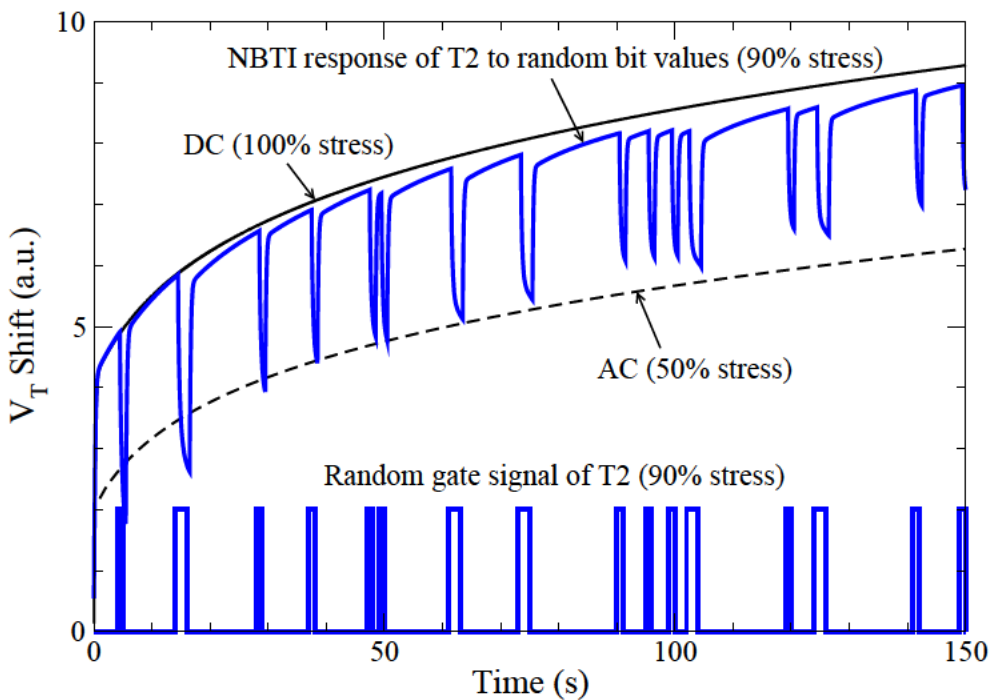


Figure 6.19: Comparison of storing random bit values every second with 90% probability for a one to DC and AC degradation of T2 for early stress times.

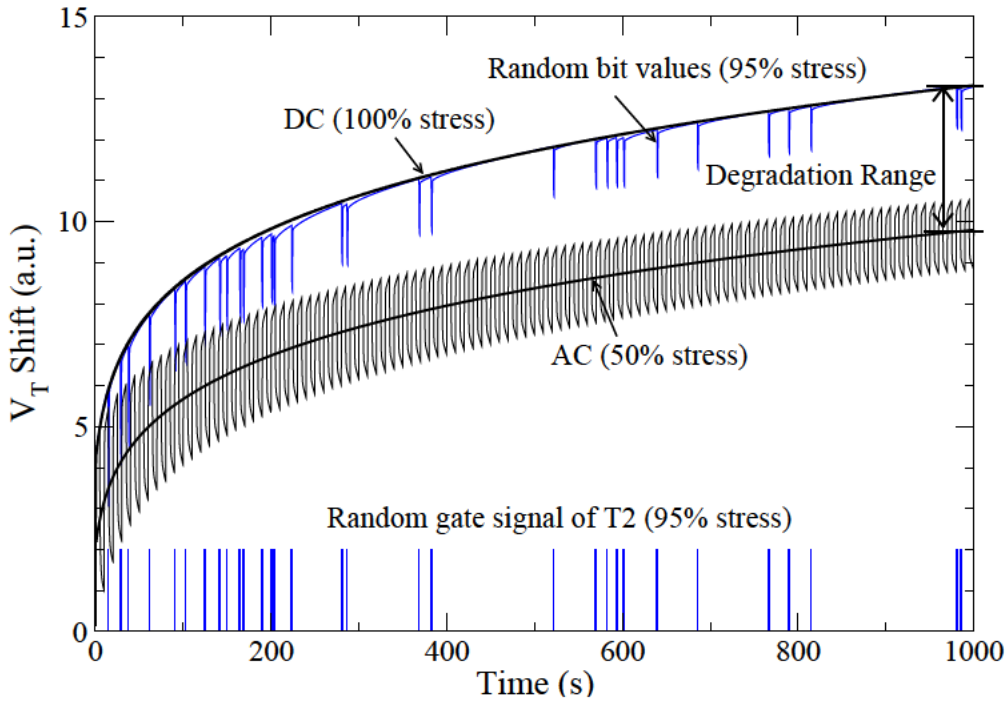


Figure 6.20: Comparison of random bit sequences with 95% probability for one to DC and AC degradation of T2.

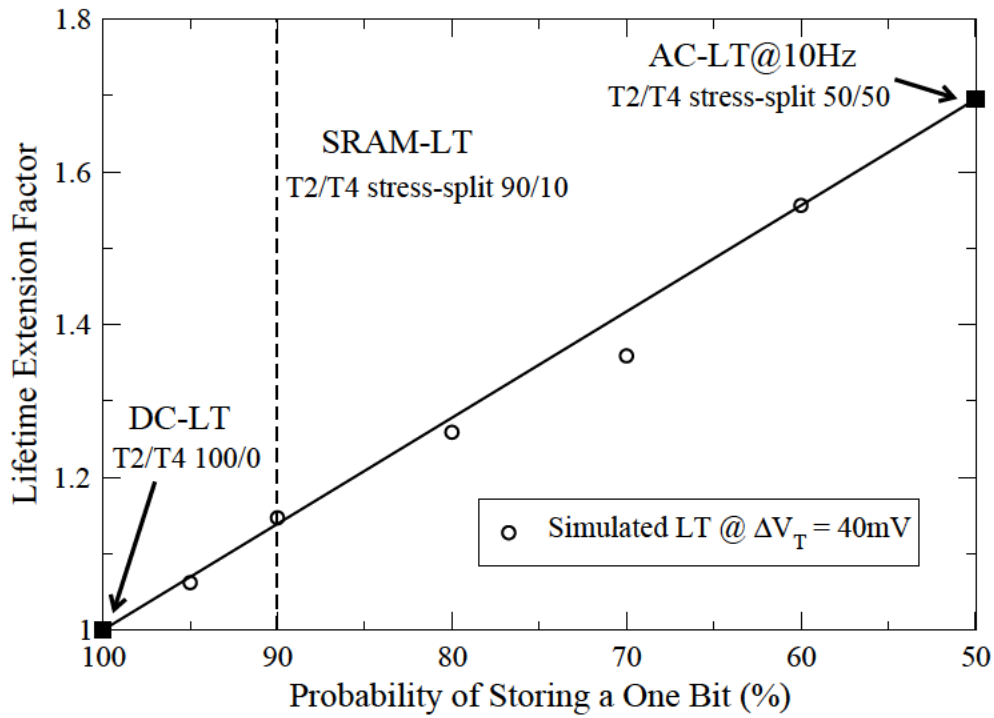


Figure 6.21: Simulated lifetime extension of the SRAM cell related to the DC lifetime of the cell for different on-time probabilities of T2.

Chapter 7

Summary and Conclusion

Channel material innovations will be required from the 65nm node onward to overcome the performance limitations of bulk silicon or process-induced uniaxial strain in order to maintain continued commensurate device scaling. Biaxially strained silicon, high germanium content SiGe alloys, and germanium are attractive materials for advanced CMOS technology due to their enhanced carrier mobilities. However, ion implantation process parameters for these target materials, necessary to produce a desired dopant distribution and junction depth, which are typically available for silicon, are not currently available. In this dissertation implantation of boron and arsenic at different energies and doses were investigated in selected high-mobility materials by using experimental results and physics-based simulations with MCIMPL-II.

Starting with an introduction to semiconductor doping theory and ion implantation technology, the general physical models necessary for the calculation of ion implantation distributions in crystalline targets were outlined. The Monte Carlo method is based on computing a large number of individual ion trajectories in the simulation domain by using scaled random numbers. The functionality of the ion implantation simulator MCIMPL-II was explained and the implemented models used for the trajectory calculation in silicon were discussed. The simulator uses locally either a crystalline or an amorphous model for searching the next collision partner of the ion. The application of the amorphous model in crystalline materials depends on a certain probability which is derived from the already produced local damage concentration. Therefore, this dynamic simulation approach considers channeling of ions as well as the transition of a semiconductor region to the amorphous state during the implantation process. However, the recent integration of MCIMPL-II with the Wafer-State-Server simulation environment was extensively tested and some improvements were made to the simulator (e.g. advanced smoothing procedure, addition of a one-dimensional grid generator). The accomplishment of a three-dimensional implantation application was demonstrated with the improved simulator for a non-planar structure in the WSS format. For the extension of the simulator from crystalline silicon to other group-IV materials, the crystalline model was modified and the empirical parameters of the electronic stopping model and of the damage model were calibrated. The accuracy of the obtained simulation results was evaluated by comparison of predicted doping profiles with SIMS measurements.

In this study a shift to shallower doping profiles was found for the implantation of boron and arsenic into SiGe layers with increasing germanium content at a given ion energy. The trend to shallower profiles is caused by the larger nuclear and electronic stopping power of the heavier

germanium atoms. It is shown that the projected range R_p of the boron distribution in $\text{Si}_{0.5}\text{Ge}_{0.5}$ lies well within the boundaries defined by the R_p values of the distributions in silicon and in germanium. While a strong shift to the wafer surface is observed for dopant implantations in SiGe alloys with low germanium concentrations (Ge content $< 50\%$), the profiles in SiGe with high germanium concentrations are all very similar. The formation of ultra-shallow junctions in a strained Si/ $\text{Si}_{0.8}\text{Ge}_{0.2}$ system was performed by introducing ions at very low energies. While the reduced atomic density in strained silicon of approximately 99% of unstrained silicon (in-plane strain of $\varepsilon_{\parallel} \approx 0.75\%$) has almost no impact on the boron profile, the arsenic profile in strained silicon shows a slightly deeper penetration compared to unstrained silicon. A special focus was put on the boron implantation in germanium due to the large hole mobility enhancement of germanium. The simulated point responses revealed that the boron distribution is significantly reduced in germanium in vertical direction, while the lateral profile is quite similar in silicon and germanium. An advantage of the Monte Carlo simulation is that the generated point defects can be estimated, which are associated with a specific implantation profile. We found that the higher displacement energy in germanium, the stronger backscattering effect, and the smaller energy transfer from the ion to the primary recoil of a collision cascade are mainly responsible for the significantly reduced damage accumulation in the germanium crystal.

Since the introduction of heavily nitrided gate oxides, NBTI has become a severe reliability problem for high-performance CMOS technologies. Therefore, the NBTI reliability was systematically investigated for a 90nm CMOS technology. Experiments for different gate voltages, frequencies, and duty cycles were performed in order to analyze the degradation of the p-MOSFET parameters. It was acceptably verified that the R-D model can explain static and dynamic NBTI data. The gate voltage and frequency dependence of NBTI was included by means of an empirical relationship. All measured data could be well reproduced by the performed numerical simulations. The presented simulation approach allows to predict the lifetime for advanced CMOS technology, which depends strongly on the applied stress operating conditions. Numerical simulations of the V_T degradation were performed with the calibrated model in order to analyze NBTI degradation and lifetime of a CMOS SRAM cell. It turned out that the SRAM lifetime is 1.14 times longer than the DC lifetime for using an unsymmetry of 90% in the stress-split between the two p-MOSFETs of the cell. Thereby, it is demonstrated that the R-D model is useful to study the NBTI response not only for driving the transistor gate with periodic signals but also for storing random bit sequences in an SRAM cell.

Finally, the extended simulator MCIMPL-II was applied to three-dimensional ion implantation problems to facilitate the introduction of high-mobility materials in future silicon-compatible advanced CMOS and optoelectronic device applications. A multi-dimensional TCAD-simulation analysis is advantageous over one-dimensional SIMS profiles, because the dopant distributions in the device structure can be studied. For instance, shadowing effects which arise for self-aligned large-tilt-angle implantations can be visualized, or the resulting dopant distribution after multiple implantation steps can be easily optimized by tuning the process parameters of a single step. However, an accurate ion implantation treatment of complex target structures requires very long simulation runtimes on a modern computer workstation. Future work will concentrate on both the speed-up of the methods used for trajectory calculation and on the parallelization of the trajectory calculation for shared-memory multiprocessor systems. It may be necessary to extend the simulator to a wider range of ion species or target materials. Since the calibration of empirical model parameters is a tremendous task, it would be useful to replace the empirical electronic stopping model by a more physically based model.

Appendix A

Wafer-State-Server Environment

The Wafer-State-Server [77] has been developed to integrate several three-dimensional process simulation tools used for etching and deposition, ion implantation, and thermal annealing processes. The Wafer-State-Server is an advanced software library for storage, access and manipulation of simulation data. It holds the complete information describing the simulation domain in a volume mesh discretized format and it provides convenient methods to access these data. On the one hand, process simulators make use of the provided access methods to initialize their internal data structures (due to performance reasons), and on the other hand, the simulators report their modifications of the wafer structure to the Wafer-State-Server. Thereby a consistent status of the wafer structure can be sustained during the whole simulated semiconductor manufacturing process flow.

A.1 Architecture of the Wafer-State-Server

The goal of the Wafer-State-Server is to store all properties of the simulation domain and to provide convenient methods to access and to modify these properties. Three major problems have to be solved by the Wafer-State-Server, namely I/O operations, meshing, and the handling

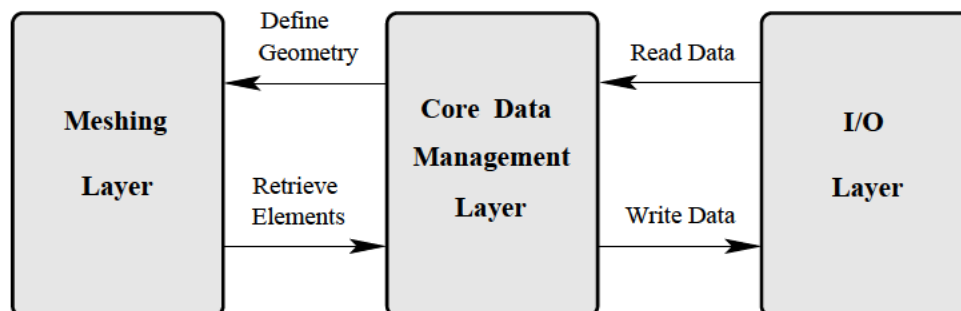


Figure A.1: Conceptual view of the Wafer-State-Server.

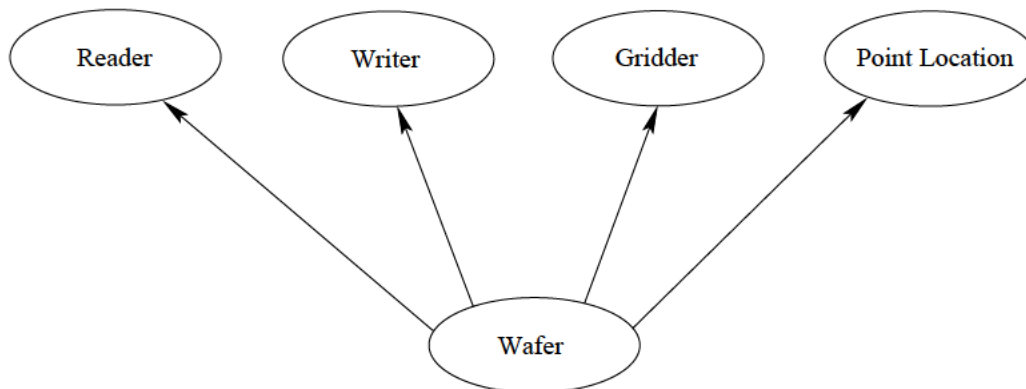


Figure A.2: Public interfaces of the Wafer-State-Server.

of the topology of the simulation domain and of the distributed quantities contained in the simulation domain. Corresponding to these three TCAD problems, the Wafer-State-Server provides three logical layers. Fig. A.1 shows the layers *I/O*, *Core Data Management*, and *Meshing* as well as their interactions. The *I/O* layer contains various data adapters to support the WSS format and other file formats. The *Core Data Management* layer takes care of data storage, point location, and topological operations like extracting the hull of a geometry or finding the interface between two geometries. Finally, the *meshing* layer handles all sort of gridding tasks, for instance, the interpolation of attributes from one grid onto another one. The layers are designed in an object-oriented way. Each layer consists of an interface and an implementation part. Within the Wafer-State-Server the functionality of a layer is exclusively accessed via the layer interface. This ensures that the desired implementation or algorithm of the problem can be controlled by the simulator without the need of changing the program code within the Wafer-State-Server library. The simulator instantiates an object of the desired class that implements the interface. Due to the support of dynamic instantiation of implementations, the desired algorithm can be selected at runtime. Fig. A.2 gives an overview of the defined interfaces which are visible from the application. Except for the point-location, all implementations inherit from their parent class. The implemented point-location code uses the C++ template mechanism to support several implementations. The syntactically more complicated template polymorphism was chosen to ensure the best possible performance for algorithms defined on the core data-structures. In addition to pure point-location functionality, the point-location interface provides topological analysis methods too, while the wafer interface itself provides global repair and update mechanisms for the simulators.

A.2 WSS File Format

The WSS format is an ASCII-based file-format which allows for an easy “by hand” generation of simple geometries. Since the *Reader* and *Writer* interfaces are implemented, the WSS file format is the native file format for the simulation of ion implantation with MCIMPL-II. The WSS format is a hierarchical data structure where the top-level object is the *Wafer*. The *Wafer* contains several sub-objects called *Segments*. A segment describes a single connected region

```

VERSION "1.4"
NAME Example_Boron_Implant
DIMENSION 1 # One-dimensional wafer structure
POINTS # Global point list
{
    0.0000 # 0
    3.7990 # 1
    3.8000 # 2
}
SEGMENTS
{
    Si # Segment 1 is named "Si"
    {
        GRID gr_Si # Index value list of Si
        {
            0 1
        }
        ATTRIBUTES
        {
            MaterialType # Property 1 of Si
            {
                "Si"
            }
            Density # Property 2 of Si
            {
                2328.0
            }
            CrystalOrientation # Property 3 of Si
            {
                "100"
            }
        }
    }
    SiO2 # Segment 2 is named "SiO2"
    {
        GRID gr_SiO2 # Index value list of SiO2
        {
            1 2
        }
        ATTRIBUTES
        {
            MaterialType # Property 1 of SiO2
            {
                "SiO2"
            }
            Density # Property 2 of SiO2
            {
                2270.0
            }
        }
    }
}
    
```

Figure A.3: Example of a WSS file for a structure with two material segments.

within the wafer (simulation domain) with similar physical properties, for instance, a region consisting of one material. This does not mean that one material has necessarily to be modeled by only one segment. No matter how complex a simulation domain is, it can always be composed of single connected regions. Fig. A.3 shows a one-dimensional input WSS file for the simulation of ion implantation with MCIMPL-II. The described target is a (100) silicon wafer which has a native oxide layer of 1nm in thickness on its surface.

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Curriculum Vitae

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High school graduation (*Matura*) at the Gymnasium Hagenmüllergasse.

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Enrolled in Electrical Engineering focused on Computer Engineering at the Vienna University of Technology, Austria.

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Graduation from College for Communications Engineering and Electronics (*HTL Matura*) at the Technologisches Gewerbemuseum (TGM) with distinction.

January 1989 – January 1997

Held a position as hardware and software development engineer in the division for PABX Systems at the Kapsch Group AG, Wien.

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Received degree of *Diplom-Ingenieur (M.Sc.)* in Computer Engineering from the Vienna University of Technology with distinction.

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Entered the position of teaching assistant at the Institute for Microelectronics, Vienna University of Technology. Enrolled in doctoral program at the same institution under the supervision of Prof. Siegfried Selberherr.

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Held a position as a visiting researcher at the design center of Cypress Semiconductor Corp. in San Jose, USA.