Investigation of Low-Frequency Noise Behavior After Hot-Carrier Stress in an n-Channel Junctionless Nanowire MOSFET

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***Abstract*—The dc performance and low-frequency (LF) noise behaviors after hot-carrier (HC)-induced stress were compared for a junctionless nanowire transistor (JNT) and an inversion-mode nanowire transistor (INT). Less dc degradation was found in the JNT than in the INT. Due to the low lateral peak electric field (E-field) and electrons traveling through the center of the nanowire, the LF noise increment after HC-induced stress in the JNT is much lower than that in the INT. Furthermore, due to the higher lateral peak E-field located under the gate and the conduction path that occurs near the surface, the LF noise of the INT is very sensitive to HC stress.**

***Index Terms*—Hot-carrier (HC)-induced degradation, junctionless nanowire transistor (JNT), low-frequency (LF) noise, multigate.**

I. Introduction

IT IS widely known that the electrical characteristics of conventionally structured MOSFETs are degraded by strong short-channel effects in highly scaled-down devices. Due to the excellent gate controllability to the channel and the enhanced carrier-transport properties, 3-D structures are considered to be promising candidates beyond the 22-nm node [1]. Recently, a junctionless nanowire transistor (JNT) that removes the junction between the source/drain and the channel has been introduced [2]. The doping structure of the source, channel, and drain in conventional inversion-mode MOSFETs is either n-p-n or p-n-p, which makes the formation of the abrupt junction very difficult when the channel length is highly scaled down.

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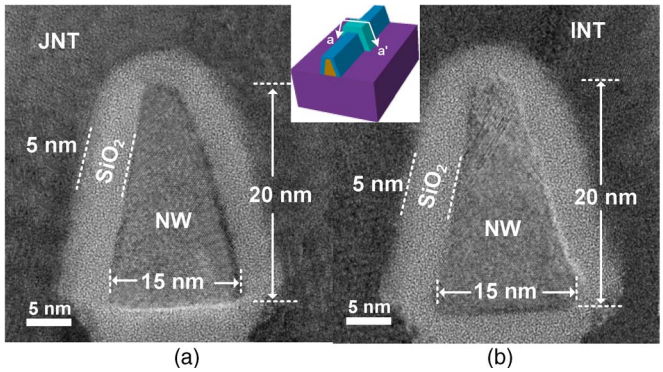

Fig. 1. Cross-sectional TEM image along the a−a′ direction (see the inset) for the (a) JNT and (b) INT [8]. The inset shows a schematic of the fabricated devices.

However, the source, channel, and drain of JNTs are doped with same dopant concentration, which facilitates fabrication of a short-channel device without junction formation. The electrical characteristics of JNTs have been studied in depth [3] [4] [5]. However, to date, there have been no reports of the low-frequency (LF) noise behavior after electrical stress. The LF noise is important to achieving a trustworthy and nondestructive characterization, as it provides a defect profile in the dielectric that can be used to evaluate reliability, such as the lifetime of a device [6], [7].

As described in this letter, hot-carrier (HC)-induced device degradation, including dc characteristics and LF noise behaviors, have been experimentally compared for the JNT and the inversion-mode nanowire transistor (INT). We clearly observed that the noise increment after HC stress in the JNT is 60× lower than that in the INT.

II. Experiment

To fairly compare the electrical characteristics of the JNT and the INT, both devices were fabricated on a silicon-on-insulator wafer (UNIBOND) using the same processing steps, except an undoped channel region and spacer formation was used to prevent dopant diffusion into the channel for the INT. To define a precise nanowire pattern, we used electron-beam lithography and an inductively coupled plasma dry etch. The gate oxide was grown by rapid thermal oxidation. To make the threshold voltage V_{TH} of the devices similar, P^+ polysilicon and TiN were used as gate materials for the JNT and the INT, respectively. Fig. 1 shows the cross-sectional TEM images for both devices.

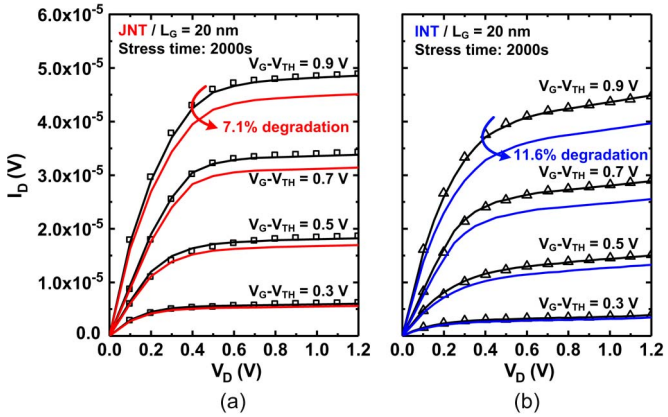

Fig. 2. Measured output characteristics (I_D-V_D) of the (a) JNT and (b) INT before and after HC stress. Both devices were stressed at $V_G - V_{\rm TH} = V_D = 1.9$ V for 2000 s (line: measured; symbol: simulated).

They both have a similar nanowire shape and oxide thickness, which enables a fair comparison of the electrical characteristics. The gate lengths L_G of the JNT and the INT were patterned in the range of 20–250 nm. The channel, source, and drain in the JNT were uniformly implanted with a concentration of $1-2 \times 10^{19}$ cm^{-3}. Arsenic dopant was used to make the n-channel devices. The detailed process is described in previous work [8]. The HC stress was automatically performed using a Keithley 4200 semiconductor characterization system. The stress bias condition was $V_G - V_{\rm TH} = V_D$, at which point the threshold voltage was much more degraded than at the $V_G = V_D/2$ condition conventionally chosen in planar devices [9]. The drain-current noise spectral density $S_{\rm id}$ in the frequency range of 10 Hz–10 kHz was measured using a BTA9812 noise analyzer in conjunction with Cadence NoisePro software. $S_{\rm id}$ was measured in the linear operation region at $V_D = 50$ mV. We used the Atlas 3-D device simulator to determine the HC-induced degradation in both devices [10].

III. Results and Discussion

Fig. 2 shows the dc output characteristics (I_D-V_D) and degradation after HC stress of both devices with an L_G of 20 nm. The HC stress condition was $V_G - V_{\rm TH} = V_D = 1.9$ V for 2000 s. The $V_{\rm TH}$ of both devices was nearly the same, which is approximately 0.15 V. The constant current threshold method was used to extract $V_{\rm TH}$. By making the $V_{\rm TH}$ values of both devices equal, the V_G of the devices during the HC stress condition also became equal, and thus, the vertical E-field had similar intensities applied at the channel regions. After HC stress for 2000 s, the I_D degradation was measured as 7.1% and 11.6% from the JNT and the INT, respectively. Fig. 3 shows the supply voltage V_D with a ten-year guarantee for both devices. The criterion for the HC lifetime is 10% $I_{\rm ON}$ degradation, and the plotted data are the mean values from five samples. The ten-year lifetimes of the JNT and the INT were expected to be about 1.43 and 1.32 V, respectively. Although the JNT exhibited superior HC reliability, both the JNT and the INT were able to satisfy the requirement of the International Technology Roadmap for Semiconductors. Fig. 4 shows the normalized drain-current noise spectral density

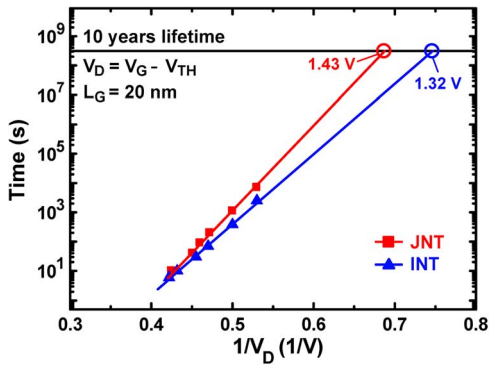

Fig. 3. HC lifetime and V_D for a ten-year guarantee of the JNT and the INT with the 20-nm L_G. The criterion for the HC lifetime is 10% $I_{\rm ON}$ degradation.

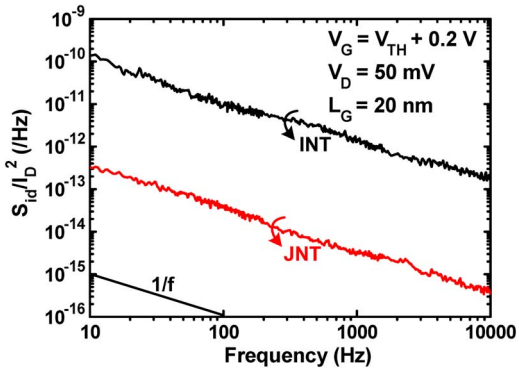

Fig. 4. Normalized $S_{\rm id}$ $(S_{\rm id}/I_D^2)$ measurements of the JNT and the INT before HC stress at $V_G = V_{\rm TH} + 0.2$ V and $V_D = 50$ mV.

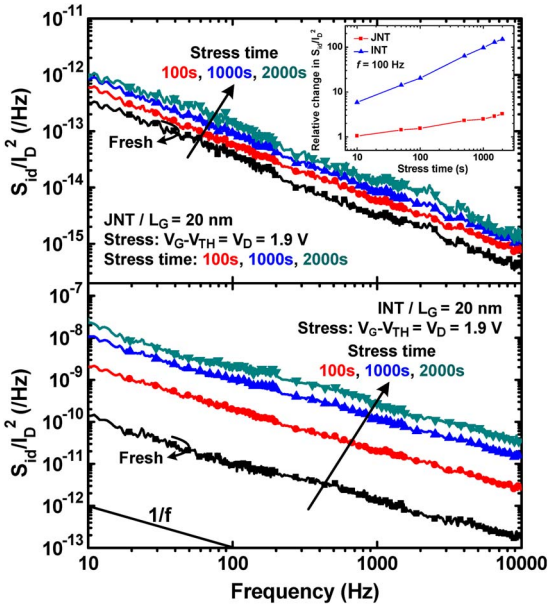

Fig. 5. Normalized $S_{\rm id}$ $(S_{\rm id}/I_D^2)$ measurements of the JNT and the INT during HC stress at $V_G = V_{\rm TH} + 0.2$ V and $V_D = 50$ mV. The inset shows the relative change of $S_{\rm id}/I_D^2$ versus the stress time. It can be observed that the INT has a greater increase in noise after HC stress compared with the JNT.

$(S_{\rm id}/I_D^2)$ measurement for both devices at $V_G - V_{\rm TH} = 0.2$ V and $V_D = 50$ mV. The JNT noise spectrum was about two orders lower than that of the INT prior to the HC stress. The noise spectra during HC stress are shown in Fig. 5. The noise of the JNT increased by a factor of 3, whereas the noise for the

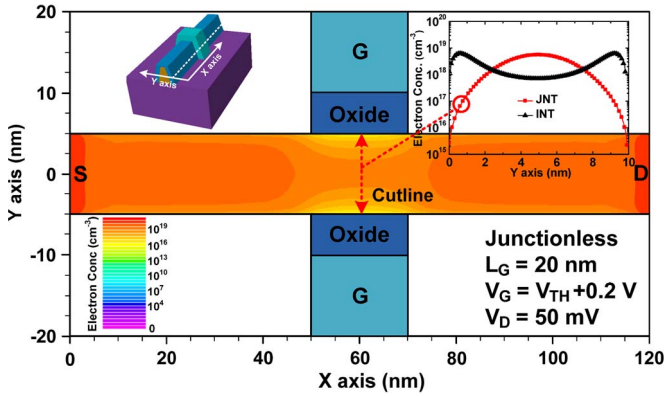

Fig. 6. (Center) Graphical display of the simulated electron concentration of the JNT. (Left top) Schematic of the JNT for device simulation. (Right top) Electron concentration of the JNT and the INT plotted along the cutline.

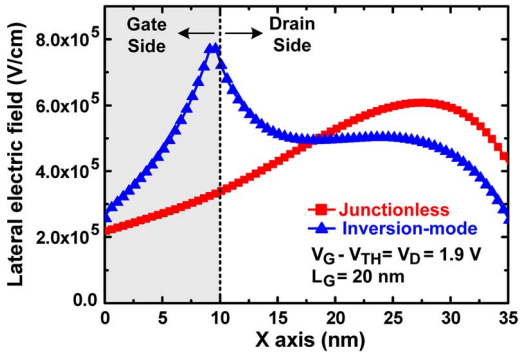

Fig. 7. Lateral electric fields of the JNT and the INT plotted along the x-axis.

INT increased by a factor of approximately 170. Consequently, the JNT showed noise about four orders lower than the noise from the INT. Here, we explain why the JNT was strongly immune to device degradation caused by HC stress. Fig. 6 shows the carrier concentrations in the JNT and the INT at the same conditions as when the noise spectra were measured. The INT figure shows that most of the electrons traveled near the surface of the nanowire at the inversion regime; however, the electron conduction of the JNT mainly occurred at the center of the nanowire channel. This caused the electrons of the JNT to be relatively free from the effects of surface roughness scattering, and there was less probability that the electrons would interact with the interface and oxide traps [11]. The lateral electrical fields (E-fields) in both devices at the HC stress conditions are shown in Fig. 7. A higher lateral E-field was observed in the INT than in the JNT, which rapidly accelerated the electrons. In addition, the peak E-field in the JNT was located in the drain side, whereas that of the INT appeared under the gate. Because of the peak value and the location of the E-field, more HCs would be likely to be trapped under the gate in the INT than in the JNT [12], which can lead to higher degradation of the LF noise in the INT.

IV. Conclusion

The effects of HC-induced stress on the dc performance degradation and the LF noise in the n-channel JNT and the INT with a 20-nm gate length have been investigated. After HC stresses, the JNT showed less $I_{\rm ON}$ deterioration, a higher ten-year lifetime voltage, and less LF noise degradation. The lower noise degradation was due to electron transport through the center of the nanowire, as well as the lower peak value of the E-field and its location near the drain side. The low-noise characteristic of the JNT leads to reduced signal-to-noise ratios, and therefore, it is considered to be a promising candidate for sensors with ultrahigh sensitivity.

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