Junctionless Transistors: Physics and Properties

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J. P. Colinge, C. W. Lee, N. Dehdashti Akhavan, R. Yan, I. Ferain, P. Razavi, A. Kranti and R. Yu

Abstract Junctionless transistors are variable resistors controlled by a gate electrode. The silicon channel is a heavily doped nanowire that can be fully depleted to turn the device off. The electrical characteristics are identical to those of normal MOSFETs, but the physics is quite different. This paper compares the conduction mechanisms in three types of MOS devices: inversion-mode, accumulation-mode and junctionless MOSFET.

1 Introduction

All existing transistors are based on the use of semiconductor junctions. Because of the laws of diffusion and the statistical nature of the distribution of the doping atoms in the semiconductor, the formation of ultrashallow junctions with high doping concentration gradients has become an increasingly difficult challenge for the semiconductor industry. Junctionless transistors (also called gated resistor) have no junctions and no doping concentration gradients. These devices have full CMOS functionality and are made using silicon nanowires.

The key to fabricating a junctionless gated resistor is the formation of a semiconductor layer that is thin and narrow enough to allow for full depletion of carriers when the device is turned off. The semiconductor also needs to be heavily doped to allow for a decent amount of current flow when the device is turned on.

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Putting these two constraints together imposes the use of nanoscale dimensions and high doping concentrations [1, 2].

2 Conduction Mechanisms

MOSFETs (including accumulation-mode FETs) are normally off devices, as the drain junction is reverse biased and blocks any current flow if no channel is created between source and drain. To turn the device on, the gate voltage is increased in order to create an inversion channel. The junctionless transistor, on the other hand, is basically a normally on device where the workfunction difference between the gate electrode and the silicon nanowire shifts the flatband voltage and the threshold voltage to positive values. When the device is turned on and in flatband conditions, it basically behaves as a resistor and the electric field perpendicular to current flow is basically equal to zero in the "bulk" channel.

Figure 1 shows the drain current as a function of gate voltage in the three types of SOI MOSFETs: inversion-mode "N^+PN^+", accumulation-mode "N^+NN^+" and heavily doped junctionless "$N^+N^+N^+$" transistor.

- Below threshold the inversion-mode device is depleted (either fully or partially) and the flat-and voltage is situated below the threshold voltage, at a gate voltage at which the device is off (Fig. 1a). Below flatband the body is p-type neutral. Above threshold, the body of the channel is depleted and a surface inversion layer is formed.
- Below threshold accumulation-mode devices are fully depleted. Threshold is reached when the gate voltage is increased in such a way that a portion of the channel region is no longer depleted. At that point, the channel region is technically partially depleted. As gate voltage is further increased, flat-band is

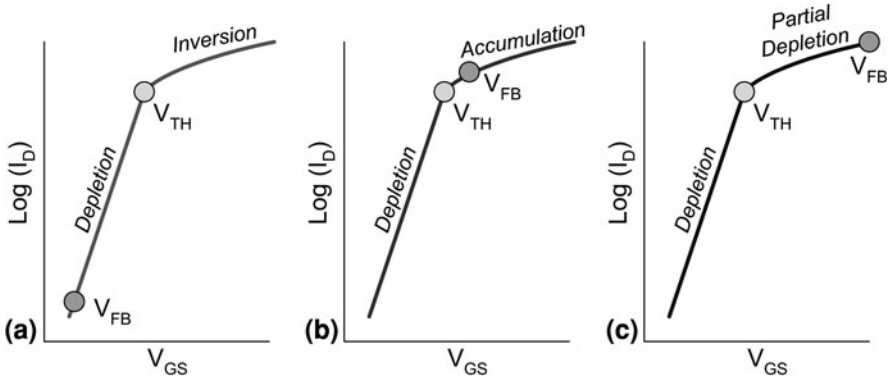

Fig. 1 Drain current (log scale) as a function of gate voltage in **a** an inversion-mode MOSFET; **b** an accumulation-mode MOSFET and **c** a heavily-doped junctionless transistor

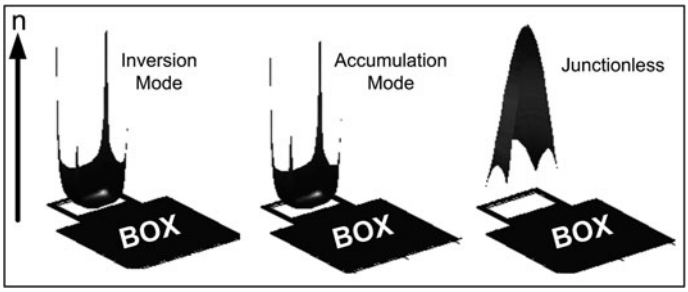

Fig. 2 Electron concentration profile above threshold

reached: the channel region is now neutral (i.e. no longer depleted, even partially). Further increasing the gate voltage creates a surface accumulation channel (Fig. 1b).

- The heavily doped junctionless transistor is fully depleted below threshold. As gate voltage is increased, the electron concentration in the channel increases, and threshold is reached when the peak electron concentration in the channel reaches the doping concentration N_D. Further increasing the gate voltage increases the "diameter" of the region where $n = N_D$, until the entire cross-section of the device becomes neutral (i.e. no longer depleted, even partially), at which point flatband is reached (Fig. 1c). It is possible to further increase the gate voltage to create accumulation channels, but this is probably not desirable, as the high doping concentration in the channel already insures a large current drive.

Figure 2 compares the electron profile above threshold in an inversion-mode pi-gate MOSFET, an accumulation-mode pi-gate transistor and a junctionless pi-gate device in the on state (above threshold). In the inversion-mode the electrons are confined in inversion layers at the top of the device and along its sidewalls, with marked peaks at the corners. The cross-section of the silicon channel is 10 nm × 10 nm. If confinement effects are neglected, there is no significant volume inversion. The profile carrier concentration in the accumulation-mode device is remarkably similar to that in the inversion-mode device, and the majority of the electrons are confined in inversion layers at the top of the device and along its sidewalls, again with marked peaks at the corners. The electron concentration in the center of the device is equal to the doping concentration ($N_D = 10^{17}$ cm^{-3}), such that a small body current is added to the current in the accumulation layers.

Below threshold, the junctionless channel is depleted of electrons, and the current varies exponentially with gate voltage (Fig. 3a). At threshold, a neutral silicon filament forms between source and drain (Fig. 3b). The cross-section of filament increases when gate voltage is increased (Fig. 3c) until depletion disappears and the device is in flatband condition (Fig. 3d).

When the device is turned off (Fig. 3a), the effective channel length, hereby defined as the distance between the non-depleted source and drain regions varies

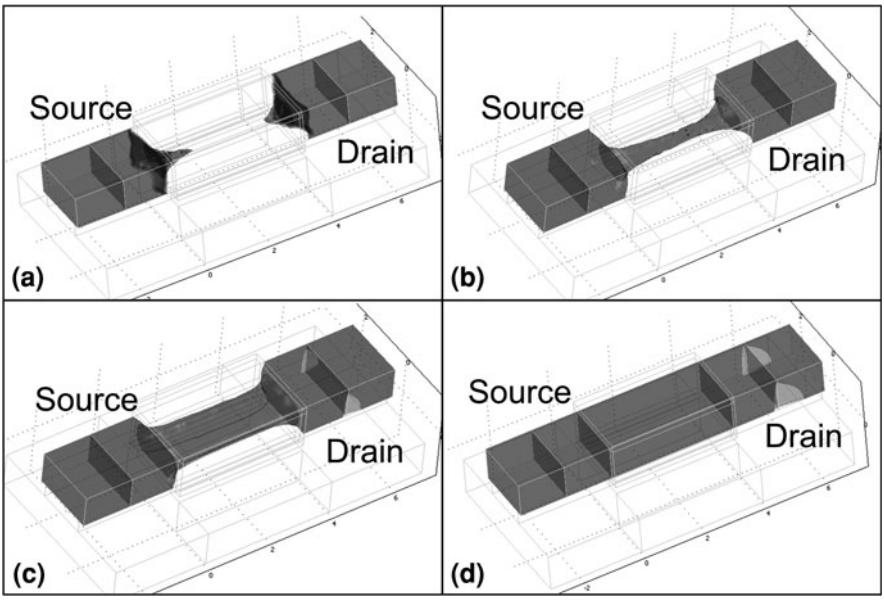

Fig. 3 Electron concentration contour plots in an *n*-type junctionless transistor for $V_{DS} = 50$ mV. **a** $V_G < V_{TH}$; **b** $V_G = V_{TH}$; **c** $V_G > V_{TH}$; **d** $V_G = V_{FB} \gg V_{TH}$

from a distance less than the physical gate length in the center of the nanowire to a distance larger than the physical gate length near the periphery of the nanowire. When the gate voltage is negative enough, the distance between the non-depleted source and drain regions can be larger than the physical gate length across the entire section of the device. This has a significant impact on short-channel properties. In a "regular", inversion-mode trigate device, assuming the distance between the source and drain junctions is exactly equal to the physical gate length (Fig. 4a), the presence of PN^+ junctions creates a reduction of the effective gate length, resulting in a short-channel effect (SCE). This effect has been quantified by Skotnicki et al. [3] using the voltage-doping transformation model (VDT). The VDT can be used to translate the effects of shrinking device parameters such as gate length or drain voltage into electrical parameters. In the particular case of the SCE and the drain-induced barrier lowering (DIBL), the following expressions can be derived from the VDT model [4].

$$\mathrm{SCE} = 0.64\frac{\varepsilon_{Si}}{\varepsilon_{ox}}\left[1+\frac{x_j^2}{L_{el}^2}\right]\frac{t_{ox}}{L_{el}}\frac{t_{dep}}{L_{el}}V_{bi} \equiv 0.64\frac{\varepsilon_{Si}}{\varepsilon_{ox}}EI\ V_{bi} \tag{1}$$

and

$$\mathrm{DIBL} = 0.80\frac{\varepsilon_{Si}}{\varepsilon_{ox}}\left[1+\frac{x_j^2}{L_{el}^2}\right]\frac{t_{ox}}{L_{el}}\frac{t_{dep}}{L_{el}}V_{DS} \equiv 0.80\frac{\varepsilon_{Si}}{\varepsilon_{ox}}EI\ V_{DS} \tag{2}$$

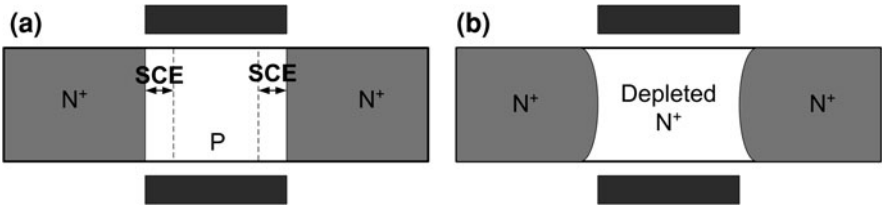

Fig. 4 Illustration of effective channel length in an inversion-mode device (**a**) and a junctionless transistor (**b**)

where L_{el} is the electrical (effective) channel length, V_{bi} is the source or drain built-in potential, tox is the gate oxide thickness, x_j is the source and drain junction depth and tdep is the penetration depth of the gate field in the channel region, which is equal to the depth of the depletion region underneath the gate in a bulk MOSFET. The parameter EI is called the "Electrostatic Integrity" factor. It depends on the device geometry and is a measure of the way the electric field lined from the drain influence the channel region, thereby causing SCE and DIBL effects. Based on the above expressions, the threshold voltage of a MOSFET with a given channel length Lel can be calculated using the following relationship:

$$V_{TH} = V_{TH\infty} - \text{SCE} - \text{DIBL} \tag{3}$$

where $V_{TH\infty}$ is the threshold voltage of a long-channel device. The decrease of threshold voltage with decreased gate length is a well-known short-channel effect called the "threshold voltage roll-off". The SCE is illustrated in Fig. 4a for an inversion-mode transistor. In a junctionless device in the off state, the electrostatic squeezing effect causes the distance between the non-depleted source and drain regions to be larger than the physical gate length (Fig. 4b). This is a beneficial factor that reduces short-channel effects [2] and can possibly reduce source-to-drain direct tunneling in very short-channel devices.

Unlike accumulation-mode and inversion-mode devices the channel of junctionless transistors is in the bulk of the nanowire (i.e. it is not a surface channel). As a result, carriers in the channel are exposed to a low electric field in the directions to current flow. This strongly reduces the degradation of mobility when gate voltage is increased in the on state [5]. Figure 5 shows the position of the channel in both subthreshold operation and above threshold. In an inversion-mode device, subthreshold conduction mainly takes place in the top corners of the device (Fig. 5a). Above threshold, surface channels are formed on three sides of the nanowire, with carrier concentration peaks in the corners Fig. 5d). In an accumulation-mode transistor, the subthreshold current flows through the bulk of the device, near the center or the back of the nanowire (Fig. 5b). When the device is turned on, a small current flows through the body of the nanowire, but this current typically amounts for les than ten percents of the overall current drive. Most of the current flows in surface and corner accumulation channels, like in an inversion-mode device (Fig. 5e). In the junctionless device the subthreshold current flows in

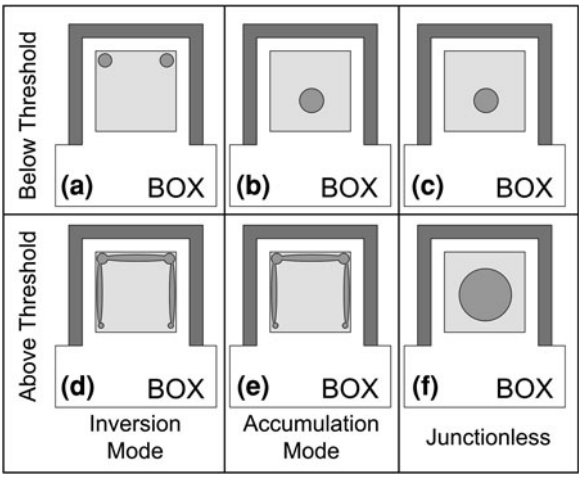

Fig. 5 Location of conduction path in the different devices. Subthreshold conduction path in **a** inversion-mode, **b** accumulation-mode and **c** junctionless devices. Conduction channels above threshold in **d** inversion-mode, **e** accumulation-mode and **f** junctionless devices

the center of the nanowire, as in the accumulation-mode device (Fig. 5c). When threshold is reached, the channel leaves full depletion and a neutral ("undepleted") channel forms between source and drain, in the center of the device (Fig. 5f). Thus, the junctionless transistor is partially depleted when it is turned on.

Above threshold, channel saturation and pinchoff occurs like in a regular MOSFET or in a JFET (Fig. 5). As a result of pinchoff, the output characteristics of junctionless transistors are virtually identical to those of conventional MOSFETs [1].

No analytical mode has been developed for the junctionless device as yet, but, in first approximation it is probably safe to use the model developed for calculating the body current of accumulation-mode transistors [6], which yields:

$$I_{Dsat} \approx \frac{1}{2}\frac{q\mu N_D W_{si} T_{si}}{L} V_{Dsat}^2 \tag{4}$$

with

$$V_{Dsat} = V_G - V_{FB} - \left(\frac{qN_D T_{si}}{2\varepsilon_{si}} + \frac{qN_D T_{si}}{C_{ox}}\right) \tag{5}$$

This is to be compared with the general expression for the current in an inversion-mode trigate device:

$$I_{Dsat} \approx \frac{1}{2}\frac{\mu C_{ox} W_{eff}}{L} V_{Dsat}^2 \text{ with } W_{eff} = 2T_{si} + W_{si} \tag{6}$$

The current drive of the inversion-mode device is directly proportional to the gate oxide capacitance, but so is the capacitance of the gate electrode. As a result, the intrinsic delay time of the device (*CV/I*) is independent on the gate oxide thickness. It can only be improved by enhancing the mobility and decreasing gate length. In the junctionless device the current is not directly related to the gate

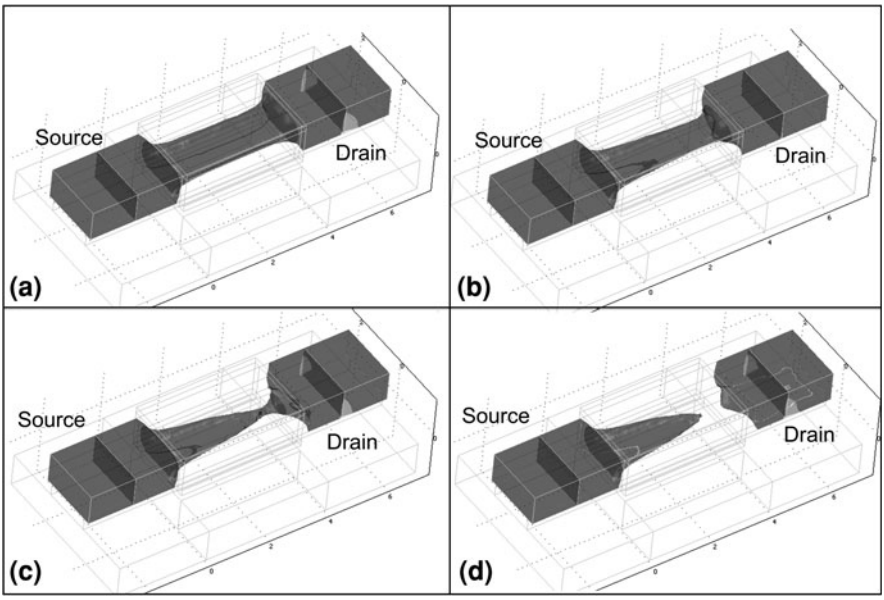

Fig. 6 Electron concentration contour plots in an *n*-type junctionless transistor. **a** $V_D = 50$ mV; **b** $V_D = 200$ mV; **c** $V_D = 400$ mV; **d** $V_D = 600$ mV

oxide thickness. It is, instead, proportional to the doping concentration in the nanowire—and the doping concentrations that are used are at the same level as in the source and drain extensions. This can give the junctionless device a speed advantage over regular devices [1] (Fig. 6).

3 Threshold Voltage

The threshold voltage of junctionless devices depends on silicon film thickness, width of the nanowire, doping concentration and gate oxide thickness (Fig. 7). One can easily obtain different threshold voltages by varying the width of the nanowires, if doping concentration is kept constant, which may be useful for producing devices with multiple values of V_{TH} on a chip. Figure 7 shows the variation of threshold voltage in a long-channel junctionless device as a function of silicon width (W_{si}) and thickness (T_{si}). The EOT is 0.5 nm and the doping concentration is 2×10^{19} cm^{-3}. Threshold voltage can be varied from 1 to −0.2 V by varying W_{si} from 5 to 20 nm and T_{si} from 5 to 15 nm.

It is also important to evaluate the sensitivity of V_{TH} variations with fabrication parameters. Figure 8 shows the results of such an analysis. If one of the dimensions (T_{si} or W_{si}) is small enough, the variations of the other dimension do not impact too much the threshold voltage. For example, if the silicon thickness is

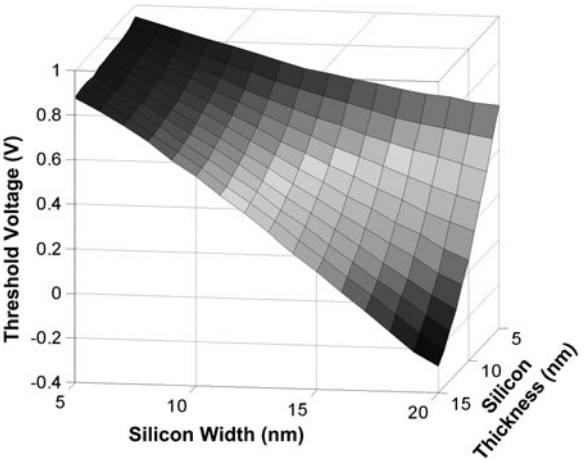

Fig. 7 Long-channel V_{TH} defined as peak in dg_m/dV_G for $T_{ox} = 0.5$ nm and $N_D = 2 \times 10^{19}$ cm^{-3}

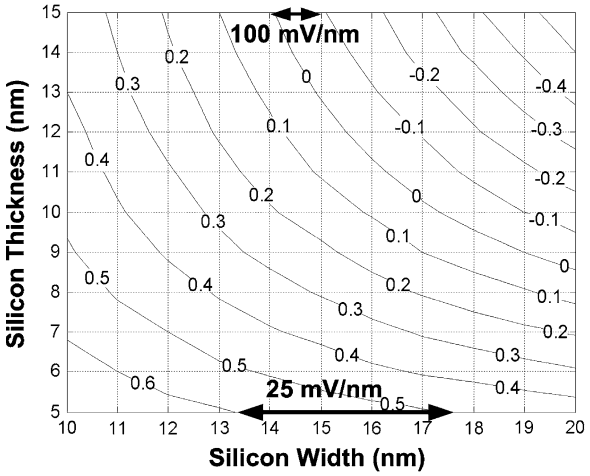

Fig. 8 Contour plot of threshold voltage in an *n*-channel junctionless device with $T_{ox} = 1$ nm and $N_D = 2 \times 10^{19}$ cm^{-3}, as a function of nanowire thickness and width

5 nm, the variation $\Delta V_{TH}/\Delta W_{si}$ is equal to 25 mV/nm. At the same time, the variation of threshold voltage $\Delta V_{TH}/\Delta T_{si}$ is equal to 100 mV/nm. Since thin-film SOI wafers with a $\sigma T_{Si} < 0.2$ nm can nowadays be produced [7], threshold voltage variations on the order of $\sigma V_{TH} < 35$ mV can be expected at wafer level, provided a lithography width control of 0.5 nm. The use of a thinner EOT decreases the sensitivity of V_{TH} on dimensions.

Doping fluctuations are a serious problem in nanoscale devices. Even in the so-called "undoped" channels the doping concentration is not equal to zero but to a value of a few 10^{15} cm^{-3}. This means that there a chance of approximately one in a thousand to find a (boron) doping atom in a device with a channel volume of $10 \times 10 \times 10$ nm^3. In the corresponding junctionless device with a doping concentration N_D of 5×10^{19} cm^{-3}, there will be an average 50 doping atoms per

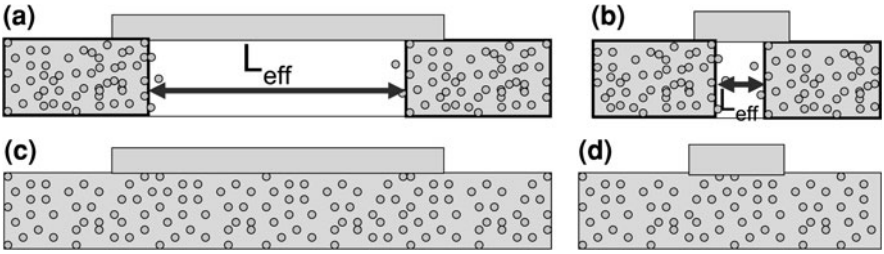

Fig. 9 Scattering of source and drain doping impurities in the channel of **a** a long-channel and **b** a short-channel inversion-mode MOSFETs; **c** long-channel and **d** short-channel junctionless devices

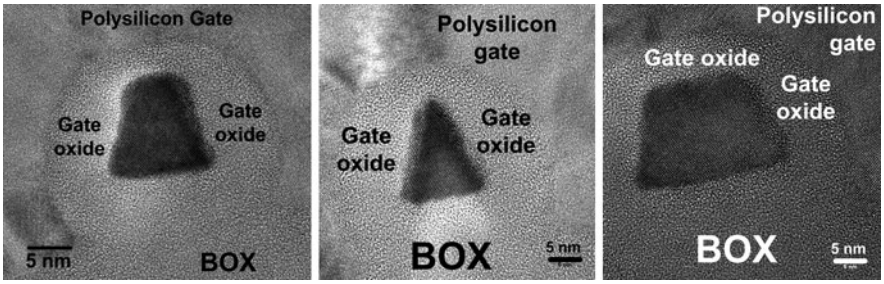

Fig. 10 TEM cross section of a junctionless transistors with increasing width from left to right

channel, which makes the device much more robust against doping fluctuation problems.

Another problem associated with the statistical distribution of doping impurities is the variation of effective channel length, L_{eff}, defined as the distance between the source junction and the drain junction [8]. This is illustrated in Fig. 9, the statistical nature of the doping atom distribution at the source and drain junctions causes the effective channel length to fluctuate from device to device. These fluctuations are inherent to the ion implant and diffusion processes. Furthermore, dopants from the source and drain can scatter in the channel region and influence the threshold voltage. In the junctionless device, there is no gradient of doping concentration between source, channel and drain. The effective channel length can no longer be defined as the distance between two junctions. The effective gate length is basically equal to the physical gate length, although it may be somewhat longer when the device is turned off (Fig. 4b).

4 Experimental Results

Junctionless gated resistor devices were made using standard SOI wafers. The SOI layer was thinned down to 15 nm and patterned into nanoribbons using e-beam

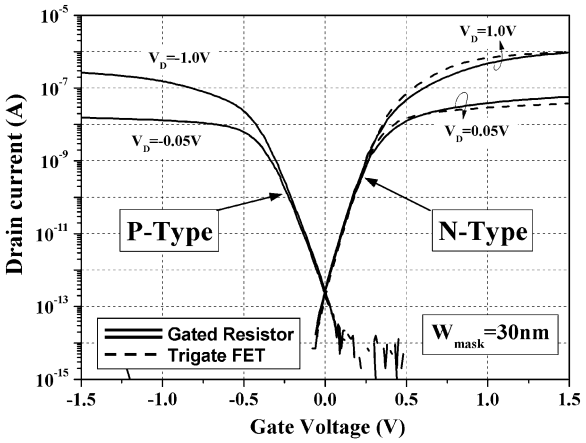

Fig. 11 Drain current versus gate voltage for N- and P-type junctionless gated resistors and a trigate inversion-mode, N-channel MOSFET. $N_D = 1 \times 10^{19}$ cm^{-3} in the junctionless device. $L = 1$ μm

lithography. Using a combination of plasma lateral overetch and gate oxidation, the thickness of the nanowires was reduced to nm, and their width was reduced to dimensions as small as 5 nm. Ion implantation was used to dope the devices uniformly N^+ or P^+ with a concentration of 1×10^{19}–5×10^{19} cm^{-3}, which is a typical LDD doping concentration, to realize N-channel and P-channel devices, respectively.

Figure 10 shows the TEM cross-section of a several devices with different widths. Due to processing parameters the cross-section of the devices is not a rectangle, but rather a trapezium or even a triangle. Devices with a silicon thickness of approximately 10 nm and a width ranging from 5 to 30 nm were made. Junctionless transistors have excellent on–off switching behavior and an on/off ratio larger than 10^5 for V_{DD}=0.5 V (Fig. 11). The off current could not be measured as it is lower than 1 fA, which is the sensitivity limit of the measuring apparatus.

The subthreshold slope at room temperature is 64 mV/decade, and it remains very close to the "ideal" value of (kT/q) ln(10) over the temperature range 225–475 K. Figure 12 shows the evolution of subthreshold slope, *SS* (in mV/decade) at V_{DS}=50 mV in a N-channel inversion-mode trigate MOSFET and a junctionless gated resistor. The subthreshold slope of both devices follows the following law: $SS = n\ (kT/q)\ ln(10)$ with $n = 1.066$, which is very close to the lowest theoretical limit ($n = 1$).

Equation 4 predicts an increase of drain current with doping concentration. This is indeed observed (Fig. 13), but it should be noted that the current increase is due not only to the reduction of channel resistivity with doping, but also to the improved conduction in the source and drain, which have the same doping concentration as the channel. In the measured devices, the length of the source, the drain and the channel region are all equal to 1 μm.

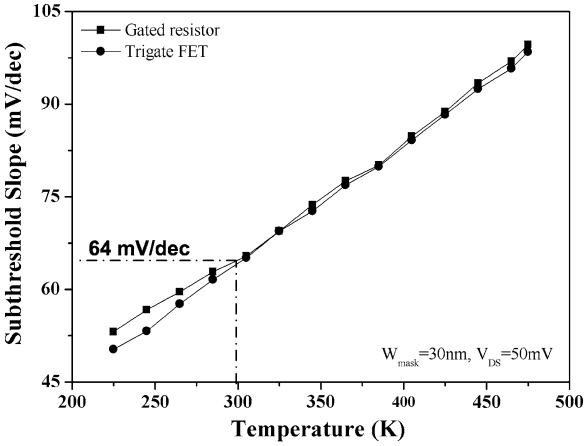

Fig. 12 Measured subthreshold slope versus temperature in a junctionless gated resistor and an inversion-mode trigate MOSFET

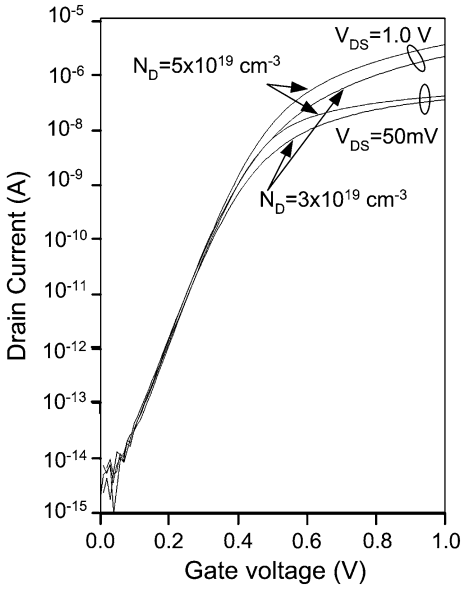

Fig. 13 Current versus gate voltage in junctionless devices with two different doping concentrations

5 Mobility Considerations

One might be concerned by the effect of the high channel doping concentration of junctionless gated resistors on carrier mobility. It is well known that ionized impurity scattering degrades carrier mobility. The electron mobility in silicon is shown in Fig. 14 as a function of donor atom concentration, N_D [9]. The mobility drops from 1,400 cm^2/Vs in lightly doped silicon to 80 cm^2/Vs for $N_D=10^{19}$ cm^{-3}.

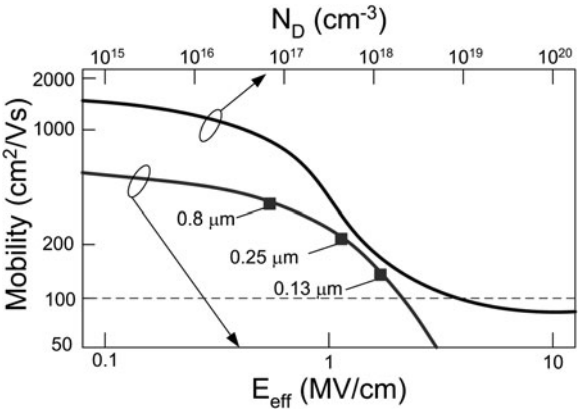

Fig. 14 Electron mobility in silicon as a function of donor doping atom concentration and as a function of electric field in the channel. The latter curve shows the mobility/field for several key technology nodes

Interestingly, mobility does not significantly degrade any further as the doping concentration is increased beyond 10^{19} cm^{-3}. A similar behavior is observed for holes in P-type doped silicon [9].

Channel mobility in inversion-mode devices is affected by the (vertical) electric field in the channel, E_{eff}. Since E_{eff} increases when the effective oxide thickness, *EOT*, is reduced, surface channel mobility has steadily decreased in successive technology nodes [10] and would now be well below 100 cm^2/Vs at the 45-nm node, if it wasn't for the introduction of strained silicon technology: dealing with mobilities of 80 cm^2/Vs in junctionless gated resistors does not sound like a completely outrageous idea when this is taken in consideration. It is also important to note that the conduction channel in junctionless devices is in the center of the device, and that the electric field perpendicular to the current flow, E_{eff}, is very small. As a result, mobility in junctionless devices is not expected to decrease as EOT is decreased [3].

Mobility in junctionless devices is largely dominated by ionized impurity scattering, and acoustic phonons seem to have little effect on mobility. Figure 15 shows the mobility, measured from the peak of transconductance as a function of gate voltage, in trigate SOI MOSFETs and in junctionless transistors. The inversion-mode trigate devices have either an undoped channel ($N_A \approx 5 \times 10^{15}$ cm^{-3}) or a doped channel ($N_A \approx 5 \times 10^{17}$ cm^{-3}). In the undoped devices the peak mobility is 350 cm^2/Vs at room temperature, but drops by 36% as temperature is increased to 200°C. The doped devices have a lower room-temperature mobility (220 cm^2/Vs) which also drops by approximately 36% as temperature is increased to 200°C. The heavily doped ($N_D \approx 2 \times 10^{19}$ cm^{-3}) junctionless devices have a much lower room-temperature mobility: 80 cm^2/Vs. However, the mobility decreases <7% as temperature is increased to 200°C. This clearly illustrated the fact that mobility is limited by ionized impurity scattering and is relatively insensitive to phonon scattering in heavily doped junctionless transistors. A similar trend is observed in p-channel devices (Fig. 15).

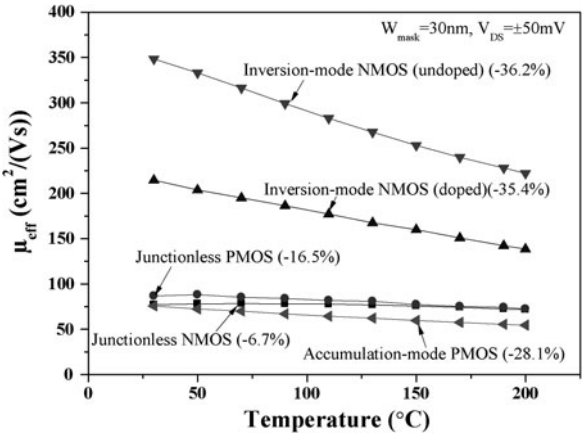

Fig. 15 Mobility in heavily doped junctionless transistors and in regular trigate MOSFETs with doped and undoped channels, as a function of temperature

6 Conclusion

Junctionless transistors are variable resistors controlled by a gate electrode. The silicon channel is a heavily doped nanowire that can be fully depleted to turn the device off. The electrical characteristics are identical to those of normal MOSFETs, but the physics is quite different. Three types of MOS devices: inversion-mode, accumulation-mode and junctionless MOSFETs are compared. The dependence of threshold voltage on device geometry and doping fluctuation effects in junctionless transistors is discussed. An analysis of mobility reduction effects is presented.

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