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Nanowire transistors without junctions

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All existing transistors are based on the use of semiconductor junctions formed by introducing dopant atoms into the semiconductor material. As the distance between junctions in modern devices drops below 10 nm, extraordinarily high doping concentration gradients become necessary. Because of the laws of diffusion and the statistical nature of the distribution of the doping atoms, such junctions represent an increasingly difficult fabrication challenge for the semiconductor industry. Here, we propose and demonstrate a new type of transistor in which there are no junctions and no doping concentration gradients. These devices have full CMOS functionality and are made using silicon nanowires. They have near-ideal subthreshold slope, extremely low leakage currents, and less degradation of mobility with gate voltage and temperature than classical transistors.

All existing transistors are based on the formation of junctions. Junctions are capable of both blocking current and allowing it to flow, depending on an applied bias. They are typically formed by placing two semiconductor regions with opposite polarities into contact with one another. The most common junction is the p–n junction, which consists of a contact between a p-type piece of silicon, rich in holes, and an n-type piece of silicon, rich in electrons. Every textbook on semiconductor device physics contains a chapter on the p–n junction, usually between the introductory chapters on semiconductor material fundamentals and the chapters dedicated to the different types of transistors. Other types of junctions include the metal–silicon 'Schottky' junction and the heterojunction, which is a p–n junction comprising two different semiconductor materials. The bipolar junction transistor contains two p–n junctions, and so does the MOSFET (metal-oxide–semiconductor field-effect transistor). The JFET (junction field-effect transistor) has only one p–n junction and the MESFET (metal–semiconductor field-effect transistor) contains a Schottky junction.

The first patent[1] for the transistor principle was filed in Canada by Austrian-Hungarian physicist Julius Edgar Lilienfield on 22 October 1925. He patented the device in the United States a few years later under the title 'Device for controlling electric current'[2], but he never published any research article on the device. The Lilienfield transistor is a field-effect device, much like modern metal-oxide–semiconductor (MOS) devices. It consists of a thin semiconductor film deposited on a thin insulator layer, itself deposited on a metal electrode. The latter metal electrode serves as the gate of the device. In operation, the current flows in the resistor between two contact electrodes, in much the same way that drain current flows between the source and drain in a modern MOSFET. The Lilienfield device is a simple resistor, and the application of a gate voltage allows the semiconductor film of carriers to be depleted, thereby modulating its conductivity. Ideally, it should be possible to completely deplete the semiconductor film of carriers, in which case the resistance of the device becomes quasi-infinite.

The Lilienfield transistor, unlike all other types of transistors, does not contain any junction. Although the idea of a transistor without junctions may seem quite unorthodox, the word 'transistor' does not, *per se*, imply the presence of junction. A transistor is a solid-state active device that controls current flow, and the word 'transistor' is a contraction of 'trans-resistor'. Technically, the Lilienfield transistor is a gated trans-resistor; that is, it is a resistor with a gate that controls the carrier density, and hence the current flow. It is the simplest and first patented transistor structure, but, unfortunately, the technology available at Lilienfield's time would never have been able to produce a working device.

Figure 1 presents a schematic view of a junctionless nanowire gated resistor. Having no junctions presents a great advantage. Modern transistors have reached such small dimensions that ultrasharp doping concentration gradients are required in junctions: typically the doping must switch from n-type with a concentration of 1×10^{19} cm^{-3} to p-type with a concentration of 1×10^{18} cm^{-3} within a couple of nanometres. This imposes severe limitations on the processing thermal budget and necessitates the development of costly millisecond annealing techniques. In a junctionless gated resistor, on the other hand, the doping concentration in the channel is identical to that in the source and drain. Because the gradient of the doping concentration between source and channel or drain and channel is zero, no diffusion can

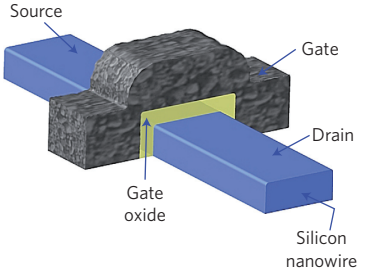

Figure 1 | Schematic of an n-channel nanowire transistor. The underlying insulator layer (buried oxide) is not shown. In a classical trigate device, the source and drain are heavily doped n-type and the channel region under the gate is lightly doped p-type. In the junctionless gated resistor, the silicon nanowire is uniformly doped n-type and the gate material is p-type polysilicon. Opposite dopant polarities are use for p-channel devices.

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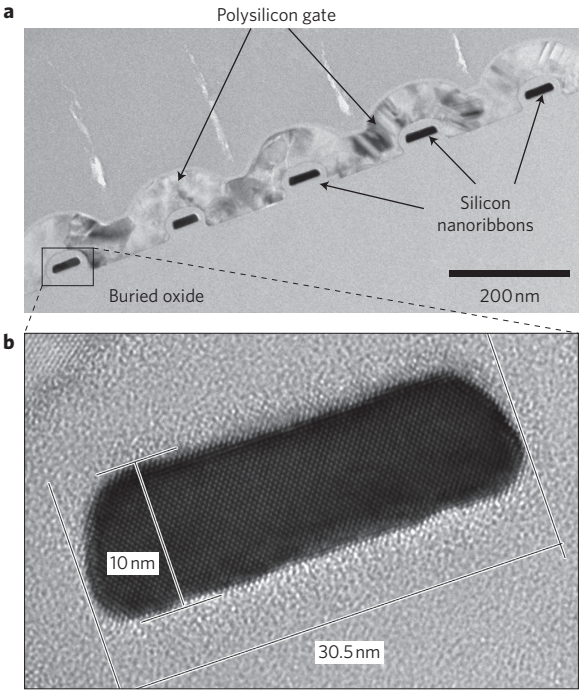

Figure 2 | Transmission electron micrograph of silicon gated resistor nanoribbons. a, Five parallel devices with a common polysilicon gate electrode. **b**, Magnification of a single nanoribbon device. Individual atomic rows can be seen in the silicon.

take place, which eliminates the need for costly ultrafast annealing techniques and allows one to fabricate devices with shorter channels.

The key to fabricating a junctionless gated resistor is the formation of a semiconductor layer that is thin and narrow enough to allow for full depletion of carriers when the device is turned off. The semiconductor also needs to be heavily doped to allow for a reasonable amount of current flow when the device is turned on. Putting these two constraints together imposes the use of nanoscale dimensions and high doping concentrations. The operation principle of the gated resistor has recently been investigated through simulations by several research groups, including the Technische Universität München, Carnegie Mellon University, IMEC and the Tyndall National Institute. The different teams used different names for their devices: vertical slit field-effect transistor (VeSFET)[3], nanowire pinch-off FET[4,5] or junctionless multigate field-effect transistor[6], but all these devices rely on the same basic principle of operation. More generally, the nanowire structure is steadily gaining acceptance as the best option for future nanoscale transistor fabrication[7–10].

An extremely simple transistor fabrication process

Silicon-on-insulator (SOI) technology can be used to produce high-quality, single-crystal silicon films with a thickness of a few nanometres. Using commercial SOI wafers and electron-beam lithography, we have defined silicon nanowires (or nanoribbons) a few tens of nanometres wide and 10 nm thick. After growing a 10-nm gate oxide, the nanowires were uniformly doped by ion implantation, using arsenic to dope the n-type devices and BF_2 to dope the p-type devices. The implant energies and doses were chosen to yield uniform doping concentrations ranging from of 2×10^{19} to 5×10^{19} atoms cm^{-3} in different wafers. Such high doping levels are traditionally reserved for source and drain extension formation in CMOS devices. In the gated resistor, high doping is required to ensure a high current drive and good source and drain contact resistance; it also imposes the use of nanowire geometries small enough to allow for the full depletion of the channel region, which is necessary to turn the device off. The gate was formed by deposition of a 50-nm-thick layer of amorphous silicon at a temperature of 550 °C in a low-pressure chemical vapour deposition (LPCVD) reactor. After heavy P^+ or N^+ gate doping using boron or arsenic ions at a dose of 2×10^{14} cm^{-2}, the samples were annealed in a nitrogen ambient at 900 °C for 30 min to activate the doping impurities and transform the amorphous silicon gate material in polycrystalline silicon. The gate electrodes were then patterned and etched in a reactive-ion etch (RIE) reactor. Figure 2 shows a transmission electron micrograph of five parallel silicon gated resistor nanoribbons with a common polysilicon gate electrode. The magnified view of a single nanoribbon device is also shown (Fig. 2b), in which individual silicon atomic rows can be observed. To obtain desirable values for the threshold voltage, a p^+ polysilicon gate is used for the n-type device and an n^+ polysilicon gate is used for the p-channel device. After gate patterning, a protective SiO_2 layer was deposited, contact holes were etched, and a classical TiW–aluminium metallization process was used to provide electrical contact to the devices. No doping step was performed after gate patterning, leaving the source and drain terminals with exactly the same doping type and concentration as the channel region. The device has a multigate (trigate, to be more specific) configuration, which means that the gate electrode is wrapped along three edges of the device (left, top and right sides of the nanoribbon)[11,12]. Classical trigate FETs were fabricated on separate wafers for comparison purposes. The fabrication process was identical to that used for the gated resistors with the following exceptions. The channel region was either left undoped or was p-type doped to a concentration of 2×10^{17} cm^{-3} (we consider here n-channel devices), n^+ polysilicon was used as the gate material, and arsenic ions were implanted at a dose of 2×10^{14} cm^{-2} with an energy of 15 keV after gate patterning to form the source and drain junctions.

Properties that rival those of the best MOS transistors

The current–voltage characteristics of the gated resistor are remarkably similar, indeed near identical, to those of a regular MOSFET. Figure 3 shows the drain current, I_D, versus gate voltage, V_G, for a drain voltage of ± 1 V in n-type and p-type devices having a width of 30 nm and a length of 1 μm. The off current is below

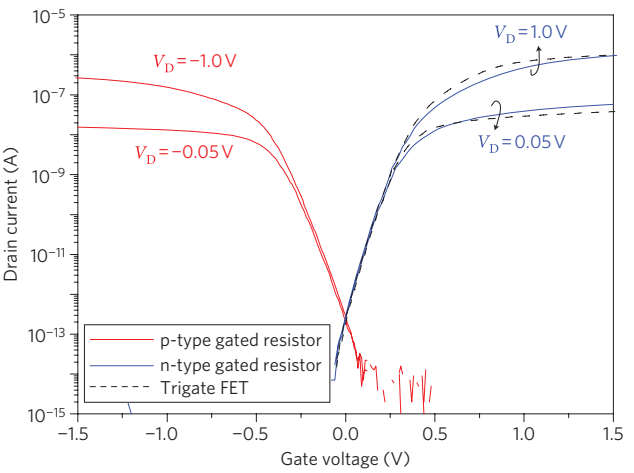

Figure 3 | Current–voltage characteristics. Drain current versus gate voltage for drain voltages of ± 50 mV and ± 1 V. The off current is below the detection limit of the measurement system (1×10^{-15} A), and the on/off current ratio for between $V_G = 0$ and $V_G = \pm 1$ V is larger than 1×10^6. The width of the device is 30 nm. The curve for a classical trigate FET is shown for comparison.

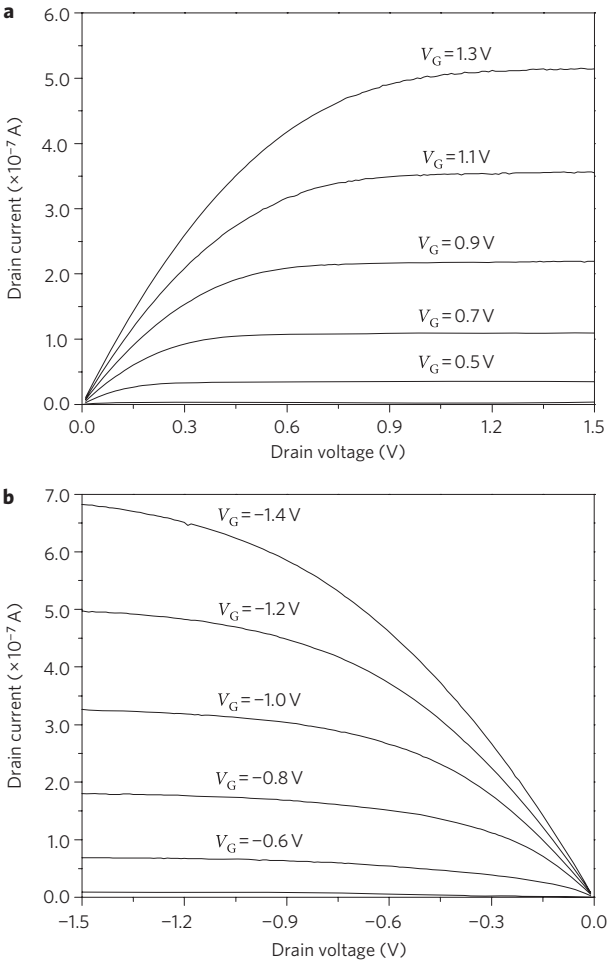

Figure 4 | Measured output characteristics of gated resistors. a,**b**, Drain current versus drain voltage for different values of gate voltage for an n-channel gated resistor (**a**) and a p-channel gated resistor (**b**). The width of the nanowires, *W*, is 20 nm and the gate length, *L*, is 1 μm, such that $W/L = 0.02$.

the detection limit of the measurement system (1×10^{-15} A), and the on/off current ratio for between $V_G = 0$ and $V_G = \pm 1$ V is larger than 1×10^6. This clearly establishes the fact that turning off the device by electrostatically depleting the channel of carriers works as well as turning it off using a reverse-biased junction. Figure 4 shows the experimental output characteristics of gated resistors. These characteristics are strikingly similar to those of regular MOSFETs.

The subthreshold slope (SS) is defined as the inverse of the slope of the log of the drain current versus gate voltage below threshold. It is expressed in millivolts per decade (mV dec^{-1}) and represents the sharpness of the on–off switching of a transistor. It has a theoretical lower (best) value of $SS = (k_B T/q)\ln(10)$, corresponding to the numerical value of 60 mV dec^{-1} at $T = 300$ K. Typical bulk MOS transistors have a subthreshold slope on the order of 80 mV dec^{-1}, and the best trigate SOI transistors come close to the theoretical limit with SS values of 63 mV dec^{-1} (ref. 13). The gated resistors reported here have a measured subthreshold slope of 64 mV dec^{-1} at 300 K, and remain within a few per cent of the ideal value of $(k_B T/q)\ln(10)$ for temperatures ranging from 225 to 475 K.

Traditional MOSFETs are fabricated as a semiconductor sandwich that is either n^+pn^+ (n^+ source, p-type channel region and n^+ drain) for n-channel devices and p^+np^+ for n-channel devices. In those devices, current flow between source and drain takes place in an inversion channel (n-type channel in p-type silicon or p-type channel in n-type silicon). In SOI, and in particular when using the trigate architecture, it is possible to realize accumulation-mode MOSFETs[14]. Traditional accumulation-mode devices are composed of an n^+nn^+ sandwich (n^+ source, n-type channel region and n^+ drain) for n-channel devices and p^+pp^+ for p-channel devices. In an accumulation-mode device, the channel is of the same polarity as the semiconductor region in which it is formed. In that regard, junctionless gated resistors are close cousins of accumulation-mode devices. There is one important difference, however. The channel region of accumulation-mode MOSFETs is lightly doped and, therefore, has a high resistance. To drive significant current through the device, a sufficiently large gate voltage must be applied to create an accumulation layer in the silicon beneath the gate oxide. This accumulation layer contains a high carrier concentration, which creates a low-resistivity path between source and drain and allows for significant current drive to flow. Inversion and accumulation carriers behave similarly in that they are confined to a very thin layer 'squeezed' along the silicon/gate oxide interface by the electric field originating from the gate electrode. The carriers are scattered by the non-zero roughness of the silicon/oxide interface and by the presence of charges trapped in the oxide or at the semiconductor interface. Scattering increases with applied gate voltage, which reduces carrier mobility and, hence, drain current.

In a gated resistor, on the other hand, the channel region is neutral in the centre of the nanowire and, because the carriers are located in neutral silicon (that is, not depleted silicon), they see a zero electric field in the directions perpendicular to the current flow. When the device is fully turned on, assuming a low drain voltage for simplicity, the entire channel region is neutral and in flatband conditions. The channel then effectively behaves as a resistor with conductivity $\sigma = q\mu N_D$, and the mobility is that of carriers travelling through bulk silicon. The mobility of electrons in heavily doped n-type silicon is ~100 cm^2 V^{-1} s^{-1}; it varies very little for doping concentrations ranging from 1×10^{19} to 1×10^{20} cm^{-2} (ref. 15). In a similar way, hole mobility hovers around 40 cm^2 V^{-1} s^{-1} in p-type silicon for the same doping concentrations. These mobility values may seem rather low, but they are to be placed in the context of modern short-channel MOSFETs. In unstrained silicon, the effective channel mobility of bulk MOSFETs drops from 400 cm^2 V^{-1} s^{-1} at the 0.8 μm node to 100 cm^2 V^{-1} s^{-1} at the 0.13 μm node[16]. Similarly, a drop of peak mobility from 300 to 140 cm^2 V^{-1} s^{-1} is reported in FinFETs when the gate length is reduced from 0.9 to 0.11 μm (ref. 17). If it was not for straining techniques, the electron mobility at the 45 nm node would be well below 100 cm^2 V^{-1} s^{-1}. These straining techniques can, of course, be applied to gated resistors as well inversion-mode transistors.

In a MOSFET, carriers are confined in an inversion channel in which scattering events rapidly increase in frequency with gate voltage, thereby decreasing transconductance and current drive. In the heavily doped gated resistor, the drain current essentially flows through the entire section of the nanoribbon, instead of being confined in a surface channel. Figure 5 shows the electron concentration in an n-type junctionless gated resistor for different values of gate voltage ranging from device pinch-off (Fig. 5a) to flatband conditions (Fig. 5d). The conduction path is clearly located near the centre of the nanowire, and not at the silicon–SiO_2 interfaces. This allows for the electrons to move through the silicon with bulk mobility, which is influenced much less by scattering than the surface mobility experienced by regular transistors. It is, however, possible to create surface accumulation channels by increasing the gate voltage beyond the flatband voltage, if a further increase of drain current is desired. Because it operates under bulk conduction rather than channel conduction, the gated

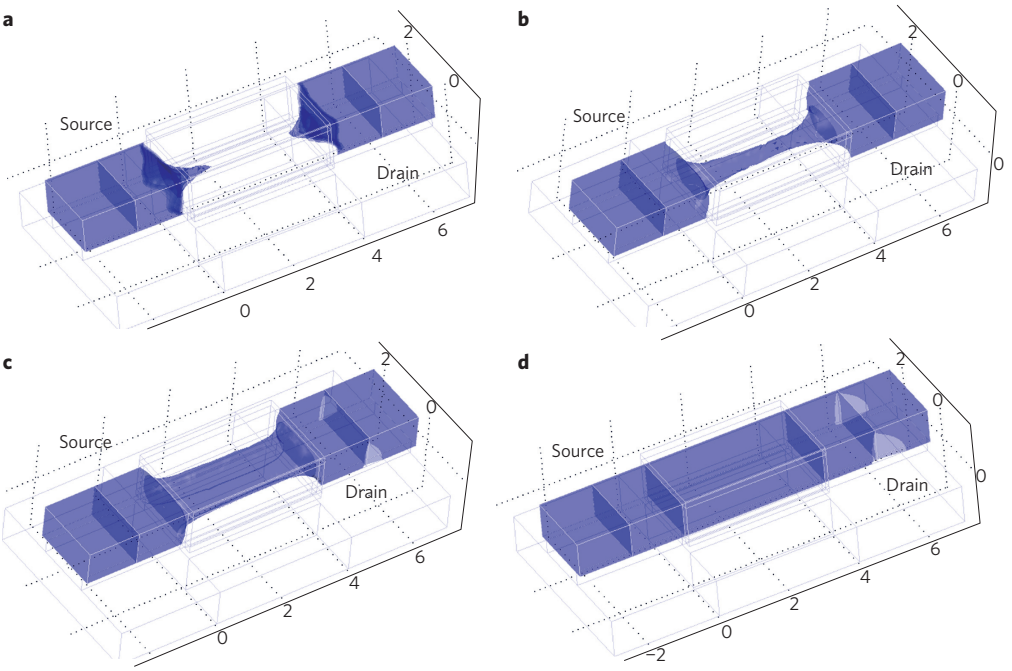

Figure 5 | Electron concentration contour plots in an n-type junctionless gated resistor. a–d, Plots result from simulations carried out for a drain voltage of 50 mV and for different gate voltage (V_G) values: below threshold ($V_G < V_{TH}$) the channel region is depleted of electrons (**a**); at threshold ($V_G = V_{TH}$) a string-shaped channel of neutral n-type silicon connects source and drain (**b**); above threshold ($V_G > V_{TH}$) the channel neutral n-type silicon expands in width and thickness (**c**); when a flat energy bands situation is reached ($V_G = V_{FB} \gg V_{TH}$) the channel region has become a simple resistor (**d**). The plots were generated by solving the Poisson equation and the drift-diffusion and continuity equations self-consistently. The device has a channel width, height and length of 20, 10 and 40 nm, respectively. The n-type doping concentration is 1×10^{19} cm^{-3}.

resistor sees its transconductance degrade much more slowly when gate voltage is increased. As a result, higher current and, therefore, higher-speed performance, can be expected from the gated resistor.

The variation of the threshold voltage of a gated resistor with temperature is similar to that of a bulk MOSFET, with values of approximately -1.5 mV °C^{-1} measured in our devices. Interestingly, the decrease of mobility with temperature is much smaller in the gated resistors than in trigate FETs. In a lightly doped FET, the mobility is little affected by impurity scattering and tends to be phonon-limited, so it shows a strong temperature dependence. In the highly doped gated resistor, on the other hand, mobility is limited by impurity scattering rather by phonon scattering, and its variation with temperature is much smaller. For instance, the electron mobility measured at room temperature in trigate FETs and gated resistors is 300 and 100 cm^2 V^{-1} s^{-1}, respectively. When heated to 200 °C, the trigate FETs show a 36% loss of mobility, whereas the gated resistor has a reduction in mobility of only 6%.

Perspectives for CMOS logic

Even though the electrical characteristics of the gated resistor are extremely similar to those of a regular MOS transistor, there is a fundamental difference between the two devices. MOSFETs (including FinFETs and trigate FETs) are normally-off devices, as the drain junction is reverse biased and blocks any current flow if no channel is created between source and drain. To turn the device on, the gate voltage is increased to create an inversion channel. The drain current in such a device is classically given by

$$I_D \approx \mu C_{ox} \frac{W_{si}}{L} (V_{DD} - V_{TH})^2$$

where W_{si} is the width of the device, L the gate length, V_{DD} the supply voltage and C_{ox} the gate oxide capacitance. The capacitance of the gate electrode, C, is given by $C \approx C_{ox} W_{si} L$, and the intrinsic delay time of the device, τ, is given by

$$\tau = \frac{CV}{I} \approx \frac{C_{ox} W_{si} L V_{DD}}{\mu C_{ox} (W_{si}/L)(V_{DD} - V_{TH})^2} \approx \frac{L^2}{\mu V_{DD}}$$

Speed performance can therefore be increased by either reducing the gate length or by increasing mobility, hence the use of strain silicon to boost the performance of MOSFETs[16]. It is interesting to note that τ is independent of gate oxide thickness, as any increase in current—and thus an increase in speed—brought about by a reduction of the effective gate oxide thickness (EOT) is exactly matched by an increase of C, which slows the device down.

The gated resistor, on the other hand, is basically a normally-on device in which the workfunction difference between the gate electrode and the silicon nanowire shifts the flatband voltage and the threshold voltage to positive values. When the device is turned on and in flatband conditions, it essentially behaves as a resistor and the drain current is given by

$$I_D \approx q\mu N_D \frac{T_{si} W_{si}}{L} V_{DD}$$

where T_{si} is the thickness of the silicon and N_D the doping concentration. Note that the current is independent of the gate oxide capacitance. Current can be increased simply by increasing the doping concentration of the device. The capacitance of the gate electrode is the same as that in a regular MOSFET, and thus the intrinsic delay time is given by

$$\frac{CV}{I} \approx \frac{C_{ox} W_{si} L V_{DD}}{q\mu N_D (T_{si} W_{si}/L) V_{DD}} \approx \frac{C_{ox} L^2}{q\mu N_D T_{si}}$$

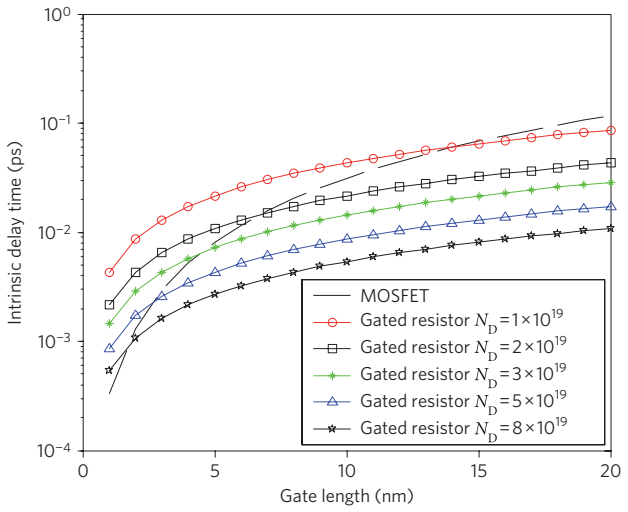

Figure 6 | Intrinsic device delay time for a MOSFET and for gated resistors. The delay (CV/I) is plotted as a function of gate length. The different curves for the gated resistor are for different channel doping concentrations ranging from 1×10^{19} to 8×10^{19} cm^{-3}. The effective gate oxide thickness, EOT, is equal to 1 nm for all gated resistors, but scales according to ITRS roadmap rules for the MOSFET.

In sharp contrast to the regular MOSFET, τ decreases when EOT is increased in a gated resistor. As a result, it is not necessary to reduce the gate oxide thickness as much as in a MOSFET to increase performance. Figure 6 shows the intrinsic delay time τ in a MOSFET and in gated resistors as a function of gate length. EOT is equal to 1 nm for all gated resistors, and it can be assumed that $T_{si} = L$. One can clearly see the increase of performance brought about by increasing the doping concentration in the gated resistor.

We find that the variability of the threshold voltage is larger in gated resistors than in traditional ultrathin-film, inversion-mode SOI transistors. Simulations indicate a dV_{TH}/dT_{Si} of 80 mV nm^{-1} in devices with a doping concentration of 1×10^{19} cm^{-3} and an EOT of 2 nm, which is approximately twice the variation observed in lightly doped, ultrathin inversion-mode SOI devices[18]. Because thin-film SOI wafers with a σT_{Si} of less than 0.2 nm can now be produced[18], threshold voltage variations on the order of $\sigma V_{TH} = 20$ mV can be expected at wafer level.

Conclusions

In conclusion, we report full CMOS operation of gated resistors. The devices have no junctions and are made in n^+ or p^+ silicon nanowires. The devices have full CMOS functionality, but they contain no junctions or doping gradients and are, therefore, much less sensitive to thermal budget issues than regular CMOS devices. Gated resistors have a near-ideal subthreshold slope, close to 60 mV dec^{-1} at room temperature, and extremely low leakage currents. Gated resistors exhibit less degradation of mobility than classical transistors when the gate voltage is increased.

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Author contributions

I.F., B.O'N., A.B., M.W., A.M.K. and B.McC. were responsible for device processing and I.F. and R.M. for device layout. A.A., N.D.A., R.Y., C.W.L. and P.R. performed device simulations. C.W.L. performed the electrical measurements and J.P.C. designed the devices and wrote the paper. All authors discussed the results and commented on the manuscript.

Additional information

The authors declare no competing financial interests. Supplementary information accompanies this paper at www.nature.com/naturenanotechnology. Reprints and permission information is available online at http://npg.nature.com/reprintsandpermissions/. Correspondence and requests for materials should be addressed to J.P.C.