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Junctionless Nanowire Transistor (JNT): Properties and design guidelines

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ABSTRACT

Junctionless transistors are variable resistors controlled by a gate electrode. The silicon channel is a heavily doped nanowire that can be fully depleted to turn the device off. The electrical characteristics are identical to those of normal MOS-FETs, but the physics is quite different. Conduction mechanisms in Junctionless Nanowire Transistors (gated resistors) are compared to inversion-mode and accumulation-mode MOS devices. The junctionless device uses bulk conduction instead of surface channel conduction. The current drive is controlled by doping concentration and not by gate capacitance. The variation of threshold voltage with physical parameters and intrinsic device performance is analyzed. A scheme is proposed for the fabrication of the devices on bulk silicon.

1. Introduction

It has been known for several years that the multigate nanowire transistor architecture, first proposed in 1995 [1], offers the best possible control of the channel by the gate and, therefore, the highest degree of control of short-channel effects [2]. All existing transistors are based on the use of semiconductor junctions, most of the time these are PN junctions. As MOS transistors enter the decananometer regime, extremely high doping density gradients are required to for these PN junctions. Because of the laws of diffusion and the statistical nature of the distribution of the doping atoms in the semiconductor, the formation of ultrashallow junctions with high doping concentration gradients has become an increasingly difficult challenge for the semiconductor industry, such that novel doping techniques and ultrafast annealing techniques must developed. The recently proposed Junctionless Nanowire Transistor (JNT, also called gated resistor), on the other hand, has no junctions and no doping concentration gradients. These devices have full CMOS functionality and are made using silicon nanowires [3].

2. Device physics

The key to fabricating a high-performance JNT is the formation of a semiconductor layer that is thin and narrow enough to allow for full depletion of carriers when the device is turned off. The semiconductor also needs to be heavily doped to allow for a decent amount of current flow when the device is turned on. Putting these two constraints together imposes the use of nanoscale dimensions and high doping concentrations [4,5]. The device is turned off not by a reverse-biased junction, as in the case of a conventional MOSFET, but by full depletion of the channel region. This depletion is caused by the workfunction difference between the gate material and the doped silicon in the nanowire. Fig. 1 shows the energy-band diagram for an *n*-channel JNT, assuming a P^+ polysilicon gate electrode. Flat-band condition is achieved when a positive gate bias equal to the workfunction difference between the nanowire and the gate material is applied to the gate (Fig. 1A). In that case the device is turned on. When a zero gate bias is applied, the channel region is fully depleted (Fig. 1B). The band curvature in the nanowire (ΔE in Fig. 1B) can be estimated assuming a gate-all-around configuration and a square cross-section where the width of the nanowire, W_{si}, is equal to its thickness, t_{si}. Using the Poisson equation with the depletion approximation we find:

$$\frac{d^2\Phi}{dx^2}+\frac{d^2\Phi}{dx^2}=2\frac{d^2\Phi}{dx^2}=-\frac{qN_D}{\varepsilon_{Si}}\rightarrow \Delta E=\frac{qN_D}{\varepsilon_{Si}}\frac{t_{Si}^2}{16}$$

The value of ΔE is typically around 100 meV, which means that in full depletion, the electron concentration at the Si–SiO_2 interfaces is approximately 50 times lower than in the center of the channel region. Assuming a doping concentration of 10^{19} cm^{-3} in the channel, the drain current can thus be decreased by approximately $\frac{10^{19}}{50n_i}=7.5$ orders of magnitude before the hole concentration at the Si–SiO_2 interfaces becomes equal to the electron concentration. It is thus safe to assume that the device operates with one type of carriers only (electrons).

The electrical characteristics of the JNT are remarkably identical to those of regular trigate MOSFETs. Fig. 2 shows $I_D(V_G)$ characteristics of an *n*-channel JNT. The device has an effective width of 25 nm and $L_g = 1$ nm. Extrapolating using $V_{DS} = 1$ V, $V_{Goff} = V_{TH} - 0.3$ V and $V_{Gon} = V_{TH} + 0.7$ V, $L = 20$ nm (assuming the current

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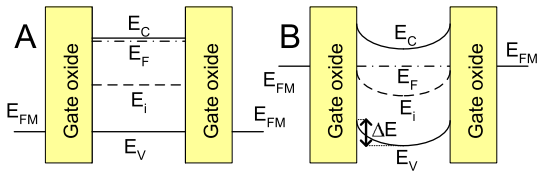

Fig. 1. Energy-band diagram for an *n*-channel JNT in (A) flat-band condition (the device is turned on) and (B) in the off state (the channel region is fully depleted).

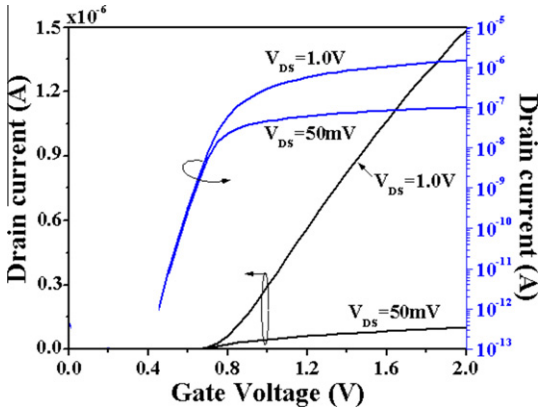

Fig. 2. Measured $I_D(V_G)$ characteristics of an *n*-channel device with $W = 25$ nm and $L = 1$ μm.

is proportional to 1/L) and a pitch of 50 nm one finds that the device is capable of I_{off} and I_{on} of 1 nA/μm and 1000 μA/μm, respectively, without using any mobility-enhancing technique such as strain. The conversion from "amperes" to "amperes per micron" is obtained by multiplying the current (A) by 1 μm divided by the pitch. Thus if the pitch is 50 nm, there are 20 parallel nanowires for a micron width and the current, expressed in A/μm, is 20 times the current (expressed in amperes) in a single nanowire.

The physics of the JNT, however, is quite different from that of standard multigate FETs. Depletion of the heavily doped nanowire creates a large electric field perpendicular to current flow below threshold, but above threshold the field drops to zero, because the conducting channel is electrically neutral (*i.e.* not depleted). This is the opposite of inversion-mode (IM) or even accumulation-mode (AM) devices where the field is highest in the channel when the device is turned on. In absence of strain-based mobility enhancement techniques, the electron mobility in the channel of an inversion-mode MOSFET can fall to values below 20 $cm^2/V\,s$ (assuming EOT = 1 nm and $V_G = 1$ V) because of the high electric field in the channel. In a JNT, the electric field in the channel, perpendicular to the current flow, is essentially equal to zero, which ensures bulk mobility values [6]. Fig. 3 compares the different operation regimes of inversion-mode, accumulation-mode and JNT devices. In an *n*-channel *inversion-mode* device, the substrate is p-type and the flatband voltage, V_{FB} is located well below the threshold voltage V_{TH}. Between V_{FB} and V_{TH}, in subthreshold operation, the silicon is depleted (weak inversion is included in the term "depletion"). Above V_{TH} the silicon surface is in inversion. Volume inversion can also occur if the silicon film is thin enough. In an *n*-channel *accumulation-mode* device, the substrate is lightly doped n-type. In subthreshold operation, the silicon is depleted. Threshold voltage is reached when a portion of the silicon becomes neutral (*i.e.* no longer depleted). Bulk current then flows in a neutral channel. Flatband voltage is reached at a slightly higher gate voltage, when the entirety of the silicon is neutral. Between V_{FB} and V_{TH}, the device is partially depleted. Any further increase of gate voltage creates a surface accumulation layer. In an *n*-channel *junctionless* device, the substrate is heavily doped n-type. In subthreshold operation, the silicon is depleted. Threshold voltage is reached when a portion of the silicon becomes neutral (*i.e.* no longer depleted). Bulk current then flows in a neutral channel. This current is much larger than the bulk current of the accumulation-mode device because the channel is heavily doped. As gate voltage increases, depletion decreases and the diameter of the neutral channel increases. The device is then partially depleted. The entire channel region becomes neutral (assuming low V_{DS}) when the devices reaches flatband voltage. It is possible to create an accumulation layer by further increasing the gate voltage, although this is not suitable for optimum device operation.

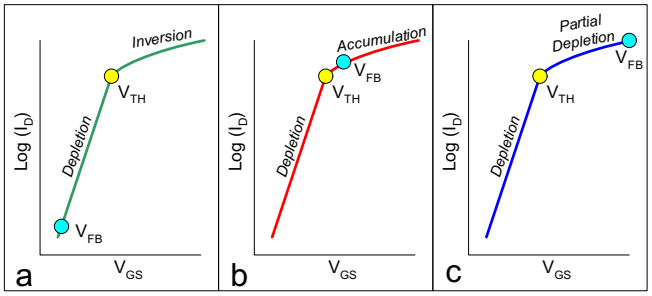

Fig. 3. Current in inversion-mode (a), accumulation-mode (b) and junctionless (c) nanowire MuGFETs. Note the very different positions of the flatband voltage, V_{FB}.

Like a regular MOSFET, the JNT enters saturation when the drain voltage is increased and, therefore, presents output characteristics that are identical to those of standard MOS devices. Fig. 4 shows the neutral (non-depleted) regions of a JNT above threshold, for different values of drain voltage. The solid contour (or colored volume) represent the regions where the electron concentration is equal to N_D (=10^{19} cm^{-3}). The transparent portion of the silicon nanowire represents the depletion region where the electron concentration is lower than N_D. In a way, the JNT basically behaves like a JFET [7] where the gate PN junction has been replaced by an MOS gate stack.

3. Device design

The threshold voltage of a JNT depends on the doping concentration N_D, on the effective gate oxide thickness EOT, on the nanowire thickness t_{si} and its width W_{si}. Figs. 5–7 give examples of V_{TH} variation with nanowire width and thickness, for selected values of N_D and EOT. Quite clearly, the V_{TH} variation with W_{si} offers high flexibility for achieving devices with different threshold voltages. For instance, for a P^+ polysilicon gate, a channel doping concentration $N_D = 2 \times 10^{19}$ cm^{-3}, $t_{si} = 8$ nm and EOT = 1 nm, a device with $V_{TH} = 0.5$ V is obtained if $W_{si} = 11$ nm and a device with $V_{TH} = 0.2$ V is obtained if $W_{si} = 17$ nm (Fig. 5).

On the flip side, one might wonder if the sensitivity of V_{TH} on t_{si} and W_{si} may not result in unacceptable variation of electrical parameters on a wafer and from wafer to wafer. The silicon film of modern SOI wafers is controlled within less than 0.5 nm. More worrisome is the control of the nanowire width. If a 15 nm-thick SOI layer is used, the threshold voltage variation with linewidth is very high ($dV_{TH}/dW_{si} = 100$ mV/nm). If t_{si} is reduced to 5 nm, on the other hand, a much more acceptable variation is obtained: $dV_{TH}/dW_{si} = 25$ mV/nm (Fig. 5). Reducing N_D and EOT improves threshold control. For instance, if $t_{si} = 5$ nm, EOT = 1 nm and $N_D = 10^{19}$ cm^{-3}, the value of dV_{TH}/dW_{si} is equal to 10 mV/nm (Fig. 7).

The use of undoped channels in thin SOI devices of multigate FETs has been shown to minimize threshold voltage variations caused by random impurity fluctuation effects [8]. However, an "undoped" device still has an "unintentional" doping concentration of approximately 1×10^{15} cm^{-3}. If one considers a device with a cross-section of 10 nm × 10 nm and a gate length of 20 nm, there

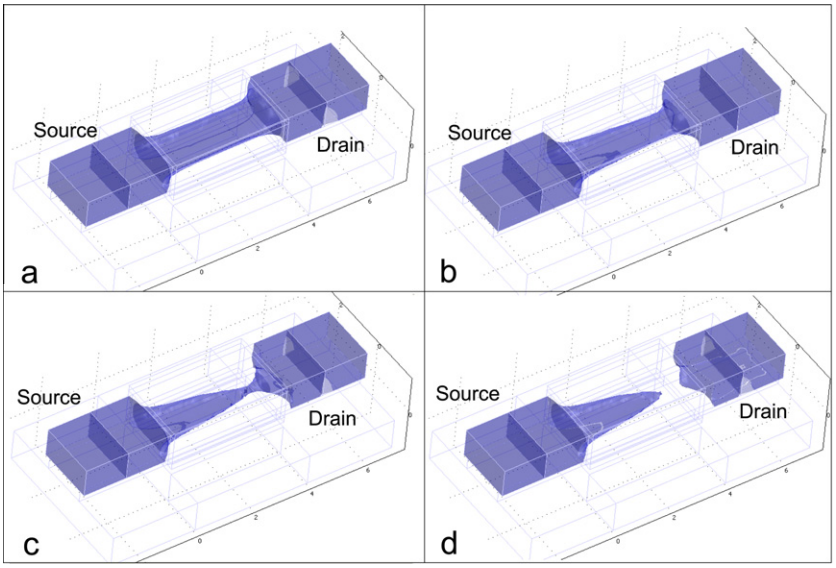

Fig. 4. Electron concentration contour plots in an n-type junctionless transistor. A: V_D = 50 mV; B: V_D = 200 mV; C: V_D = 400 mV; D: V_D = 600 mV. $V_G > V_{TH}$. Device parameters are: L = 40 nm, W_{si} = 20 nm, t_{si} = 10 nm, t_{ox} = 2 nm $N_D = 10^{19}$ cm^{-3}. Simulation was carried out by solving drift–diffusion, continuity and Poisson's equations. The simulation results were obtained using Comsol Multiphysics [14].

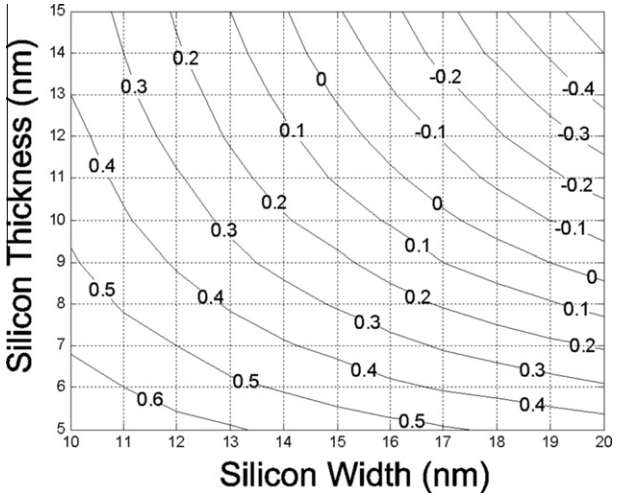

Fig. 5. Long-channel threshold voltage *vs.* nanowire width and thickness for $N_D = 2 \times 10^{19}$ cm^{-3} and EOT = 1 nm. Gate material is P$^+$ polysilicon. The simulation results were obtained using Comsol Multiphysics [8].

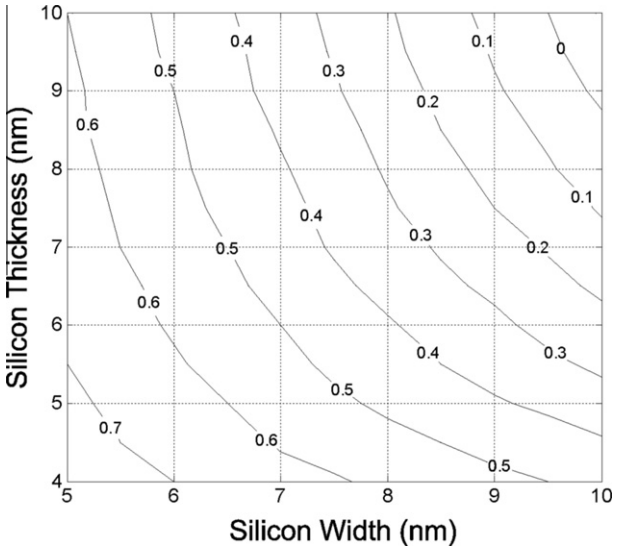

Fig. 6. Long-channel threshold voltage (volts) *vs.* nanowire width and thickness for $N_D = 5 \times 10^{19}$ cm^{-3} and EOT = 0.5 nm (P$^+$ polysilicon gate).

will statistically be one doping atom for every 500 transistors. The presence of either zero or one doping atom in a device causes a random threshold voltage variation of several tens of millivolts [9–11]. A similar fluctuation can be expected in JNTs: the channel of device with a cross-section of 10 nm × 10 nm, a gate length of 20 nm, an EOT of 1 nm and a doping concentration of 10^{19} cm^{-3} contains an average 20 doping atoms. Adding or removing one atom corresponds to a ±5% variation of doping concentration and a threshold voltage variation of ±15 mV. These variations are similar to those predicted in inversion-mode devices. Another source of fluctuations is the scattering of source/drain doping atoms into the channel [12]. This source of fluctuations is eliminated in JNTs because of the absence of junctions or doping gradients.

4. Bulk version of the device

We have analyzed the feasibility of a bulk silicon version of the JNT using 3D simulations. The cross-section ($W_{si} \times T_{si}$) of the N$^+$–N$^+$–N$^+$ device in Fig. 8 is 5 × 5 nm^2. The EOT is 2 nm. The extension, d, of side gates into the moderately doped (10^{17} cm^{-3}) p-type region was optimized to control SCEs and leakage current. Due to the N$^+$–N$^+$–N$^+$ design of MOSFET no lateral S/D junction (along the current flow path) is formed, but a vertical PN junction is required for device isolation. The device is still "junctionless" in the direction of current flow, even though a PN junction is used to insulate it from the substrate. Although the N$^+$ region is heavily doped (8×10^{19} cm^{-3}) to allow for high current flow in the on-state, the small cross-section of bulk-JLMOS ensures full depletion resulting in low leakage current down to 10 nm devices as demonstrated in Fig. 9. The gate is P$^+$ polysilicon. It should be noted that the leakage current of ~10 pA can be achieved in 25 nm bulk JLMOSFET and full device functionality is observed even in the absence of reversed biased lateral (in the direction of current flow) PN-junctions (Fig. 9).

Fig. 10 shows the dependence of subthreshold slope (S-slope) and drain induced barrier lowering (DIBL) parameters for the

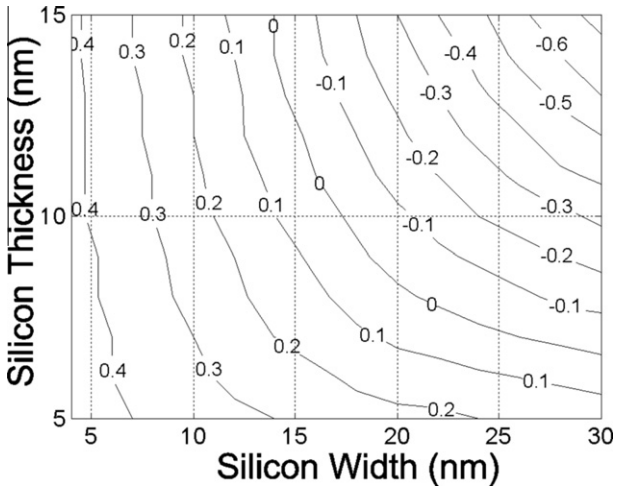

Fig. 7. Long-channel threshold voltage *vs.* nanowire width and thickness for $N_D = 10^{19}$ cm^{-3} and EOT = 1 nm (midgap metal gate).

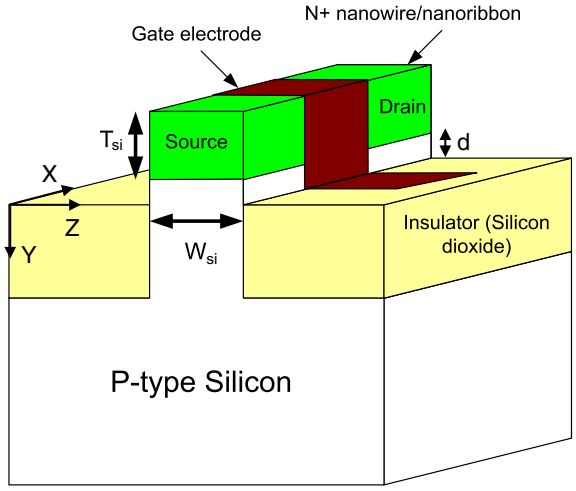

Fig. 8. Schematic diagram of a bulk JNT.

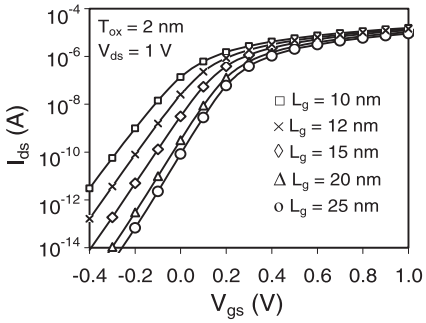

Fig. 9. Subthreshold characteristics of bulk JNT for different gate lengths (L_g). The gate workfunction is 5.5 eV and the drain voltage (V_{DS}) is 1. The extension of side gates (d) into the p-type region is 5 nm. The EOT is 2 nm. $W_{si} \times T_{si} = 5 \times 5$ nm^2. Simulation results obtained using Silvaco Atlas software. [15].

bulk-JNT device. Subthreshold slope and DIBL can be limited to less than 80 mV/decade and 100 mV/V, respectively, in bulk JNT devices for gate lengths down to 12 nm, in spite of the relatively thick gate oxide thickness of 2 nm. DIBL was extracted as difference in threshold voltages for drain bias of 50 mV and 1 V. An inversion-mode intrinsic bulk MOSFET designed with buried ground plane ($N_a \sim 10^{19}$ cm^{-3}) and 'idealized' abrupt S/D junction with

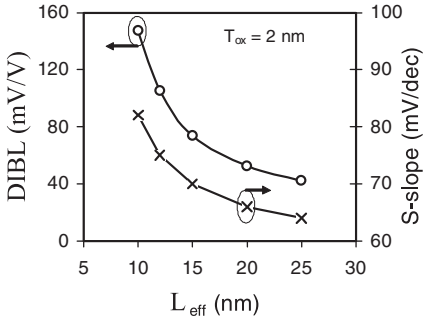

Fig. 10. DIBL and Subthreshold slope of bulk multi-gate JNTs for various gate lengths (L_g). *S*-slope was extracted at V_{DS} = 1 V. The EOT is 2 nm. $W_{si} \times T_{si} = 5 \times 5$ nm^2.

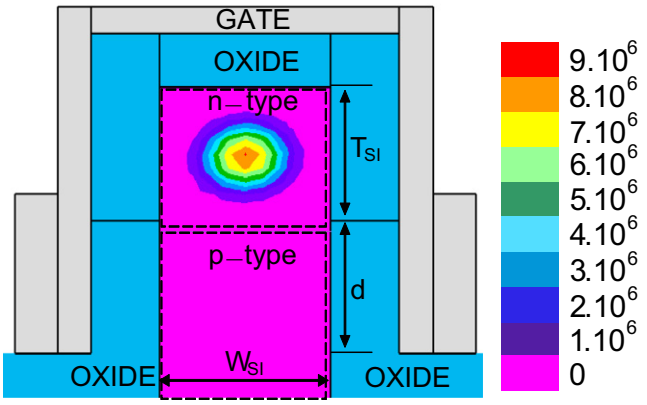

Fig. 11. 2D cut-plane showing total current density (A/cm^2) at V_{GS} = 0.4 V and V_{DS} = 50 mV for 20 nm-long bulk JNT. Simulation results obtained using Silvaco Atlas software [14].

L_g = 15 nm achieves a degraded *S*-slope of 78 mV/dec and DIBL of 95 mV/V when compared to 70 mV/dec and 74 mV/V respectively, for a JLMOSFET with same gate length. The *S*-slope and *DIBL* parameter for inversion mode devices can be reduced by adopting an underlap channel architecture [13]. However, such an approach will require precise control of S/D doping gradient in the S/D extension regions and additional process complexity which will be extremely difficult to optimize and be an added source of variability in the nanoscale regime. The bulk-JNT device offers greater flexibility in selecting device parameters to limit SCEs along with simpler fabrication process. The DIBL performance of the bulk JNT is similar to that of the SOI JNT. The subthreshold slope of the bulk JNT, on the other hand, is more degraded at short gate length than in the case of SOI devices [4].

Fig. 11 shows a current density contour plot in a cross-section of the bulk JNT, perpendicular to current flow in the channel, halfway between source and drain. The gate bias is 0.4 V. The entire flow of current is located in the center of the N$^+$ region. There is no current flowing in the p-type substrate underneath the N$^+$ nanowire.

5. Performance

The drain current of the JNT is proportional to the channel doping concentration and the cross-section of the nanowire, and *not* to the gate oxide capacitance. Fig. 12 shows the on current at $V_G = V_D$ = 1 V in SOI JNTs with a gate length L_g = 25 nm, as a function of device width and doping concentration. The aspect ratio (AR) of the nanowire is defined as AR = t_{si}/W_{si}. The devices in Fig. 12 have a square cross-section and thus $W_{si} = t_{si}$ and AR = 1.

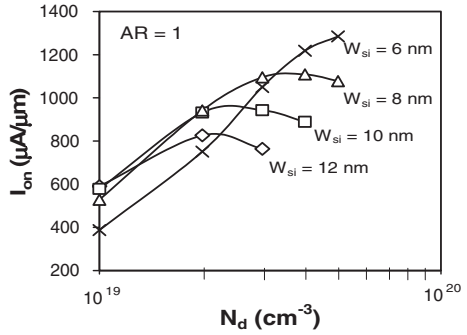

Fig. 12. I_{Dsat} in JNTs with $W_{si} = t_{si}$ and $L_g = 25$ nm. $t_{ox} = 1$ nm and a P^+-poly gate is used. $V_{DD} = 1$ V and $I_{off} = 100$ nA/μm.

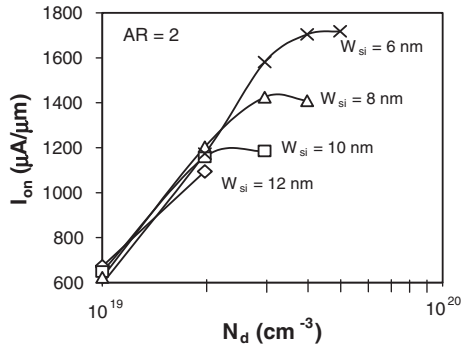

Fig. 13. I_{Dsat} in JNTs with $t_{si} = 2 \times W_{si}$ and $L_g = 25$ nm; $t_{ox} = 1$ nm and a P^+-poly gate is used. $V_{DD} = 1$ V and $I_{off} = 100$ nA/μm.

In all devices, the workfunction of the gate material is chosen such that $I_{off} = 100$ nA/μm, where I_{off} is the drain current at $V_D = 1$ V and $V_G = 0$ V. Assuming a nanowire pitch equal to $2 \times W_{si}$, where W_{si} is expressed in nanometers, the off current in each JNT is thus equal to $I_{off} \times 2 \times W_{si}/1000$. Thus, for example if $W_{si} = 10$ nm, the off current is 2 nA. One can see that on-current values on the order of 1000 μA/μm can be reached. Fig. 13 shows the on current for devices with an aspect ratio equal to 2 (*i.e.* $t_{si} = 2 \times W_{si}$). One can also see that a 30–40% increase in drain current is obtained by using an aspect ratio of 2 instead of 1. Note that the increase of current is less than 2, probably due to a less efficient control of the channel by the gate in the taller device.

6. Conclusion

This paper describes the conduction mechanisms in junctionless nanowire transistors. These devices do not operate in inversion or accumulation, but only in full or partial depletion. The threshold voltage depends on doping, EOT as well as on the width and thickness of the nanowires. In addition, the concept of a bulk multi-gate MOSFET without any lateral source/drain junctions is proposed. It has been demonstrated that JNT can exhibit low leakage currents and excellent short channel behavior at shorter gate lengths. Simulations show that the JNT is a strong contender for future CMOS as it delivers on/off ratio and current drive compatible with ITRS requirements.

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