Junctionless Transistors

Jean-Pierre Colinge
Tyndall National Institute, University College Cork
Lee Maltings, Cork, Ireland

Abstract—**This paper describes the physics and basic properties of junctionless transistors. These FETs are less subject to short-channel effects than devices with junctions, including excellent subthreshold slope and DIBL.**

Keywords-MOSFET, SOI, accumulation, nanowire transistor, multigate transistor

I. INTRODUCTION

The junctionless transistor (JLT) is a multigate FET with no PN nor N^+N or P^+P junctions. The device is basically a resistor in which the mobile carrier density can be modulated by the gate. In the on state there is a large body current due to the relatively high doping concentration in the channel region, to which surface assumulation current can be added. In the off state the channel is turned off by depletion of carriers due to the difference in workfunction between the semiconductor and the gate material. The doping in the JLT needs to be high in order to achieve suitable current drive, and the cross section of the devices needs to be small enough in order to be able to turn the device off. Both n-channel and p-channel silicon JLTs have been demonstrated, using both polysilicon and midgap gate materials. Polysilicon, germanium, Indium-Tin-Oxide and GaAs JLTs have been demonstrated as well.

II. COMPARISON WITH STANDARD FETS

Junctionless trasnsistors have electrical characteristics very similar to those of standard multigate FETs. Both output characteristic and subthreshold characteristics resemble those of inversion-mode devices. The JLT is a close cousin of the accumulation-mode FET.

A. Current drive and mobility

Fig. 1 shows the different conduction mechanisms in inversion-mode (IM), accumulation-mode (AM) and JLT devices. Conduction in the bulk of the AM device is negligible compared to accumulation surface conduction.

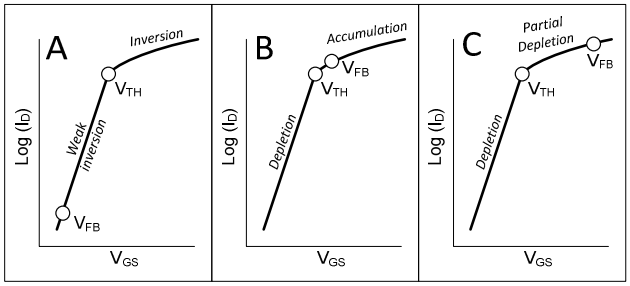

Figure 1: Conduction mechanisms in A: inversion-mode; B: accumulation-mode and C: junctionless FETs.

In the JLT bulk conduction is much larger and can account for up to 100% of the drain current. A simple but useful physically-based model that encompasses both bulk and accumulation currents in a JLT can be found in Table 1.

TABLE 1: Expressions for the drain current in a JLT [1].

Bias	Drain current
$V_{GS}>V_{po}$ $V_{GS}<V_{FB}$ $V_{DS}<V_{DSat1}$	$I_D = \frac{q\mu_b N_D}{L_{effb}}\left(\frac{1}{n+1}\frac{S_{max}-S_{min}}{(V_{FB}-V_{po})^n}\left((V_{GS}-V_{po})^{n+1} - (V_{GS}-V_{DS}-V_{po})^{n+1}\right) + S_{min}V_{DS}\right)$
$V_{GS}>V_{po}$ $V_{GS}<V_{FB}$ $V_{DS}>V_{DSat1}$	$I_D = \frac{q\mu_b N_D}{L_{effb}}\left(\frac{1}{n+1}\frac{S_{max}-S_{min}}{(V_{FB}-V_{po})^n}(V_{GS}-V_{po})^{n+1} + S_{min}V_{DS}\right)$
$V_{GS}>V_{FB}$ $V_{DS}<V_{DSat2}$	$I_D = \frac{q\mu_b N_D}{L_{effb}}S_{max}C_{ox} + \frac{\mu_{acc}C_{ox}W_{eff}}{L_{effacc}}\left(V_{DS}(V_{GS}-V_{FB}) - \frac{1}{2}V_{DS}^2\right)$
$V_{GS}>V_{FB}$ $V_{DS}<V_{DSat1}$ $V_{DS}>V_{DSat2}$	$I_D = \frac{q\mu_b N_D}{L_{effb}}\left((S_{max}-S_{min})(V_{GS}-V_{FB}) + S_{min}V_{DS} + \frac{S_{max}-S_{min}}{n+1}\frac{\left((V_{FB}-V_{po})^{n+1}-(V_{GS}-V_{DS}-V_{po})^{n+1}\right)}{(V_{FB}-V_{po})^n} + \frac{1}{2}\frac{\mu_{acc}C_{ox}W_{eff}}{L_{effacc}}(V_{GS}-V_{FB})^2\right)$
$V_{GS}>V_{FB}$ $V_{DS}>V_{DSat1}$	$I_D = \frac{q\mu_b N_D}{L_{effb}}\left(S_{max}(V_{GS}-V_{FB}) + \frac{S_{max}+nS_{min}}{n+1}(V_{FB}-V_{po})\right) + \frac{1}{2}\frac{\mu_{acc}C_{ox}W_{eff}}{L_{effacc}}(V_{GS}-V_{FB})^2$

TABLE 2: Detail of symbols used in Table 1 [1].

Symbol	Value
V_{po0}	Linear pinch-off voltage at V_D=0V
V_{po}	Pinch-off *voltage* $V_{po} = V_{po0} - \eta V_{DS}$
η	DIBL coefficient
W_{eff}	Channel perimeter
S	Neutral (non-depleted) cross section of the channel; $S=S_{min}$ when the surface is inverted and $S=S_{max}$ when the surface is accumulated
V_{DSat1}	Drain saturation voltage for the neutral bulk channel $V_{DSat1}=\frac{V_{GS}-V_{po0}}{1-\eta}$
V_{DSat2}	Drain saturation voltage for the accumulation channel $V_{DSat2} = V_{GS}-V_{FB}$
L_{effacc}, L_{effb}	Effective length of the accumulation channel and the neutral bulk channel
μ_{acc}, μ_b	Accumulation and bulk mobilities

978-1-4673-0836-6/12/$31.00 ©2012 IEEE

While the bulk mobility for electrons is low (≈60-80 $cm^2V^{-1}s^{-1}$) in heavily-doped ($10^{19}cm^{-3}$) silicon, mobility increases with applied gate voltage [2] and higher than bulk values are frequently being reported for JLTs operating in moderate accumulation [3]. This effect may be due to the screening of ionized impurities by the accumulation electrons, which reduces Coulomb scattering and increases mobility [4-6]. Figure 2 shows the mobility measured by the CV-split technique in long-channel planar and nanowire JLTs with $N_D \approx 5 \cdot 10^{18}/cm^3$. V_{TH} is the bulk channel threshold voltage and V_{FB} is approximately 0.4V higher than V_{TH}. Mobility increases with carrier concentration in all devices, including planar JLTs, but the increase is faster in narrow devices where higher concentration of mobile carriers can be obtained, which increases the screening effect.

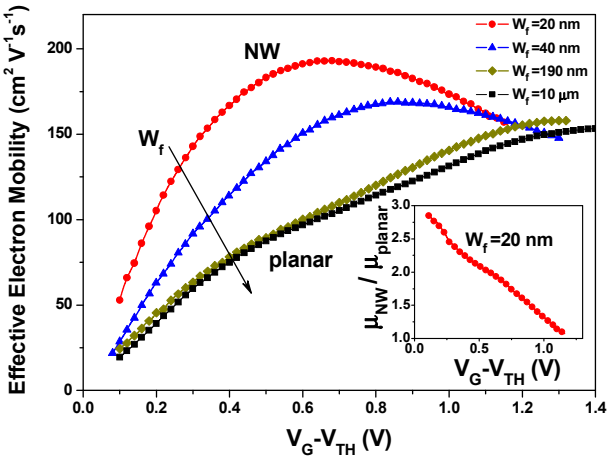

Figure 2: Effective electron mobility *vs*. gate voltage overdrive extracted for planar and nanowire JLTs with different fin widths. Inset shows this mobility improvement factor in a NW device with W_f=20 nm over the planar device. T_{si}=10nm and EOT=1.2nm.

B. Short-channel effects

In an IM FET the source and drain have some overlap with the gate, and the lateral extension of the S/D depletion charges in the channel region are causing short-channel effects such as DIBL and degraded subthreshold slope. These are absent in a JLT.

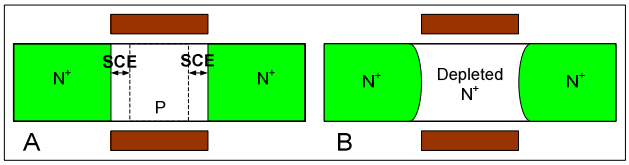

Figure 3: Illustration of SCE origin in junctioned and junctionless transistors.

In the off mode, the effective distance between the source and drain "junctions" is longer than the physical gate length (i.e. the channel depletion extends into the source and drain), unlike in a junctioned device with some S/D overlap with the gate (Figure 3). Further improvement of the short-channel effects can be obtained by increasing the extension of the gate control deeper in the source and drain regions using high-κ spacers. Table 3 compares the short-channel effects in IM and JLT nanowire devices with L=20nm, EOT=5nm, T_{si}=20nm and W_{si}=10nm.

TABLE 3: Comparison between inversion-mode and junctionless silicon transistors [7].

	Inversion mode	**Junctionless**
Subthreshold slope	75 mV/decade	92 mV/decade
DIBL	10 mV/V	78 mV/V
I_{ON}	1000 µA/µm	1000 µA/µm
I_{ON}/I_{OFF}	5×10^6	5×10^6

III. BEYOND SILICON

The JLT architecture is very simple and the elimination of junctions greatly simplifies processing, especially in non-silicon materials. Junctionless transistors have been demonstrated in polysilicon, germanium, GaAs and indium-tin-oxide (ITO) [9-12]. In polysilicon, the use of a heavily-doped channel decreases grain boundary potential barriers, which greatly improves current drive [9].

This work was supported by the Science Foundation Ireland grants 10/IN.1/I2992, the European project SQWIRE under Grant Agreement No. 257111 and the European Community (EC) Seventh Framework Program through the Network of Excellence Nano-TEC under Contract 257964.

REFERENCES

[1] M. Berthomé, S. Barraud, A. Ionescu, T. Ernst, "Physically-based, multi-architecture, analytical model for junctionless transistors", Proc. of the 12th International Conference on Ultimate Integration on Silicon (ULIS), Cork, Ireland, pp. 11-13, March 2011

[2] R. Rios, A. Cappellani, M. Armstrong, A. Budrevich, H. Gomez, R. Pai, N. Rahhal-orabi, and K. Kuhn, "Comparison of junctionless and conventional trigate transistors with lg down to 26 nm", IEEE Electron Device Letters, Vol. 32, pp. 1170-1172, 2011

[3] D.-Y. Jeon, S.J. Park, M. Mouis, M. Berthomé, S. Barraud, G.-T. Kim and G. Ghibaudo, "Electrical characterization and revisited parameter extraction methodology in junctionless transistors" Proceeding EUROSOI Conference, Montpellier (France), pp. 109-110, January 2012

[4] H.K. Sy, D.K. Desai, C.K. Ong, "Electron screening and mobility in heavily doped silicon, Physica Status Solidi (b), vol. 130, pp. 787-792, 1985.

[5] Y. Ohno, Y. Okuto, "Electron mobility in n-channel depletion-type MOS transistors", IEEE Transactions on Electron Devices, vol. 29, pp. 190-194, 1982

[6] J.B. McKeon, G. Chindalore, S.A. Hareland, W.-K. Shih, C. Wang, A. F. Tasch, Jr., C. M. Maziar, "Experimental determination of electron and hole mobilities in MOS accumulation layers", IEEE Electron Device Letters, vol. 18, pp. 200-202, 1997

[7] Chan-Hoon Park, Myung-Dong Ko, Ki-Hyun Kim, Chang-Woo Sohn, Chang Ki Baek,Yoon-Ha Jeong, and Jeong-Soo Lee, "Comparative study of fabricated junctionless and inversion-mode nanowire FETs", Proceedings 69th Annual Device Research Conference, Santa Barbara, CA, USA, pp. 179-180, 2011

[8] S. Gundapaneni, S. Ganguly and A. Kottantharayil, "Enhanced electrostatic integrity of short-channel junctionless transistor with high- κ spacers", IEEE Electron Device Letters, Vol. 32, pp. 1325-1327, 2011

[9] Chun-Jung Su Tzu-I Tsai Yu-Ling Liou Zer-Ming Lin Horng-Chih Lin Tien-Sheng Chao, "Gate-All-Around Junctionless Transistors With Heavily Doped Polysilicon Nanowire Channels", IEEE Electron Device Letters, vol. 32, pp. 521-523, 2011

[10] Dan Dan Zhao, T. Nishimura, Choong Hyun Lee, K. Nagashio, K. Kita and A. Toriumi (2011), "Junctionless Ge p-Channel Metal–Oxide–Semiconductor Field-Effect Transistors Fabricated on Ultrathin Ge-on-Insulator Substrate", Applied Physics Express 4, 031302

[11] Seongjae Cho, Se Hwan Park, Byung-Gook Park, and J.S. Harris Jr.,"Silicon-Compatible Bulk-Type Compound Junctionless Field-Effect Transistor", Proceedings of ISDRS 2011, College Park, MD, USA, December 7-9, 2011,

[12] Jie Jiang, Jia Sun, Wei Dou, Bin Zhou, and Qing Wan, "Junctionless in-plane-gate transparent thin-film transistors", Applied Physics Letters, vol. 99, p. 193502, 2011