Physically-based, multi-architecture, analytical model for junctionless transistors

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1. Abstract

In this paper we propose a new physically-based analytical model for junctionless transistors. Various MOSFET architectures based on single-gate (SG), double-gate (DG) and Gate-All-Around (GAA) transistors are studied. In particular the trade-off between the electrostatic control and the current drivability (first-order evaluation) is evaluated. Comparisons between numerical and analytical results are done in order to verify assumptions for pinch-off voltage and depletion regions. Traditional analytical expressions for this phenomenon are re-explored, and used to derive some technological guidelines.

2. Introduction

Junctionless Nanowire Transistors have been introduced recently [1,2] as a potential way of coping with the continuing degradation of the mobility in ultra-scaled transistors. The use of an undepleted channel [3] instead of an inversion layer opens some novel possibilities, because there are no source/drain junctions, and because the carriers are located in a "neutral region" relatively far from any surface.

The absence of junctions potentially simplifies the transistor technological process; there is no more need for ultra abrupt junctions [4]. The fact that the channel is undepleted means that the carriers are located in the whole silicon film, with a low transverse electric field region. This has potential advantages, in terms of mobility [5], especially to reduce the surface-roughness scattering.

The scaling rules and the (actual) current drivability of junctionless transistors is subject of discussions in several papers [1,6]. Then, the development of a physically-based analytical model, validated with TCAD simulations, is necessary to predict both the performances and the scalability of junctionless transistors .

The electrical performances of MOSFET devices are usually investigated though the analysis of various physical quantities as the carrier mobility, the access resistances, the carrier ballisticity, but also by studying the devices electrostatics. This paper mainly focuses on the latter assuming that quantum confinement effects are negligible both on electrostatics and transport. This first-order model includes most "classical" effects of heavily doped silicon [7-9] and enables the investigation of the operation of junctionless transistors. We propose to re-explore traditional hypothesis of junctionless/accumulation-mode models whatever the MOSFET architecture (SG, DG, GAA). Subsequently, as for usual inversion-mode models, effective mobility, short channel effects may be added in this model.

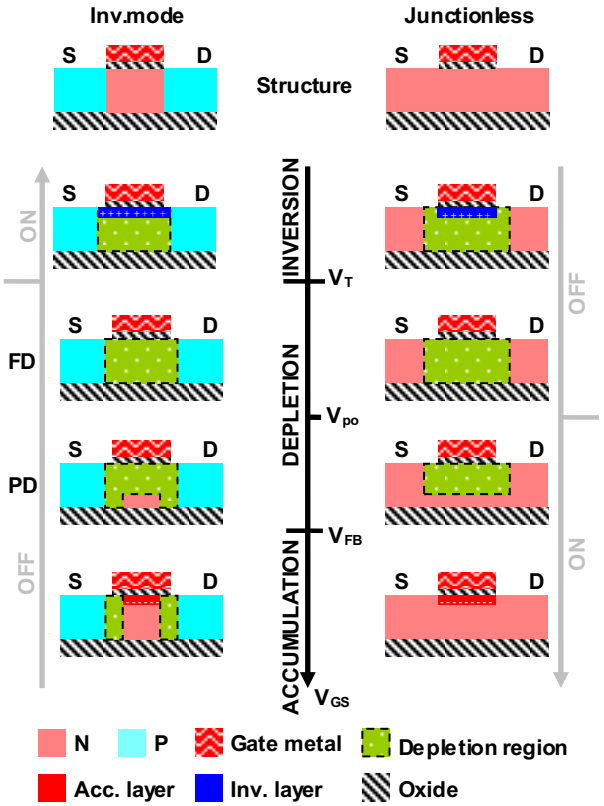

Fig. 1 *Differences of operating regimes between standard MOSFET (PMOS) and junctionless MOSFET (NMOS).*

3. Analytical model

First, we consider the pinch-off voltage (V_{po}) as a parameter of the model defined as the gate voltage at which the channel becomes not fully depleted. We consider that, above the pinch-off voltage, the carriers can be clearly separated into bulk (undepleted region) and accumulated (accumulation layer, above the flat-band voltage V_{FB}) carriers.

The variation of the depletion region with the gate voltage is not deduced from the Poisson equation integration, but by using an empirical expression, with a power-law

variation of the neutral undepleted channel between the pinch-off voltage and the flat-band voltage. This enables to easily address multiple architectures, and makes more explicit the pinch-off voltage in the drain current formulation, as is usually the case for the threshold voltage in the inversion-mode models.

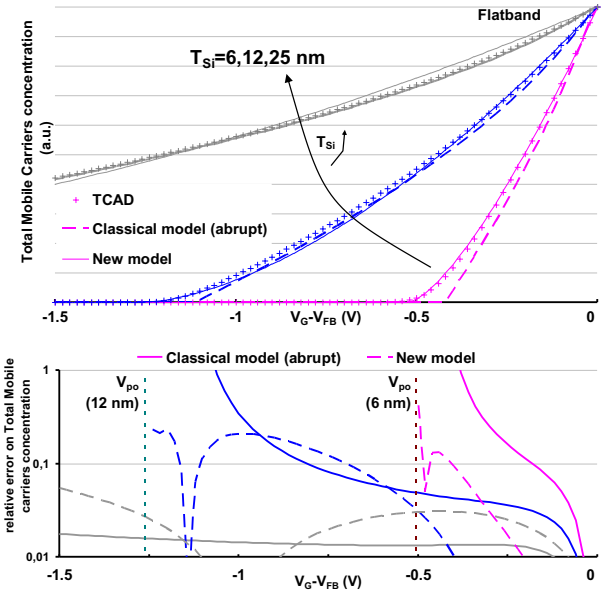

Fig. 2 *Top : Comparison between TCAD simulation (symbol) and abrupt depletion approximation model(solid line) Bottom : Relative error between abrupt model and TCAD and between our model and TCAD, showing an overall better agreement, especially for thin films and around the pinch-off. T_{Si}=6,12,25 nm, T_{ox}=1nm, N=2×10^{19}cm^{-3} for Double-Gate geometry*

Then, the derivation of the drain current equations follows the gradual channel approximation [10], with the following mobile charge concentrations: for a given channel potential V_c and a gate voltage V_{GS}, the undepleted region carriers charge is given by:

$$Q_{neut} = qNS_{ch} = qN\begin{cases} S_{\min} & V_{GS}-V_C < V_{po} \\ S_{\min} + (S_{\max} - S_{\min})\left(\dfrac{V_{GS}-V_C-V_{po}}{V_{FB}-V_{po}}\right)^n & V_{po} < V_{GS}-V_C < V_{FB} \\ S_{\max} & V_{GS}-V_C > V_{FB} \end{cases} \quad (1)$$

The accumulation mobile charge is given by:

$$Q_{acc} = P_{ch}C_{ox}\left(V_{GS} - V_{FB} - V_C\right) \quad (2)$$

The parameter P_{ch} is the perimeter of the channel cross-section transverse to the transport (e.g. for a cylindrical GAA it is $2\pi R = \pi T_{Si}$). The section of the channel S_{ch} is the area available for the transport. For a cylindrical GAA it is $\pi R^2 = \pi T_{Si}^2/4$, and for a trigate, planar or DG it is WT_{Si}, etc. $S_{\min}$ and $S_{\max}$, are the undepleted sections when the surface is inverted and accumulated, respectively.

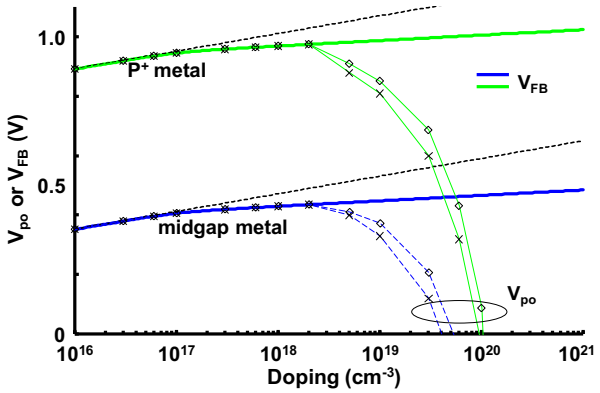

Fig. 3 *Flat-band voltage for an N-type film for P$^+$-type (band edge workfunction) gate metal (blue dashes) and mid-gap metal (solid green). In light dashes are shown the flat-band voltage that would result from Boltzmann approximation. In light solid lines and symbols, the pinch-off voltage determined with abrupt depletion approximation (diamonds) or our model (crosses), for T_{Si}=10nm, T_{ox}=1nm, for Double-Gate geometry*

The fit between the power-law and the TCAD simulations is not perfect, but this scheme still retains the most important feature: gradual opening of the channel above pinch-off voltage, up to the flat-band voltage.

The use of the pinch-off voltage to describe the drain current is indeed descriptive of, e.g., given current characteristics, but it is not enough predictive. Indeed, the relation between the geometry (thickness, oxide, etc), the doping and the pinch-off voltage is not explicit. In previous models [11-13] the abrupt depletion approximation was used to obtain both the pinch-off voltage and the variation of the depletion region. TCAD simulations have shown that the abrupt depletion is not entirely suitable for very small films compared to the Debye length, as seen in Fig. 2.

The pinch-off voltage could of course be determined by solving the Poisson-Boltzmann (or more accurate Poisson-Fermi-Dirac) equations for the potential:

$$\frac{d^2\Phi}{dx^2} = \frac{-\rho}{\varepsilon_0\varepsilon_{Si}} = \frac{\pm qN}{\varepsilon_0\varepsilon_{Si}}\left(\frac{n_i^2}{N^2}e^{\Phi/V_t} + 1 - e^{-\Phi/V_t}\right) \quad (3)$$

The determination of the pinch-off voltage for a given geometry is inspired from previous works on the solution of the Poisson-Boltzmann equations in thin films [14,15]: beginning with an estimation of the potential (e.g. from the abrupt depletion approximation), we obtain the mobile charge by applying the majority carriers part of the right hand side of (3) to the potential estimation. The criteria for the pinch-off is not defined as the junction of the depletion region edges, but as the gate voltage for which the integrated mobile charge in the whole channel (electrons in N-type silicon) is equal to $P_{ch}C_{ox}V_t$. This definition of the pinch-off is consistent with the analytical model: just above the pinch-

off voltage, the channel contains just enough mobile charge to rise above the thermal noise and the channel is just opened.

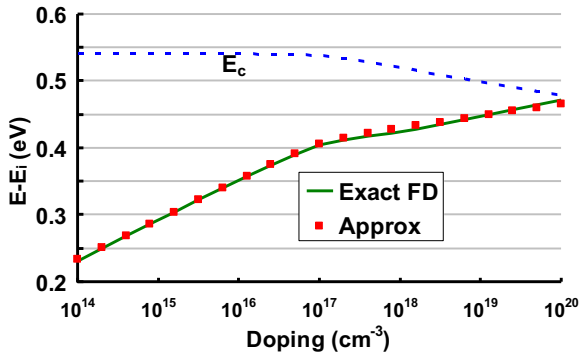

Fig. 4 *Exact Fermi neutrality resolution (solid line). Variable intrinsic concentration approximation (dots). Conduction Band edge (dashed line), relative to the intrinsic Fermi level.*

Typically, the geometry and doping determine the interval between the pinch-off and the flat-band voltages for a given device. It is important to note that the flat-band voltage itself is not dependent on the geometry.

The determination of the flat-band voltage needs to take into account the degeneracy because of the high doping levels that are required in this kind of transistor. The Fermi level could be determined via the resolution of the non linear neutrality equation using Fermi-Dirac integrals, with the bandgap and electron affinity depending on the doping level. Instead of using time-consuming nonlinear resolution, we will use an effective intrinsic concentration model (see Fig. 4), where the intrinsic concentration is dependent on the doping level N.

$$\left|E_F - E_{i0}\right| = k_B T \ln\left(\frac{N}{n_i(N)}\right) \qquad n_i(N) = n_{i0}\exp\left(-\frac{\Delta E_g(N)}{k_B T}\right)$$ where

$E_g(N)$ is based on a bandgap narrowing model. Φ_M is the gate metal workfunction. Oxide charges are gathered in Q_{ox}. Flat band voltages for N and P films are shown in Fig. 3. We see that with abrupt depletion and without degeneracy taken into account, we can severely overestimate the pinch-off voltage.

$$V_{FB} = \Phi_M - \chi(N) + (E_F - E_{i0})(N) - E_g(N) - \frac{Q_{ox}}{C_{ox}} \qquad (4)$$

With the pinch-off voltage and drain current models, we can, for example, determine the geometry needed to have a constant V_{po}. The example we chose is 0.5V. The gate metal is the best scenario of a P^+ metal on an N^+ film, as already discussed in [1]. Then, the I_{ON} current (formulations in annex) is calculated at V_{GS}=1V and V_{DS}=1V. We see that keeping V_{po} constant actually does not increase the I_{ON} current with increasing doping, it can actually decrease it. The needed thickness to keep V_{po} constant rapidly decreases to critical dimensions (5nm and below), as seen in Fig. 5. Without model parameter fit, the model predictions and the TCAD simulations follow quite closely.

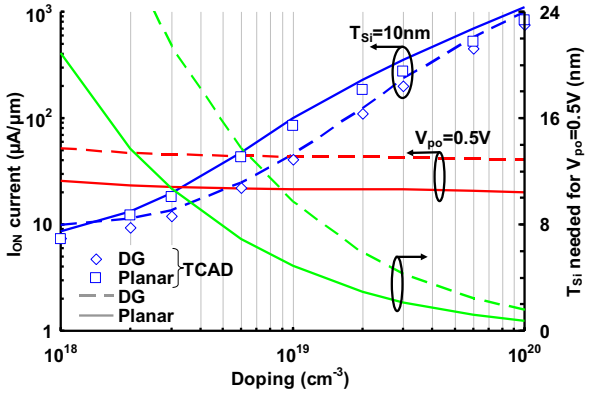

Fig. 5 *I_{ON} current (V_{GS}=1V, V_{DS}=1V), T_{ox}=1nm, metal workfunction 5.2 eV. For Planar and DG geometry (Width 1μm, L_G=1μm). Symbols are corresponding TCAD simulations.*

4. Conclusions and Further work

A new first-order model for a junctionless transistor has been derived. It permits a first order description of the drain current, the pinch-off and flat-band voltages, useful for technological parameters evaluation. Further study in more advanced modeling (quantum corrections, short channel effects, subthreshold conduction) is under investigation.

Annex: Drain current expressions

The drain current expressions for all possible terminal voltages are described below, with the terminology explained.

Acknowledgments

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V_{FB}	Flat band voltage
V_{po0}	linear Pinch-off voltage (zero drain voltage)
V_{po}	$V_{po0} - \eta V_{DS}$ Pinch-off voltage
η	DIBL coefficient
C_{ox}	gate oxide capacitance, (normalized by the channel perimeter)
P_{ch}	channel perimeter
S_{ch}	Channel surface
V_{DSat1}	$\frac{V_{GS} - V_{po0}}{1-\eta}$ saturation voltage for the neutral channel
V_{DSat2}	$V_{GS} - V_{GB}$ saturation voltage for the accumulation channel
L_{effb} L_{effacc}	effective channel lengths (neutral, accumulation)
μ_b μ_{acc}	effective mobilities (neutral, accumulation)

- $V_{GS} > V_{po}$ $V_{GS} < V_{FB}$ $V_{DS} < V_{DSat1}$

$$I_D = \frac{\mu_b e N_D}{L_{effb}} \left(\frac{1}{n+1} \frac{S_{\max} - S_{\min}}{(V_{FB} - V_{po})^n} \left((V_{GS} - V_{po})^{n+1} - (V_{GS} - V_{DS} - V_{po})^{n+1} \right) + S_{\min} V_{DS} \right)$$

- $V_{GS} > V_{po}$ $V_{GS} < V_{FB}$ $V_{DS} > V_{DSat1}$

$$I_D = \frac{\mu_b e N_D}{L_{effb}} \left(\frac{1}{n+1} \frac{S_{\max} - S_{\min}}{(V_{FB} - V_{po})^n} (V_{GS} - V_{po})^{n+1} + S_{\min} V_{DS} \right)$$

- $V_{GS} > V_{FB}$ $V_{DS} < V_{DSat2}$

$$I_D = \frac{\mu_b e N_D}{L_{effb}} S_{\max} V_{DS} + \frac{1}{L_{effacc}} \mu_{acc} C_{ox} P_{ch} \left(V_{DS} (V_{GS} - V_{FB}) - \frac{1}{2} V_{DS}^2 \right)$$

- $V_{GS} > V_{FB}$ $V_{DS} < V_{DSat1}$ $V_{DS} > V_{DSat2}$

$$I_D = \frac{\mu_b e N_D}{L_{effb}} \left(\begin{array}{l} (S_{\max} - S_{\min})(V_{GS} - V_{FB}) + S_{\min} V_{DS} \\ + \frac{S_{\max} - S_{\min}}{n+1} \frac{1}{(V_{FB} - V_{po})^n} \left((V_{FB} - V_{po})^{n+1} - (V_{GS} - V_{DS} - V_{po})^{n+1} \right) \end{array} \right) + \frac{1}{2 L_{effacc}} \mu_{acc} C_{ox} P_{ch} (V_{GS} - V_{FB})^2$$

- $V_{GS} > V_{FB}$ $V_{DS} > V_{DSat1}$

$$I_D = \frac{\mu_b e N_D}{L_{effb}} \left[S_{\max} (V_{GS} - V_{FB}) + \frac{S_{\max} + n S_{\min}}{n+1} (V_{FB} - V_{po}) \right] + \frac{1}{2 L_{effacc}} \mu_{acc} C_{ox} P_{ch} (V_{GS} - V_{FB})^2$$

5. References

[1] J.P. Colinge et al., "Nanowire transistors without junctions," *Nature Nanotechnology*, vol. 5, Mar. 2010, pp. 225-229.

[2] B. Soree et al., "Silicon nanowire pinch-off FET : Basic operation and analytical model," *Ultimate Integration of Silicon, 2009. ULIS 2009. 10th International Conference on*, 2009, pp. 245-248.

[3] J.P. Colinge et al., "SOI gated resistor: CMOS without junctions," *SOI Conference, 2009 IEEE International*, 2009, pp. 1-2.

[4] ITRS, "ITRS PIDS, 2009 Edition."

[5] V.K. Arora, "High-Field Distribution and Mobility in Semiconductors," *Japanese Journal of Applied Physics*, vol. 24, 1985, pp. 537-545.

[6] A. Kranti et al., "Junctionless Nanowire Transistor (JNT): Properties and Design Guidelines," *Proc. European Solid State Device Research Conf. (ESSDERC)*, Seville, Spain: 2010, pp. 357-360.

[7] H.S. Bennett et al., "Majority and Minority Mobilities in Heavily Doped Silicon for Device Simulations," *Numerical Modeling of Processes and Devices for Integrated Circuits, 1992. NUPAD IV. Workshop on*, 1992, pp. 123-128.

[8] S. Ristić et al., "Dependance of Static Dielectric Constant of Silicon on Resistivity at Room Temperature," *SERBIAN JOURNAL OF ELECTRICAL ENGINEERING*, vol. 1, Jun. 2004, pp. 237-247.

[9] D. Schroeder et al., "Comparison of transport models for the simulation of degenerate semiconductors," *Semiconductor Science and Technology*, vol. 9, 1994, p. 364.

[10] W. Shockley, "A Unipolar "Field-Effect" Transistor," *Proceedings of the IRE*, vol. 40, 1952, pp. 1365-1376.

[11] Y.S. Yu et al., "A compact analytical current conduction model for a depletion-mode n-type nanowire field-effect transistor with a bottom-gate structure," *Semiconductor Science and Technology*, vol. 23, 2008, p. 035025.

[12] K.W. Su et al., "Analysis of current conduction in short-channel accumulation-mode SOI PMOS devices," *Electron Devices, IEEE Transactions on*, vol. 44, 1997, pp. 832-840.

[13] J.P. Colinge, "Conduction mechanisms in thin-film accumulation-mode SOI p-channel MOSFETs," *Electron Devices, IEEE Transactions on*, vol. 37, 1990, pp. 718-723.

[14] J. Sleight et al., "A continuous compact MOSFET model for fully- and partially-depleted SOI devices," *Electron Devices, IEEE Transactions on*, vol. 45, 1998, pp. 821-825.

[15] Z. Jian et al., "One-dimensional continuous analytic potential solution to generic oxide–silicon–oxide system," *Chinese Physics B*, vol. 19, 2010, p. 067304.