Performance of InP/InGaAs Heterojunction Bipolar Transistors For 40Gb/s OEIC Applications

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Abstract

A high performance InP/InGaAs SHBT technology will be presented. InP SHBT is advantageous in terms of low-cost monolithic integration with photodiodes for high-speed optical receiver front-end applications. We will demonstrate that, through optimized CAD geometries, the fabricated HBTs showed uniform and improved device performance. Our best results show that an f_T of over 160 GHz and f_{max} of greater than 250 GHz are achieved on InP/InGaAs SHBTs with a collector thickness of 3000Å.

INTRODUCTION

OEICs have drawn much attention over the past few years as optical networking plays an ever-increasing role in next-generation high-speed communication systems. In >40Gb/s DWDM systems, InP-based HBTs have been identified as one of the viable contenders among currently available device technologies.

In addition to OEIC capabilities, InP HBTs have inherent material advantages in terms of faster electron transport properties as well as higher breakdown voltages when compared with SiGe technologies. These devices also allow the incorporation of higher indium composition materials than that in GaAs-based counterparts. The higher electron saturation velocity, low emitter/base turn-on voltage, and low surface recombination velocity make them the most promising device technologies for very high-speed optoelectronic circuit applications. Many device performance reports have been published on both InP SHBT and DHBTs. A most recent report shows that a maximum f_T of over 340 GHz can be achieved using submicron InP DHBTs with reasonable breakdown voltages [1]. The comparable high frequency performance combined with large-scale integration capability make InP HBTs a favorable device choice over InP HEMTs.

Despite their impressive device performance, InP technologies suffer from high material cost and a lack of mature manufacturing techniques. InP-based circuits have been mostly research interests [2-4]. Nevertheless, with the increasing demand in wideband high-speed optoelectronic systems, much interest has been focused on the manufacturability of InP technologies.

In this paper, we are in particularly interested in InP/InGaAs SHBT technology because it is advantageous in terms of low-cost monolithic integration with photodiodes for optical receiver front-end applications. We will demonstrate that, through the optimized CAD geometries, fabricated HBTs showed uniform and improved device performance. Our best results show that f_T of over 160 GHz and f_{max} of greater than 250 GHz were achieved on C-doped HBTs with base doping of 4E19 cm^{-3}.

DEVICE FABRICATION AND DESIGN ISSUES

To accommodate the monolithic integration of PINs and SHBTs without increasing fabrication complexity, PIN diodes are fabricated using the base, collector, and sub-collector layers in an SHBT structure. As collector thickness increases, the intrinsic layer thickness of the PIN increases and DC responsivity increases. However, the collector transit time of the corresponding SHBT increases, and transistor speed will decrease. Therefore, the collector

thickness should be optimized considering the trade-offs between HBT speed and PIN photodiode performance.

The baseline 2-inch InP HBT fabrication process is a 14-mask-layer process. It starts with the emitter metal deposition. The emitter metal serves as the emitter mesa etching mask, and then a thin layer of self-aligned base metal is deposited. After the collector mesa etching, a layer of collector metal is evaporated and the devices are isolated. The device etchings are done using selective wet-etching techniques. Isolated devices are then planarized and via holes are fabricated by RIE dry etching. Device interconnect is achieved through the overlap of vias with a metal1 contact layer. The NiCr resistor has a nominal sheet resistance of 50 Ω/□ and silicon nitride films are used for MIM capacitors as well as anti-reflection coatings for the PINs.

Self-aligned hexagonal-shaped emitters are used in both discrete device and circuit designs. Hexagonal emitter designs were originally proposed in submicron InP DHBT to achieve high f_T and f_{max} values [5]. With an optimized base geometry design, the base-emitter gap resistance, as well as the extrinsic base-collector capacitance, can be reduced improving device speed.

RESULTS AND DISCUSSIONS

The 2-inch InP HBT wafers are grown by MOCVD. The carbon-doped base has a concentration of ~1.7E19 cm^{-3} and the collector thickness is 5000Å. The emitter dimensions under study vary from 1.5×5 μm^2 to 3×10 μm^2 due to the photolithographic limitation of contact aligners. The devices are characterized using an HP4142B and an HP8510C (0.25-50 GHz) vector network analyzer for DC and S-parameter measurement. An on-wafer SOLT calibration is used to move the measurement reference planes past the pads, up to the feeds of the devices. The unit current gain frequency, f_T, and maximum frequency of oscillation, f_{max}, are obtained from the extrapolation of short-circuit gain (h_{21}) and unilateral power gain (U), respectively, to 0 dB, assuming a slope of -20 dB/decade.

Standard hexagonal 3×10-μm^2-emitter HBTs are evaluated on the fabricated wafer. A typical I-V curve is shown in Fig.1. The device has a turn-on offset voltage of 0.1 V and a BV_{ceo} of 4.8 V. The measured device results show that the average common-emitter current gain is 69 with a standard deviation of 5.9% across the 2-inch wafer. The average f_T and f_{max} are 110 GHz and 147 GHz with standard deviations of 1.7% and 3.2%, respectively. Figure 2 shows a histogram of the f_T distribution across a 2-inch wafer. The maximum f_T and f_{max} are obtained at a current density of 80 kA/cm^2 and V_{cb} = 0.25 V. Both f_T and f_{max} drop at higher current density due to the Kirk effect.

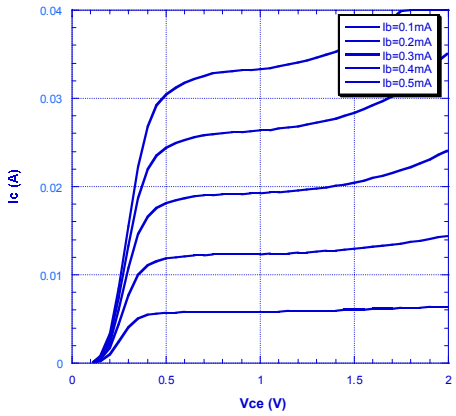

Fig. 1 A typical I-V curve for a hexagonal-3×10-μm^2-emitter HBT

Power consumption is a major concern in most circuit applications. Smaller HBT dimensions can simultaneously reduce the power consumption and enhance the RF performance if the device is properly scaled. SHBTs with emitter stripe width ranging from 1.5 to 3 μm are fabricated and tested. The dependences of f_T and f_{max} on the emitter stripe width are shown in Fig. 3. The stripe length is fixed at 5 μm. The results show that the f_T's decrease slightly as the emitter width shrinks. On the other hand, f_{max} increases significantly from 170 GHz to 190 GHz as the emitter width decreases from 3 μm to 1.5 μm.

The slight decrease in f_T is due to the non-scalable extrinsic base-to-collector capacitance ($C_{BC,ext}$), as the emitter resistance increases with the decrease in emitter stripe width. However, this effect is minimized in current designs and the change in f_T is small. In contrast, the significant improvement in f_{max} is a direct result of the decrease in the base spreading resistance under the emitter [6]. The base metal is designed in such a way that the base contact resistance variations due to alignment errors can be minimized. The results also indicate that the

device scaling is effective for maintaining high f_T and f_{max} with reduced power consumption.

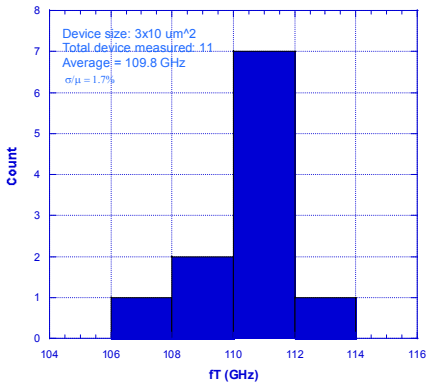

Fig. 2 A histogram of f_T on 3×10-μm^2 HBTs across a 2-inch wafer

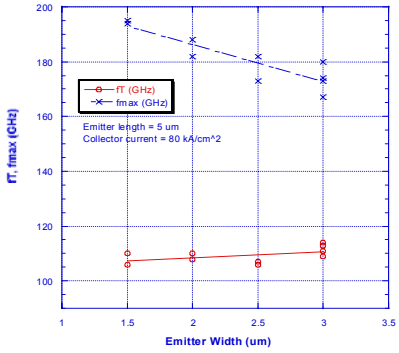

Fig. 3 f_T and f_{max} plot against the emitter stripe widths

It is believed that MOCVD systems suffer more severe hydrogen passivation problems than GSMBE in the growth of carbon-doped InGaAs p-type layer, and hence the base doping capability is limited. In the integrated PIN/SHBT structure, the reduction in the base resistance is one of the crucial issues for higher RF performance for both devices.

We processed GSMBE-grown C-doped SHBTs with a base doping of 4E19 cm^{-3} and a 3000Å-thick InGaAs collector. The measured results show that the common-emitter current gain is 41 (Fig. 4) and BVceo is 4.3 V for standard 3 × 10 μm^2 devices.

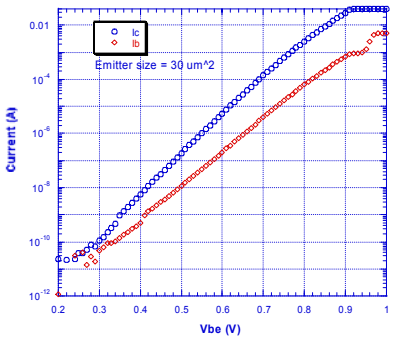

Fig. 4 A gummel plot of a SHBT with 4E19 cm^3 base doping

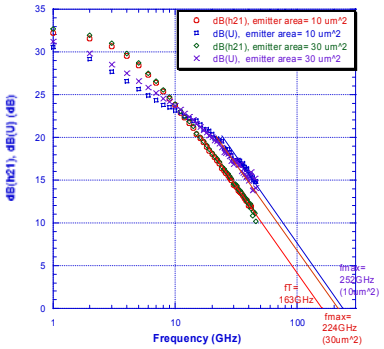

Fig. 5 A plot of $|h_{21}|$ and U for 3 × 10 μm^2 and 2 × 5 μm^2 SHBTs. The S-parameters are measured from 0.25 GHz to 40 GHz

Shown in Fig. 5 are plots of frequency dependent current gain $|h_{21}|$ and unilateral power gain |U| for 3×10 μm^2 and 2×5 μm^2 SHBTs. The devices are biased at V_{cb} = 0.25 V and I_c = 100 kA/cm^2. Both devices have f_T of >160 GHz. The f_{max} of 224 GHz is obtained in a 3 × 10 μm^2 device and a f_{max} of 252 GHz is achieved in a 2 × 5 μm^2 device. The high f_T and f_{max} is a result of reduced base resistance and shorter transit time in the collector region. Compared with the most recent submicron SHBT results from another group with a similar layer structure [7], our fabricated devices show comparable f_T and f_{max}. To our knowledge, this is among the best RF performance obtained in non-submicron InP/InGaAs SHBTs.

CONCLUSIONS

A high performance of SHBT technology has been presented. Through optimized CAD geometries, fabricated HBTs showed uniform and

improved device performance using a less stringent contact alignment technique. Our best results show that an f_T of over 160 GHz and f_{max} of greater than 250 GHz were achieved on 2×5 μm^2 SHBTs with a base doping of 4E19 cm^{-3}. With the availability of more sophisticated alignment tools, one can expect reduced power consumption and higher RF performance under this effective device scaling scheme.

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REFERENCES

[1] M. Ida, et al., " InP/InGaAs DHBTs with 341-GHz fT at high current density of over 800 kA/cm2," in Technical digest of 2001 IEEE International Electron Device Meetings, Dec. 2001, Washington D.C.

[2] M. Bitter, et al. " Monolithic InGaAs-InP pin/HBT 40Gb/s optical receiver module," IEEE Photonic Technology Letters, Vol. 12, no.1, Jan. 2000, pp. 74-76

[3] D. Huber, et al. " InP-InGaAs single HBT technology for photoreceiver OEIC's at 40Gb/s and beyond," IEEE J. of Lightwave Techno. Vol. 18, No.7, July 2000, pp. 992-1000

[4] M. Bitter, et al. " Monolithically integrated 40Gb/s InP/InGaAs PIN/HBT optical receiver module," Techncal Digest of 11thInternational Conf. on Indium Phosphide and Related Materials, 16-20 May, 1999, pp. 381-384

[5] S. Yamahata, et al. "Over-220-GHz-fT-and-fmax InP/InGaAs double-heterojunction bipolar transistors with a new hexagonal-shaped emitter," in Technical Digest of GaAs IC Symposium, 1995, pp. 163-166

[6] M. J. W. Rodwell, et al, "Submicron Scaling of HBTs," IEEE Trans. on Electron Devices, vol. 48, No. 11, Nov. 2001, pp. 2606-2624

[7] A. Fujihara, et al., " High-speed InP/InGaAs DHBTs with ballistic collector launcher structure," in Technical digest of 2001 IEEE International Electron Device Meetings, Dec. 2001, Washington D.C.

ACRONYMS

OEIC: Optoelectronic Integrated Circuits
DWDM: Dense Wavelength Division Multiplexing
HEMT: High Electron Mobility Transistors
SHBT: Single HBT
DHBT: Double HBT
RF: Radio Frequency
SOLT: Short-Open-Load-Through
CAD: Computer Aided Design
PIN: p-intrinsic-n
MOCVD: Metal-Organic Chemical Vapor Deposition
GSMBE: Gas-Source Molecular Beam Epitaxy
MIM: Metal-Insulator-Metal