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Experimental demonstration of pseudomorphic heterojunction bipolar transistors with cutoff frequencies above 600 GHz

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Pseudomorphic InP/InGaAs heterojunction bipolar transistors (PHBTs) using a compositionally graded collector (10% indium grading) and graded base (6% indium grading) to reduce the transit time of the device are reported. A 0.4×6 μm^2 HBT achieves excellent f_T values of 604 GHz (associated $f_{MAX}=246$ GHz) at a collector current density of 16.8 mA/μm^2, with a dc gain of 65 and a breakdown voltage of $BV_{CEO}=1.7$ V. © *2005 American Institute of Physics*.
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Following Bardeen's and Brattain's discovery of the transistor[1] and the identification of minority carrier injection and collection as the physical principle underlying transistor action, followed by Shockley's development of *p-n* junction theory and junction transistors,[2] the transistor and the development of integrated circuits[3,4] revolutionized the military and consumer electronic industry. The concept of a wide band-gap semiconductor emitter[5,6] has been used to achieve high minority carrier injection efficiency in a heterojunction bipolar transistor (HBT), with the InP material system demonstrating the fastest transistors, now operated at speeds (f_T) above 500 GHz.[7,8] Efforts to improve f_T are focusing on the reduction of electron transit time by vertically scaling the base and collector thicknesses at the cost of increasing base-collector parasitic capacitance as demonstrated in SiGe HBTs, as well as Types I and II InP DHBTs.[7–12] In this work, we design a compositionally graded collector (with a 10% indium mole fraction, from the subcollector to the base/collector interface) and graded base (with a 6% indium mole fraction from the base/collector interface to the base/emitter interface) in the HBT to reduce the transit time and improve operating current density, namely, a pseudomorphic InP/InGaAs HBT (PHBT). A compositionally graded InGaAs to InAs emitter cap was engineered to reduce emitter resistance and thus improve junction charging times. These band-gap engineering improvements demonstrate record speed performance, with f_T values of 604 GHz and illustrate the InP/InGaAs PHBT material system as a prime candidate for THz-bandwidth transistors.

The epitaxial structure for these devices was grown by molecular-beam epitaxy on semi-insulating InP substrates. The subcollector structure consists of a 250 nm heavily doped N^+ InP subcollector, a 50 nm $In_{0.53}Ga_{0.47}As$ layer, and a 10 nm strained $In_{0.63}Ga_{0.37}As$ contact layer silicon doped to 5×10^{19} cm^{-3}. The collector, lightly doped at 3×10^{16} cm^{-3} to suppress the Kirk effect, is then linearly graded over 62.5 nm from $In_{0.63}Ga_{0.37}As$ at the collector/subcollector interface, to $In_{0.53}Ga_{0.47}As$ (lattice matched) at the base/collector junction. The 20 nm carbon-doped base (8×10^{19} cm^{-3}, $R_{SB}=1350$ Ω/sq) is then graded 6% indium mole fraction to $In_{0.47}Ga_{0.53}As$ at the base/emitter junction. The emitter structure consist of a 35 nm InP emitter, a compositionally graded cap ($In_{0.53}Ga_{0.47}As$ to InAs), and a 10 nm InAs emitter cap, doped to 8×10^{19} cm^{-3}. An energy-band diagram of this HBT is shown in Fig. 1. An InAs emitter cap was employed, as it has been shown to effectively reduce the emitter contact resistance R_{EE} by 50% for small-area emitters.[13] Due to the large parasitic base-to-collector capacitance associated with the vertically scaled epitaxial structure, small emitter areas are required to allow lateral device scaling to maintain respectable unity power gain (f_{MAX}) frequencies. Replacing InGaAs with InP in the bulk of the subcollector and leaving only a thin InGaAs contact layer for low resistance ohmic contacts results in a 15% reduction in the total thermal resistance of the device when compared with a conventional lattice-matched InGaAs subcollector.

HBT devices were fabricated using an all wet-etch process detailed elsewhere,[14] with emitters designed to have a width of 0.5 μm after electrode evaporation. Corresponding physical emitter/base junction widths are 0.4 μm after the emitter etch, and emitter lengths range from 1 μm to 6 μm. The devices were passivated in benzocyclobutene. A scanning-electron micrograph of a device before passivation is shown in Fig. 2.

The common-emitter current-voltage curves exhibit excellent dc characteristics, and are shown in Fig. 3 for a 0.4

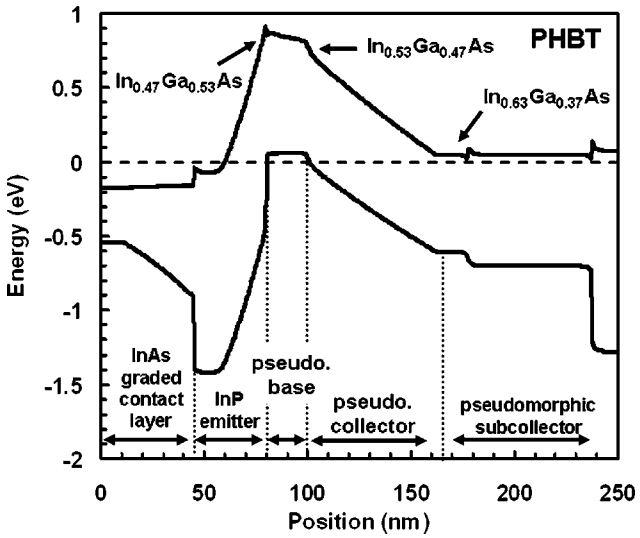

FIG. 1. Energy band diagram for PHBT, displaying a 16% indium grading over the base and collector layers.

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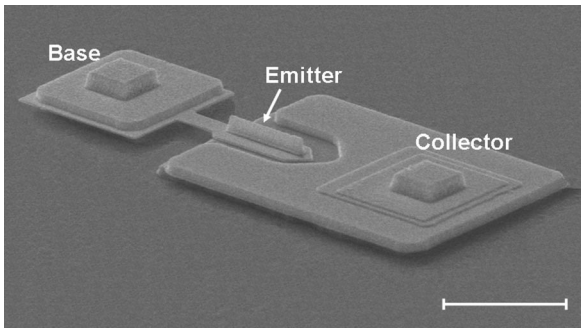

FIG. 2. Scanning electron microscopy of a fabricated HBT before passivation. Scale bar represents 5 μm.

$\times 6\ \mu m^2$ emitter device. The knee voltage is less than 0.6 V at current densities in excess of 18 $mA/\mu m^2$. The output conductance is very low, exhibiting superior output characteristics compared to pseudomorphic high-electron mobility transistors with similar rf performance.[15] The common emitter breakdown voltage, defined when the current density reaches 100 A/cm^2, is $BV_{CEO}=1.7$ V. Gummel characteristics exhibit peak dc gain (β) of 65 and idealities of 1.1 and 1.62 for the collector and base junctions, respectively.

Microwave performance at room temperature was characterized from 0.5 GHz to 50 GHz using an HP8510C network analyzer, with calibration performed using on-wafer short, open, load, and through standards. The measurement of a through standard after calibration showed a deviation of less than ±0.015 dB, assisting in the verification in the calibration accuracy. The extrapolations of h_{21}, U, and maximum stable gain/maximum available gain are shown in Fig. 4(a) for a $0.4\times 6\ \mu m^2$ device, operating at a collector current density, J_C, of 16.82 $mA/\mu m^2$. The cutoff frequencies are extrapolated using a least-squares fit of a −20 dB/decade line, and show a peak f_T of 604 GHz and associated f_{MAX} of 246 GHz. Thermal resistance was calculated using an emitter thermal-shunt model,[16] with a $0.4\times 6\ \mu m^2$ device exhibiting a normalized thermal resistance of 9.6 °C μm^2/mW, corresponding to a temperature increase of 148 °C and a power dissipation of 36 mW when biased at peak f_T. Figure 4(b) shows the device cutoff frequency scaling trend for 0.4 μm HBTs versus emitter length, with f_T remaining relatively flat

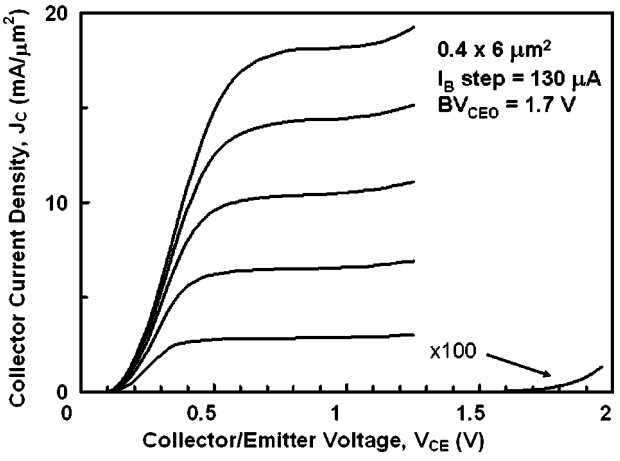

FIG. 3. Common-emitter curves for a $0.4\times 6\ \mu m^2$ HBT. Measurements are taken at room temperature, and indicate BV_{CEO} values of 1.7 V. Current density at peak $f_T=16.82\ mA/\mu m^2$ at a $V_{CE}=0.907$ V.

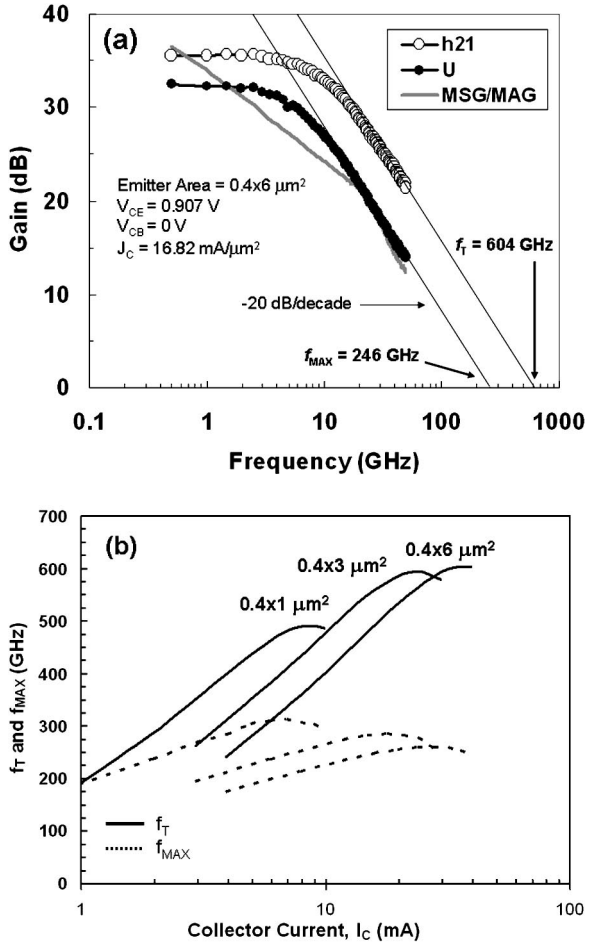

FIG. 4. (a) h_{21}, U, and MSG/MAG plotted versus frequency for $0.4\times 6\ \mu m^2$ HBT. Room-temperature measurements exhibit $f_T=604$ GHz and $f_{MAX}=246$ GHz, obtained from a −20 db/decade extrapolation of a least-squares fit, and (b) f_T (solid) and f_{MAX} (dashed) versus I_C for 0.4 μm emitter widths and varying lengths.

for emitter lengths above 3 μm and f_{MAX} monotonically increasing for shorter emitters.

Equivalent circuit parameters were extracted/optimized from measured S parameters and device geometry for a $0.4\times 6\ \mu m^2$ HBT, where $r_E=kT/I_C$ is the dynamic emitter resistance (0.8 Ω), R_{EE} is the emitter contact resistance (2.1 Ω), R_C is the collector resistance (0.9 Ω), C_{JE} is the emitter junction capacitance (54 fF), and C_{BC} is the total base-collector capacitance (21.83 fF). The calculated delay times are shown in the bar graph of Fig. 5. The current cutoff frequency, f_T, for an HBT is given in Eq. (1), where τ_B and τ_C represent the base and collector transit times,

$$\frac{1}{2\pi f_T}=\tau_{EC}=\tau_B+\tau_C+\tau_E+\tau_{CC}, \tag{1}$$

respectively. The junction charging times consist of the emitter charging time, defined as $\tau_E=r_E*C_{JE}$, and the collector charging time, $\tau_{CC}=(r_E+R_{EE}+R_C)*C_{BC}$. The forward delay τ_F, obtained from extrapolating the total delay, τ_{EC} versus $1/I_C$ to $1/I_C=0\ A^{-1}$, is measured to be 204 fs, indicating a base and collector transit time of $\tau_B+\tau_C=137$ fs. Comparing a similar HBT with a 75 nm collector and 25 nm base operating with $f_T=509$ GHz,[7] a 16% reduction in total transit time τ_{EC} is observed, 7% of which is due to a reduction in the collector transit time, 5% from the base transit time, and

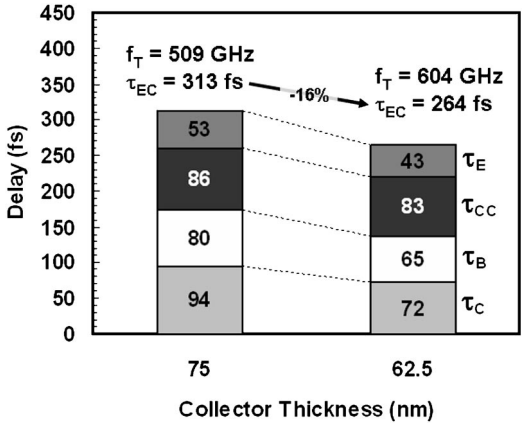

FIG. 5. Delay terms obtained from extracted device parameters showing effect of scaling between a 62.5 nm collector device (this work), and a 75 nm collector HBT. A reduction of 16% is observed in the total delay time.

3% from the emitter charging time. The collector charging time is observed to have a negligible change from the 75 nm collector device (83 fs versus 86 fs for the 62.5 and 75 nm collectors, respectively), despite the thinner collector thickness; the increase in C_{BC} from the thinner collector is offset by the increase in the operating current density, effectively keeping the charging time constant. The decrease in emitter charging time ($\Delta\tau_E = 10$ fs) is due to the low dynamic emitter resistance, also a benefit from the high current density operation. The transit time compromises roughly half of the total device delay, indicating parasitic capacitances (C_{BC} primarily) have been adequately controlled through layout and processing techniques. The benefit obtained through the use of the 10% compositionally graded collector is estimated to result in an 11% reduction in collector transit time compared with a lattice-matched collector of the same thickness, resulting in an average velocity in excess of 4.3×10^7 cm/s through the collector. The boost in the drift velocity is due to faster drift transport in the graded indium composition of InGaAs collector.

In conclusion, the benefit of vertical scaling is clearly demonstrated through the drastic reduction in transit time by thinning the base and collector layers, while nullifying the effect of the charging capacitances through high current density operation. Pseudomorphic grading in the collector and base allows the transit time to be reduced over a nongraded structure. These results solidify the HBT device structure, as well as the InP/InGaAs material system, as a leading candidate for THz-bandwidth devices.

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[1]J. Bardeen and W. H. Brattain, Phys. Rev. **74**, 230 (1948).
[2]W. Shockley, Bell Syst. Tech. J. **28**, 435 (1949).
[3]J. S. Kilby, U.S. Patent No. 3,138,743 (23 June 1964).
[4]R. N. Noyce, U.S. Patent No. 2,981,877 (25 April 1961).
[5]W. Shockley, U.S. Patent No. 2,569,347 (25 September 1951).
[6]H. Kroemer, Proc. IRE **45**, 1535 (1957).
[7]W. Hafez, J. W. Lai, and M. Feng, Electron. Lett. **39**, 1475 (2003).
[8]M. Feng, W. Hafez, and J. W. Lai, Indium Phosphide and Related Materials Conference Kagoshima, Japan, 31 May-4 June 2004 (IEEE, New York, 2004), pp. 653–658.
[9]J.-S. Rieh, B. Jagannathan, H. Chen, K. Schonenberg, S.-J. Jeng, M. Khater, D. Ahlgren, G. Freeman, and S. Subbanna, Indium Phosphide and Related Materials Conference, Santa Barbara, California, 12-16 May 2003 (IEEE, New York, 2003), pp. 374–377.
[10]M. Ida, K. Kurishima, K. Ishii, and N. Watanabe, Proceedings GaAs IC Symposium, 2003. 25th Annual Technical Digest (2003), pp. 211–214.
[11]B. F. Chu-Kung and M. Feng, Electron. Lett. **40**, 1305 (2004).
[12]C. Bolognesi, M. W. Dvorak, N. Matine, O. J. Pitts, and S. P. Watkins, Jpn. J. Appl. Phys., Part 1 **41**, 1131 (2002).
[13]W. Hafez and M. Feng, IEE Electron. Lett. **40**(18), 1151 (2004).
[14]W. Hafez, J. W. Lai, and M. Feng, IEEE Electron Device Lett. **24**(5), 292–294 (2003).
[15]Y. Yamashita, A. Endoh, K. Shinohara, K. Hikosaka, T. Matsui, S. Hiyamizu, and T. Mimura, IEEE Electron Device Lett. **23**, 573 (2002).
[16]W. Hafez, F. Dixon, and M. Feng, 2004 International Conference on Compound Semiconductor Manufacturing Technology, Miami Beach, Florida, 3-6 May 2004 (GaAs MANTECH, Inc., 2004), pp. 269–272.