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LETTER

Floating-bulk transistors: An alternative design technique for CMOS low-voltage analog circuits

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Abstract This letter details a novel floating-bulk transistor technique for low-voltage design. The approach is derived from two previous well-known techniques: bulk-driven and quasi floating-gate. The floating-bulk technique uses an input capacitive coupling through a floating bulk of a PMOS allowing modulation of the drain current. A fabricated common-source amplifier was tested on CMOS 0.5 µm technology and the feasibility of the proposal was demonstrated.

Keywords: bulk-driven, floating-gate, quasi floating-gate, CMOS, low-voltage amplifier

Classification: Integrated circuits

1. Introduction

Nowadays, the shrinking supply voltages of modern CMOS technologies lead analog designers to use novel techniques in order to preserve circuit functionality under low-voltage conditions. One such technique is *bulk-driven* MOSFET, introduced by Blalock *et al.* [1], where a contact in the N-well bulk of a PMOS is used as an input (Fig. 1(a)). In this case the gate voltage is used only for biasing purposes or "turning on" the transistor. Moreover, the bulk as an input can avoid a V_{Th} requirement in the signal path facilitating low-voltage operation. However, the voltage swing to the bulk must be small to prevent high currents from the forward biasing of the P^+/N_{well} source junction. Another useful technique, known as *floating gate* [2], has evolved to *quasi-floating gate* [3] (Fig. 1(b)). This technique deals with the problem of the initial trapped charge, commonly present and difficult to remove in real floating gate circuits. Quasi-floating gate requires a high value resistor, R_{Large}, typically implemented by a single transistor connected to a DC biasing voltage and a capacitor, C_i, connected to the AC input voltage in order to work properly. Low voltage analog circuits have been widely improved by using these Bulk Driven [4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16] and Floating Gate [17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30] techniques, and from them we derive the new technique presented in following section.

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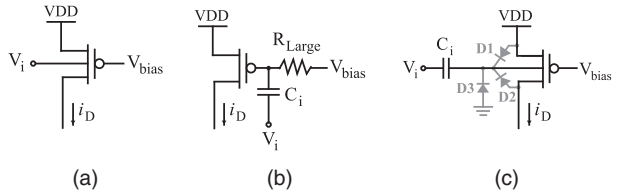

Fig. 1. Techniques for low-voltage CMOS design: (a) Bulk-driven PMOS. (b) Quasi-floating gate PMOS. (c) Floating-bulk PMOS with parasitic PN-junctions represented with diodes.

2. Floating-bulk transistor

A floating-bulk transistor is a PMOS built inside an N-well bulk, where this bulk terminal is left floating, only connected to an input capacitor, and the gate terminal of the PMOS can be used for biasing purposes (Fig. 1(c)). For DC analysis of bulk potential, three PN-junctions must be considered: source to N-well, drain to N-well, and P-substrate to N-well. These junctions are schematically shown as the diodes D1, D2 and D3, respectively, in Fig. 1(c). Considering that source terminal is typically connected to a higher voltage than the drain is, and the P-substrate is connected to *VSS*, this means that D1 is directly biased, while D2 and D3 are reverse biased. Let us call I_{S1}, I_{S2}, and I_{S3} the inverse saturation currents of diodes D1, D2 and D3, respectively. Then, by Kirchhoff's current law, we have

$$I_{S1}e^{(V_S-V_B)/\phi_T} = I_{S2} + I_{S3}, \tag{1}$$

where V_S and V_B are source voltage and bulk voltage, respectively, and $\phi_T = kT/q$ is the thermal voltage, where q is the electron charge; k, the Boltzmann constant; and T, absolute temperature. The previous equation establishes that the source-bulk junction must provide in forward biasing the total current of the other two junctions in reverse biasing. Due to the exponential growth of the latter current, it follows that the difference $V_S - V_B$ has to be small (some tens of millivolts). For example, with 78 mV of difference, the left member of Equation (1) yields a current of $20I_{S1}$ (with $\phi_T \approx 26$ mV at room temp.). For AC analysis, the input capacitor connected to the floating bulk and the source-bulk diode produces a clamping circuit which adds a DC component of almost VDD to input V_i preserving the voltage swing. Therefore, the bulk potential can be modulated by the input and consequently the drain current of PMOS.

3. Experimental results

A floating-bulk common source amplifier was designed in order to demonstrate the functionality of the technique; the chip was fabricated using CMOS 0.5 µm technology (Fig. 2(a)). PMOS threshold voltage $V_{Th,P}$ was −0.98 V and NMOS $V_{Th,N}$ was 0.7 V. The aspect ratio of transistor M1 was $W/L = 6\,\mu m/1.2\,\mu m$, and the input coupling capacitor C_i was *poly*1/*poly*2 with 126 fF. A microphotograph of the circuit is shown in Fig. 2(b). The output measurement in the time domain with a voltage input of 200 mV_{pp} at 5 kHz is depicted in Fig. 2(c). For this test VDD = 1.5 V; the bias current $I_b = 15\,\mu A$; $V_{bias} = 0.16$ V and $C_L = 95$ pF.

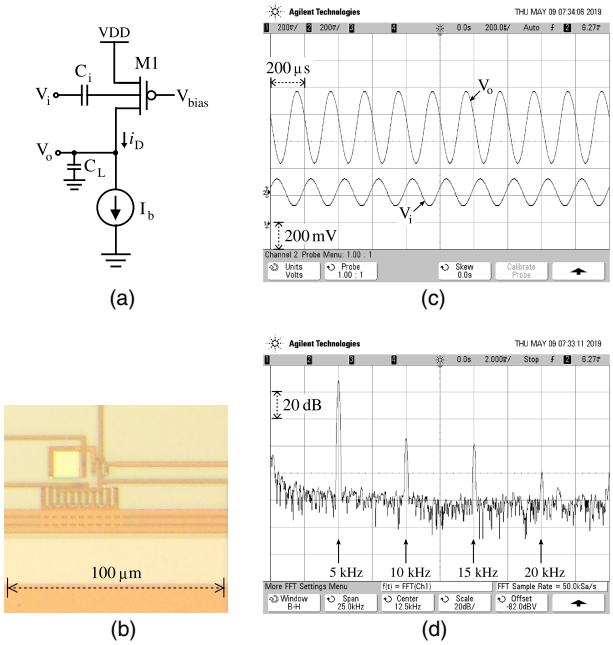

Fig. 2. Floating-bulk amplifier: (a) Electrical diagram. (b) Microphotograph of the fabricated circuit. (c) Time domain measurement showing an AC gain close to −3. (d) FFT of the output signal.

In spite of the small transconductance of the floating-bulk technique, the amplifier presents a gain of close to −3; the measurement demonstrates the feasibility of the technique using a very small input capacitor. (In the next section we explore in greater depth the dependence of the gain with respect to C_i and other parameters of the circuit.) The FFT of the output signal is depicted in Fig. 2(d) showing good linearity with a second harmonic 40 dB below the fundamental. Thus, a total harmonic distortion (THD) below 1% was obtained.

4. Low-frequency gain

To obtain an analytical expression for the gain of circuit in Fig. 2(a), we call R_o the parallel between the output resistance of M1 and the output resistance of the non-ideal current source I_b; C_{fb} is the feedback capacitance between the drain and bulk of M1, and C_{par} is the sum of all the parasitic capacitances connected to the N-well bulk of M1, including C_{fb}. Thus, the gain of the amplifier is given by

$$\frac{v_o}{v_i} = -\frac{g_{mb}\,R_o\dfrac{C_i}{C_i + C_{par}}}{1 + g_{mb}\,R_o\dfrac{C_{fb}}{C_i + C_{par}}}. \tag{2}$$

Note that this expression is the closed-loop transfer function of the amplifier for low frequencies. It also can be expressed in the form $v_o/v_i = -A_o/(1 + A_o\beta)$, where $A_o = g_{mb}R_oC_i/(C_i + C_{par})$ is the open-loop gain, and $\beta = C_{fb}/C_i$ is the feedback factor of the circuit. The feedback effect can be negligible if C_{fb} is maintained 100 times smaller than $C_i + C_{par}$.

5. Simulation of an ultra low-voltage amplifier

The clamping effect on the bulk of the PMOS can be used also by the NMOS counterpart. In this case, the produced offset brings an important voltage overdrive beyond the supply rail to the NMOS. The amplifier of Fig. 3(a) works as follows: the circuit voltage supply is VDD = 0.85 V; therefore M2 works in subthreshold bringing a bias current of 16 nA. The M2 size is $W/L = 6\,\mu m/1.5\,\mu m$. For the NMOS in this case, $V_{GS} \approx$ VDD; thus, M1 must have a small aspect ratio, in this case $W/L = 3\,\mu m/6\,\mu m$, in order to bring a small bias current and achieve an output V_o operating point close to $\frac{1}{2}$VDD.

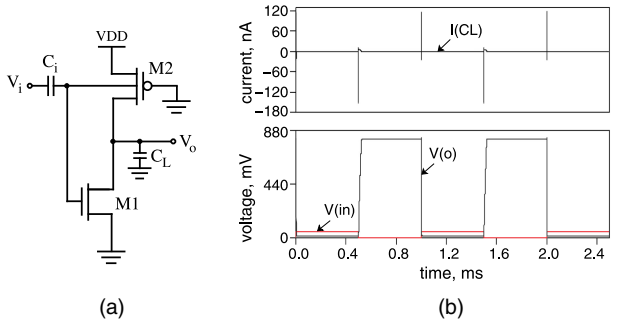

Fig. 3. Ultra low-voltage amplifier: (a) Electrical diagram. (b) Time-domain Spice simulations.

A time-domain simulation using Spice is depicted in Fig. 3(b), using a square input signal with an amplitude of 50 mV and a frequency of 1 kHz. In this case, $C_i = 1$ pF and $C_L = 0.1$ pF. As the input signal goes high, M2 is turned off via the bulk potential and M1 is turned on. In this sense, the load capacitor is charged and discharged with currents little larger than the bias current achieving class AB operation.

6. Two-stage ultra low-power amplifier

The floating-bulk technique was also implemented in a two-stage differential amplifier as shown in Fig. 4(a). It consists of a PMOS differential pair as input stage formed by floating-bulk transistors M1 and M2 and a second gain stage of the same type provided by M6. Transistor sizes W/L (in µm/µm) are M1 = M2 = 30/1.5, M3 = M4 = 300/1.5, M5 = M6 = 12/1.5, and M7 = 12/1.5. Capacitors are $C_{i1} = C_{i2} = C_{i3} = 1$ pF, $C_c = 3$ pF, and $C_L = 5$ pF,

with a supply voltage of VDD = 0.9 V. Similar to the previous example, M5 provides a biasing current of 180 nA; M7 was biased to sink 200 nA. This results in a total static power dissipation of 342 nW. Following the same analysis as before, the overall open-loop gain is given by $A_o = A_{v1}A_{v2} = (g_{mb1,2}R_{o1})(g_{mb6}R_{o2})$, where $g_{mb1,2}$ and g_{mb6} are the bulk transconductances in M1–M2 and M6, respectively. $R_{o1} = r_{o2} \parallel r_{o4}$ and $R_{o2} = r_{o6} \parallel r_{o7}$ are the output resistances of the first and second gain stages, respectively. The circuit was simulated using Spectre and the results of an AC analysis are shown in Fig. 4(b). The simulation yields an open-loop gain of $A_o = 45$ dB, a dominant pole at $\omega_{po} = 1/R_{o1}C_c(1 - A_{v2}) = 130$ Hz, a Gain Bandwidth product of GB $= A_o\omega_{po} \approx 21$ kHz, and a phase margin of 37 degrees. Observe that, due to the extremely low power consumption, the speed of operation is limited compared to other topologies. However, it is well suited for other applications such as biomedical implementations like, for instance, body implants, were ultra-low power consumption is essential and operational frequency lays within the operation of the amplifier.

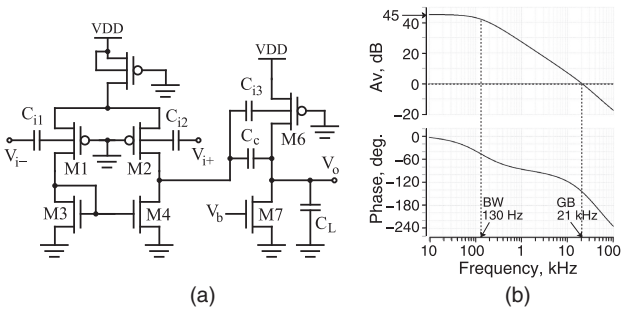

Fig. 4. Two-stage ultra-low power amplifier: (a) Electrical diagram. (b) Frequency-domain Spectre simulations.

7. Discussion

The floating-bulk technique can be seen as occupying a position between the bulk-driven principle and the quasi floating-gate technique. However, unlike with the bulk-driven principle, here the input capacitor prevents all the P^+/N_{well} junctions from strong forward biasing; otherwise, high currents can increase power consumption considerably. Compared to quasi-floating gate, floating-bulk does not need a high-value resistor; nevertheless, the transconductance in the case of floating-bulk will be always less than with quasi-floating gate. The floating-bulk technique can be useful for achieving many improvements in the analog domain, such as low voltage, and class AB, among others.

8. Conclusions

A principle denominated *floating-bulk transistor* was presented. The idea can be considered a useful technique for improving the performance of analog circuits; these improvements are commonly achieved using bulk-driven and quasi-floating gate techniques.

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