3-GHz Silicon Photodiodes Integrated in a 0.18-μm CMOS Technology

Berkehan Ciftcioglu, Jie Zhang, Lin Zhang, John R. Marciante, Jonathan D. Zuegel, Roman Sobolewski, and Hui Wu

***Abstract*—A new PIN photodiode (PD) structure with deep n-well (DNW) fabricated in an epitaxial substrate complementary metal–oxide–semiconductor (epi-CMOS) process is presented. The DNW buried inside the epitaxial layer intensifies the electric field deep inside the epi-layer significantly, and helps the electrons generated inside the epi-layer to drift faster to the cathode. Therefore, this new structure reduces the carrier transit time and enhances the PD bandwidth. A PD with an area of 70×70 μm^2 fabricated in a 0.18-μm epi-CMOS achieves 3-dB bandwidth of 3.1 GHz in the small signal and 2.6 GHz in the large signal, both with a 15-V bias voltage and 850-nm optical illumination. The responsivity is measured 0.14 A/W, corresponding to a quantum efficiency of 20%, at low bias. The responsivity increases to 0.4 A/W or 58% quantum efficiency at 16.2-V bias in the avalanche mode.**

***Index Terms*—Integrated optoelectronics, optoelectronic devices, photodiodes (PDs), p-i-n photodiodes (PDs), semiconductor devices.**

I. Introduction

SHORT-DISTANCE optical communication systems such as fiber channel, gigabit ethernet, and emerging optical interconnects require efficient, high-speed detection of optical signals to achieve the high data rates needed, and typically employ discrete PIN photodiodes (PDs) built in III–V compound semiconductors. Recently, integrated complementary metal–oxide–semiconductor (CMOS) PDs have become increasingly attractive at near-infrared wavelengths (e.g., 850 nm) because monolithic integration of PDs with CMOS circuitry not only removes the bottleneck of sensitivity and bandwidth degradation at the interface between the PD and front-end circuitry [1], [2], but also enables low-cost, fully integrated optical receivers and systems-on-chip. Unfortunately, CMOS PDs are severely limited by the low optical absorption coefficient of Si at near-infrared wavelengths, which leads to a small responsivity-bandwidth product. Specifically, the PD bandwidth is limited by both the transit time of photogenerated carriers, and the diffusion current in the thick undepleted Si substrate. The latter is due to the fact that only the Si surface layer in a CMOS PD is depleted, which is not thick enough to absorb all photons. Using a thinner Si layer, by either changing the substrate to silicon-on-insulator [3], [4] or building PDs on polysilicon layers above the CMOS substrate [5], solves the substrate diffusion current problem, but severely limits the responsivity. For PDs fabricated in standard CMOS with a bulk Si substrate, the substrate diffusion carriers can be suppressed by using another PN junction (e.g., between an n-well and the substrate in [6]) to isolate the substrate from the photogeneration region on the surface, which effectively creates a thin active Si layer for the PD. Another method was to construct a differential PD with alternate illuminated/dark patterns and hence subtract the diffusive carrier contribution from the total photogeneration current [7], [8]. Note that the area of the photogeneration region was effectively reduced by half. The bandwidth improvement in both cases, however, was achieved by sacrificing responsivity due to thinner and/or smaller photogeneration regions. On the other hand, the responsivity of high-speed CMOS PD can be improved by enlarging the depleted photogeneration region using deep trenches [9] or wells [10]. These approaches, however, either require special process steps, or limit further bandwidth improvement due to the longer carrier transit time.

In this letter, we present a new integrated CMOS PD structure using a readily available layer, deep n-well (DNW), to enhance the drift time of the carriers in the depletion region and hence improving the PD bandwidth without sacrificing responsivity. This new structure is fully compatible with standard CMOS processes with an epitaxial substrate.

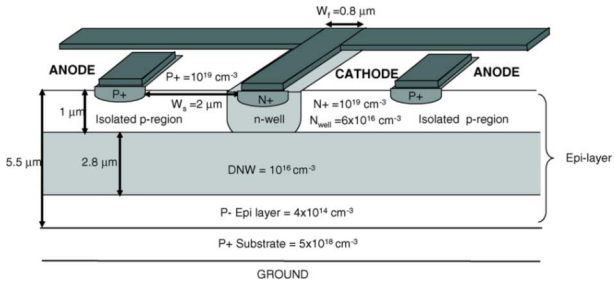

Fig. 1. Cross section of a PIN PD with DNW in an epi-CMOS process, showing one finger. The output is taken from cathode. Doping concentration numbers are approximate average values.

Manuscript received June 28, 2008; revised September 08, 2008. First published October 31, 2008; current version published December 12, 2008. This work was supported by the U.S. DOE Office of Inertial Confinement Fusion under Cooperative Agreement DE-FC52-08NA28302, by the University of Rochester, and by the New York State Energy Research and Development Authority. The support of DOE does not constitute an endorsement by DOE of the views expressed in this article.

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Digital Object Identifier 10.1109/LPT.2008.2006404

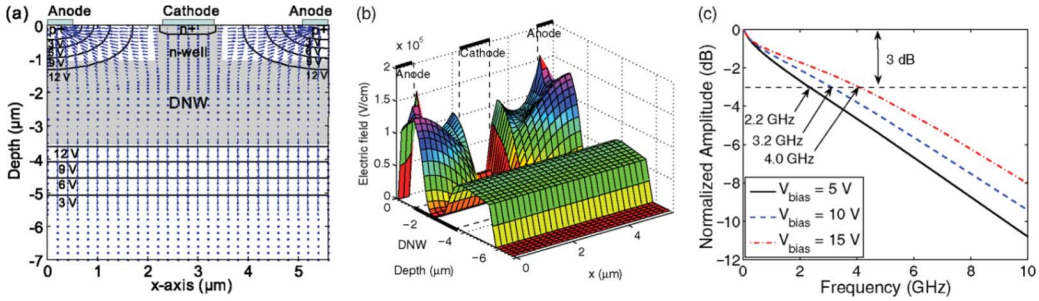

Fig. 2. (a) Simulated potential contours and electric field vectors as well as (b) electric field magnitude inside the active region of the $70 \times 70\ \mu\text{m}^2$, 2-$\mu$m finger spacing PD at 15-V bias. (c) Simulated small-signal frequency response of this PD at different bias voltages.

II. DNW PD in Epi-CMOS

In an epitaxial substrate CMOS (epi-CMOS) process, a lightly doped p-type epitaxial layer (epi-layer) is grown on top of a heavily doped p-type substrate. Because of its larger thickness and lower doping, the epi-layer is better suited to serve as the intrinsic region in a PIN PD [11], as compared to the n-well typically used in a PIN PD on a bulk CMOS substrate [6]. Further, the heavily doped substrate (below the epi-layer) in epi-CMOS enhances recombination of the photogenerated carriers before they reach the depletion region. Hence the diffusive carriers contribute less to the total PD current, and the PD bandwidth increases [13], [14].

Recently, a n-type layer buried inside the epi-layer, DNW, has been introduced to epi-CMOS technologies to improve transistor isolation and reduce substrate noise coupling in mixed-signal and RF circuits [12]. In this work, we utilize DNW to construct a new PIN PD structure. As shown in Fig. 1, this structure is based on a lateral PIN PD in epi-CMOS [11], with the additional DNW layer connected to the n-wells (cathode). DNW separates the active region into two PN junctions: one between n-well/DNW and the now isolated epi-layer on the surface, and the other between DNW and the lower part of the epi-layer and P+ substrate below. Compared to the case without DNW, the upper PN junction is now a hybrid lateral-vertical PIN structure, and the lower one is new. Both measures intensify the electric field deep inside the epi-layer significantly even at lower bias voltages. Therefore, this new PIN structure enhances the PD bandwidth, and/or reduces the bias voltage needed for high-speed operation.

It is noteworthy that this new structure is largely independent of CMOS technology scaling since it does not rely on the thickness or doping concentration of any surface regions such as n-well or N+/P+ source/drain, given that the epi-layer thickness and doping concentration will remain constant. Particularly, a thinner DNW layer with higher doping concentration will improve the PD bandwidth while maintaining the responsivity.

Using a device simulator DAVINCI, several prototype PDs with the new structure were designed and characterized. Each PD has an area of $70 \times 70\ \mu\text{m}^2$, and the best performance one reported here has a finger spacing of 2 μm, which is a good trade-off between the parasitic capacitance and carrier drift time. Fig. 2(a) and (b) shows the potential and electric field distribution in the active region. The two PN junctions and their electric field enhancement can be clearly seen. The simulation results showed that the 3-dB bandwidth of the PD was 4 GHz at 15-V bias, and 2.2 GHz at 5 V [Fig. 2(c)]. The responsivity was 0.24 A/W up to 10 V, and increased to 0.25 A/W at 15 V.

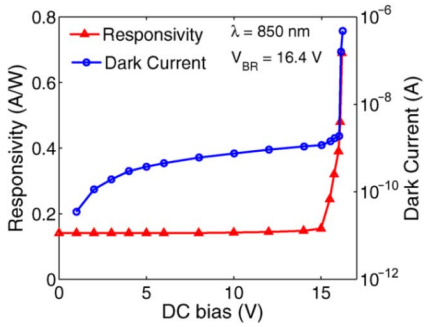

Fig. 3. Measured responsivity and dark current of the prototype PD at different bias voltages.

III. Test Setup and Measurement Results

The prototype PD was fabricated in a commercial 0.18-μm epi-CMOS process. To facilitate the dark current measurement, a dummy duplicate with its active region covered with metal was added on the test chip. Three types of measurements were performed to characterize its dc response (responsivity and dark current), impulse response, and small-signal frequency response. In these measurements, the test chip was glued to a custom printed circuit board (PCB) using conducting epoxy, and hence the chip backside was connected to ground. The PD output ground-signal-ground pad was wirebonded to a 50-Ω transmission line on the PCB and connected to instruments via RF connectors located at the edge of the PCB.

In dc measurements, a high-speed 10-Gb/s vertical-cavity surface-emitting laser (VCSEL), (Finisar HFE8004-103), with an optical power of 2 mW, was used as the light source at 850 nm. As shown in Fig. 3, the responsivity for the PD was 0.141 A/W (20% quantum efficiency) at low bias up to 14 V. This value increased to 0.152 A/W at 15 V, 0.4 A/W at 16.2 V, and 0.7 A/W at 16.4 V. The dark current was below 1 nA up to 13 V. The breakdown voltage of the PD was measured as 16.4 V, when the dark current reached 1 μA. A constant 16.2-V bias was applied on the PD for a week, and no aging effects have been observed.

In impulse response measurements, we used a tunable mode-locked Ti:Al_2O_3 femtosecond pulsed laser, operating between 700 and 1000 nm, as the light source with a repetition rate of 76 MHz. The pulsewidth was 100 fs, and could be treated as an impulse for the PD measurements. Time-domain waveforms of

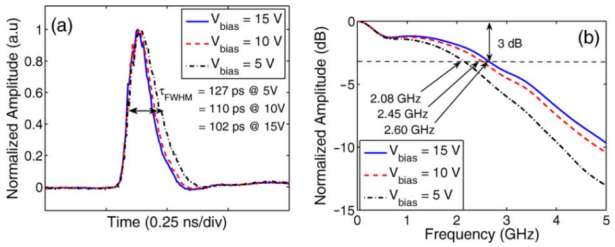

Fig. 4. (a) Impulse response and (b) its spectrum by DFT of the prototype PD. Measurements were done under 850-nm illumination for different bias conditions.

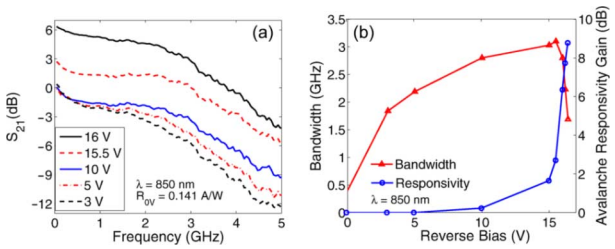

Fig. 5. (a) Measured small-signal frequency response of the prototype PD at different bias. (b) 3-dB bandwidth and gain variation with respect to bias.

the PD were measured at 850 nm and different bias voltages, using a 20-GHz oscilloscope. The incident laser power on the PD was 0.27 mW, which corresponded to 3.55-pJ optical energy per pulse. Our impulse response results were, subsequently, converted to the frequency response by means of the discrete Fourier transform (DFT).

Fig. 4 shows the measured impulse [Fig. 4(a)] and DFT-converted frequency [Fig. 4(b)] responses of our PD at different bias. The pulsewidths were 127 and 102 ps at 5 and 15 V, respectively. The rise time was almost constant (57 ps) between 5 and 15 V, since it was mainly limited by the instantaneous charge injection and the instrument bandwidth. The fall time decreased from 147 ps at 5 V to 117 ps at 15 V. The DFT results show that the PD had a large-signal bandwidth above 2 GHz at 5-V bias, and reached 2.6 GHz when increasing the bias voltage to 15 V.

In frequency response measurements, the aforementioned 10-Gb/s VCSEL was connected to one port and the PD to the second port of a 50-GHz vector network analyzer. As shown in Fig. 5, the PD achieved 3-dB bandwidth of 1.87 GHz at 3 V, 2.19 GHz at 5 V, 2.8 GHz at 10 V, and 3.1 GHz at 15 V. As the bias was further increased to 16 V, the 3-dB bandwidth dropped to 2.8 GHz while responsivity increased by 6-dB due to avalanche mode operation. Note that there still was 1.5-dB low-frequency roll-off due to the diffusive substrate carriers, which can be easily compensated by the receiver electronics.

The extrinsic capacitance of the PD was measured to be 0.83 pF at 5 V, 0.73 pF at 10 V, and 0.7 pF at 15 V. The corresponding RC time constant, calculated by multiplying the extrinsic capacitance at 15 V with the 50-Ω port impedance was 35 ps, which translated into a 3-dB bandwidth of 4.48 GHz. This limitation can be removed by further shrinking the PD area, e.g., to 50×50 μm^2, close to the dimensions of a multimode fiber.

IV. Conclusion

We conclude that the proposed PD with DNW, combining the features of vertical and lateral PIN devices, enhances the electric field inside the epi-layer and increases the drift speed of electrons, even at lower bias voltages. Therefore, it can achieve large bandwidth without sacrificing responsivity. Our prototype PD with an area of 70×70 μm^2 achieved small-signal bandwidth of 3.1 GHz and large-signal bandwidth of 2.6 GHz, both at 15-V bias and under 850-nm illumination. At 5-V bias, we measured over 2-GHz bandwidth. Our PD's responsivity was 0.14 A/W at low bias and more than 0.4 A/W at 16.2 V. The dark current values were kept at $\sim$1-nA level at 15-V. PDs with such parameters can easily find applications in fully integrated high-speed photonic integrated circuits.

Acknowledgment

The authors would like to thank B. Chatterjee, A. Bahai, P. Holloway, M. Bohsali, J. Yu, A. Shah, V. Abellera, P. Misich, and J. Wan of National Semiconductor for their support in chip fabrication. They also thank X. Li for her help in the optical test setup.

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