An Accurate Photodiode Model for DC and High Frequency SPICE Circuit Simulation

T. N. Swe and K. S. Yeo

Nanyang Technological University, School of Electrical and Electronic Engineering
Nanyang Avenue, Singapore 639798, etnswe@ntu.edu.sg

ABSTRACT

An accurate photodiode model for DC as well as high frequency SPICE circuit simulation is presented in this paper. The accuracy of the proposed model is verified with the measured data obtained from two different types of photodiodes, namely, n^+/p-substrate photodiode and n-well/p-substrate photodiode, which are fabricated using a conventional 0.25µm CMOS technology. The simulation results of the proposed model are compared with the measured I-V characteristics and high frequency response of up to 10GHz.

Keywords: Photodiode model, SPICE circuit simulation, CMOS, PN junction photodiode, photonic.

1 INTRODUCTION

With the rapid pace of development in low-cost CMOS technology, silicon photodiodes are currently recognized as promising core devices for photonic systems such as image formation and millimeter wave optical communications [1-3]. Moreover, the ever down sizing of Complementary Metal Oxide Semiconductor (CMOS) technology and the demand for high-speed performance have driven the IC design to a higher level of integration with higher operating frequencies [4]. Therefore, a compact and an accurate photodiode model, which can represents the DC as well as the high frequency characteristics, is needed for IC designers to perform circuit simulations before committing their designs on chips. Although some photodiode's models have validated the DC analysis, not much or no attention has been paid to the high frequency modeling [5]. In this paper, an accurate photodiode model is presented for the DC and high frequency SPICE circuit simulation.

2 PHOTODIODE MODEL AND DEVICE FABRICATION

A photodiode is similar in structure to the PN junction diode except that its junctions can be exposed to external light, that forming a third optical "terminal". The front of the wafer is usually heavily doped with an opposite dopant type of substrate by ion implantation in such as to produce a shallow junction. The depletion region has a built-in electric field, which is caused by the space charges due to

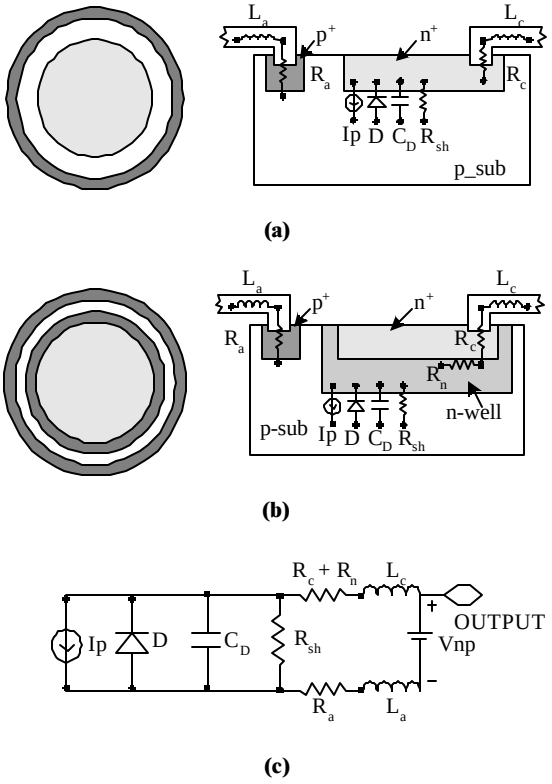

Figure 1 (a) Layout top and schematic cross sectional view of n^+/p-substrate photodiode (b) n-well/p-substrate photodiode (c) Proposed photodiode model (R_n=0 for n^+/p-substrate photodiode).

diffusion of majority carries across the interface of p and n regions. This region is important to the photodiode's performance (efficiency) as it converts photons into electron hole pairs. When light signal or photons of energy (hv) incident to the front surface of the photodiode, they penetrate into and absorbed by the silicon. If the energy of the photons is larger than the energy band gap of the silicon (i.e. about 1.12eV), the absorbed photon will excite an

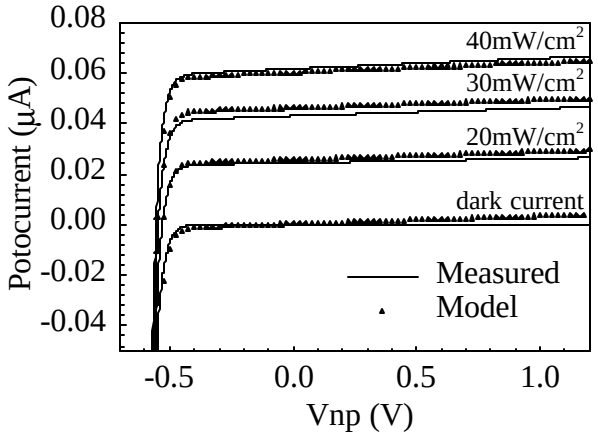

Figure 2. Measured and simulated I-V characteristics of an n^+/p-substrate photodiode for different light intensities.

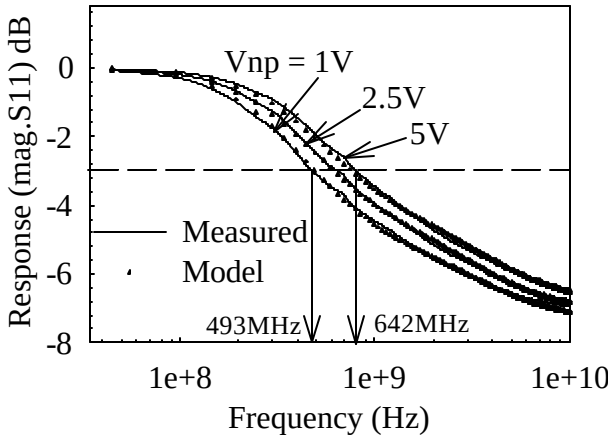

Figure 4. Measured and simulated frequency response of an n^+/p-substrate photodiode at different reversed bias conditions.

electron from the valance band to the conduction band and leaves a hole in valance band. In other words, it generates an electron-hole pair. When an electron-hole pair is created inside the depletion region, these electrons and holes are rapidly drift in opposite direction by the built-in electron field. This produces the photocurrent flow.

A P type, <100> silicon wafer with a resistivity ρ = 7.5 Ω cm was used for the fabrication. Using the N-well mask, well implantation was carried out with a doubly-charge Phosphorus at an energy of 490keV and a dose of $2\times10^{13}cm^{-2}$. The N-well depth is about 1.4μm from the surface. Arsenic (60keV, $3\times10^{15}cm^{-2}$) implant and BF_2^+ (40keV, $3\times10^{15}cm^{-2}$) implant were used to form the N^+ and P^+ regions, respectively. The N^+ and P^+ diffusion depths were found to be around 0.25μm with a sheet rho of 100Ω/sq. Finally, Titanium self-aligned-silicide (salicide) process was performed to reduce the contact resistance of the N^+ and P^+ regions. The layout top view and schematic cross sectional view of two different types of photodiodes are shown in Figure 1. In the n^+/p-substrate photodiode, cathode and anode regions of the photodiode are formed at the n^+ and p-substrate, respectively, and p^+ region is used for the p-substrate contact as shown in Figure 1(a). Therefore in this structure, the PN junction is formed between n^+ and p-substrate. Figure 1(b) shows the layout top view and schematic cross sectional view of the n-well/p-substrate photodiode. In this layout, the n-well and p-substrate become the cathode and anode regions, respectively of the photodiode; and the n^+ and p^+ are used as the n-well contact and p-substrate contact, respectively. Hence, a PN junction is formed.

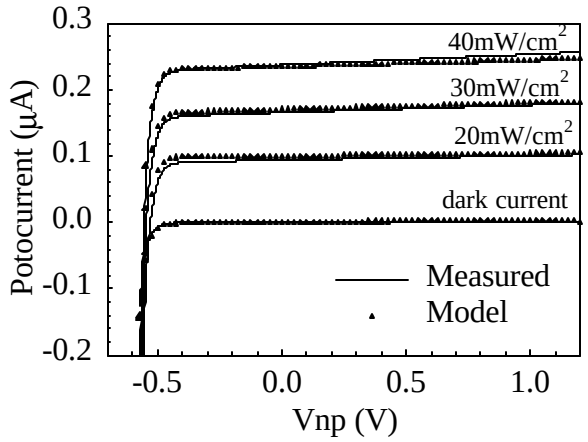

Figure 3. Measured and simulated I-V characteristics of an n-well/p-substrate photodiode for different light intensities.

The equivalent circuit model of the photodiode is shown in Figure 1(c) The conventional PN junction diode (D) model is used for the core of the photodiode model. R_{sh} represents the shunt resistance and C_D is the depletion capacitance of the diode at the reverse bias condition. R_c and R_a model the series resistance at the cathode and anode side of the diode, respectively. To account for the parasitic inductances associated with interconnection lines, L_c and L_a are added in series with R_c and R_a at the cathode and anode side, respectively. The current generator (Ip) models the light input terminal of the photodiode and the photocurrent generation is given by the equation:

	Dimension Diameter (μm)	Photocurrent @ 30mW/cm^2 (μA)	Capacitance (pF)	3dB bandwidth @1V (GHz)	Dark current (pA)
n^+/p-sub	75	0.047	0.48	0.493	0.34
n-well/p-sub	75	0.179	1.68	6.27	0.68

Table 1. Some important parameters for the fabricated photodiodes. Photodiodes are measured under a light wavelength of 850nm.

$$Ip=\eta q\lambda\phi/hc \quad (1)$$

where q=electron charge, λ=incident light wavelength, ϕ=incident flux density, h=Planck's constant, c=speed of light in vacuum. The quantum efficiency, $\eta(\%)=1.24\times10^5 R(A/W)/\lambda(nm)$, in which the responsivity, R, is defined as the ratio of output current to the input power.

3 RESULTS AND DISCUSSIONS

Two types of photodiodes, n-well/p-substrate and n^+/p-substrate, having a diameter of 75μm were fabricated using a 0.25μm CMOS technology to verify the accuracy of the model. The I-V and high frequency characteristics of the photodiodes are measured under an illuminated light wavelength of 850nm. Frequency responses are measured in frequency domain using the HP8510C network analyzer and GHz probes under a reversed biased of 1V, a light intensity of 30mW/cm^2 and a load impedance of 50Ω. Before the measurement, calibrations were carried out to correct the losses on the cables and connectors of the probes [6]. Probe pad de-embedding was also performed to remove parasitic capacitances of the probe pads. Some important parameters are tabulated in Table 1. The SPICE model parameters of the diode (D) are extracted under forward bias conditions. The measured and simulated I-V characteristics of n^+/p-substrate photodiodes is shown in Figure 2 for the different light intensities. The excellent agreements between measurement and simulation results are observed for all the light intensities. To verify the validity of the propose model for the different device structure, measured and simulated I-V characteristics of N-well photodiode are plotted in Figure 3. Figures 4 and 5 compare the measured and simulated frequency responses from 50MHz to 10GHz for 3 different reversed bias conditions. Their 3dB compression points at reversed bias of 1V and 5V are also indicated in the figures. The new model shows close agreements with the measured results for a wide frequency range from 50MHz to 10GHz. These excellent corresponding verified the validity of our propose model.

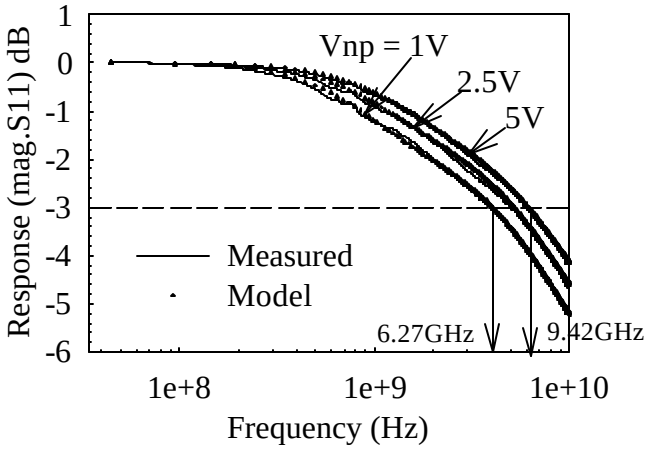

Figure 5 Measured and simulated frequency response of an n-well/p-substrate photodiode at different reversed bias conditions.

4 CONCLUSION

An accurate photodiode model has been proposed for DC and high frequency circuit simulation. The accuracy of the proposed model is verified for two different types of silicon photodiodes. The excellent agreements between simulated and measured I-V characteristics and high frequency response of up to 10GHz have also been demonstrated.

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REFERENCES

[1] E. R. Fossum, "CMOS Image Sensors: Electronic Camera On A Chip," IEDM, P. 17, 1995.

[2] T. K. Woodward and A. V. Krishnamoorthy, "1-Gb/s Integrated Optical Detectors and Receivers in Commercial CMOS Technologies," IEEE Journal of Selected Topics in Quantum Electronics, Vol. 5, No. 2, P. 146, 1999.

[3] C. L. Schow, J. D. Schaub, R. Li, J. Qi, and J. C. Campbell, "A 1-Gb/s Monolithically Integrated Silicon

NMOS Optical Receiver," IEEE Journal of Selected Topics in Quantum Electronics, Vol. 4, No. 6, P. 1035, 1998.

[4] B. L. Kasper and J. C. Compbell, "Multigigabit Per Second Avalanche Photodiode Lightwave Receiver," J. Lightwave Technol., Vol. LT-5, P. 1351, 1987.

[5] R. J. Perry and K. Arora, "Using PSPICE to Simulate the Photoresponse of Ideal CMOS Integrated Circuit Photodiodes," IEEE Proceeding of Southeastcon '96, P. 375, 1996.

[6] P. J. V. Wijnen, H. R. Claessen and E. A. Wolsheimer, "A New Straightforward Calibration and Correction Procedure for "On Wafer" High Frequency S-parameter Measurements (45MHz-18GHz)," IEEE Bipolar Circuit and Technology Meeting, P. 70, 1987.