SPICE Modeling of Capacitors

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ABSTRACT

Computer simulation and modeling have been an enormous aid in forecasting and envisioning actual movement and stresses for mechanical assemblies. The application of these same goals to circuit design and simulations have now begun to impact improvements in cycle time reduction in the introduction of new electronic products to market.

SPICE

These electrical simulation programs have grown out of SPICE. SPICE is an acronym that stands for ***S**imulation **P**rogram for **IC E**mulation*. This is a tool originally intended to aid in the understanding of the performance of integrated circuits (ICs). Today, SPICE modeling has moved well beyond integrated circuit emulation to full circuit emulation with some packages also allowing for environmental effects. This tool is seen by many as an effective means of reducing cycle time from circuit design to manufacturing by eliminating most of the prototype work needed in circuit board design. However good the software, its practical application may be hindered because individual components often do not always behave as predicted by ideal models.

Discussions with our customers affirmed their need for more realistic models. Much performance information on capacitors already existed in our files, so our primary objective was to reduce this empirical data to a "SPICE-friendly" format.

We desired to purchase a SPICE software package that was popular and used models that were compatible with other software packages. However the software available today is so numerous and different that the "most popular" category was never definable. Their differences also eliminated generating models on a universal basis. However, most software did allow creation of sub-circuits that could be substituted for components, or the importing of frequency related data that would allow a component to be created.

Discussing with SPICE practitioners who were interested in realistic capacitor emulation directed us to the use of a general mathematical software for the capacitor models. We started our analysis by using Mathcad® software to generate the frequency responses necessary. In addition, we could use this software to generate ASCII table listings of Frequency, Impedance, ESR (effective series resistance), Capacitance, DF (dissipation factor or resistance divided by reactance), and Phase Angle throughout the chosen frequency spectrum. These could then be imported into many other packages, including spreadsheet software.

FIGURE 1

The simple RLC model (Figure 1) is often considered as a good representative of the component in varying frequency applications. Many papers and charts have depicted this model as representative of a capacitor's behavior over frequency and some newer instruments have capability of defining the elements in a component under test. However, things are never as simple as they seem. For example, the resistive elements change with frequency, and electrolytic capacitors have a fairly steep capacitance roll-off at higher frequencies. These reactions now make the ESR and capacitance frequency dependent. These dependencies can be handled as mathematical dependencies, or the complexity of the model could be increased to a more complex circuit representation. We have used both methods in our models.

Ceramic Model

The resistive element in a ceramic capacitor distinguishes itself with a response to changing frequency that usually shows the minimum ESR near the self-resonant point. There appears to be very little capacitance change, based on the measurements well below self-resonance. Also, based on the results well above self-resonance, the inductive element (ESL) appears to be constant regardless of frequency.

The self-resonance is determined by the capacitance (*Cnom*) and ESL of the component, and in many cases the ESL is derived from the known capacitance and measured self-resonance frequency. Because the capacitance change with frequency is so little for the ceramic capacitor, it can be ignored for the model and the self-resonance frequency *(fr)* is calculated as follows:

$$fr = \frac{1}{2\pi \times \sqrt{ESL \times C_{NOM}}}$$

Inductance is determined by the constraint of current within a physical dimension over a fixed length. The ESL of the capacitor is fixed by the design of the capacitor. As such, the ESL can be listed for each style and capacitance value. Slight variations in designs to compensate for material changes will have very little effect on this value of ESL. With the determination of the self-resonance and using this frequency as the point of minimum ESR, the other ESRs can then be factored as the frequency moves away from this self-resonant frequency.

$$ESR = Rnom\left[1 + 10^{(|\log\{\frac{fr}{ftest}\}| - 1.5)}\right]$$

Rnom is the minimum resistance to be achieved near self-resonance *(fr)*. The frequency of application is entered as *ftest.* The response is widened out near self-resonance by the 1.5 factor, chosen as a best fit to actual data.

Figure 2 depicts the projected behavior of a 0.1 uFd ceramic capacitor, with an X7R dielectric, and an ESL of 2.5 nH, over a frequency range from 100 Hz to 1 GHz. The band represents a range of typical performance with the capacitance tolerance (±10%) applied plus an additional ±20% tolerance to the ESR. No two pieces from a lot will behave exactly the same, but they should fall within this band of performance. The 20% ESR band is meant to be representative of a typical range within a lot, but may be inadequate when considering lot-to-lot variations. A 30% band to consider lot-to-lot variations might be a more conservative choice.

Except for the NP0 or C0G dielectrics, bias voltage will have a suppressive effect on ESR and capacitance. Combining these two responses, those familiar with typical 1 KHz measurements of the ceramics' capacitance and DF versus DC bias, will also recognize that the DF decays quite rapidly with increasing bias because the resistance decays while the capacitive reactance increases.

The temperature effects on a ceramic capacitor's capacitance are defined by the EIA classification. An X7R is allowed a ± 15% change in capacitance over the temperature range of -55°C through +125°C. This 30% range of change is not typical, but only an envelope of acceptance to this classification. Typical changes are from -12% at -55°C, to nominal value at +25°C, to -13% at +125°C. It is this typical response for each different body type that is used in the model for temperature compensation of capacitance. The C0G materials have changes listed as PPM/°C, and for the purpose of this model, they are treated as if they do not change.

Assuming that the peak capacitance for an X7R dielectric occurs at or near +30°C, with a maximum change of -12% at both +125°C and -55°C, the ralationship might be expressed as follows:

$$Cap = Cnom\left[1 - \left(\frac{Ttest - 30}{85}\right)^2 \text{ x } 0.12\right]$$

For the Y5V with a peak capacitance near 15°C and a decay to -80% at +85°C and at -55°C, then the relationship might be expressed as follows:

$$Cap = Cnom\left[1 - \left(\frac{Ttest - 15}{70}\right)^2 \text{ x } 0.80\right]$$

Temperature also effects the ESR. Figure 3 details the typical response of the ESR at a singular frequency with respect to temperature for C0G and X7R dielectrics.

Figure 4 represents the model we used in calculating the response throughout the frequency spectrum. The RLC components now show the ESR as temperature, frequency, and VDC dependent, and the capacitance as temperature and VDC dependent. In addition to the series RLC components, there is an additional parallel resistance (the leakage resistance or insulation resistance) given as Rp, which is also temperature dependent. An additional RC network in parallel represents a capacitance (Cp) that shunts the RLC elements due mainly to that capacitance from the termination faces separated by the length of the chip, and its associated ESR (Rcp). This branch will cause a secondary or parallel resonance to occur well above the initial self-resonance that is a series resonance. Because the secondary resonance is parallel and would depict a decreasing impedance with increasing frequency, a provision for some external inductance (Lx) is also included. This external

FIGURE 2

Calculated Bands of Performance
0805 X7R 104 (±10%) @ 25°C & 0VDC Bias

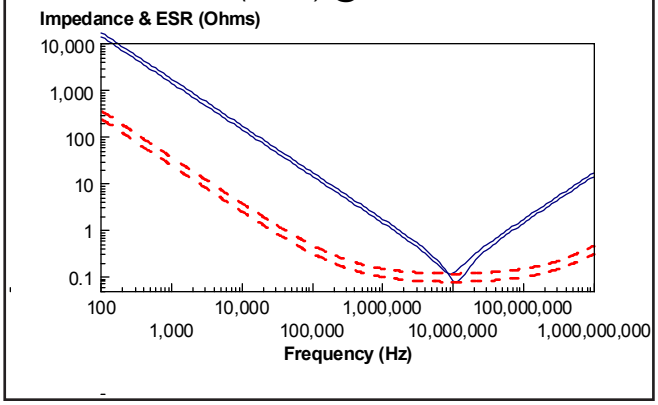


FIGURE 3

ESR versus Temperature

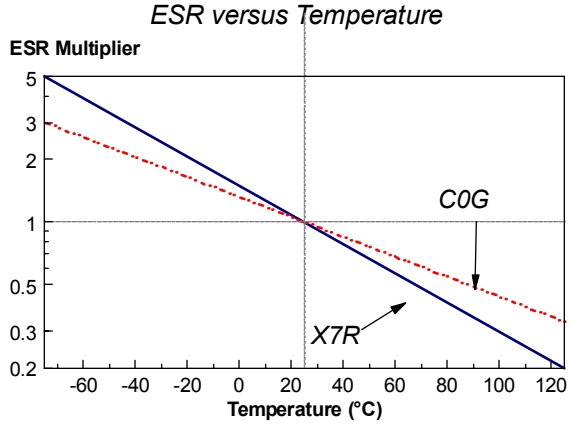
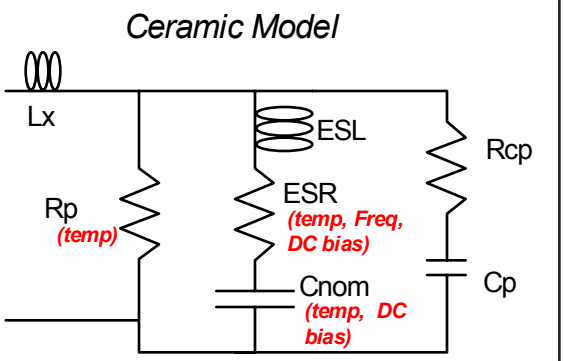


FIGURE 4



inductance may swamp the parallel resonance or give it short life to the point where another series resonance will occur and result in increasing impedance with increasing frequency. The external inductance is initially set to 0.1 nH, enough to account for inductance associated with the pad and high enough to check the parallel resonance effect. The parallel capacitance is a very small value and comes into play only at the very high frequencies (>=1GHz) and is dependent on body and chip size.

Additional dependencies applied to the ceramic model's elements include temperature and voltage effects. For X7R and Z5U or Y5V dielectrics, both the capacitance and ESR will decay with applied DC bias. The rate at which capacitance for these devices decays is independent of their rated voltages, yet dependent on materials and designs. To establish conformity with the models, the voltage at which each capacitor model loses 20% of its capacitance was arbitrarily selected as an additional point of information for calculating the capacitance decay due to DC bias. The relationship of decay is assumed as a first order approximation, to be linear through the -20% range. There is also a decay in ESR proportional to the capacitance drop with DC bias. Again, there are no DC bias effects on capacitance or ESR for the NPO or C0G dielectrics. The capacitance and ESR are calculated as:

$$Cap = C_{NOM}\left(1 - \frac{V_{TEST}}{V_{NOM}} \times 0.2\right)$$

$$ESR = R_{NOM}\left(1 - \frac{V_{TEST}}{V_{NOM}} \times 0.2\right)$$

Here the resultant capacitance and ESR, *Cap* and *ESR*, is based on the nominal value, *Cnom* and *Rnom*, and factored by the bias application, *Vtest*, divided by the -20% voltage, *Vnom*, times the 20% decay. Be aware that the near linearity applies only to the -20% decay level, and assumptions beyond this could lead to significant errors.

Based on the responses shown earlier in Figure 3, the ESR for the NPO at -55°C, will increase to approximately 2.4 times that observed at 25°C. At +125°C, the ESR will decay to 1/3 the observed ESR at 25°C.

For the X7R, this relationship will be 3.6 times at -55°C and one-fifth (1/5 x) at +125°C. Both of these would appear as linear relationships on a semi-log plot (log ESR multiplier and linear temperature), and can be factored in the relationship. Looking back again at an earlier graph, Figure 2 actually shows two bands of performance for the 0805 104 X7R, one at +25°C, and the other at +125°C. Corrected ESR for both NP0 and X7R, and capacitance for X7R is as follows:

$$ESR = R_{NOM} \times 3^{\left(\frac{25 - T_{TEST}}{100}\right)} \qquad \textbf{(C0G)}$$

$$ESR = R_{NOM} \times 5^{\left(\frac{25 - T_{TEST}}{100}\right)} \qquad \textbf{(X7R)}$$

For Z5U and Y5V, the relationship of ESR versus temperature is similar to the X7R relationship up to +85°C. At this point, the ESR will reach its minimum and then start to increase dramatically. As long as the device does not exceed an application of +85°C, this unit's performance can be effectively predicted using the created models. These corrections are as follows:

The model combines all elements to calculate the complex impedance at each frequency, then deduces the ESR and capacitance or inductance from that impedance.

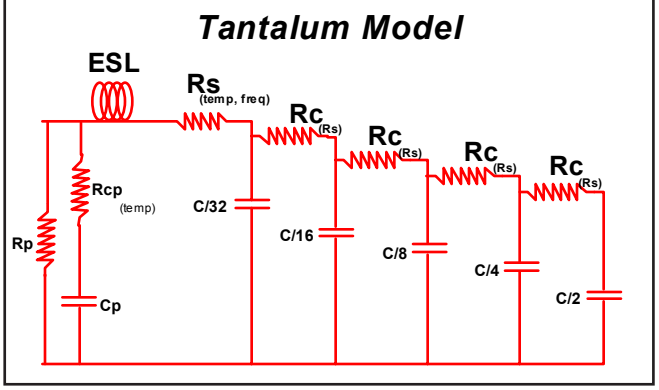
Tantalum Model

The tantalum capacitor brings the additional effect of frequency-dependent capacitance changes. The resonance cannot be easily calculated as the ceramic and using the point of self-resonance and nominal capacitance to calculate the ESL is absolutely wrong. Though the capacitance of a ceramic may decay by 1% per decade of frequency, this is insignificant in modeling the performance and is disregarded. The tantalum can decay 20% or more per decade.

This has always been explained as a RC-Ladder type of phenomenon, and various RC-Ladders have been proposed to define the performance. There have even been instances where a model for a specific device has been detailed, yet none has included elemental definition (capacitance and resistance values for all values) for a series of capacitors.

Figure 5 shows an RC-Ladder with consistent resistive elements between capacitive elements, and increasing capacitive elements as the depth increases in the ladder. This model was the simplest form to allow us to adequately fit the actual performance of these devices. It is not the first model attempted as many variations were tried with the resistive elements increasing with depth and capacitive elements constant, but these would never give the response needed. All the Rc elements are factors of the Rs element, and since it is factored by temperature and frequency, they all are.

FIGURE 5



By using only 5 capacitive elements, we were successful in duplicating the actual performance in terms of capacitance roll-off, impedance and ESR with frequency.

The physical representation of this effect can be shown in Figure 6. The resistive chain is the MnO_2 electrode that penetrates the tantalum block in between the tantalum particles. These channels have limited width, yet must penetrate to the center of the tantalum block to electrically connect the deepest capacitive elements. The deeper the penetration, the higher the resistance of that path. As frequency increases, the period for each capacitor element to respond and contribute to the total capacitance decreases. It will eventually reach a period where there is too high of a resistance for the deeper elements to contribute, and starting at the center and working out towards the surface, more and more capacitive elements are unable to make any contribution to the total capacitance.

This electrical presentation of the tantalum capacitor also fit with our understanding of the physical aspects of the capacitor: the capacitance decays with increasing frequency, and less of the signal penetrates the depth of the anode bulk. The capacitance available to the circuit at higher frequency is all located near the outer surface of the anode as depicted in Figure 7.

With the tantalum capacitor, there is no noted effect of DC biases while the temperature affects the ESR and capacitance. The relationship for the ESR is similar to the X7R ceramics, but at -55°C, the noted change is ~2.4 times the 25°C ESR, and the +125°C ESR is one-third (1/3 x) the 25°C ESR.

$$Radj = Rmin * 3 \left(\frac{25 - Ttest}{100}\right)$$

Again, the ESR is frequency sensitive, but tantalum capacitors' behavior appears to posses two nodes where the ESR changes slopes. The first lies between 1 KHz and 10 KHz, while the second appears near 10 MHz. The variance of these frequency nodes seems to be related to the size and materials of the anode. Figure 8 shows a typical tantalum chip's behavior for different temperatures. Normally, the ESR and capacitance are allowed to vary according to their tolerances, but this band of performance was omitted here to reduce confusion. This relationship is expressed as:

$$Rs = Radj * \left[1 + 10^{(Fx - \log(ftest))} + 10^{(\log(ftest) - 7)}\right]$$

Where *Rs* is the calculated ESR, *Rc* is the minimum ESR, *Fx* is the $\log_{10}$ of the first node, and 7 represents the $\log_{10}$ of the second node (10 MHz), while *ftest* is the frequency of application.

The calculation of complex impedance is then made from the inside (C/2) out to Rp, or from the right of the ladder to the left. After the impedance is calculated, the reactance determines weather the response is inductive or capacitive. For this device, because there is such a roll-off of capacitance with frequency, the capacitance calculation is the "real capacitance" devoid of inductive influences.

All the models generated were adjusted to allow them to duplicate typical responses from data gathered from the actual frequency scans of our components. Figure 9 depicts the pro-

FIGURE 6

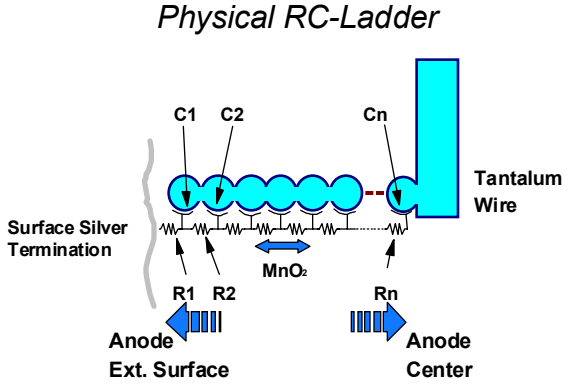


FIGURE 7

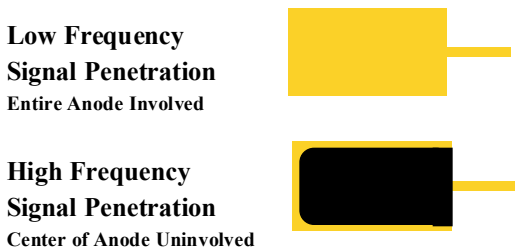


FIGURE 8

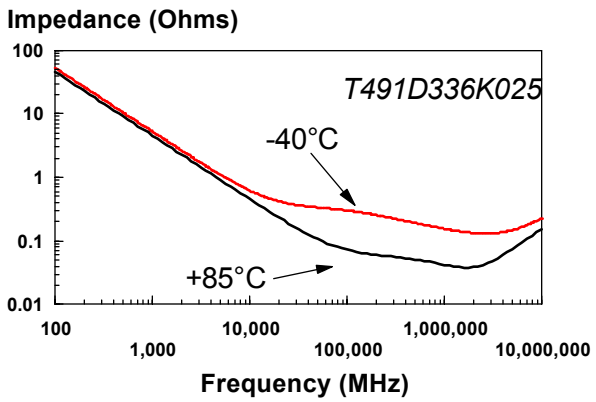
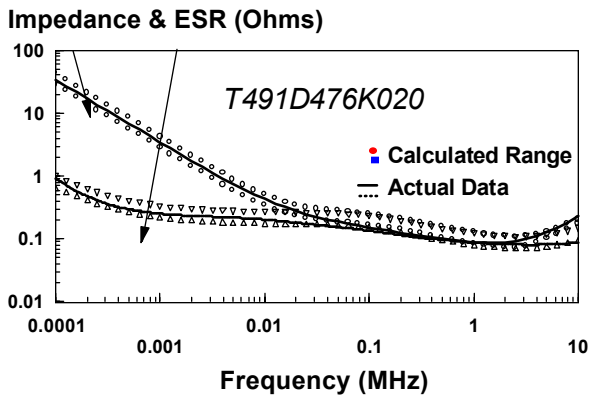


FIGURE 9



jected typical response and that of an actual piece. This trace shows an almost perfect fit for this piece, but this piece represented a response very close to the average response for several pieces of this style. The allowance of the tolerance bands on capacitance and ESR accommodates the variations that will be seen from lot to lot and within a manufactured lot of pieces.

KEMET's SPICE Models

KEMET is striving to offer the best possible models to aid our customers in their SPICE use. Based on a survey conducted with our customers who use SPICE, we are using Mathcad® generated models with all those values of 1206, 0805, and 0603 ceramic chips, of NP0 and X7R (Y5V is coming) as listed in our catalog.

For tantalum chips we offer a range of part types of different capacitance and voltage ratings for the T491 and T495 surface mount designs. The diskette offered contains the Mathcad® models (Version 4.0) plus an ASCII listing (at room ambient temperature and no DC bias ONLY - even these are quite numerous and take up the majority of diskette space) for each value of each part type for frequency, impedance, ESR and capacitance . Additionally, for those who may be able to place the frequency, temperature, and bias relationships in their SPICE software, tables of sub-element values will be included for the ceramic and tantalum models, for each specific capacitor type and capacitance.

Attached are two printouts, one each from the ceramic and tantalum models. The operator only needs to enter an index or array pointer as all the values and styles are held in a matrix. Optional entries include ambient temperature, applied DC bias, tolerance of capacitance and resistive elements, and in the case of the ceramics, an external inductance.

Finally, for the ceramics, along with the electrical elements of the model, a coefficient for large pad thermal transfer is included. Five distinct frequency values and their associated current levels may be entered to allow the operator to view the individual and cumulative temperature rise. For the tantalum, these five discrete frequencies and currents will result in individual and cumulative power dissipation levels.

PLEASE NOTE: These detailed responses are not intended to define the limits of behavior for each specific part type, but relate performance as typical response over frequency with various electrical and ambient conditions.

Bibliography

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