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8x16 analog switch array chip CH446Q

5x24 analog switch array chip CH446X

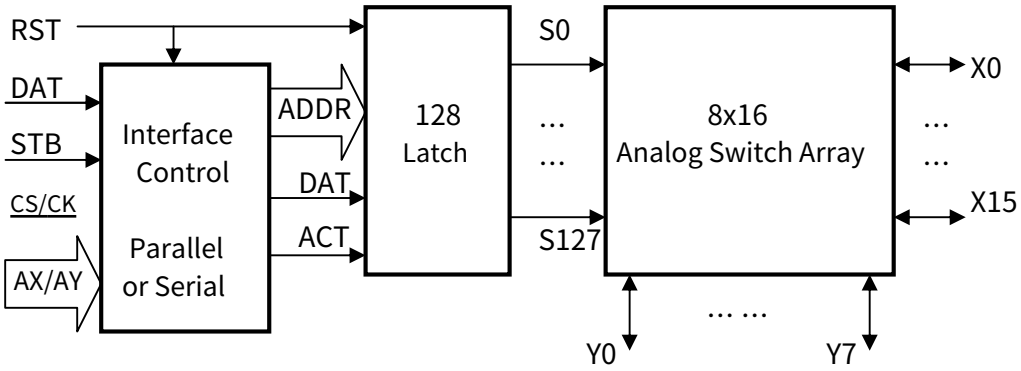
manual

Version: 1D

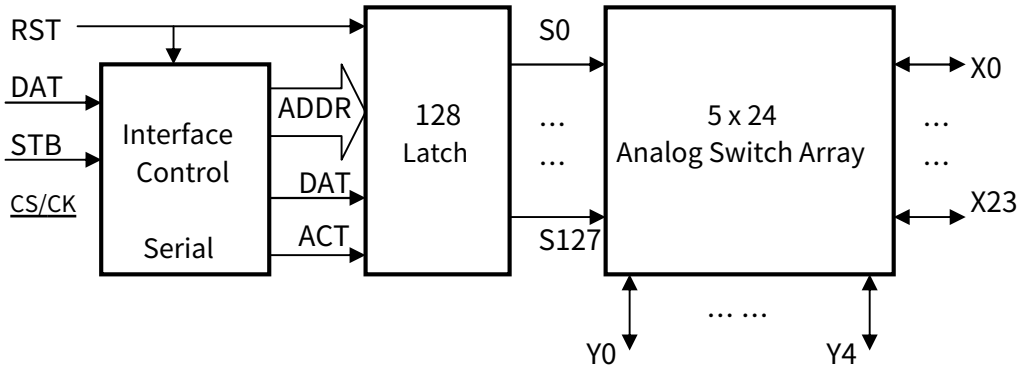
http://wch.cn

1 Overview

CH446Q is an 8x16 matrix analog switch chip. CH446Q contains 128 analog switches, which are distributed at each intersection of the 8x16 signal channel matrix. Each analog switch can be turned on or off independently, thereby realizing any routing of the 8x16 signal channel.



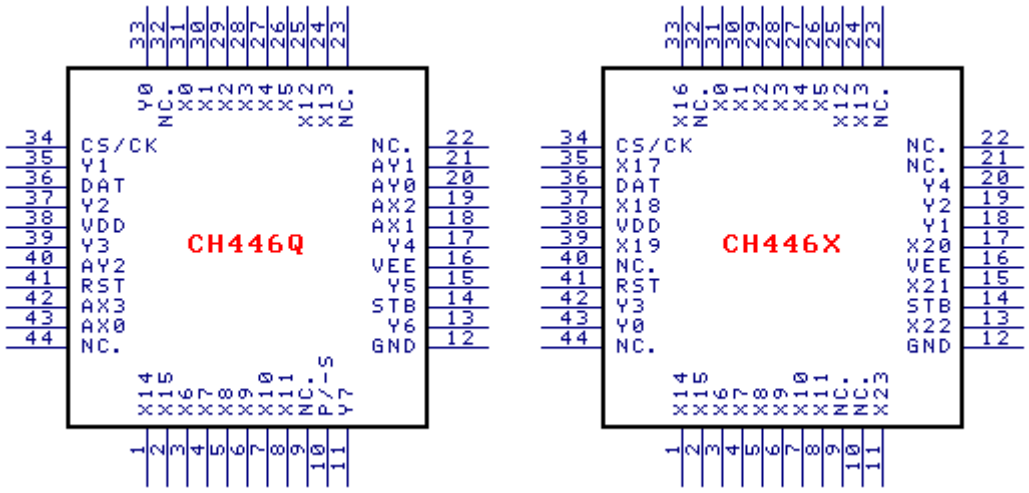
CH446X is a 5x24 matrix analog switch chip. CH446X contains 120 analog switches, which are distributed at each intersection of the 5x24 signal channel matrix. Each analog switch can be turned on or off independently, thereby realizing any routing of the 5x24 signal channels.



2. Features

- CH446Q has built-in 128 independent analog switches, which are distributed at each intersection of the 8x16 signal channel matrix.
- CH446X has built-in 120 independent analog switches, which are distributed at each intersection of the 5x24 signal channel matrix.
- CH446Q supports 7-bit parallel address input and is compatible with existing similar products.
- Supports serial address shift input, saving pins.
- Supports single power supply voltage from 4V to 12V, and dual power supply voltages of +5V and -7V.
- When the voltage difference between positive and negative power supplies is 12V, the maximum on-resistance Ron is 65Ω, and △Ron does not exceed 10Ω.
- Pure CMOS technology, low static power consumption.
- Adopt LQFP-44 lead-free package, compatible with RoHS, and provide conversion board to PLCC44 package.

3. Encapsulation



Package form	width		Pin spacing		Package Description	Order model
LQFP-44	10*10mm		0.8mm	31.5mil	Standard LQFP44 pin patch	CH446Q
LQFP-44	10*10mm		0.8mm	31.5mil	Standard LQFP44 pin patch	CH446X

4. Pin

4.1. CH446Q pins

Pin number	Pin name	type	Pin description
38	VDD	power supply	Positive power supply, the voltage must be greater than or equal to GND
12	GND	power supply	Public ground, digital signal reference ground, voltage is 0V
16	VEE	power supply	Negative power supply, the voltage must be less than or equal to GND
41	RST	enter	External manual reset input, active high level
10	P/-S	enter	Address input method selection: High level is parallel input mode; low level is serial input mode.
36	DAT	enter	In serial address mode, it is serial data input and switch data input; In parallel address mode, it is switch data input. When it is high level, it is turned on, when it is low level, it is turned off.
14	STB	enter	Strobe input, active at high level
34	CS/CK	enter	In serial address mode, it is the serial clock input, and the rising edge is valid; In parallel address mode, it is chip select input and is active at high level.
43, 18, 19, 42	AX0～AX3	enter	In serial address mode, it is an unused pin and must be directly connected to GND; In parallel address mode, the address input selected for the X port
20, 21, 40	AY0～AY2	enter	In serial address mode, it is an unused pin and must be directly connected to GND; In parallel address mode, the address input selected for the Y port
31, 30, 29, 28, 27, 26, 3, 4, 5, 6, 7, 8, 25, 24, 1, 2	X0～X15	analog signal input Output	8x16 Matrix Analog Switch X Port
33, 35, 37, 39, 17, 15, 13, 11	Y0～Y7	analog signal input Output	Y port of 8x16 matrix analog switch
9, 22, 23, 32, 44	NC.	Empty feet	Unused pins, connection prohibited

4.2. CH446X pins

Pin number	Pin name	type	Pin description
38	VDD	power supply	Positive power supply, the voltage must be greater than or equal to GND
12	GND	power supply	Public ground, digital signal reference ground, voltage is 0V
16	VEE	power supply	Negative power supply, the voltage must be less than or equal to GND
41	RST	enter	External manual reset input, active high level
36	DAT	enter	Serial data input and switch data input; When used as a switch data input, high level is on and low level is off.
14	STB	enter	Strobe input, active at high level
34	CS/CK	enter	Serial clock input, valid on rising edge
31, 30, 29, 28, 27, 26, 3, 4, 5, 6, 7, 8, 25, 24, 1, 2, 33, 35, 37, 39, 17, 15, 13, 11	X0～X23	analog signal input Output	X port of 5x24 matrix analog switch
43, 18, 19, 42, 20	Y0～Y4	analog signal input Output	Y port of 5x24 matrix analog switch
9, 10, 21, 40, 22, 23, 32, 44	NC.	Empty feet	Unused pins, connection prohibited

5. Function description

Referring to the block diagram on the homepage, the CH446Q chip is divided into three parts: interface control logic, 128 latches, and 128 analog switch arrays. The interface control logic also includes serial address to parallel address conversion.

128 analog switches are distributed at each intersection point of the 8x16 matrix composed of 16 X ports and 8 Y ports, so that any X port and any Y port can be connected or disconnected when needed, and even Make certain two X ports conduct to a certain Y port respectively to realize indirect conduction between any two X ports or between any two Y ports.

128 latches are used to control the on or off of 128 analog switches respectively. The 128 latches are addressed from 0 to 127 and are selected after decoding from the 7-bit addresses ADDR6~ADDR0. Inputting a high reset signal from the RST pin clears all latches to 0, causing all analog switches to open. When it is necessary to turn on or off an analog switch, the address of the latch should be provided through the 7-bit ADDR, and the switch data should be provided through DAT (1 means on, 0 means off), and then an ACT activation pulse is generated to change the switch data. Write to the latch specified by ADDR decoding to control a specified analog switch.

The interface control logic is mainly used to generate ADDR address and ACT activation pulses. In the parallel address input mode, the pins AX0~AX3 and AY0~AY2 form a 7-bit address input ADDR0~ADDR6 from low to high. When the chip select signal input by the CS/CK pin is high level, the STB pin The input high-level strobe pulse generates an ACT activation pulse. When the CS/CK pin is low, no ACT signal is generated. In the serial address input mode, the CS/CK pin inputs the clock, and at each rising edge, ADDR6, ADDR5 to ADDR1, ADDR0 are input from the DAT pin in sequence (corresponding to AY2, AY1 to AX1, AX0 respectively) , the CS/CK pin needs to provide 7 rising edges to get 7 bit address, and the high-level strobe pulse input from the STB pin directly generates the ACT activation pulse.

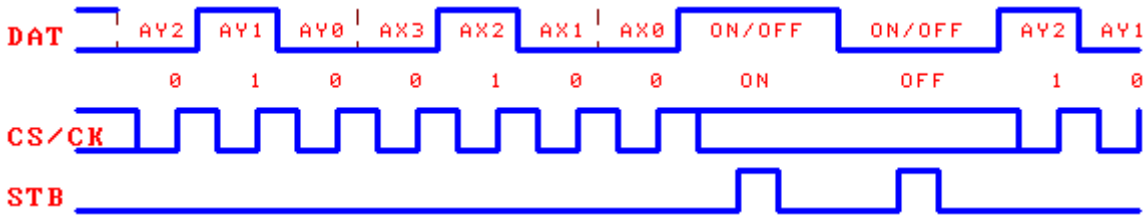
In fact, in the parallel address input mode, the ACT signal is the "AND" of the CS/CK pin input and the STB pin input. , while in string In the row address input mode, the ACT signal is only input from the STB pin. The RST reset signal has priority over the ACT signal. When the RST input is high, the ACT signal will be ignored and all latches are always cleared to 0. During the period when the ACT activation pulse is valid, the DAT pin can dynamically change the input switch data and make the corresponding analog switch turn on or off in real time, but before the ACT signal ends (that is, before the falling edge of STB), the input data to the DAT pin should remain stable in order to latch the data correctly.

CH446X has similar functions to CH446Q, with three differences: ①. The former is a 5x24 matrix composed of 24 X ports and 5 Y ports, while the latter is an 8x16 matrix composed of 16 X ports and 8 Y ports; ②. The former only supports Serial address mode, the latter supports both parallel address and serial address modes; ③. Although CH446X also has 128 latches, it only has 120 analog switches, and 8 latches have no use.

The following table is CH446Q chip 7-bit address ADTranslation of DR codetruth table, alsoIt's 128 moldpseudo switch ofAddressing table.

intersection Y end-X end	ADDR6 AY2	ADDR5 AY1	ADDR4 AY0	ADDR3 AX3	ADDR2 AX2	ADDR1 AX1	ADDR0 AX0	Addressing serial number
Y0-X0	0	0	0	0	0	0	0	00H
Y0-X1	0	0	0	0	0	0	1	01H
Y0-X2	0	0	0	0	0	1	0	02H
Y0-X3	0	0	0	0	0	1	1	03H
Y0-X4	0	0	0	0	1	0	0	04H
Y0-X5	0	0	0	0	1	0	1	05H
Y0-X6	0	0	0	0	1	1	0	06H
Y0-X7	0	0	0	0	1	1	1	07H
Y0-X8	0	0	0	1	0	0	0	08H
Y0-X9	0	0	0	1	0	0	1	09H
Y0-X10	0	0	0	1	0	1	0	0AH
Y0-X11	0	0	0	1	0	1	1	0BH
Y0-X12	0	0	0	1	1	0	0	0CH
Y0-X13	0	0	0	1	1	0	1	0DH
Y0-X14	0	0	0	1	1	1	0	0EH
Y0-X15	0	0	0	1	1	1	1	0FH
Y1-X0	0	0	1	0	0	0	0	10H
Y1-X1	0	0	1	0	0	0	1	11H
.....								
Y1-X14	0	0	1	1	1	1	0	1EH
Y1-X15	0	0	1	1	1	1	1	1FH
Y2-X0	0	1	0	0	0	0	0	20H
.....								
Y2-X15	0	1	0	1	1	1	1	2FH
.....								
Y7-X0	1	1	1	0	0	0	0	70H
.....								
Y7-X14	1	1	1	1	1	1	0	7EH
Y7-X15	1	1	1	1	1	1	1	7FH

The figure below is an example of serial address input, which controls the analog switch at address 24H (between Y2 and X4), first on and then off.



The following table is CH446X chip 7-bit address ADTranslation of DR codetruth table, alsoIt's 120 moldpseudo switch ofAddressing table.

intersection Y end-X end	ADDR6	ADDR5	ADDR4	ADDR3	ADDR2	ADDR1	ADDR0	Addressing serial number
Y0-X0	0	0	0	0	0	0	0	00H
Y0-X1	0	0	0	0	0	0	1	01H
Y0-X2	0	0	0	0	0	1	0	02H
Y0-X3	0	0	0	0	0	1	1	03H

Y0-X4	0	0	0	0	1	0	0	04H
Y0-X5	0	0	0	0	1	0	1	05H
Y0-X6	0	0	0	0	1	1	0	06H
Y0-X7	0	0	0	0	1	1	1	07H
Y0-X8	0	0	0	1	0	0	0	08H
Y0-X9	0	0	0	1	0	0	1	09H
Y0-X10	0	0	0	1	0	1	0	0AH
Y0-X11	0	0	0	1	0	1	1	0BH
Y0-X12	0	0	0	1	1	0	0	0CH
Y0-X13	0	0	0	1	1	0	1	0DH
Y0-X14	0	0	0	1	1	1	0	0EH
Y0-X15	0	0	0	1	1	1	1	0FH
Y0-X16	0	0	1	0	0	0	0	10H
Y0-X17	0	0	1	0	0	0	1	11H
Y0-X18	0	0	1	0	0	1	0	12H
Y0-X19	0	0	1	0	0	1	1	13H
Y0-X20	0	0	1	0	1	0	0	14H
Y0-X21	0	0	1	0	1	0	1	15H
Y0-X22	0	0	1	0	1	1	0	16H
Y0-X23	0	0	1	0	1	1	1	17H
Y4-X0	0	0	1	1	0	0	0	18H
Y4-X1	0	0	1	1	0	0	1	19H
Y4-X2	0	0	1	1	0	1	0	1AH
Y4-X3	0	0	1	1	0	1	1	1BH
Y4-X4	0	0	1	1	1	0	0	1CH
Y4-X5	0	0	1	1	1	0	1	1DH
no connection	0	0	1	1	1	1	0, 1	1EH, 1FH
Y1-X0	0	1	0	0	0	0	0	20H
				.....				
Y1-X23	0	1	1	0	1	1	1	37H
Y4-X6	0	1	1	1	0	0	0	38H
				.....				
Y4-X11	0	1	1	1	1	0	1	3DH
no connection	0	1	1	1	1	1	0, 1	3EH, 3FH
Y2-X0	1	0	0	0	0	0	0	40H
				.....				
Y2-X23	1	0	1	0	1	1	1	57H
Y4-X12	1	0	1	1	0	0	0	58H
				.....				
Y4-X17	1	0	1	1	1	0	1	5DH
no connection	1	0	1	1	1	1	0, 1	5EH, 5FH
Y3-X0	1	1	0	0	0	0	0	60H
				.....				
Y3-X23	1	1	1	0	1	1	1	77H
Y4-X18	1	1	1	1	0	0	0	78H
				.....				
Y4-X23	1	1	1	1	1	0	1	7DH
no connection	1	1	1	1	1	1	0, 1	7EH, 7FH

6. Parameters

6.1. Absolute maximum value (critical or exceeding the absolute maximum value may cause the chip to work abnormally or even be damaged)

name	Parameter Description	minimum value	maximum value	unit
TA	Ambient temperature during operation	- 40	85	℃
TS	Ambient temperature during storage	- 55	125	℃
VDD	When VEE=GND=0V, VDD power supply voltage	- 0.5	16	V
VEE	When VDD=GND=0V, VEE power supply voltage	- 16	+ 0.5	V
Vaio	The voltage on the analog signal input or output pin, VDD>=GND>=VEE	VEE-0.5	VDD+0.5	V
Vdio	The voltage on the digital signal input or output pin, VDD>=GND>=VEE	GND-0.5	VDD+0.5	V
Isw	Analog switch continuous current flow	0	15	mA
Iall	The sum of the continuous through currents of all analog switches	0	100	mA

6.2. Recommended operating voltage

name	Parameter Description		minimum value	maximum value	unit
VDD	GND=0V,	VDD supply voltage	4	13.2	V
VEE	The voltage difference between VDD and VEE is less than 13.2V	VEE supply voltage	- 8.8	0	V
Vaio	The voltage on the analog signal input or output pin, VDD>=GND>=VEE		VEE	VDD	V
Vdio	The voltage on the digital signal input or output pin, VDD>=GND>=VEE		GND	VDD	V

The power supply voltage should meet two conditions: VDD>GND>=VEE and VDD>GND+4V. The following combinations are recommended:

VDD=12V & GND=0V & VEE=0V (VDD-GND=12V, VDD-VEE=12V)
VDD=5V & GND=0V & VEE=0V (VDD-GND=5V, VDD-VEE=5V) VDD=
6V & GND=0V & VEE=-6V (VDD-GND=6V, VDD-VEE=12V) VDD=5V &
GND=0V & VEE=-7V (VDD-GND=5V, VDD-VEE=12V) VDD= 5V &
GND=0V & VEE=-5V (VDD-GND=5V, VDD-VEE=10V)

6.3. Electrical parameters (test conditions: TA=25°C, VDD=12V, GND=0V, VEE=0V, voltage difference across the analog switch is 0.4V)

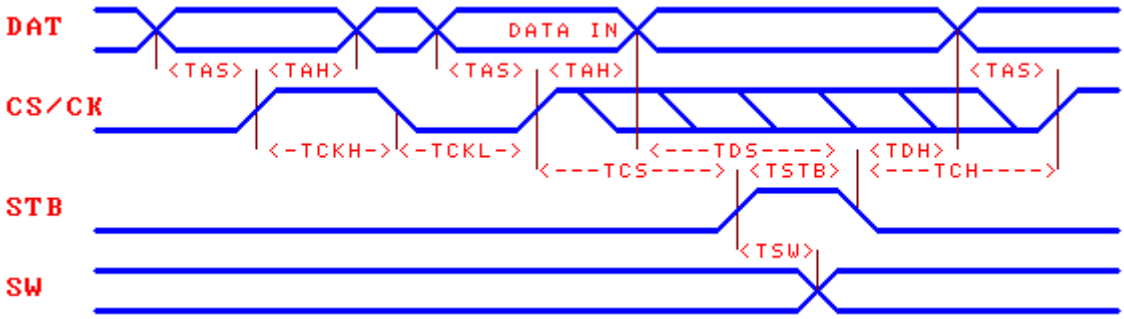
name	Parameter Description	minimum value	Typical value	maximum value	unit
ICC0	Quiescent supply current, all digital pins connected to VDD or GND		1	100	uA
ICC5	Quiescent supply current, VDD=5V, all digital pins 2.4V		0.4	1.5	mA
ICC12	Quiescent supply current, all digital pins 3.4V		5	15	mA
VIL	Digital pin low level input voltage, VDD-GND=5V	- 0.5		0.8	V
VIH	Digital pin high level input voltage, VDD-GND=5V	2.0		VDD+0.5	V
VIH12	Digital pin high level input voltage	3.3		VDD+0.5	V
ILEAK	Input Leakage Current of Digital Pins		0.1	10	uA
IOFF	Analog switch leakage current in closed state		±1	±500	nA
RON12	Analog switch on-resistance, VDD-VEE=12V, 25°C		45	65	Ω
RON12T	Analog switch on-resistance, VDD-VEE=12V, 85°C		55	80	Ω
RON5	Analog switch on-resistance, VDD-VEE=5V, 25°C		120	185	Ω
RON5T	Analog switch on-resistance, VDD-VEE=5V, 85°C		150	225	Ω
△RON	Difference in on-resistance of multiple analog switches, VDD-VEE=12V		5	10	Ω

6.4. Analog switching timing parameters (test conditions: TA=25°C, VDD=5V, GND=0V, VEE=-7V, analog signal 2Vpp)

name	Parameter Description	minimum value	Typical value	maximum value	unit
CSW	Analog switch port pin capacitance, F=1MHz		10	25	pF
CFT	Analog switch feedthrough capacitor, F=1MHz		0.5		pF
F3DB	Analog switching frequency response, 3DB, RL=3KΩ		50		MHz
TPS	Analog switch signal pass delay, RL=1KΩ, CL=50pF		12	30	n

6.5. Interface timing parameters (test conditions: TA=25°C, VDD=5V, GND=0V, VEE=-7V, refer to the attached figure)

name	Parameter Description	minimum value	Typical value	maximum value	unit
CDI	Pin capacitance of digital signal input, F=1MHz		7	15	pF
TPAS	Setup time of parallel input address to STB rising edge	8			n
TPAH	Parallel input address hold time for STB falling edge	6			n
TAS	DAT input address to CS/CK rising edge setup time	7			n
TAH	DAT input address hold time for CS/CK rising edge	3			n
TDS	DAT input data to STB falling edge setup time	8			n
TDH	DAT input data hold time for STB falling edge	6			n
TCS	CS/CK rising edge to STB rising edge setup time	10			n
TCH	CS/CK rising edge to STB falling edge hold time	7			n
TCKL	CS/CK clock signal low level width	10			n
htK	CS/CK clock signal high level width	10			n
TSTB	STB input high level active pulse width	10			n
TRST	RST input high level active pulse width	15			n
TSW	DAT, STB or RST to analog switch execution delay	5	30	70	n



7. Application

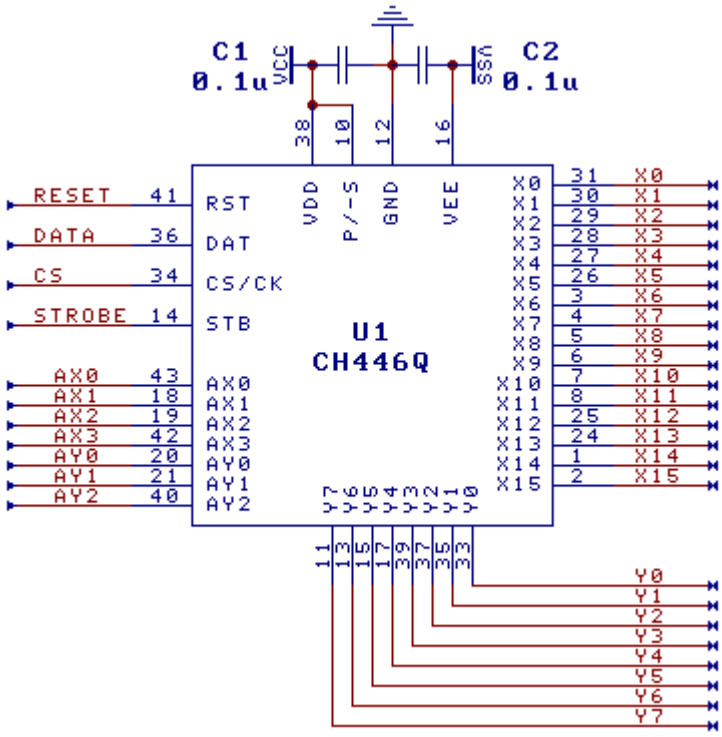
7.1. Parallel address input (picture below)

Control steps in parallel address input mode: provide address through AX0~AX3 and AY0~AY2 pins, provide data through DAT pin, and provide a high level pulse to STB pin (and CS/CK pin).

In the parallel address input mode, in order to save the control pins of the microcontroller, the CS/CK pin can be short-circuited with the STB pin or the VDD pin, leaving only the STB pin controlled by the microcontroller.

If VEE is connected to negative voltage, the analog switch can pass analog signals with negative voltage. Otherwise, if VEE is connected to GND, the analog switch can only pass analog signals higher than -0.3V.

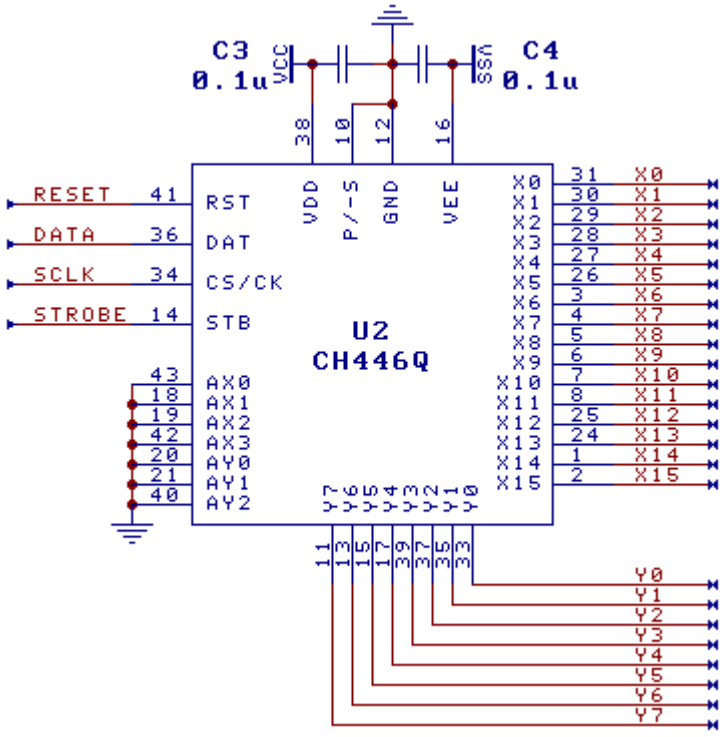
Since analog circuits and digital circuits share VDD, in order to reduce interference, the VDD and VEE pins must be connected to external decoupling capacitors, and it is recommended to appropriately slow down the edge of the digital input signal and reduce the transmission frequency. In addition, for application environments with strong interference, the microcontroller can refresh CH446 regularly every few seconds to ensure that each analog switch is in the correct switching state.



7.2. Serial address input (picture below)

Control steps in the serial address input mode: Provide the 7-bit address in sequence through the DAT pin and move it into CH446 using the 7 rising edges of the CS/CK pin, provide data through the DAT pin, and provide a high-level pulse to the STB pin .

If the microcontroller is connected to CH446 through the SPI bus, then bit 7 of one byte of 8-bit data provided by SPI will be discarded by CH446, bit 6 of SPI is used as an address, and bit 0 is used as the address. The serial data output pin of the microcontroller SPI is connected to the DAT pin to provide a switch. Data, the microcontroller uses an independent pin to control the STB pin of CH446.



7.3. Microcontroller interface program

The website provides C language and ASM assembly interface programs for commonly used microcontrollers.

7.4. Pin conversion

In parallel address input mode, CH446Q is basically functionally compatible with MT8816, but the packages and pins are different. The difference is that some of the pins of the X port of the 8x16 matrix analog switch are different (or their addressing is different) , please refer to the table below for differences.

ADDR3-ADDR0 or AX3-AX0 addressing	CH446Q in LQFP44 package		MT8816 in PLCC44 package	
	Pin number	Pin name	Pin number	Pin name
0110	3	X6	31	X12
0111	4	X7	30	X13
1000	5	X8	9	X6
1001	6	X9	10	X7
1010	7	X10	11	X8
1011	8	X11	12	X9
1100	25	X12	13	X10
1101	twenty four	X13	14	X11

The PLCC44 package conversion board can convert LQFP44 to PLCC44 by adjusting the pin sequence according to the above table through internal PCB wiring.