DDR3 Demo for the LatticeECP3 Versa Evaluation Board

User's Guide

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Introduction

This document provides technical information and instructions for using the LatticeECP3™ DDR3 demo design. This demo design demonstrates the functionality of the Lattice DDR3 IP operating core at a speed of 400 MHz and 800 Mbps using the LatticeECP3 Versa Evaluation Board. The LatticeECP3 Versa Evaluation Board, USB cable, power supply and demo files are included in the LatticeECP3 Versa Development Kit. This document provides a circuit description of the demo logic as well as instructions for running the DDR3 demo.

The LatticeECP3 Versa Evaluation Board has an on-board 16-bit DDR3 SDRAM. The demo design generates 16-bit test data, and writes it to the onboard RAM. The design reads the DDR3 SDRAM data and compares it with original expected data. When there is a mismatch between the standard and read data, the design will flag an error signal. The demo design also allows the user to run the design with different parameters using on-board DIP switches.

The demo package includes the following:

- DDR3 IP core configuration files (.lpc, .ipx)
- Verilog source code for the demo logic design
- Lattice Diamond™ implementation project file (.ldf) and preference file (.lpf) for the demo project
- Aldec® Active-HDL™ simulation scripts (.do) and a Verilog test bench
- DDR3 demo bitstream file (.bit)

Demo design hardware requirements:

- LatticeECP3 Versa Evaluation Board with LatticeECP3-35EA FPGA, 484-ball fpBGA package.
- 12V DC power supply for LatticeECP3 Versa Evaluation Board
- Windows PC or Linux machine for implementing the demo project and downloading the bitstream
- USB cable for programming the LatticeECP3 device

Demo design software requirements:

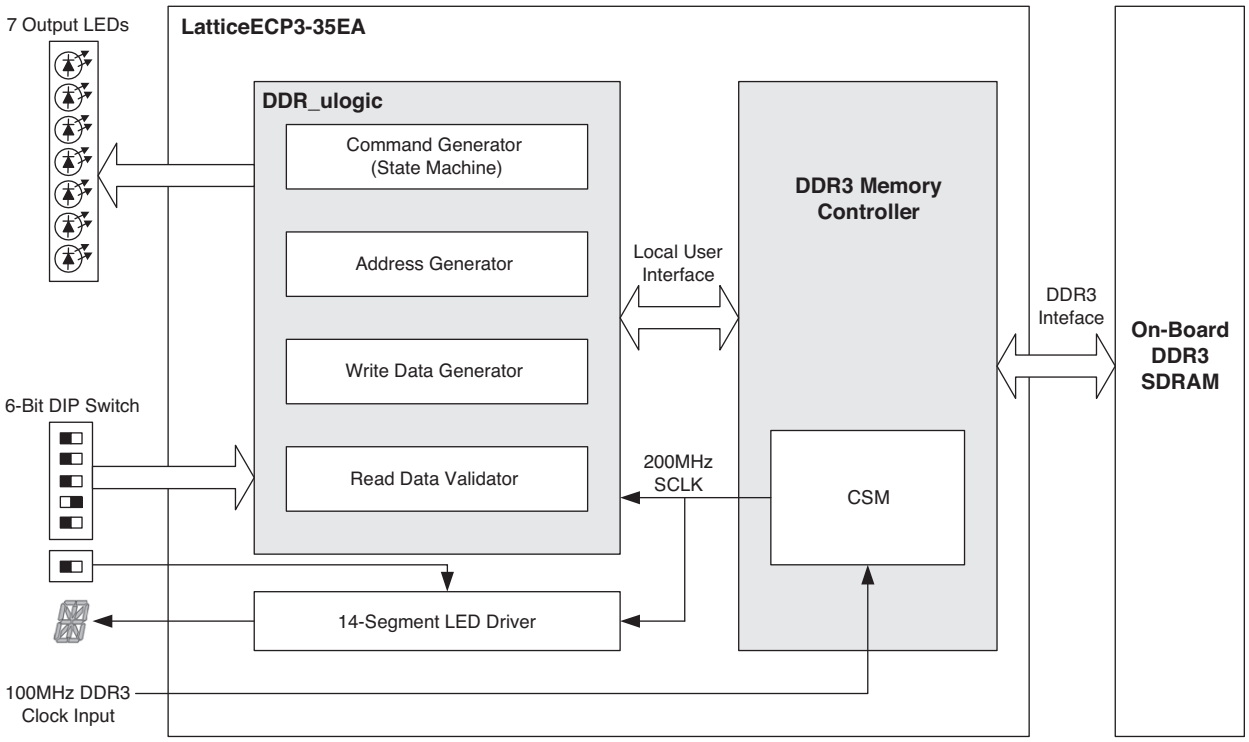
- Lattice Diamond design software, version 1.2 or later
- ispVM™ System software (version 18 or later) for bitstream download

DDR3 Demo Design Overview

The DDR3 demo design consists of two major parts: a DDR3 controller IP core and the user logic block. The DDR3 SDRAM Controller IP core interfaces to the on-board external DDR3 SDRAM directly and performs control, read and write operations. The latter includes a function block that exercises and analyzes the DDR3 data stream. The user logic block generates test data to be written on the SDRAM. The DDR3 Controller then writes the data on the on-board DDR3 SDRAM. The DDR3 controller also reads the SDRAM data which it passes to the user logic block. The user logic block compares the read data with the standard expected data and flags an error if it encounters a data mismatch. The demo parameters can be modified using on-board DIP switches. The status of the running demo design is displayed with the help of on-board LEDs.

Further sections describe the sub-modules in the user logic design in detail. Figure 1 illustrates a block diagram of the demo design.

Figure 1. DDR3 Demo Design Block Diagram



DDR3 SDRAM Controller IP Core

The IP core used to generate the DDR3 controller core is the DDR3 SDRAM Controller IP core, version 1.2. The user must install version 1.2 before generating the IP core and running the demo. The core generated with this IP core interfaces directly with the external, on-board DDR3 SDRAM and performs control operations. The demo has been designed to support a DDR3 data bus width of 16 bits since the DDR3 memory module installed in the LatticeECP3 Versa Evaluation Board is 16 bits wide. See EB62, the LatticeECP3 Versa Development Kit User's Guide for further information on the DDR3 SDRAM module used in this demo. Once a DDR3 core is generated with a supported data width, the whole demo design can be simulated and implemented without modifying the code. A DDR3 IP core configuration file (ddr3core.lpc) is provided in the demo package. This configuration file should be used to make changes to the core and/or regenerate the core. In the Linux platform, the DDR3 SDRAM Controller IP core should be downloaded, uncompressed and placed in the folder diamond/1.2/module. The DDR3 SDRAM Controller IP core will appear in the IP core tree.

User Logic

The user logic implemented in the DDR3 demo design provides the following functions:

- State machine programs the mode registers and controls DDR3 read and write operations
- Address generation
- Write data generation
- Read data validation
- Control and observation

Demo Control State Machine

The state machine controls the demo using the user control input through a 6-bit DIP switch. Once the LatticeECP3 device is programmed or a system reset is applied by pressing the GSR button, the state machine programs all DDR3 mode registers (MR0~MR3) based on the user test configuration (DIP switch setting). Then, it gen-

erates a write command sequence. The write command can be repeated up to 32 times using either the command burst feature of the core or multiples of single write commands depending on the user setting. After the write command sequence, a read command sequence is initiated. The read command sequence can also be repeated up to 32 times in the same way as the write command sequence. The read command sequence that follows the write command sequence must include the same number of commands as the as the write command sequence. The state machine makes sure that both the write and the following read command sequences are always the same even when the user test configuration is changed at any time during the command sequences. This allows the DDR3 demo to be dynamically reconfigurable.

Address Generation
The address generation block provides the start address for the current user read/write command which is generated by the state machine. When the burst command mode is enabled, the address generation block automatically calculates the next address according to the demo control input.

Write Data Generation
The demo uses both PRBS and sequential data patterns. When PRBS is selected, a 128-bit PRBS pattern generator is implemented to the local write data bus to generate a 16-bit DDR3 data pattern. For 16-bit DDR3 data, the lower 64 bits [63:0] of the 128-bit PRBS is allocated to the local data bus. For the sequential data pattern, the demo design uses only a 32-bit sequential data pattern generator to provide 16-bit DDR3 data. This 32-bit data pattern is allocated to each 32-bit wide local data bus slot. For example, a 16-bit DDR3 bus requires a 64-bit local data bus which has two identically sequenced 32-bit patterns allocated on two 32-bit slots. The write data generation is enabled and driven by the datain_rdy signal assertions.

Read Data Validation
The read data checker validates the read data from the DDR3 memory module. To do this, it generates the expected data patterns using exactly the same data sequences as the Write Data Generator block. The expected data generation is enabled and driven by the read_data_valid signal assertions. The read data captured by read_data_valid is compared with the expected data generated from the Expected Data Generator block. When there is a mismatch between both data patterns, the demo design will flag the error detection signal.

Control and Observation
The Control and Observation block includes the demo control input and result display functions. The demo control input uses six out of eight DIP switches available on the LatticeECP3 Versa Evaluation Board. The demo result is displayed through the seven LEDs on the board. See the following section for descriptions of the demo control input switches and the result display LEDs. A 14-segment LED display is also provided for a quick assessment of the operation. When the read and write operation is running and there is no data mismatch, the segments of the display blink in a clockwise pattern. The blink rate is dependent on the amount of data that is read. As soon as an error is detected, all 14 segments blink simultaneously.

LatticeECP3 Versa Evaluation Board

This section describes the LatticeECP3 Versa Evaluation Board as it relates to the DDR3 demo.

DDR3 Memory

The LatticeECP3 Versa Evaluation Board has on-board 16-bit DDR3 memory. The DDR3 memory module on the board that is used for the DDR3 demo is a 96-pin unbuffered DDR3 SDRAM. The demo design uses up to 1GB of memory space with one chip select configuration.

Programming Cable Connections

The LatticeECP3 device on the LatticeECP3 Versa Evaluation Board can be programmed via the USB port or through the SPI Flash interface. If the USB port is used, it can both program the device and use the Reveal™ logic analyzer to trace internal signal paths. The J2 connector is used for the USB cable. This demo uses the USB port. The instructions to set up the LatticeECP3 Versa Evaluation Board for use with this demo are discussed later in this document.

Port Assignments and Descriptions

Table 1 lists all the signals used by the DDR3 SDRAM Controller IP core in the demo design to control and interface to the on-board DDR3 SDRAM. For details, refer to IPUG80 DDR3 SDRAM Controller IP Core User's Guide.

Table 2 lists all the interfaces which are available to the user to either dynamically configure the parameters of the design (input mode) or observe the running status of the demo (output mode).

Table 1. DDR3 Bus Interface

Port Name	Active	Direction	Description
em_ddr_reset_n	Low	Output	Asynchronous reset signal from the controller to the memory device. Asserted by the controller for the duration of power on reset or GSR_N
em_ddr_clk[CLKO_WIDTH-1:0]	N/A	Output	400 MHz memory clock generated by the controller
em_ ddr_clk_n[CLKO_WIDTH-1:0]	N/A	Output	400 MHz complimentary memory clock generated by the controller
em_ ddr_cke[CKE_WIDTH-1:0]	High	Output	Memory clock enable generated by the controller
em_ ddr_addr[ROW_WIDTH-1:0]	N/A	Output	Memory address bus, multiplexed row and column address for the memory
em_ ddr_ba[2:0]	N/A	Output	Memory bank address
em_ ddr_data[DATA_WIDTH-1:0]	N/A	In/Out	Memory bi-directional data bus
em_ ddr_dm[(DATA_WIDTH/8)-1:0]	High	Output	DDR3 memory write data mask
em_ ddr_dqs[DQS_WIDTH-1:0]	N/A	In/Out	Memory bi-directional data strobe
em_ ddr_dqs_n[DQS_WIDTH-1:0]	N/A	In/Out	Memory complementary bi-directional data strobe
em_ ddr_cs_n[CS_WIDTH-1:0]	Low	Output	Memory chip select
em_ ddr_cas_n	Low	Output	Memory column address strobe
em_ ddr_ras_n	Low	Output	Memory row address strobe
em_ ddr_we_n	Low	Output	Memory write enable
em_ ddr_odt[CS_WIDTH-1:0]	High	Output	Memory on-die termination control

Table 2. Demo User Interface Ports

Port Name	Active	Direction	Description
Clk_in	N/A	Input	Reference clock connected to a dedicated PLL clock input of the LatticeECP3-35EA FPGA.
Reset_n	Low	Input	Asynchronous reset connected to the GSRN button (SW1). This resets the entire demo system including the DDR3 IP core when asserted.
seg[14:0]	N/A	Output	14-Segment LED Display. The segments of the 14-segment display (D23) blink in a clockwise pattern as long as no data mismatch has occurred. As soon as a data mismatch occurs, all the LED segments blink together in Alarm mode. A system reset must be applied to start the transactions afresh.
Dip_sw[5:0]	N/A	Input	User test configuration input. See the Control and Observation Port Description section of this document for further information.
Oled[6:0]	N/A	Output	Demo result LED indicator output. See the Control and Observation Port Description section of this document for further information.

Control and Observation Port Descriptions

The Control and Observation Ports include the user interface ports as described in Table 2. This section describes in detail the two main control (DIP switch) and observation (LED) ports. Table 3 describes the functionality of each DIP switch and how design parameters can be changed by changing the position of the switches. The recommended default setting for the DIP switch is for all switches to be in the OFF position (towards the edge of the board). The ON position is when the DIP switch level is towards ON which is printed on the DIP Switch case.

Table 3. DIP Switch Definitions

Signal Name	DIP Switch Number	Assigned Function Control	Setting	Description
dip_sw[0]	SW3-1	Burst Length Selection	OFF	Set Burst Length to BL8
			ON	Set Burst Length to BC4
dip_sw[1]	SW3-2	On-the-Fly (OTF) Mode. Works with Burst Length Selection.	OFF	Fixed burst size mode. The core is set to BL8 or BC4 during initialization depending on the Burst Length Selection setting. BL8 or BC4 is set by dip_sw[0].
			ON	OTF mode. Dynamic burst length change is controlled by the Burst Length Selection switch.
dip_sw[2]	SW3-3	Command Burst Enable. The core repeats a user R/W command as many times as specified by the Maximum Command Size setting.	OFF	Enable command burst mode. 32-command burst when Maximum Command Size = 1. User-selectable burst size when Maximum Command Size = 0.
			ON	Disable command burst mode. Demo works in the single command mode. Manual single command repetitions are performed instead of using the command burst mode. The single command repetition is also controlled by the Maximum Command Size setting.
dip_sw[3]	SW3-4	Maximum Command Size	OFF	Use maximum command burst size/repetition When the command burst mode is enabled, the DDR3 core performs a 32-command burst on a user read or write command. When disabled, the maximum single command repetition is defined to 32 times. The demo back-end logic generates consecutive 32 single read or write commands.
			ON	Use user-specified command burst size Both the command burst and single command repetition modes use the burst size value (UsrCmdBrstCnt) defined in the ddr3_test_params.v file. The allowed values are 2, 4, 8, 16 or 32 with the default value set to 2. Note that 1 can be used only when OTF is disabled because dynamic OTF change from BC4 to BL8 may result in read data corruption due to the limitation of addressing.
dip_sw[4]	SW3-5	Data Mode	OFF	PRBS data patterns are used for the DDR3 demo. 128-bit pseudo random patterns are generated. In this demo (16-bit DDR3 SDRAM), the lower half [63:0] of the 128-bit PRBS data is used for the 64 bit local data bus.
			ON	Sequential data patterns. 32-bit sequential data pattern generators are used. For example, the 16-bit DDR3 demo has two 32-bit sequential patterns allocated to each 32-bit slot on a local data bus.
dip_sw[5]	SW3-6	14-Segment Enable	OFF	Enables the 14-segment LED display (D23). The segments of the 14-segment display blink in circular fashion as long as no data mismatch has occurred. As soon as a data mismatch occurs, the LED segment blinks in Alarm mode to indicate there is a data mismatch. A system reset must be applied to restart the transactions.
			ON	Disable

Output Status LEDs

Seven LEDs are used to indicate the demo progress and results. In Table 4, the Assigned column shows the LatticeECP3 ball numbers printed on the LatticeECP3 Versa Evaluation Board. Each LED indicates a particular status or condition of the DDR3 demo design, DDR3 controller core to be specific.

Table 4. Output LED Definitions

Signal Name	Assigned	Function	Color	Status	Description
OLED[0]	D25	Heartbeat indicator	Yellow	Blink	This LED indicates that the board is alive, and the core is receiving the clock input.
				OFF	The core is unable to receive the clock signal.
OLED[1]	D24	INIT done and core ready indicator	Yellow	ON	This LED indicates that the core and memory initialization is complete, and the core is ready to accept user commands.
				OFF	The core is not ready to accept new commands.
OLED[2]	D22	Write indicator	Green	ON	This LED indicates that the core's write operation is properly working by detecting the datain_rdy signal assertions.
				OFF	The core is not ready to receive write data from the user.
OLED[3]	D21	Read indicator	Green	ON	This LED indicates that the core's read operation is properly working by detecting the read_data_valid signal assertions.
				OFF	Indicates invalid data on read-data bus.
OLED[4]	D26	Error indicator	Red	Blink	This LED will start blinking when the first data mismatch error is detected. A system reset must be applied to clear this indicator.
				OFF	No error detected
	D27	Not used			
OLED[5]	D28	DDR3 transaction indicator	Blue	Blink	This LED indicates that DDR3 write-then-read operations are occurring. The more read data that comes in, the faster this LED blinks.
				OFF	No valid read data is detected
OLED[6]	D29	Valid data indicator	Blue	Blink	This LED confirms that proper DDR3 read/write transactions are being performed with actual valid data. If the received data is null (all "0" or all "1") this LED will not blink.
				OFF	The received data is null (all '0' or '1').

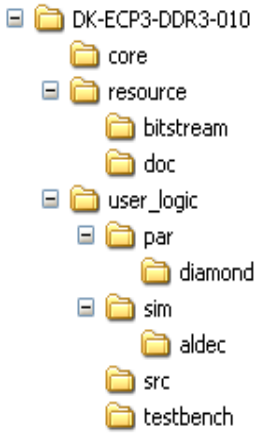
Table 5 indicates the status of all LEDs during successful operation of the demo.

Note: After downloading the bitstream, the Error Indicator LED (D26) blinks and other LEDs continue work as expected. The GSRN button should be pressed to reset the error counter.

Demo Package Directory Structure

By default the DDR3 demo package is installed in **C:\Lattice_DevKits\DK-ECP3-DDR3-010\.** You can, however, install the DDR3 demo package in a location of your choice (<*demo_directory*>) in Windows and root/DK-ECP3-DDR3-010 in Linux. You need to untar the *.tar.gz file. The directory structure of DDR3 demo package is shown in Figure 2. The demo package includes three top-level folders: the core folder, resource folder and user_logic folder.

Figure 2. DDR3 Demo Package Directory Structure



Core Folder

The core folder includes a DDR3 IP core configuration file (ddr3core.lpc). A complete DDR3 IP core can be updated and regenerated using this file through the IPexpress™ tool.

Resource Folder

The resource folder includes the following subfolders:

- **Bitstream** – This folder includes a 16-bit demo bitstream. This bitstream is fully tested and can be used to verify the demo setup.
- **Doc** – This folder contains user documents.

User_logic Folder

The user_logic folder includes the following subfolders:

- **Par** – This folder includes the implementation project files for the Diamond design software and other necessary files including the place and route (PAR) preference and the post-route trace preference files.
- **Sim** – This folder includes the simulation script file for running a simulation in Aldec Active-HDL.
- **Src** – This folder includes all RTL source files used for the demo.
- **Testbench** – This folder includes the test bench file for the demo design (ddr3_test_top_tb.v).

Running the Demo

Step 1. Core Generation

The DDR3 demo design does not come with a fully-generated DDR3 SDRAM Controller IP core. The user must generate the core using the default lpc file (**ddr3core.lpc**) provided in *<demo_directory>***\core** folder. Follow these steps to generate the core using IPexpress.

a. Open the IPexpress tool by selecting:

   Start->Programs->Lattice Diamond 1.2->Accessories->IPexpress

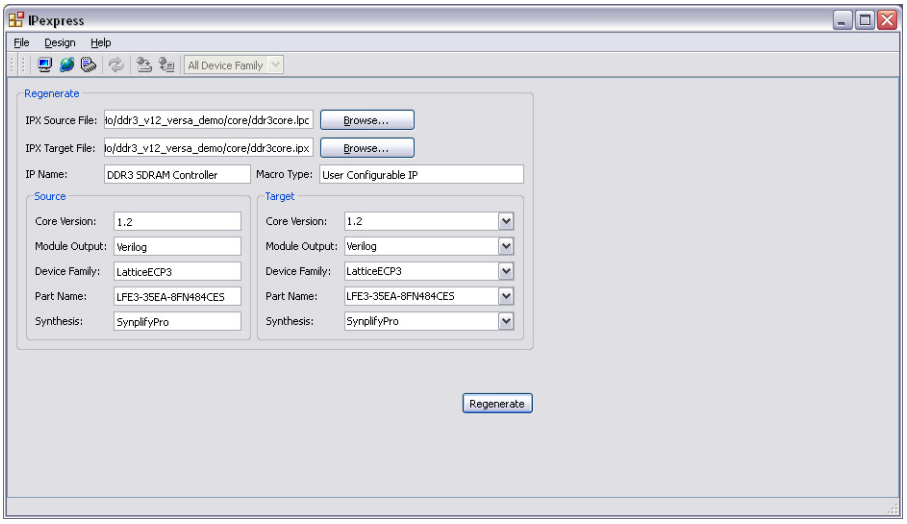
   Note: this invokes IPexpress as a standalone program without having to go through the Diamond Design Software.

b. Select the **Regenerate** icon (3rd icon from the left)

c. Browse to the core folder where the lpc file is located. Select the ddr3core.lpc file and select **Open**.

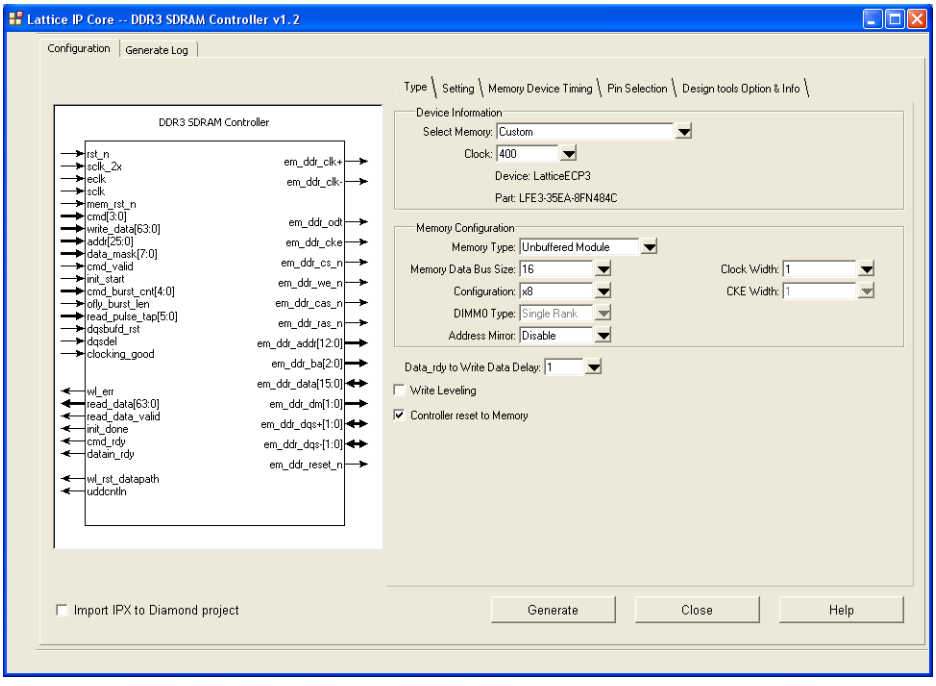
d. Make sure the Source and Target devices are the same (family, package, speed) as shown in Figure 3.

Figure 3. DDR3 SDRAM Controller v1.2 Regenerate Window



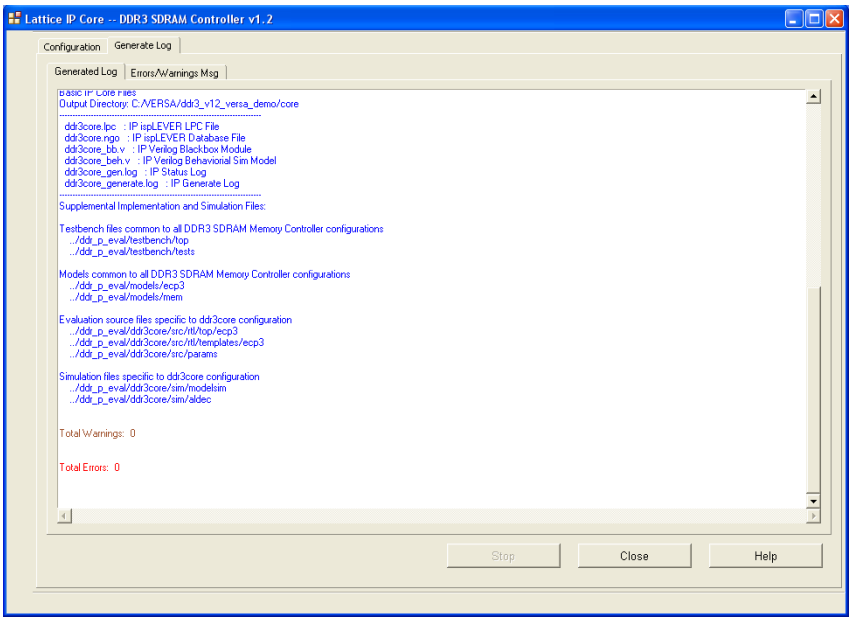
e. Select **Regenerate**. A window similar to the DDR3 SDRAM Controller IP core GUI shown in Figure 4 is launched.

Figure 4. DDR3 SDRAM Controller v1.2 Configuration Window



f. Select **Generate**. The DDR3 IP core files for the configurations as specified in the DDR3 SDRAM Controller IP core .lpc file and GUI will be generated inside the core folder where the .lpc file is located. Upon successful completion, you should see output similar to Figure 5.

Figure 5. DDR3 SDRAM Controller v1.2 Generate Log Window



g. Select **Close** to exit IPexpress.

Step 2. Running Simulation (Windows Only)

The demo package provides the simulation scripts for Active-HDL.

a. Open the simulation script file, **ddr3_ecp3_demo.do**, located in *<demo_directory>***\user_logic\sim\aldec** and update the SIM_PWD and Lattice Tool path names with your local folder names. You can update this file with your favorite editor outside of Diamond or you can update the file from within Diamond using the source editor or from within Active-HDL.

b. Copy the following core behavioral model and the IP core top-level file to the designated names:

- Copy *<demo_directory>***\core\ddr3core_beh.v** to *<demo_directory>***\core\ddr3core.v**.
- Copy *<demo_directory>***\core\ddr_p_eval\ddr3core\src\rtl\top\ecp3\ddr3_sdram_mem_top_wrapper.v** to *<demo_directory>***\core\ddr3_sdram_mem_top.v**

Note: The renaming of the above Verilog files ensures that specific behavioral simulation files are chosen, with the same name, as instantiated in the files placed higher in the hierarchy.

c. Launch Active-HDL Lattice Edition from within Diamond by selecting **Tool->Active-HDL Lattice Edition**. A **Getting Started** dialog box appears. Select **Cancel** since you don't need to create a new workspace.

d. In Active-HDL, select **Tools->Execute Macro**, and then browse to the folder where the Active-HDL script is located: *<demo_directory>***\user_logic\sim\aldec**.

e. Select the **ddr3_ecp3_demo.do** file and then select **Open**.

f. Once the simulation is finished, check the status of the err_det signal along with other signals of interest. The err_det signal should remain low at all times for a successful demo.

g. Exit Active-HDL.

The simulation run time is set to 10 us by default.

Step 3. Running Place & Route

This section illustrates how to synthesize the design, and subsequently place & route the design to generate the bitstream file to download into the device. It has to be ensured that the preference file **ecp3_ddr3.lpf** located in *<demo_directory>***user_logic\par\diamond** is used in the design. The same procedure should be followed in the Linux platform also. For details on the Linux version of Diamond design software, refer to the Lattice Diamond Installation Notice.

a. Launch the Lattice Diamond design software.

b. Select **File->Open-> Project** and browse to *<demo_directory>***user_logic\par\diamond**.

c. Select the DDR3 demo project file for Diamond, **ecp3_ddr3.ldf**, then select **Open**.

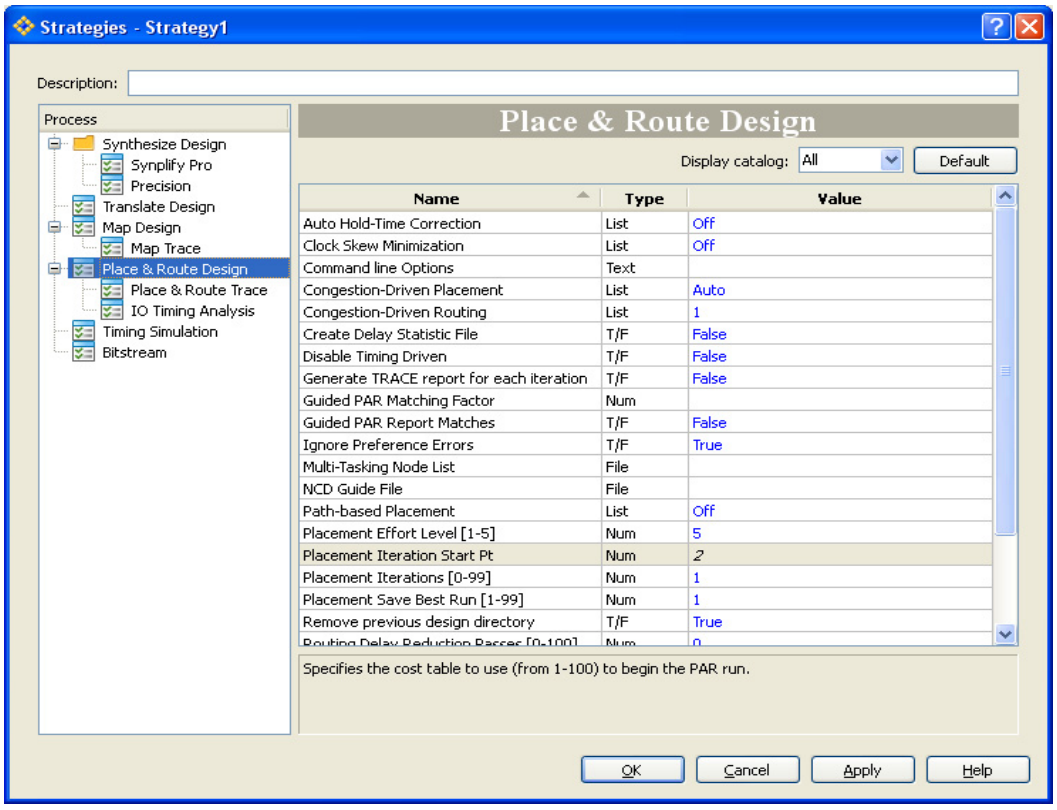
d. Double-click **Place & Route Design** in the **Process** pane. The software will run synthesis, and place and route. When place & route is complete, you will see **Done: completed successfully** in the console window.

e. Double-click **Place & Route Trace** under **Place & Route Design** in the **Process** window. In the **Reports** window, select **Place & Route Trace** under **Analysis Reports**.

f. Check the static timing results from the Analysis Result pane. All user timing constraints are displayed in the report. Any violation is indicated in red, otherwise the constraints are displayed in blue on passing. If there is a violation, it means that the PAR result for the current seed run does not meet the all timing requirements.

g. If a violation is reported, change to the next placement seed and check the timing result again. To change to the next placement seed, select the **File List** tab, and double-click on **Strategy 1** under the **Strategies** heading. A window opens as shown in Figure 6. Select **Place & Route Design**. Select **Placement Iteration Start Pt** (as shown in the figure) and repeat this process until all timing requirements are met.

Figure 6. Lattice Diamond Software Strategy Settings



h. When you have a successful timing result, you can exit the Timing Analysis window. Then, double-click on **Bitstream File** in the **Process** pane to generate a bitstream file that will be downloaded onto the LatticeECP3 Versa Evaluation Board.

Step 4. Setting Up the DDR3 Demo

a. Be sure all switches for the SW3 DIP switch are in the OFF position.

b. Connect a USB cable to connector on the board.

c. Connect the USB cable to a PC that has Lattice Diamond design software and Lattice ispVM software.

d. Turn the board power on by connecting the power adapter plug into the board power jack, J1.

Step 5. Running the Demo

a. Launch the ispVM System software, which is outside of Diamond on the **Accessories** menu. For Linux , type **ispvm** in the command line. Please refer to the Lattice Diamond Installation Notice for proper setting of Environment Variables.

b. Scan the JTAG chain by selecting the **Scan Chain** button (or **F2**).

c. If the tool does not detect the LFE3-35EA device or USB cable, go to **Options->Cable and I/O Port Setup**. The Cable and I/O Port Setup window opens. Select **Auto Detect** and select **USB2**. Select **OK** and select **Scan** as described in step b.

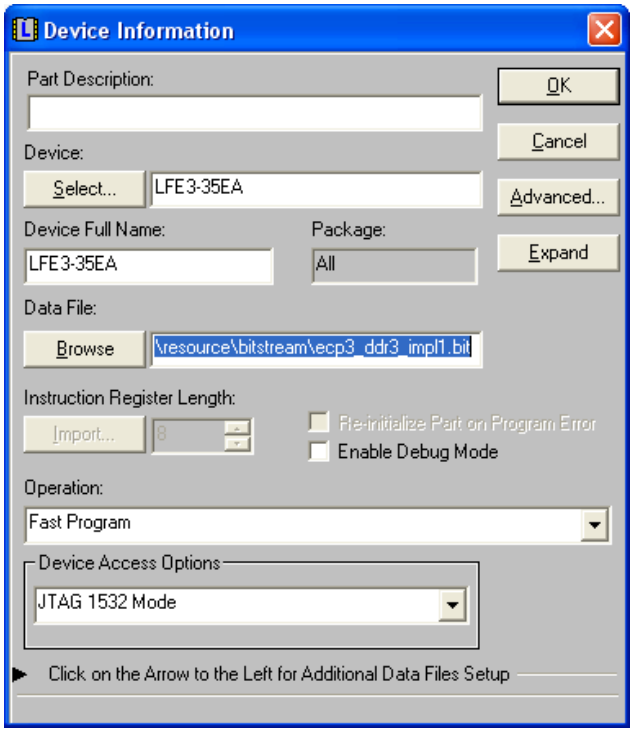
If the board does not get detected in the Linux platform, refer to the ispVM System Linux Installation and Setup Manual (ispVMLinuxInstallation.pdf) in the ispVM System installation directory

d. The device **LFE3-35EA** is displayed under **Device List** section in the **Configuration** setup window of the ispVM window. Double-click the identified device name (**LFE3-35EA**). The **Device Information** dialog box will appear as shown in Figure 7.

e. Set **Device Access Options** to **JTAG1532 Mode** and **Operation** to **Fast Program** (default setting).

f. Double-click on the blank tab under the section **File Name** adjacent to LFE3-35EA device. Click the **Browse** button for the Data File entry and browse to the project implementation folder where the generated bitstream file is located **(**<*demo_directory*>**\user_logic\par\diamond\impl1**). Double-click on **ecp3_ddr3_impl1.bit**. The file is displayed in the Device Information dialog box, as shown in Figure 7.

Figure 7. ispVM Download Mode Settings



h. Select the **Go** button from the main ispVM GUI window to download the bitstream.

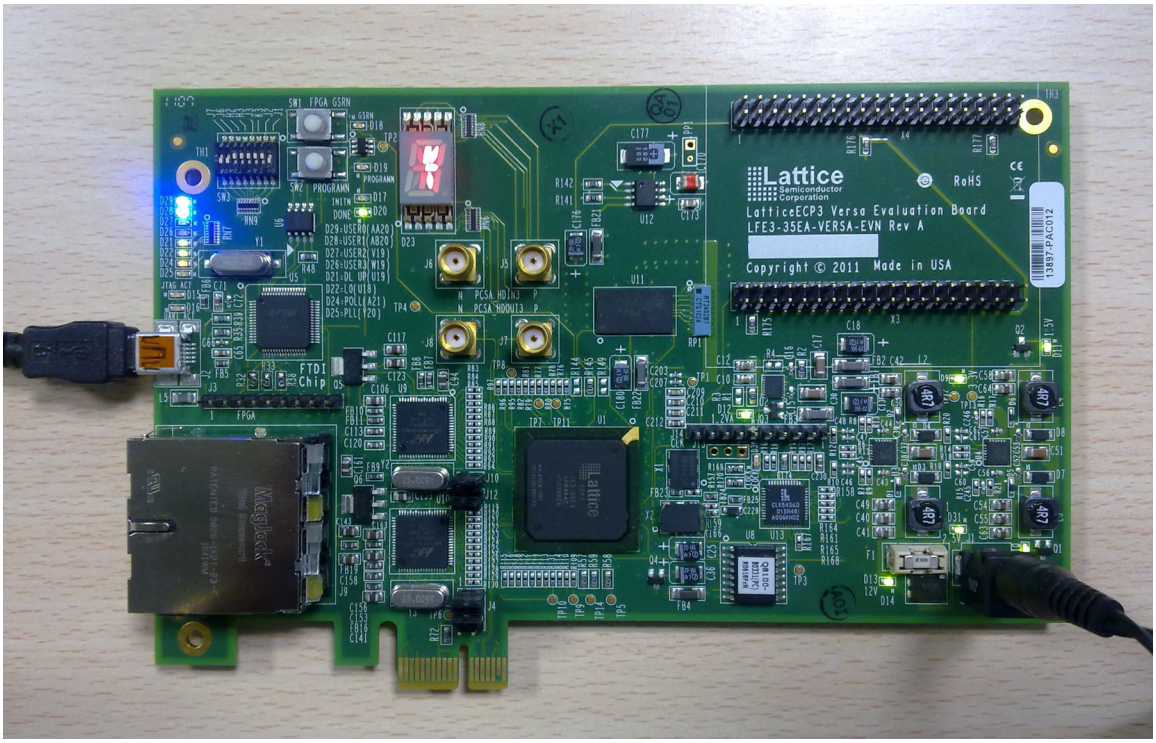
i. Refer to Table 5 to verify whether LEDs are blinking as mentioned. If the red LED-D26 (Error) blinks and all segments of 14-segment display blink together, press the **GSRN** button (SW1) to clear the error counter and reset the design.

Table 5. Expected LED Status from Successful Demo

Name	Expected Status	Remark
D25	Blink	Yellow LED with constant blinking rate.
D24	ON	Yellow LED.
D22	ON	Green LED.
D21	ON	Green LED.
D26	OFF	Red LED. Begins blinking if a data mismatch error is detected.
D27	OFF	Not used.
D28	Blink	Blue LED. Blinking rate changes according to the data rate.
D29	Blink	Blue LED.

j. A LatticeECP3 Versa Evaluation Board running the DDR3 demo is shown in Figure 8. Sometimes, changing a DIP switch position may not show the expected results. The **GSRN** button should be pressed in this case. For example, by setting SW3-2 to **ON**, the demo enters On-the-Fly mode. In this mode, SW3-1 can be set to ON or OFF to dynamically change the burst length. You can observe the change in the blinking rate of D28 and the 14-segment LED display. If this mode does not initiate, press the **GSRN** button after the SW3-2 transition.

Figure 8. LatticeECP3 Versa Evaluation Board



References

The following documents provide more information:

- DS1021, LatticeECP3 Family Data Sheet
- EB62, LatticeECP3 Versa Evaluation Board User's Guide

Technical Support Assistance

Hotline: 1-800-LATTICE (North America)
+1-503-268-8001 (Outside North America)
e-mail: techsupport@latticesemi.com
Internet: www.latticesemi.com

Revision History

Date	Version	Change Summary
April 2011	01.0	Initial release.
May 2011	01.1	