Transmission of High-Speed Serial Signals Over Common Cable Media

Technical Note

FPGA-TN-02196-1.9

December 2019

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1. Introduction

Designers are often faced with moving serial data from one location to another, over moderate distances, and in the most efficient manner. Transmitting large blocks of parallel data originally required large banks of parallel line drivers and receivers. With the introduction of serializer/deserializer (SERDES) devices, designers can convert wide parallel data buses into a serial data stream. This permits smaller, less expensive cables and connectors to be used, and reduces the interference and EMI generated in large cable bundles. Today, Lattice Semiconductor offers SERDES devices that can transfer serial data at several gigabits per second (Gbps) over backplane and cable mediums.

Lattice SERDES devices comply with many industry interface standards. Each industry standard specifies the requirements for an electrical layer of a differential (balanced) interface. Although the standards define a theoretical maximum signaling rate specified across a short trace length on a printed circuit board, as the transmission distance increases, the effects of connectors and cabling reduce this rate. Cable effects can become the primary factor limiting system performance once lengths of tens of meters have been reached.

For some time, electrical connections of very great length over lossy interconnect have been problematic and often times thought not possible for many applications. As transmission rates have increased, higher performance twisted pair cabling has become a necessity. Use of twisted pair cabling for backbone interfaces has pushed the performance past its original specifications. This use of common copper cabling has driven the industry to introduce many new products. This technical note will report the results of the performance of traditional twisted pair cables, compare the use of higher performance cabling from Tyco Electronics and report the results using PCIe cables.

2. Categories 5, 5E, and 6

One standard, the TIA/EIA–568A Commercial Building Telecommunications Cabling Standard, defines the transmission requirements for commercial building telecommunication wiring. It classifies cabling into different categories based upon attenuation and crosstalk losses over frequency. Twisted-pair is classified in different categories. Most differential signaling applications requiring cabling utilize CAT5 and CAT5E cable. The allowable attenuation vs. frequency for CAT5 cable is specified in TIA/EIA–568A.

This report illustrates the performance of differential CML serializer/deserializer devices using different clock-rate and different lengths of standard CAT5-unshielded twisted pair (UTP), CAT5E-Standard-shielded pair (SSP) and CAT6 cable between the serializer/transmitter and receiver/deserializer. The setup used an evaluation board equipped with SMA connectors. These connectors were cabled to an interposer module (Figure 2.1) which translates the SMA connections to an RJ-45 connection.

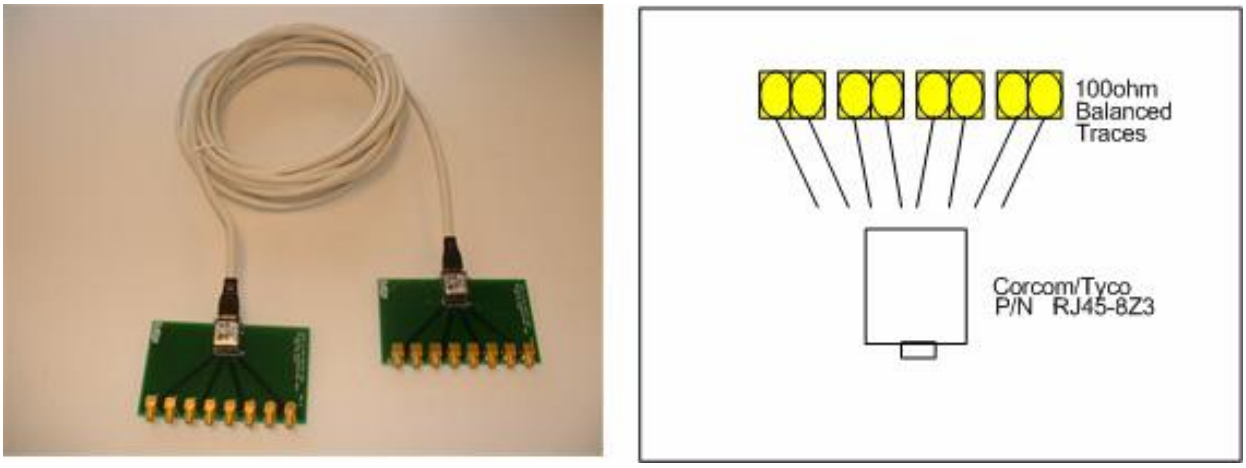

Figure 2.1. SMA to RJ-45 Interposer

Results are presented as cable length vs. data rate. The test was performed using a single channel serial Bit Error Rate Tester (BERT) capable of running up to 3.5 Gbps. Tests were performed by transmitting PRBS 2^{7-1} data from the BERT to

the deserializer and serializer under test and back again. This means that data and clock had to be properly recovered to avoid errors.

The basic test setup is shown in Figure 2.2. The experiment was conducted using two transmit and two receive channels (as shown in diagram) as well as two channels operating independently in a loopback mode. No errors were detected when both channels were running in parallel eliminating any crosstalk concerns.

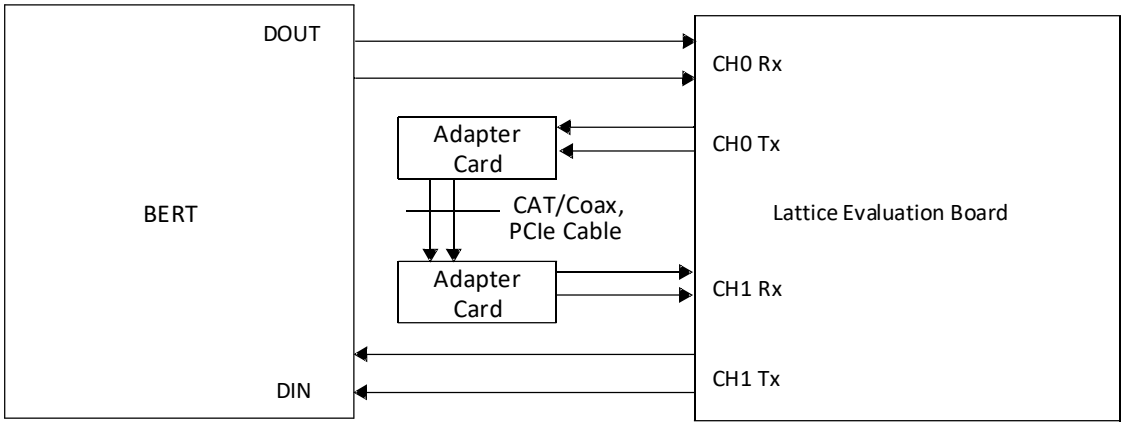

Figure 2.2. Test Set-Up

The results show how increased cable lengths affect bit error rate, while varying the cable connections between the serializer and deserializer. When the cable length is increased, performance will degrade to a point where the link between serializer and deserializer is not longer usable.

The BERT equipment can provide outputs in different formats. The results were determined by go/no-go testing using standard error ratio format. This ratio is simply the number of wrong data bits detected (bit errors) divided by the total number of data bits received. As the different test parameters were changed the test to fail point was recorded. The results are summarized in Table 2.1.

Table 2.1. CAT5, CAT5E and CAT6 Cable Test with PRBS 2^{7-1} Data

Data Rate	Cable Type	Maximum Cable Length Recommended			
		LatticeSC/M Wire Bond Packages	LatticeSC/M Flip-Chip Packages	LatticeECP2M	LatticeECP3
1.25 Gbps	CAT5	30 feet	30 feet	Not Recommended	Not Recommended
	CAT5E	50 feet	50 feet	6 feet	50 feet
	CAT6	50 feet	50 feet	10 feet	50 feet
1.5 Gbps	CAT5	20 feet	30 feet	Not Recommended	Not Recommended
	CAT5E	25 feet	50 feet	6 feet	50 feet
	CAT6	25 feet	50 feet	10 feet	50 feet
2.0 Gbps	CAT5	10 feet	10 feet	Not Recommended	Not Recommended
	CAT5E	25 feet	25 feet	6 feet	50 feet
	CAT6	25 feet	25 feet	10 feet	50 feet
2.5 Gbps	CAT5	Not Recommended	Not Recommended	Not Recommended	Not Recommended
	CAT5E	25 feet	25 feet	6 feet	25 feet
	CAT6	25 feet	25 feet	10 feet	25 feet
3.125 Gbps	CAT5	Not Recommended	Not Recommended	Not Recommended	Not Recommended
	CAT5E	Not Recommended	Not Recommended	Not Recommended	10 feet
	CAT6	Not Recommended	Not Recommended	Not Recommended	25 feet

Note: Test data targeted BER = 1E-12

A similar experiment was also performed using coax cable. The test setup for this experiment is identical to the test setup in Figure 2.2. The performance results using coax cable are summarized in Table 2.2.

Table 2.2. Coax Cable Test with PRBS 2^{7-1} Data

		Maximum Cable Length Recommended	
Data Rate	**Cable Type**	**LatticeSC/M**	**LatticeECP2M**
600 Mbps	Coax (50 ohm)	80 feet	TBD
1.25 Gbps	Coax (50 ohm)	80 feet	TBD
2.5 Gbps	Coax (50 ohm)	40 feet	TBD
3.125 Gbps	Coax (50 ohm)	40 feet	TBD

3. Tyco Electronics 1mm Giga I/O Cable Performance

Tyco Electronics has introduced a hybrid cable assembly that utilizes passive equalization in a very small form factor connector. Utilization of this cable assembly and the on-chip pre-emphasis lengthens the reach of SPP cable mediums. The 1 mm Giga I/O Cable has proven higher data rates can be achieved across longer lengths of cable.

Figure 3.1. Tyco's 1 mm Giga I/O Assembly

Experimentation utilized a LatticeSC/M evaluation board and clock source. The data was looped outside of the LatticeSC/M device through the 1 mm Giga I/O cable and SMA interposer board as shown in Figure 3.2. The LatticeSC/M was programmed with an internal 2-7 PRBS generator/checker. Data was transmitted from the device and looped back to the receiver. The pass/fail condition was based on the success of data and clock being properly recovered without errors detected by the checker

The SERDES reference clock was swept to failure. Test results showed that the 26 ft (8 m) cable with passive equalization and LatticeSC/M provisioned to 48% pre-emphasis could run up to 3.125 Gbps in wire bond packages and up to 3.8 Gbps in flip-chip packages as shown in Table 3.1.

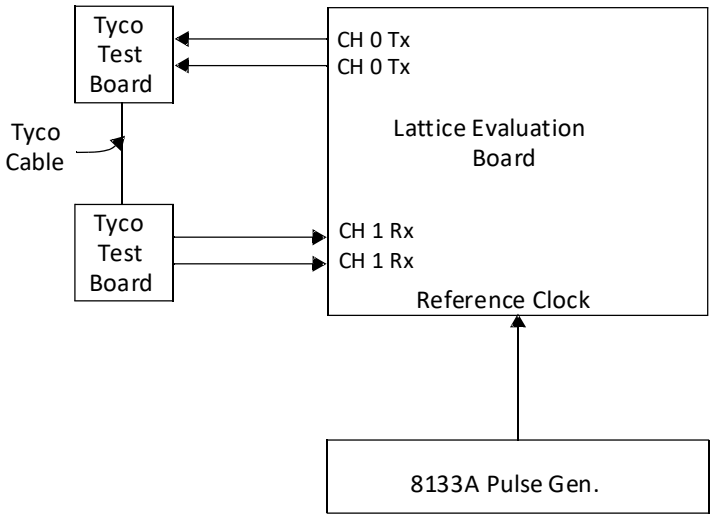

Figure 3.2. 1 mm Giga I/O Test Setup

Table 3.1. Tyco 26 Foot Giga I/O Cable Test with PRBS 2^{7-1} Data

Package Type	Data Rate	Cable Length
LatticeSC/M Wire Bond	3.125 Gbps	26 feet
LatticeSC/M Flip-Chip	3.8 Gbps	26 feet

4. PCIe Cable Performance

PCI Express is the third generation of multi-purpose I/O interface that can be used across the computing industry, from mobile through high-end servers and communication equipment. The broad usage and versatility of this technology allows for system extensions to external input/output subsystems that meet the needs for specific target applications and/or environments.

Cabled PCI Express targets a large number of applications, including but not limited to:

- Split-systems, or disaggregate PCs, with a desktop console that contains removable media drives, memory modules, I/O ports and audio jacks
- I/O expansion to extend the I/O card capabilities of the main system for support of different form factors, including legacy, test and measurement and instrumentation equipment
- Server expansion I/O to support conventional PCI Express add-in cards and/or ExpressModules
- Location of the graphic subsystem external to the main systems unit

System-level support for cabled PCI Express is possible through implementation on expansion cards or direct from a system board.

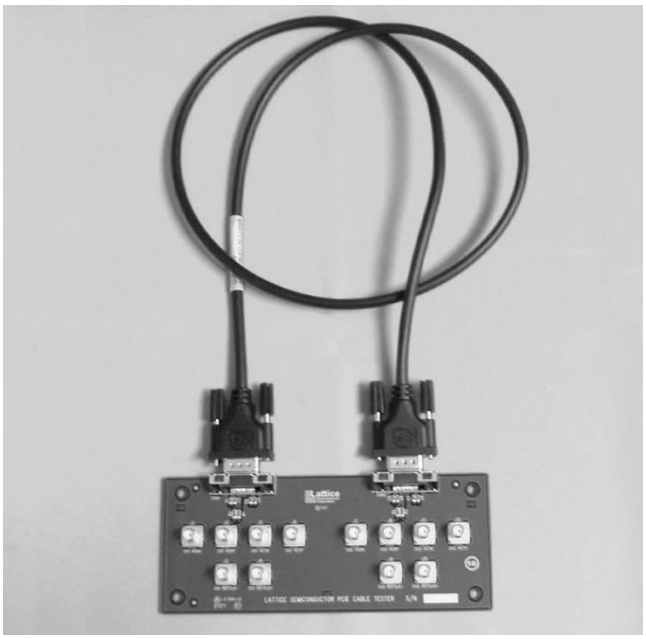

Figure 4.1. PCIe Cable Adapter

Experimentation utilized Lattice evaluation boards and clock source. Results are presented as error free cable length at 2.5 Gbps data rate. The test was performed using a single channel serial bit Error Rate Tester (BERT). Tests were performed by transmitting PRBS 27-1 and CJPAT data from the BERT to the SERDES under test and back again. This means the data and clock had to be properly recovered to avoid errors.

The test setup for this experiment is identical to the test setup in Figure 2.2. The results are summarized in Table 4.1.

Table 4.1. PCIe Cable Test with PRBS 2^{7-1} and CJPAT Data

Data Rate	Cable Type	Maximum Cable Length Recommended	
		Lattice SC/M	Lattice ECP2M
2.5 Gbps	PCI Express	7 meters	7 meters

5. Conclusion

The use of twisted pair cabling is possible for high-speed serial data rates. Lattice SERDES devices allow easy system design migration into wired back-bone configurations. The use of SSP and UTP cables for patch-cord and cross connect jumpers is possible when the designer understands the attenuation trade-offs. To ensure overall system integrity for data rate over 1 Gbps, cables need to be terminated with high quality connecting hardware.

For longer cable applications, the use of hybrid cable assemblies plays a vital role. Serial data rates greater than 2.5 Gbps can be achieved across moderate distances of cable. This is possible because of the rapid advances in the SERDES I/O and copper interconnect design that can accommodate or even compensate for frequency dependent parameters. With careful system design, designers, who optimize the passive cable equalization and the active pre-emphasis and equalization of the Lattice SERDES, will achieve reliable high-speed systems.

Appendix A. Adapter Card Schematics

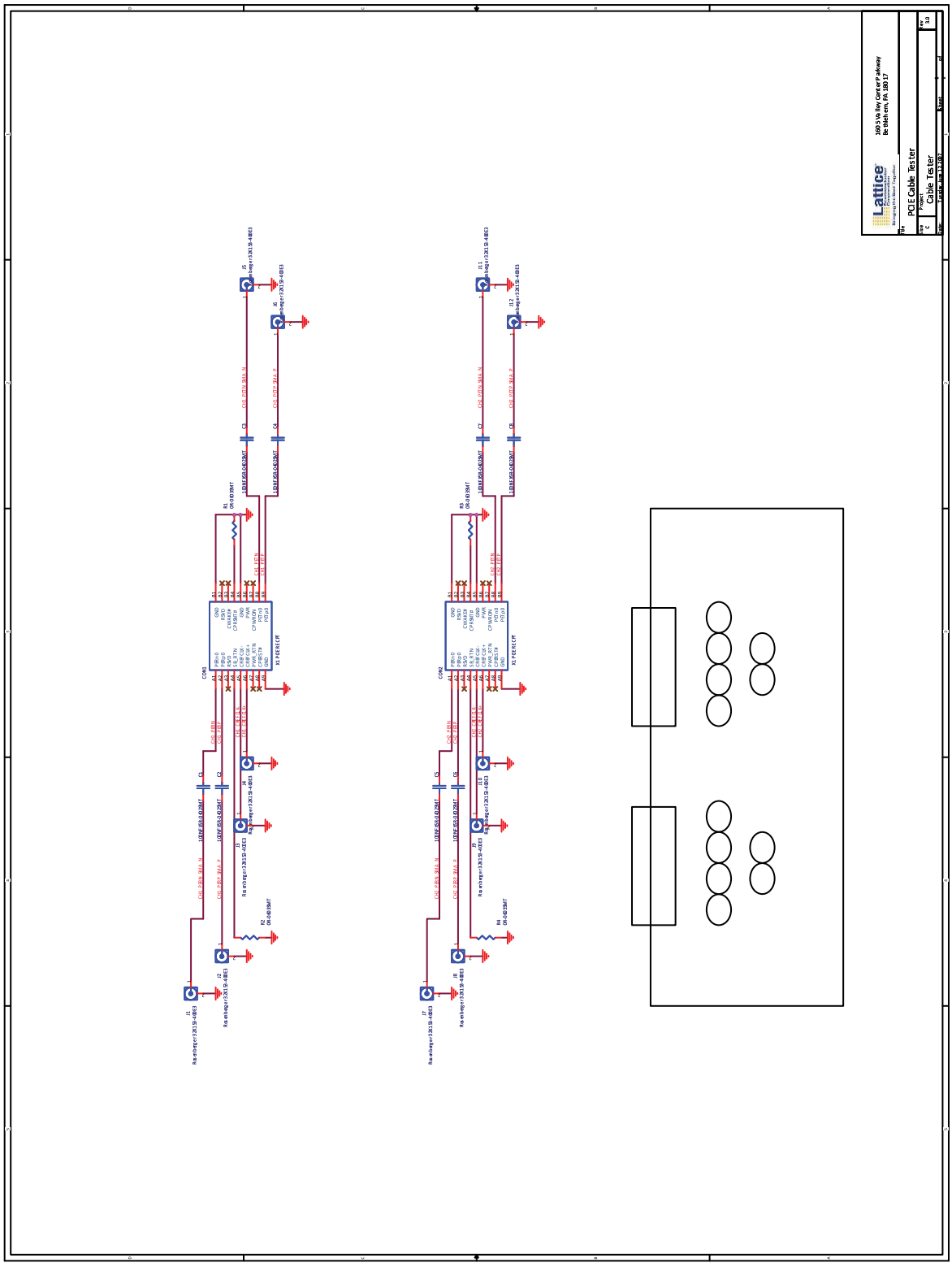

Figure A.1. PCI Express Cable Adapter

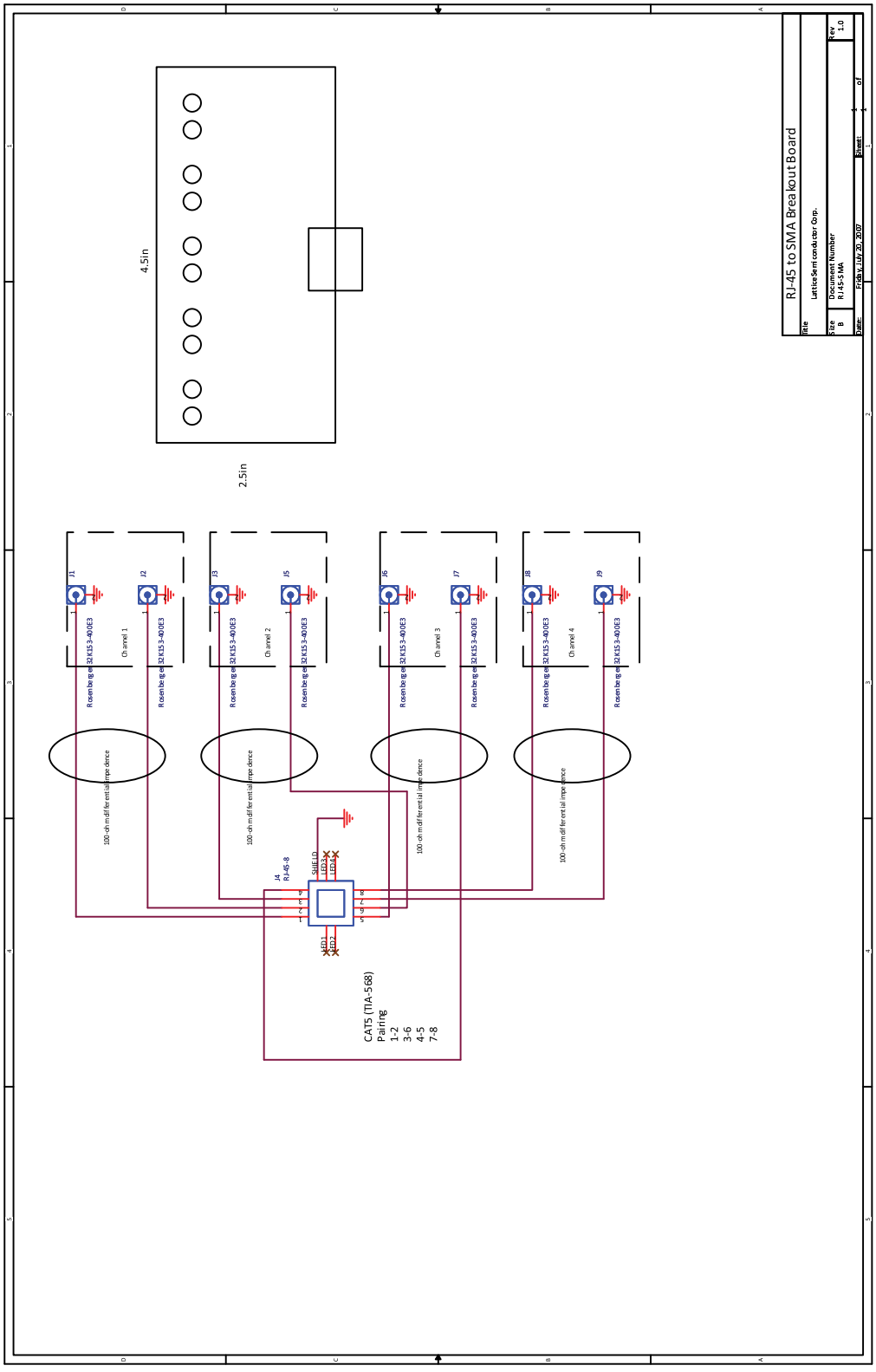

Figure A.2. SMA to RJ-45 Interposer

References

- LatticeECP3 Family Data Sheet (FPGA-DS-02074)
- LatticeECP2M Family Data Sheet
- LatticeSC/M Family Data Sheet
- Tyco Electronics - 1mm GIGA I/O Cable Assembly Customer Evaluation Kit User's Guide
- PCI Express External Cabling Specification, Revision 1.0

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

Revision History

Revision 1.9, December 2019

Section	Change Summary
All	• Changed document number from TN1066 to FPGA-TN-02196. • Updated document template.
Disclaimers	Added this section.

Revision 1.8, February 2012

Section	Change Summary
All	Updated document with new corporate logo.

Revision 1.7, October 2011

Section	Change Summary
Categories 5, 5E, and 6	Updated Table 2.1., CAT5, CAT5E and CAT6 Cable Test with PRBS 27-1 Data.

Revision 1.6, August 2010

Section	Change Summary
Categories 5, 5E, and 6	Added LattticeECP3 Family and 3.125 Gbps data to Table 2.1., CAT5, CAT5E and CAT6 Cable Test

Revision 1.5, July 2008

Section	Change Summary
Appendix A	Added Appendix A. Adapter Card Schematics.

Revision 1.4, January 2008

Section	Change Summary
Categories 5, 5E, and 6	Corrected description of basic test setup on page 4.

Revision 1.3, September 2007

Section	Change Summary
All	Updated to include LatticeECP2M FPGA family.

Revision 1.2, July 2007

Section	Change Summary
All	Corrected typos for PRBS 2^7 to PRBS 2^7-1.

Revision 1.1, June 2007

Section	Change Summary
All	Updated for LatticeSC/M FPGA family.

Revision 1.0, March 2004

Section	Change Summary
All	Initial release.

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