LatticeECP3 sysIO Usage Guide

Technical Note

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Contents

Figures

Tables

Acronyms in This Document

A list of acronyms used in this document.

Abbreviation	Definition
ASCII	American Standard Code for Information Interchange
DDR	Double Data Rate
GUI	Graphical User Interface
HDL	Hardware Description Language
HSTL	High-Speed Transceiver Logic
LVCMOS	Low-Voltage Complementary Metal Oxide Semiconductor
LVDS	Low-Voltage Differential Signaling
LVPECL	Low Voltage Positive Emitter Coupled Logic
LVTTL	Low Voltage Transistor-Transistor Logic
PCI	Peripheral Component Interconnect
PIC	Programmable I/O Cell
PIO	Programmable I/Os
PPLVDS	Point-to-Point LVDS
SDR	Single Data Rate
SSTL	Stub Series Terminated Logic
TRLVDS	Transition Reduced LVDS

1. Introduction

The LatticeECP3™ sysIO™ buffers give the designer the ability to easily interface with other devices using advanced system I/O standards. This technical note describes the sysIO standards available and how to implement them using Lattice's ispLEVER® design software.

2. sysIO Buffer Overview

The LatticeECP3 sysIO interface contains multiple Programmable I/O Cell (PIC) blocks. Each PIC contains two Programmable I/Os (PIO), PIOA and PIOB, that are connected to their respective sysIO buffers. Two adjacent PIOs can be joined to provide a differential I/O pair (labeled as "T" and "C").

Each PIO includes a sysIO buffer and I/O logic (IOLOGIC). The LatticeECP3 sysIO buffers support a variety of single-ended and differential signaling standards. The sysIO buffer also supports the DQS strobe signal that is required for interfacing with the DDR memory. One of every 12 PIOs in the LatticeECP3 contains a delay element to facilitate the generation of DQS signals. The DQS signal from the bus is used to strobe the DDR data from the memory into input register blocks. For more information on the architecture of the sysIO buffer, refer to the LatticeECP3 Family Data Sheet (FPGA-DS-02074).

The IOLOGIC includes input, output and tristate registers that implement both single data rate (SDR) and double data rate (DDR) applications along with the necessary clock and data selection logic. Programmable delay lines and dedicated logic within the IOLOGIC are used to provide the required shift to incoming clock and data signals and the delay required by DQS inputs in DDR memory. The DDR implementation in the IOLOGIC and the DDR memory interface support are discussed in more detail in LatticeECP3 High-Speed I/O Interface (FPGA-TN-02184).

3. Supported sysIO Standards

The LatticeECP3 sysIO buffer supports both single-ended and differential standards. Single-ended standards can be further subdivided into internally ratioed standard such as LVCMOS, LVTTL and PCI; and externally referenced standards such as HSTL and SSTL. The buffers support the LVTTL, LVCMOS 1.2, 1.5, 1.8, 2.5 and 3.3 V standards. In the LVCMOS and LVTTL modes, the buffer has individually configurable options for drive strength, bus maintenance (weak pull-up, weak pull-down, or a bus-keeper latch). Other single-ended standards supported include SSTL and HSTL. Differential standards supported include LVDS, RSDS, BLVDS, LVPECL, differential SSTL and differential HSTL. LatticeECP3 also support mini-LVDS, PPLVDS (Point-to-Point LVDS) and TRLVDS (Transition Reduced LVDS). Table 3.1 lists the sysIO standards supported in the LatticeECP3 devices.

Table 3.1. Supported Input Standards

Input Standard	V_{REF} (Nominal)	V_{CCIO} (Nominal)
Single Ended Interfaces		
LVTTL	—	3.3
LVCMOS33	—	3.3[1]
LVCMOS25	—	2.5[1]
LVCMOS18	—	1.8
LVCMOS15	—	1.5
LVCMOS12	—	—
PCI33	—	—
HSTL18 Class I, II	0.9	—
HSTL15 Class I	0.75	—
SSTL33 Class I, II	1.5	3.3, 2.5
SSTL25 Class I, II	1.25	3.3, 2.5, 1.8
SSTL18 Class I, II	0.9	—
SSTL15	0.75	—
Differential Interfaces		
Differential SSTL33 Class I, II	—	3.3, 2.5
Differential SSTL18 Class I, II	See Note 2	—
Differential SSTL25 Class I, II	—	3.3, 2.5, 1.8
Differential HSTL15 Class I	—	—
Differential HSTL18 Class I, II	—	—
Differential SSTL 15	See Note 2	—
LVDS	—	—
Transition Reduced LVDS	—	3.3
LVPECL	—	3.3
Bus LVDS	—	—
MLVDS	—	—

Notes:

1. For LVTTL33, LVCMOS33 and LVCMOS25, if PCICLAMP is OFF, they can be used independently of V_{CCIO} in the top banks.
2. VREF is required when using Differential SSTL to interface to DDR memory.

Table 3.2. Supported Output Standards

Output Standard	Drive	V_{CCIO} (Nominal)
Single Ended Interfaces		
LVTTL	4 mA, 8 mA, 12 mA, 16 mA, 20 mA	3.3
LVCMOS33	4 mA, 8 mA, 12 mA, 16 mA, 20 mA	3.3
LVCMOS25	4 mA, 8 mA, 12 mA, 16 mA, 20 mA	2.5
LVCMOS18	4 mA, 8 mA, 12 mA, 1 6mA, 20 mA[3]	1.8
LVCMOS15	4 mA, 8 mA, 12 mA[3], 16 mA[3], 20 mA[3]	1.5
LVCMOS12	2 mA, 4 mA[3], 6 mA, 8 mA[3], 12 mA[3], 16 mA[3], 20 mA[3]	1.2
PCI33	N/A	3.3
HSTL18 Class I	8 mA, 12 mA	1.8
HSTL18 Class II	N/A	1.8
HSTL15 Class I	4 mA, 8 mA	1.5
SSTL33 Class I, II	N/A	3.3
SSTL25 Class I	8 mA, 12 mA	2.5
SSTL25 Class II	16 mA, 20 mA	2.5
SSTL18 Class I	N/A	1.8
SSTL18 Class II	8 mA, 12 mA	1.8
SSTL15	10 mA	1.5
Differential Interfaces		
Differential HSTL18 Class I	8 mA, 12 mA	1.8
Differential HSTL18 Class II	N/A	1.8
Differential HSTL15 Class I	4 mA, 8 mA	1.5
Differential SSTL33 Class I, II	N/A	3.3
Differential SSTL25 Class I	8 mA, 12 mA	2.5
Differential SSTL25 Class II	16 mA, 20 mA	2.5
Differential SSTL18 Class I	N/A	1.8
Differential SSTL18 Class II	8 mA, 12 mA	1.8
Differential SSTL15	10 mA	1.5
LVDS	N/A	2.5
Point-to-Point LVDS (PPLVDS)	N/A	2.5, 3.3
RSDS, RSDSE[2]	N/A	2.5
Mini-LVDS[1]	N/A	2.5
MLVDS[2]	N/A	2.5
BLVDS[2]	N/A	2.5
LVPECL[2]	N/A	3.3

Notes:

1. Multiple Drive supported using DiffDrive and MultDrive.
2. Emulated with LVCMOS drivers and external resistors.
3. This drive strength is only available when the output is configured as open-drain.

4. sysIO Banking Scheme

LatticeECP3 devices have six general-purpose programmable sysIO banks and a seventh configuration bank. Each of the six general-purpose sysIO banks has a V_{CCIO} supply voltage and two reference voltages, VREF1 and VREF2. Figure 4.1 shows the six general-purpose banks and the configuration bank with associated supplies. Bank 8 is a bank dedicated to configuration logic and has seven dedicated configuration I/Os and 14 multiplexed configuration I/Os. Bank 8 has the power supply pads (V_{CCIO} and V_{CCAUX}) but does not have VREF pads.

On the top and bottom banks, the sysIO buffer pair consists of two single-ended output drivers and two sets of single-ended input buffers (both ratioed and referenced). The left and right sysIO buffer pair consists of two singleended output drivers and two sets of single-ended input buffers (both ratioed and referenced). The referenced input buffer can also be configured as a differential input. In 50% of the pairs, there is also one differential output driver. The two pads in the pair are described as “true” and “comp”, where the true pad is associated with the positive side of the differential input buffer and the comp (complementary) pad is associated with the negative side of the differential input buffer.

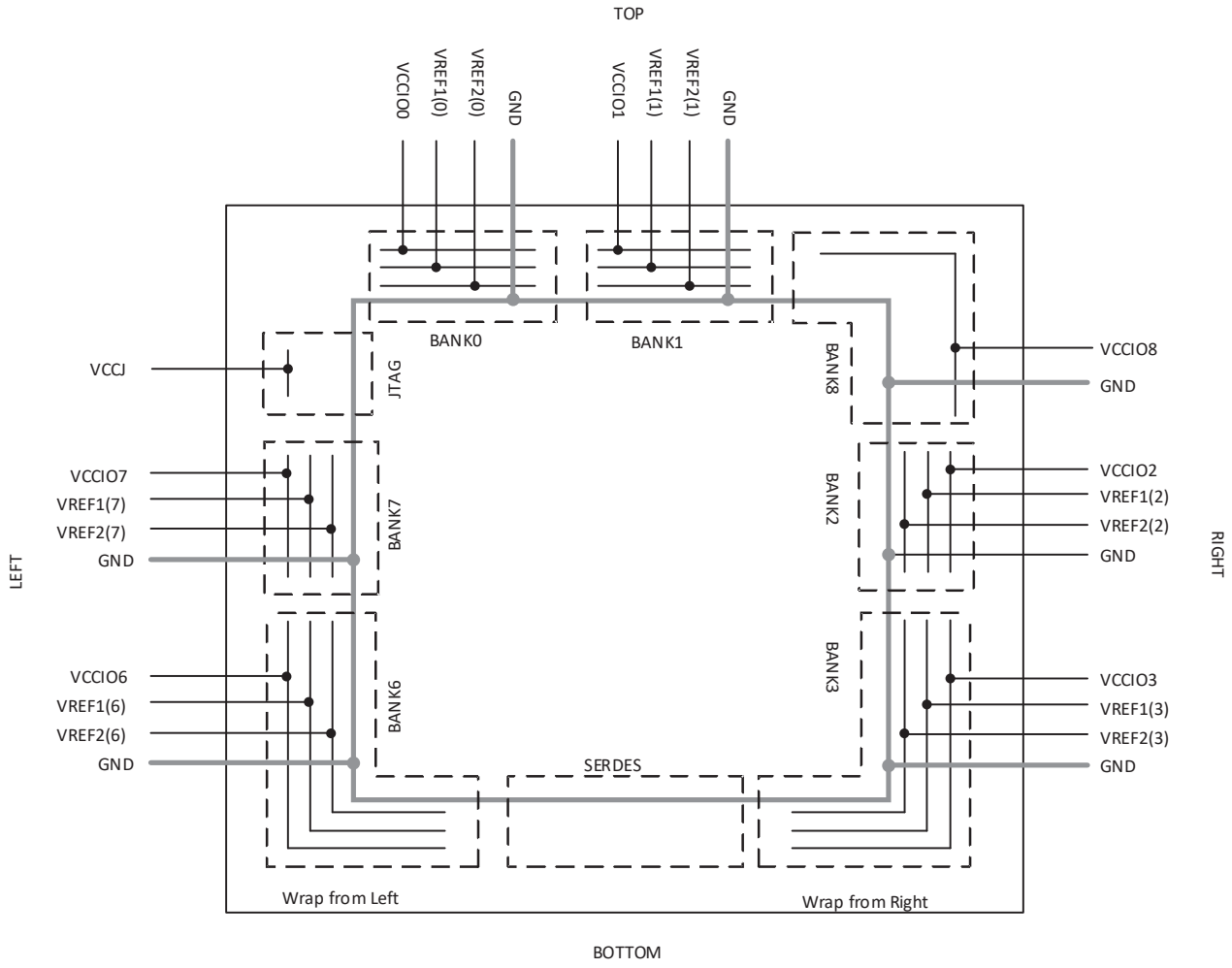

Figure 4.1. sysIO Banking

4.1. V_{CCIO} (1.2 V/1.5 V/1.8 V/2.5 V/3.3 V)

There are a total of six V_{CCIO} supplies, V_{CCIO0} - V_{CCIO8}. Each bank has a separate V_{CCIO} supply that powers the single-ended output drivers and the ratioed input buffers such as LVTTL, LVCMOS, and PCI. LVTTL, LVCMOS3.3, LVCMOS2.5 and LVCMOS1.2 inputs also have fixed threshold options allowing them to be placed in any bank. Table 4.2 and Table 4.4 list the allowed mixed-voltage support in a given bank. The V_{CCIO} voltage applied to the bank determines the ratioed input standards that can be supported in that bank. It is also used to power the differential output drivers. In addition, V_{CCIO8} is used to supply power to the sysCONFIG™ signals.

4.2. V_{CCAUX} (3.3 V)

In addition to the bank V_{CCIO} supplies, LatticeECP3 devices have a V_{CC} core logic power supply, and a V_{CCAUX} auxiliary supply that powers the differential and referenced input buffers. V_{CCAUX} is used to supply I/O reference voltage requiring 3.3 V to satisfy the common-mode range of the drivers and input buffers.

4.3. V_{CCJ} (1.2 V/1.5 V/1.8 V/2.5 V/3.3 V)

The JTAG pins have a separate V_{CCJ} power supply that is independent of the bank V_{CCIO} supplies. V_{CCJ} determines the electrical characteristics of the LVCMOS JTAG pins, both the output high level and the input threshold. Table 4.1 contains a summary of the required power supplies.

Table 4.1. Power Supplies

Power Supply	Description	Value[1]
V_{CC}	Core power supply	1.2 V
V_{CCIO}	Power supply for the I/O and configuration banks	1.2 V/1.5 V/1.8 V/2.5 V/3.3 V
V_{CCAUX}	Auxiliary power supply	3.3 V
V_{CCJ}	Power supply for JTAG pins	1.2 V/1.5 V/1.8 V/2.5 V/3.3 V

Note:

1. Refer to the LatticeECP3 Family Data Sheet (FPGA-DS-02074) for recommended min. and max. values.

4.4. Input Reference Voltage (V_{REF1}, V_{REF2})

Each bank can support up to two separate V_{REF} input voltages, V_{REF1} and V_{REF2}, that are used to set the threshold for the referenced input buffers. The location of these V_{REF} pins is pre-determined within the bank. These pins can be used as regular I/Os if the bank does not require a V_{REF} voltage.

4.5. VREF1 for DDR Memory Interface

When interfacing to DDR memory, the V_{REF1} input must be used as the reference voltage for the DQS and DQ input from the memory. A voltage divider between V_{REF1} and GND is used to generate an on-chip reference voltage that is used by the DQS transition detector circuit. This voltage divider is only present on V_{REF1} it is not available on V_{REF2}. For further information on the DQS transition detect logic and its implementation, refer to LatticeECP3 High-Speed I/O Interface (FPGA-TN-02184). When not used as VREF, these predefined voltage reference pins are available as user I/O pins.

For DDR1 memory interfaces, the V_{REF1} should be connected to 1.25 V since only SSTL25 signaling is allowed. For DDR2 memory interfaces, V_{REF1} should be connected to 0.9V since only SSTL18 signaling is allowed. For DDR3 memory interfaces, V_{REF1} should be connected to 0.75 V since only SSTL15 signaling is allowed.

4.6. VTT Termination Voltage

The VTT termination voltage on LatticeECP3 device is used for the referenced standard termination and common mode differential termination. These termination voltage pins are available on the left and right of the device only. Use of VTT is optional, these pins should be left floating if termination to VTT is not required. The allowable range for VTT is from 0.5 V to 1.25 V, independent of the value of V_{CCIO}. The user decides the best termination voltage to apply to VTT. Many applications will choose VTT to be nominally equal to the switching threshold of the interface standard being used, with a tolerance of +/- 5% (and this is usually equal to half of the driver supply voltage). VTT Termination can be dynamic for bidirectional pins (enabled when output buffer is put in tristate) or static (always on).

4.7. Hot Socketing Support

The I/Os located on the top and bottom sides of the device are fully hot socketable. The top side of the device simultaneously supports hot-socketing, mixed voltage support within a bank and programmable clamp diodes for supporting PCI. The I/Os located on the left and right sides of the device do not support hot socketing. See the LatticeECP3 Family Data Sheet (FPGA-DS-02074) for hot socketing (IDK) requirements.

4.8. Mixed Voltage Support in a Bank

The LatticeECP3 sysIO buffer is connected to three parallel ratioed input buffers. These three parallel buffers are connected to V_{CCIO}, V_{CCAUX} and to V_{CC}, giving support for thresholds that track with V_{CCIO} as well as fixed thresholds for 3.3 V (V_{CCAUX}) and 1.2 V (V_{CC}) inputs. This allows the input threshold for ratioed buffers to be assigned on a pin-by-pin basis, rather than have it track with V_{CCIO}. This option is available for all 1.2 V, 2.5 V and 3.3 V ratioed inputs and is independent of the bank V_{CCIO} voltage on the top banks when PCICLAMP is OFF. In the left and right banks, the PCICLAMP is always enabled to clamp any currents when V_{INPUT} is higher than V_{CCIO}. Hence, only 1.2 inputs and 2.5 inputs are allowed independent of V_{CCIO} as long as the V_{INPUT} is less than V_{CCIO}. For example, if the bank V_{CCIO} is 1.8 V and PCICLAMP is OFF, it is possible to have 1.2 V and 3.3 V ratioed input buffers with fixed thresholds, as well as 2.5 V ratioed inputs with tracking thresholds on the top bank. On the left and right banks, when V_{CCIO} is 1.8 V, it is possible to have only 1.2 V with fixed thresholds. But if the V_{CCIO} on the left and right sides is 3.3 V, it is possible to have a 1.2 V input with fixed thresholds as well as 2.5 V with tracking thresholds.

Prior to device configuration, the ratioed input thresholds track the bank V_{CCIO}. This option only takes effect after configuration. Output standards within a bank are always set by V_{CCIO} but can drive a lower output standard into a device that is tolerant up to that V_{CCIO}. Table 4.2 and Table 4.3 shows the sysIO standards that can be mixed in the same bank.

Table 4.2. Mixed Voltage Support in Top Banks

V_{CCIO}	Input sysIO Standards[1, 2, 3, 4, 5]					Output sysIO Standards[6]				
	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V
1.2 V	Yes	—	—	Yes	Yes	Yes	—	—	—	—
1.5 V	Yes	Yes	—	Yes	Yes	—	Yes	—	—	—
1.8 V	Yes	—	Yes	Yes	Yes	—	—	Yes	—	—
2.5 V	Yes	—	—	Yes	Yes	—	—	—	Yes	—
3.3 V	Yes	—	—	Yes	Yes	—	—	—	—	Yes

Notes:

1. Mixed voltage input support is available on the top banks only when PCICLAMP is OFF
2. All differential input buffers except LVPECL33 and TRLVDS can be supported in banks independent of V_{CCIO}. LVPECL33 can be placed on top side independent of V_{CCIO} when PCICLAMP is OFF.
3. 1.5 V and 1.8 V HSTL and SSTL reference inputs can be supported on banks with any V_{CCIO}.
4. 2.5 V SSTL reference inputs can be supported on banks with V_{CCIO} set to 1.8 V, 2.5 V or 3.3 V.
5. 3.3 V SSTL reference inputs can be supported on banks with V_{CCIO} set to 2.5 V or 3.3 V.
6. When output is configured as open drain it can be placed in bank independent of V_{CCIO}.

Table 4.3. Mixed Voltage Support in Left and Right Banks

VCCIO	Input sysIO Standards[1, 2, 3, 4]					Output sysIO Standards[5]				
	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V
1.2 V	Yes	—	—	—	—	Yes	—	—	—	—
1.5 V	Yes	Yes	—	—	—	—	Yes	—	—	—
1.8 V	Yes	—	Yes	—	—	—	—	Yes	—	—
2.5 V	Yes	—	—	Yes	—	—	—	—	Yes	—
3.3 V	Yes	—	—	Yes	Yes	—	—	—	—	Yes

Notes:

1. All differential input buffers except LVPECL33 and TRLVDS can be supported on banks with V_{CCIO} set to 2.5 V or 3.3 V. LVPECL and TRLVDS require V_{CCIO} of 3.3 V. If the V_{CCIO} is set to 1.8 V or 1.5 V, this reduces the V_{CM} (max) and V_{IN} (max) to approximately 1.7 V as the PCICLAMP is always enabled on this side when the $V_{INPUT} > V_{CCIO}$ of the bank.
2. 1.5 V and 1.8 V HSTL and SSTL reference inputs can be supported on banks with any V_{CCIO}.
3. 2.5 V SSTL reference inputs can be supported on banks with V_{CCIO} set to 1.8 V, 2.5 V or 3.3 V.
4. 3.3 V SSTL reference inputs can be supported on banks with V_{CCIO} set to 2.5 V or 3.3 V.
5. When output is configured as open drain it can be placed in bank independent of V_{CCIO}.

4.9. sysIO Standards Supported Per Bank

Table 4.4. I/O Standards Supported per Bank

Description	Top Side	Right Side	Bottom Side	Left Side
Types of I/O Buffers	Single-ended	Single-ended and Differential	Single-ended	Single-ended and Differential
Single-Ended Standards Outputs	LVTTL	LVTTL	LVTTL	LVTTL
	LVCMOS33	LVCMOS33	LVCMOS33	LVCMOS33
	LVCMOS25	LVCMOS25	LVCMOS25	LVCMOS25
	LVCMOS18	LVCMOS18	LVCMOS18	LVCMOS18
	LVCMOS15	LVCMOS15	LVCMOS15	LVCMOS15
	LVCMOS12	LVCMOS12	LVCMOS12	LVCMOS12
	SSTL15	SSTL15	SSTL15	SSTL15
	SSTL18 Class I, II	SSTL18 Class I, II	SSTL18 Class I, II	SSTL18 Class I, II
	SSTL25 Class I, II	SSTL25 Class I, II	SSTL2 Class I, II	SSTL2 Class I, II
	SSTL33 Class I, II	SSTL33 Class I, II	SSTL3 Class I, II	SSTL3 Class I, II
	HSTL15 Class I	HSTL15 Class I	HSTL15 Class I	HSTL15 Class I
	HSTL18_I, II	HSTL18 Class I, II	HSTL18 Class I, II	HSTL18 Class I, II
Differential Standards Outputs	LVCMOS33D SSTL15D SSTL18D Class I, II SSTL25D Class I, II SSTL33D Class I, II HSTL15D Class I HSTL18D Class I, II	LVCMOS33D SSTL15D SSTL18D Class I, II SSTL25D Class I, II SSTL33D Class I, II HSTL15D Class I HSTL18D Class I, II	LVCMOS33D SSTL15D SSTL18D Class I, II SSTL25D Class I, II, SSTL33D Class I, II HSTL15D Class I HSTL18D Class I, II	LVCMOS33D SSTL15D SSTL18D Class I, II SSTL25D Class I, II, SSTL33D_I, II HSTL15D Class I HSTL18D Class I, II
	LVDS25E[1] LVPECL[1] BLVDS[1] RSDSE[1]	LVDS[2, 3] RSDS[2] Mini-LVDS[2] PPLVDS[2] (point-to-point) LVDS25E[1] LVPECL[1] BLVDS[1] RSDSE[1]	LVDS25E[1] LVPECL[1] BLVDS[1] RSDSE[1]	LVDS[2] RSDS[2] Mini-LVDS[2] PPLVDS[2] (point-to-point) LVDS25E[1] LVPECL[1] BLVDS[1] RSDSE[1]
Inputs	All Single-ended and Differential TRLVDS (Transition Reduced LVDS)	All Single-ended, Differential	All Single-ended, Differential	All Single-ended, Differential
Clock Inputs	All Single-ended, Differential	All Single-ended, Differential	All Single-ended, Differential	All Single-ended, Differential
Hot Socketing	Yes	No	Yes	No
Equalization on Inputs	No[4]	Yes[4]	No	Yes
ISI Correction	For DDR3 memory	For DDR3 memory	For DDR3 memory	For DDR3 memory
On Chip Termination	No	On-Chip Parallel Termination On-Chip Differential Termination	No	On-Chip Parallel Termination On-Chip Differential Termination
PCI Support	PCI33 with or without clamp[5]	PCI33 with clamp	PCI33 with clamp	PCI33 with clamp

Notes:

1. These differential standards are implemented by using a complementary LVCMOS driver with the external resistor pack.
2. Available on 50% of the I/Os in the bank.
3. I/Os in Bank 8 are shared with sysCONFIG pins and do not support true LVDS and DDR registers.
4. I/Os in Bank 8 do not support equalization.
5. I/Os in Bank 8 do not have a programmable clamp setting. PCI clamp is always on in Bank 8.

5. sysIO Buffer Configurations

This section describes the various sysIO features available on the LatticeECP3 FPGAs.

5.1. Bus Maintenance Circuit

Each of the LVCMOS, LVTTL and PCI types of inputs has a weak pull-up, weak pull-down and weak bus keeper capability. The pull-up and pull-down settings offer a fixed characteristic which is useful in creating wired logic such as wired ORs. However, current can be slightly higher than other options depending on the signal state. The bus keeper option latches the signal in the last driven state, holding it at a valid level with minimal power dissipation. You can also choose to turn off the bus maintenance circuitry, minimizing power dissipation and input leakage. Note that in this case it is important to ensure that inputs are driven to a known state to avoid unnecessary power dissipation in the input buffer.

On the outputs, the weak pull-ups are on at all times. Users have the option to turn off the pull-up setting in the software.

5.2. Programmable Drive

Each LVCMOS or LVTTL, as well as some of the referenced (SSTL and HSTL) output buffers, has a programmable drive strength option. This option can be set for each I/O independently. The drive strength settings available are 2 mA, 4 mA, 6 mA, 8 mA, 12 mA, 16 mA and 20 mA. Actual options available vary by I/O voltage. The user must consider the maximum allowable current per bank and the package thermal limit current when selecting the drive strength. Table 5.1 shows the available drive settings for each of the output standards.

Table 5.1. I/O Standards Supported per Bank

Single-Ended I/O Standard	Programmable Drive (mA)
HSTL15_I/ HSTL15D_I	4, 8
HSTL18_I/ HSTL18D_I	8, 12
SSTL25_I/ SSTL25D_I	8, 12
SSTL25_II/ SSTL25D_II	16, 20
SSTL18_II/SSTL18D_II	8, 12
LVCMOS12 (with PCI Clamp OFF)	4, 8, 12, 16, 20
LVCMOS12 (with PCI Clamp ON)	2, 6
LVCMOS15 (with PCI Clamp OFF)	4, 8, 12, 16, 20
LVCMOS15 (with PCI Clamp ON)	4, 8
LVCMOS18 (with PCI Clamp OFF)	4, 8, 12, 16, 20
LVCMOS18 (with PCI Clamp ON)	4, 8, 12, 16
LVCMOS25	4, 8, 12, 16, 20
LVCMOS33	4, 8, 12, 16, 20
LVTTL	4, 8, 12, 16, 20

5.3. Programmable Slew Rate

Each LVCMOS or LVTTL output buffer pin also has a programmable output slew rate control that can be configured for either low noise or high-speed performance. Each I/O pin has an individual slew rate control. This allows designers to specify slew rate control on a pin-by-pin basis. This slew rate control affects both the rising edge and the falling edges.

5.4. Open Drain Control

All LVCMOS and LVTTL output buffers can be configured to function as open drain outputs. The user can implement an open drain output by turning on the OPENDRAIN attribute in the software.

5.5. Differential SSTL and HSTL Support

The single-ended driver associated with the complementary "C" pad can optionally be driven by the complement of the data that drives the single-ended driver associated with the true pad. This allows a pair of single-ended drivers to be used to drive complementary outputs with the lowest possible skew between the signals. This is used for driving complementary SSTL and HSTL signals (as required by the differential SSTL and HSTL clock inputs on synchronous DRAM and synchronous SRAM devices, respectively). This capability is also used in conjunction with offchip resistors to emulate LVPECL, and BLVDS output drivers.

5.6. PCI Support with Programmable PCICLAMP

Each sysIO buffer can be configured to support PCI33. The buffers on the top of the device have an optional PCI clamp diode that may optionally be specified in the ispLEVER design tools. The programmable PCICLAMP can be turned ON or OFF. This option is available on each I/O independently only on the top side banks.

For the other three sides of the device, the PCICLAMP is always ON.

5.7. Differential I/O Support

50% of the sysIO buffer pairs on the left and right edges contain a differential output driver that can optionally drive the pads in the pair. The standards support on these differential output pairs is as follows:

- LVDS
- Point to Point LVDS (PPLVDS)
- Mini-LVDS
- RSDS

All the other pins on all the sides of the device can support Emulated Differential standards using complementary LVCMOS drivers with external resistors. The standards supported using differential output pairs is as follows:

- BLVDS
- LVDS25E
- RSDSE
- LVPECL

The LatticeECP3 Family Data Sheet (FPGA-DS-02074) lists the LVCMOS drivers and external resistor requirements to implement these emulated standards. The data sheet also lists the electrical specifications supported for all differential standards.

5.8. Differential SSTL and HSTL

All single-ended sysIO buffers pairs support differential SSTL and HSTL. Refer to the LatticeECP3 Family Data Sheet (FPGA-DS-02074) for a detailed description of the Differential HSTL and SSTL implementations.

5.9. Differential LVCMOS33

All single-ended sysIO buffer pairs also support the LVCMOS33D (Differential) standard with configurable drive strength and slew settings. This generic 3.3V differential buffer allows the user to implement any type of 3.3 V differential buffer by configuring the drive strength and calculating the external resistor values as per the application requirements.

5.10. GTL+ Input Support

GTL+ inputs can be supported using either the SSTL15 or HSTL15_I input standard with VREF set to 1.0 V and external VTT termination to 1.5 V. GTL+ inputs implemented using this method can support the maximum speed listed for the SSTL and HSTL standards in the LatticeECP3 Family Data Sheet (FPGA-DS-02074). GTL+ outputs are not supported in the LatticeECP3 device.

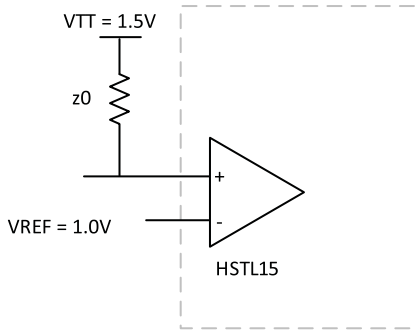

Figure 5.1. GTL+ Input Buffer Emulation Using HSTL15 Input

5.11. On-Chip Termination

LatticeECP3 devices support on-chip Parallel Termination to VTT as well Common mode differential termination using the VTT pin. On-chip termination is available on the left and right sides of the device. The VTT pin should be left to float when using common mode differential termination. Termination can be set to be dynamic for bidirectional buffers where the termination is active only when the output buffer is disabled through the tristate control. External termination to VTT should be used when implementing the DDR2 and DDR3 memory interfaces.

5.12. Equalization Setting

Equalization filtering is available for single-ended inputs on both true and complementary I/Os, and for differential inputs on the true I/Os. Equalization is required to compensate for the difficulty of sampling alternating logic transitions with a relatively slow slew rate. It is useful for the input DDR modes used in DDR3 memory and fast SPI4.2 mode signaling. It is available on the left and right sides.

Equalization acts as a tunable filter, with settings determining the level of correction. There are four settings available: Zero (none), One, Two and Three. The equalization logic resides in the I/O buffers. Each I/O can have a unique equalization setting within a DQS-12 group for DDR3 memory.

6. Software sysIO Attributes

sysIO attributes can be specified in the HDL, using the Preference Editor GUI or in the ASCII Preference file (.prf) directly. The appendices of this document provide examples of how these can be assigned using each of the methods described above. This section describes each of these attributes in detail.

6.1. IO_TYPE

This attribute is used to set the sysIO standard for an I/O. The V_{CCIO} required to set these I/O standards are embedded in the attribute name itself. There is no separate attribute to set the VCCIO requirements. Table 6.1 lists the available I/O types.

Table 6.1. IO_TYPE Attribute Values

sysIO Signaling Standard	IO_TYPE
DEFAULT	LVCMOS25
LVDS 2.5 V	LVDS25[2]
Point to Point LVDS	PPLVDS[2]
Mini-LVDS	MINILVDS[2]
RSDS	RSDS[2]
Transition Reduced LVDS	TRLVDS[3]
Emulated LVDS 2.5 V	LVDS25E[1]
Bus LVDS 2.5 V	BLVDS25[1]

sysIO Signaling Standard	IO_TYPE
LVPECL 3.3 V	LVPECL33[1]
Emulated RSDS	RSDSE[1]
MLVDS	MLVDS
HSTL18 Class I and II	HSTL18_I, HTSL18_II
Differential HSTL 18 Class I and II	HSTL18D_I HSTL18D_II
HSTL 15 Class I	HSTL15_I
Differential HSTL 15 Class I	HSTL15D_I
SSTL 33 Class I and II	SSTL33_I, SSTL33_II
Differential SSTL 33 Class I and II	SSTL33D_I SSTL3D_II
SSTL 25 Class I and II	SSTL25_I SSTL25_II
Differential SSTL 25 Class I and II	SSTL25D_I SSTL25D_II
SSTL 18 Class I and II	SSTL18_I SSTL18_II
Differential SSTL 18 Class I and II	SSTL18D_I SSTL18D_II
SSTL 15	SSTL15
LVTTL	LVTTL33
3.3 V LVCMOS	LVCMOS33
3.3 V LVCMOS Differential	LVCMOS33D
2.5 V LVCMOS	LVCMOS25
1.8 V LVCMOS	LVCMOS18
1.5 V LVCMOS	LVCMOS15
1.2 V LVCMOS	LVCMOS12
3.3 V PCI	PCI33

Notes:

1. These differential standards are implemented by using the complementary LVCMOS driver and external resistor pack.
2. Supported on 50% of the pairs on the left and right sides of the device.
3. Only inputs supported. Available only on the top side of the device.

6.2. OPENDRAIN

LVCMOS and LVTTL IO standards can be set to Open Drain configuration by using the OPENDRAIN attribute. When configuring I/Os on the left and right banks to be Open Drain, it is required that the external pull-up be less than the bank V_{CCIO}.

Table 6.2. Open Drain Attribute Values

Attribute	Values	Default
OPENDRAIN	ON, OFF	OFF

6.3. DRIVE

The DRIVE attribute will set the programmable drive strength for the output standards that have programmable drive capability

Table 6.3. DRIVE Settings

Output Standard	DRIVE (mA)	Default (mA)
HSTL15_I/ HSTL15D_I	4, 8	8
HSTL18_I/ HSTL18D_I	8, 12	12
SSTL25_I/ SSTL25D_I	8, 12	8
SSTL25_II/ SSTL25D_II	16, 20	16
SSTL18_II/SSTL18D_II	8, 12	12
LVCMOS12 (without OPENDRAIN)	2, 6	6

Output Standard	DRIVE (mA)	Default (mA)
LVCMOS12 (with OPENDRAIN)	4, 8, 12, 16, 20	12
LVCMOS15 (without OPENDRAIN)	4, 8	8
LVCMOS15 (with OPENDRAIN)	4, 8, 12, 16, 20	12
LVCMOS18 (without OPENDRAIN)	4, 8, 12, 16	12
LVCMOS18 (with OPENDRAIN)	4, 8, 12, 16, 20	12
LVCMOS25	4, 8, 12, 16, 20	12
LVCMOS33	4, 8, 12, 16, 20	12
LVTTL	4, 8, 12, 16, 20	12

6.4. DIFFDRIVE

The DIFFDRIVE setting is used to set the differential drive setting for the Mini-LVDS driver when the driver setting needs to be adjusted to support variation in external termination. An I/O bank can have differential outputs with the same DIFFDRIVE setting. Differential outputs with different DIFFDRIVE settings cannot be placed in the same I/O bank.

Table 6.4. DIFFDRIVE Values

I/O Standard	MULTDRIVE Values	Default
MINILVDS	1.6, 1.65, 1.7, 1.75,1.81, 1.87, 1.93, 2.0	1.6
LVDS	1.75	1.75
RSDS	2.0	2.0
PPLVDS	2.0	2.0

6.5. MULTDRIVE

DIFFDRIVE only partially supports variation of Mini-LVDS driver current. Therefore, in addition to DIFFDRIVE, MULTDRIVE settings must be used to adjust the output drive strength of Mini-LVDS.

Table 6.5. MULTDRIVE Values

I/O Standard	MULTDRIVE Values	Default
MINILVDS	1x, 2x, 3x, 4x	1x
LVDS	2x	2x
RSDS	1x	1x
PPLVDS	1x	1x

6.6. TERMINATEVTT

This attribute is used to set the on-chip parallel termination to VTT for reference buffer inputs. VTT pins in corresponding banks should be connected externally to the correct level. VTT of the bank should be left floating if this termination is not used.

Table 6.6. TERMINATEVTT Values

Attribute	Values	Default
TERMINATEVTT	OFF, 40, 50, 60	OFF

6.7. DIFFRESISTOR

This attribute is used to set the on-chip differential termination using common mode termination to VTT. This onchip termination is optimized to work primarily for the LVDS I/O type. When the DIFFRESISTOR attribute is set, the VTT pin should be left floating.

Table 6.7. DIFFRESISTOR Values

Attribute	Values	Default
DIFFRESISTOR	OFF, 80, 100, 120	OFF

6.8. EQ_CAL

This attribute is used to set the Equalization setting available on the input pins on the left and right sides of the device. EQ_CAL is not available in Bank 8.

Table 6.8. EQ_CAL Values

Attribute	Values	Default
EQ_CAL	0, 1, 2, 3, 4	0

6.9. PULLMODE

The PULLMODE attribute is available for all the LVTLL and LVCMOS inputs and outputs. This attribute can be enabled for each I/O independently.

Table 6.9. PULLMODE Values

PULL Options	PULLMODE Value
Pull up (Default)	UP
Pull Down	DOWN
Bus Keeper	KEEPER
Pull Off	NONE

Table 6.10. PULLMODE Settings

Buffer	Values	Default
Input	UP, DOWN, KEEPER, NONE	UP
Output	UP, DOWN, KEEPER, NONE	UP

6.10. PCICLAMP

PCICLAMP is available on all the pads of the device. On the top of the device the PCICLAMP setting can be optionally turned OFF. The rest of the banks only support the PCICLAMP value ON.

Table 6.11. PCICLAMP Values

Attribute	Values	Default
PCI33	ON, OFF	ON

6.11. SLEWRATE

The SLEWRATE attribute is available for all LVTTL and LVCMOS output drivers. Each I/O pin has an individual slew rate control. This allows designers to specify slew rate control on a pin-by-pin basis.

Table 6.12. Slew Rate Values

Attribute	Values	Default
SLEWRATE	FAST, SLOW	SLOW

6.12. INBUF

By default, all the unused input buffers are disabled. The INBUF attribute is used to enable the unused input buffers when performing a boundary scan test. This is a global attribute and can be globally set to ON and OFF.

- Values: ON, OFF
- Default: OFF

6.13. FIXEDDELAY

This attribute can be used in HDL to enable the input Fixed Delay on the input of an SDR Input register. When setto TRUE, you can achieve a zero hold time on the input register.

- Value: TRUE, FALSE
- Default: FALSE

6.14. DIN/DOUT

This attribute can be used when an I/O register needs to be assigned. Using DIN asserts an input register and using DOUT asserts an output register in the design. By default, the software will attempt to assign the I/O registers if applicable. Users can turn this OFF by using a synthesis attribute or the ispLEVER Preference Editor. These attributes can only be applied on registers.

6.15. LOC

This attribute can be used to make pin assignments to the I/O ports in the design. This attribute is only used when the pin assignments are made in HDL source. Pins can also be assigned directly using the GUI in the Preference Editor of the software. See the appendices for further information.

7. Design Considerations and Usage

This section discusses some of design rules and considerations that need to be taken into account when designing with the LatticeECP3 sysIO buffer

7.1. Banking Rules

- If V_{CCIO} or V_{CCJ} for any bank is set to 3.3 V, it is recommended that it be connected to the same power supply as V_{CCAUX}, thus minimizing leakage.
- If V_{CCIO} or V_{CCJ} for any bank is set to 1.2 V, it is recommended that it be connected to the same power supply as V_{CC}, thus minimizing leakage.
- When implementing DDR memory interfaces, the V_{REF1} of the bank is used to provide reference to the interface pins and cannot be used to power any other referenced inputs.
- Only the top bank supports programmable PCI clamps.
- On the top banks, all legal input buffers should be independent of bank VCCIO except for 1.8 V and 1.5 V buffers, which require a bank V_{CCIO} of 1.8 V and 1.5 V. On the left and right banks, 1.2 V input buffers can be assigned to a bank independent of V_{CCIO}. 2.5 V input buffers can be assigned to banks with V_{CCIO} 2.5 V and 3.3 V. All other input buffers depend on the V_{CCIO} to the bank.
- When DIFFRESITOR is used, the VTT pin for that bank should be left floating.
- When TERMINATEVTT is used, VTT should be connected to the correct voltage depending on the IO_TYPE set.

For example, for SSTL18 standards, VTT should be connected to 0.9 V.

- Both TERMINATEVTT and DIFFRESISTOR use the VTT pin, hence these are mutually exclusive in a bank.
- Equalization is only available on the left and right banks.
- PCICLAMP is programmable on the top-side banks 0 and 1. For all other banks, PCICLAMP is always ON.

7.2. Differential I/O Rules

- All banks can support LVDS input buffers. Only the banks on the right and left sides (Banks 2, 3, 6 and 7) will support True Differential output buffers. The banks on the top and bottom will support the LVDS input buffers but will not support True LVDS outputs. The user can use emulated LVDS output buffers on these banks.
- All banks support emulated differential buffers using the external resistor pack and complementary LVCMOS drivers.
- Only 50% of the I/Os on the left and right sides can provide LVDS, mini-LVDS, PPLVDS and RSDS output buffer capability. See the LatticeECP3 Family Data Sheet (FPGA-DS-02074) for the pin listing for all the true differential pairs.
- The IO_TYPE attribute for a differential buffer can only be assigned to the TRUE pad. The ispLEVER design tool will automatically assign the other I/O of the differential pair to the complementary pad.
- TRLVDS inputs are only supported on the top banks.
- LVDS, MINILVDS, RSDS, PPDS cannot co-exist in one bank.
- An I/O bank can only have differential outputs with the same DIFFDRIVE setting. Differential outputs with different DIFFDRIVE settings cannot be placed in the same I/O bank.
- DIFFRESISTOR termination is only available on the left and right sides. If enabled, the VTT of the bank should be left floating. Referenced inputs cannot be used in this bank when DIFFRESISTOR is enabled.

Appendix A. HDL Attributes

Using HDL attributes, you can assign the sysIO attributes directly in your source code. You will need to use the attribute definition and syntax for the synthesis vendor you are planning to use. Below is a list of the sysIO attributes, syntax and examples for the Synplify Pro® synthesis tool. This section only lists the sysIO buffer attributes for these devices. You can refer to the Synplify Pro user manual for a complete list of synthesis attributes. You can access these manuals through the ispLEVER software Help.

A.1. VHDL Synplify Pro

This section lists syntax and examples for all the sysIO attributes in VHDL when using Synplify Pro synthesis tools.

Syntax

Table A.1. VHDL Attribute Syntax for Synplify Pro

Attribute	Syntax
IO_TYPE	attribute IO_TYPE: string; attribute IO_TYPE of Pinname: signal is “IO_TYPE Value”;
OPENDRAIN	attribute OPENDRAIN: string; attribute OPENDRAIN of Pinname: signal is “OpenDrain Value”;
DRIVE	attribute DRIVE: string; attribute DRIVE of Pinname: signal is “Drive Value”;
DIFFDRIVE	attribute DIFFDRIVE: string; attribute DIFFDRIVE of Pinname: signal is “Diffdrive Value”;
MULTIDRIVE	attribute MULTIDRIVE: string; attribute MULTIDRIVE of Pinname: signal is “MULTIDRIVE Value”;
EQ_CAL	attribute EQ_CAL: string; attribute EQ_CAL of Pinname: signal is “EQ_CAL Value”;
TERMINATEVTT	attribute TERMINATEVTT: string; attribute TERMINATEVTT of Pinname: signal is “TERMINATEVTT Value”;
DIFFRESISTOR	attribute DIFFRESISTOR: string; attribute DIFFRESISTOR of Pinname: signal is “DIFFRESISTOR Value”;
PULLMODE	attribute PULLMODE: string; attribute PULLMODE of Pinname: signal is “Pullmode Value”;
PCICLAMP	attribute PCICLAMP: string; attribute PCICLAMP of Pinname: signal is “PCIClamp Value”;
SLEWRATE	attribute PULLMODE: string; attribute PULLMODE of Pinname: signal is “Slewrate Value”;
DIN	attribute DIN: string; attribute DIN of Pinname: signal is “ “;
DOUT	attribute DOUT: string; attribute DOUT of Pinname: signal is “ “;
LOC	attribute LOC: string; attribute LOC of Pinname: signal is “pin_locations”;
FIXEDDELAY	attribute FIXEDDELAY:string; attribute FIXEDELAY of Pinname: signal is "FIXEDDELAY Value";

Examples

IO_TYPE

--***Attribute Declaration***

ATTRIBUTE IO_TYPE: string;

--***IO_TYPE assignment for I/O Pin***

ATTRIBUTE IO_TYPE OF portA: SIGNAL IS “PCI33”;

ATTRIBUTE IO_TYPE OF portB: SIGNAL IS “LVCMOS33”;

ATTRIBUTE IO_TYPE OF portC: SIGNAL IS “LVDS25”;

OPENDRAIN

--***Attribute Declaration***

ATTRIBUTE OPENDRAIN: string;

--***Open Drain assignment for I/O Pin***

ATTRIBUTE OPENDRAIN OF portB: SIGNAL IS “ON”;

DRIVE

--***Attribute Declaration***

ATTRIBUTE DRIVE: string;

--***DRIVE assignment for I/O Pin***

ATTRIBUTE DRIVE OF portB: SIGNAL IS “20”;

DIFFDRIVE

--***Attribute Declaration***

ATTRIBUTE DIFFDRIVE: string;

--*** DIFFDRIVE assignment for I/O Pin***

ATTRIBUTE DIFFDRIVE OF portB: SIGNAL IS “2.0”;

MULTDRIVE

--***Attribute Declaration***

ATTRIBUTE MULTDRIVE: string;

--*** MULTDRIVE assignment for I/O Pin***

ATTRIBUTE MULTDRIVE OF portB: SIGNAL IS “2X”;

EQ_CAL

--***Attribute Declaration***

ATTRIBUTE EQ_CAL: string;

--*** EQ_CAL assignment for I/O Pin***

ATTRIBUTE EQ_CAL OF portB: SIGNAL IS “1”;

TERMINATEVTT

--***Attribute Declaration***

ATTRIBUTE TERMINATEVTT: string;

--*** TERMINATEVTT assignment for I/O Pin***

ATTRIBUTE TERMINATEVTT OF portB: SIGNAL IS “40”;

DIFFERESISTOR

```
--***Attribute Declaration***
ATTRIBUTE DIFFRESISTOR: string;
--*** DIFFRESISTOR assignment for I/O Pin***
ATTRIBUTE DIFFRESISTOR OF portB: SIGNAL IS “80”;
```

PULLMODE

```
--***Attribute Declaration***
ATTRIBUTE PULLMODE : string;
--***PULLMODE assignment for I/O Pin***
ATTRIBUTE PULLMODE OF portA: SIGNAL IS “DOWN”;
ATTRIBUTE PULLMODE OF portB: SIGNAL IS “UP”;
```

PCICLAMP

```
--***Attribute Declaration***
ATTRIBUTE PCICLAMP: string;
--***PULLMODE assignment for I/O Pin***
ATTRIBUTE PCICLAMP OF portA: SIGNAL IS “OFF”;
```

SLEWRATE

```
--***Attribute Declaration***
ATTRIBUTE SLEWRATE : string;
--*** SLEWRATE assignment for I/O Pin***
ATTRIBUTE SLEWRATE OF portB: SIGNAL IS “FAST”;
```

DIN/DOUT

```
--***Attribute Declaration***
ATTRIBUTE din : string;
ATTRIBUTE dout : string;
--*** din/dout assignment for I/O Pin***
ATTRIBUTE din OF input_vector: SIGNAL IS “ “;
ATTRIBUTE dout OF output_vector: SIGNAL IS “ “;
```

LOC

```
--***Attribute Declaration***
ATTRIBUTE LOC : string;
--*** LOC assignment for I/O Pin***
ATTRIBUTE LOC OF input_vector: SIGNAL IS “E3,B3,C3 “;
```

FIXEDDELAY

```
--***Attribute Declaration***
ATTRIBUTE FIXEDDELAY : string;
--*** FIXEDDELAY assignment for I/O Pin***
ATTRIBUTE FIXEDDELAY OF portA: SIGNAL IS “True”;
```

A.2. Verilog Synplicity

This section lists syntax and examples for all the sysIO Attributes in Verilog using Synplicity® synthesis tool.

Syntax

Table A.2. Verilog Synplicity Attribute Syntax

Attribute	Syntax
IO_TYPE	PinType PinName /* synthesis IO_TYPE=“IO_Type Value”*/;
OPENDRAIN	PinType PinName /* synthesis OPENDRAIN =“OpenDrain Value”*/;
DRIVE	PinType PinName /* synthesis DRIVE=“Drive Value”*/;
DIFFDRIVE	PinType PinName /* synthesis DIFFDRIVE =“DIFFDRIVE Value”*/;
MULTDRIVE	PinType PinName /* synthesis MULTDRIVE =“MULTDRIVE Value”*/;
EQ_CAL	PinType PinName /* synthesis EQ_CAL =“EQ_CAL Value”*/;
TERMINATEVTT	PinType PinName /* synthesis TERMINATEVTT =“TERMINATEVTT Value”*/;
DIFFRESISTOR	PinType PinName /* synthesis DIFFRESISTOR =“DIFFRESISTOR Value”*/;
PULLMODE	PinType PinName /* synthesis PULLMODE=“Pullmode Value”*/;
PCICLAMP	PinType PinName /* synthesis PCICLAMP =“PCIClamp Value”*/;
SLEWRATE	PinType PinName /* synthesis SLEWRATE=“Slewrate Value”*/;
DIN	PinType PinName /* synthesis DIN=“ ”*/;
DOUT	PinType PinName /* synthesis DOUT=“ ”*/;
LOC	PinType PinName /* synthesis LOC=“pin_locations”*/;
FIXEDDELAY	PinType PinName/*synthesis FIXEDDELAY = “FIXEDDELAY value”*/;

Examples

//IO_TYPE, PULLMODE, SLEWRATE and DRIVE assignment

output portB /*synthesis IO_TYPE=”LVCMOS33” PULLMODE =”UP” SLEWRATE =”FAST”
DRIVE =”20”*/;
output portC /*synthesis IO_TYPE=”LVDS25” */;

//DIFFRESISTOR

input portB /*synthesis IO_TYPE=”LVDS” DIFFRESITOR=”80” */;

//DIFFDRIVE, MULTDRIVE

output portB /*synthesis IO_TYPE=”MINILVDS” DIFFDRIVE=”2.0” MULTDRIVE=”2X”*/;

//TERMINATEVTT, EQ_CAL

input portB /*synthesis IO_TYPE=”SSTL15” TERMINATEVTT=”60” EQ_CAL=”2”*/;

//OPENDRAIN

output portA /*synthesis OPENDRAIN =”ON”*/;

//PCICLAMP

output portA /*synthesis IO_TYPE=”PCI33” PCICLAMP =”OFF”*/;

//FIXEDDELAY

input portB /*synthesis FIXEDDELAY = "true" */;

// Place the flip-flops near the load input

input load /* synthesis din=”” */;

// Place the flip-flops near the outload output

output outload /* synthesis dout="" */;

//I/O pin location

input [3:0] DATA0 /* synthesis loc="E3,B1,F3"*/;

//Register pin location

reg data_in_ch1_buf_reg3 /* synthesis loc="R40C47" */;

//Vectored internal bus

reg [3:0] data_in_ch1_reg /*synthesis loc ="R40C47,R40C46,R40C45,R40C44" */;

Appendix B. sysIO Attributes Using the ispLEVER Design Planner User Interface

sysIO buffer attributes can be assigned using the Design Planner Spreadsheet View available in the ispLEVER design tool. If you are using Lattice Diamond™ design software, see Appendix C. The Pin Attribute Sheet lists all the ports in a design and all the available sysIO attributes as preferences. Click on each of these cells for a list of all the valid I/O preferences for that port. Each column takes precedence over the next. Therefore, when you choose a particular IO_TYPE, the columns for the DRIVE, PULLMODE, SLEW-RATE and other attributes will only list the valid combinations for that IO_TYPE. Pin locations can be locked using the pin location column of the Pin Attribute sheet. Right-click on a cell to list all the available pin locations. The Design Planner will also run a DRC check to check for any incorrect pin assignments.

You can enter the DIN/ DOUT preferences using the Cell Attributes Sheet of the Design Planner. All the preferences assigned using the Design Planner are written into the logical preference file (.lpf).

Figure B.1 and Figure B.2 show the Port Attribute Sheet and the Cell Attribute Sheet views of the Design Planner. For further information on how to use the Design Planner, refer to the ispLEVER Help documentation, available in the Help menu option of the software.

Figure B.1. Port Attributes Tab of Design Planner SpreadSheet View

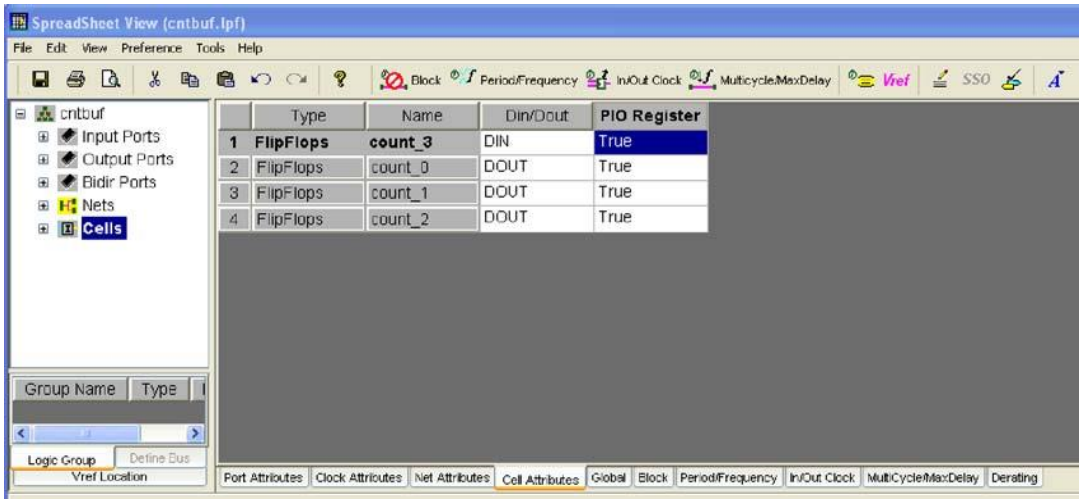

Figure B.2. Cell Attributes Tab

Users can assign V_{REF} for a bank using the V_{REF} Setting option in the Design Planner. See the software online help for a more detailed description of this setting.

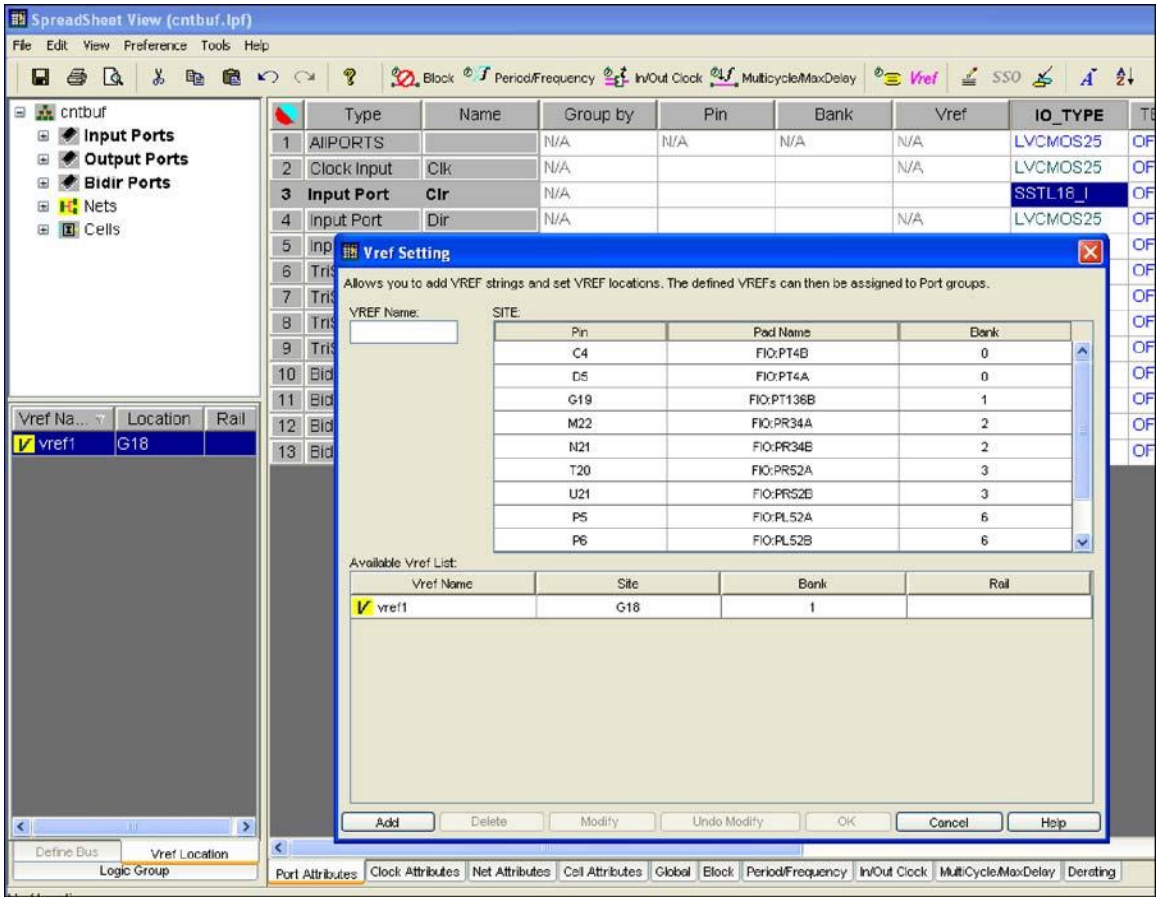

Figure B.3. V_{REF} Assignment in Design Planner

Appendix C. sysIO Attributes Using the Diamond Spreadsheet View User Interface

sysIO buffer attributes can be assigned using the Spreadsheet view in the Lattice Diamond design software. The Port Assignments Sheet lists all the ports in a design and all the available sysIO attributes in multiple columns. Click on each of these cells for a list of all the valid I/O preferences for that port. Each column takes precedence over the next. Therefore, when you choose a particular IO_TYPE, the columns for the DRIVE, PULLMODE, SLEWRATE and other attributes will only list the valid entries for that IO_TYPE.

Pin locations can be locked using the Pin column of the Port Assignments sheet or using the Pin Assignments sheet. You can right-click on a cell and go to Assign Pins to see a list of available pins.

The Spreadsheet View also has an option to run a DRC check to check for any incorrect pin assignments. You can enter the DIN/ DOUT preferences using the Cell Mapping tab. All the preferences assigned using the Spreadsheet view are written into the logical preference file (.lpf).

Figure B.3 shows the Port Assignments Sheet of the Spreadsheet view. For further information on how to use the Spreadsheet view, refer to the Diamond Help documentation, available in the Help menu option of the software.

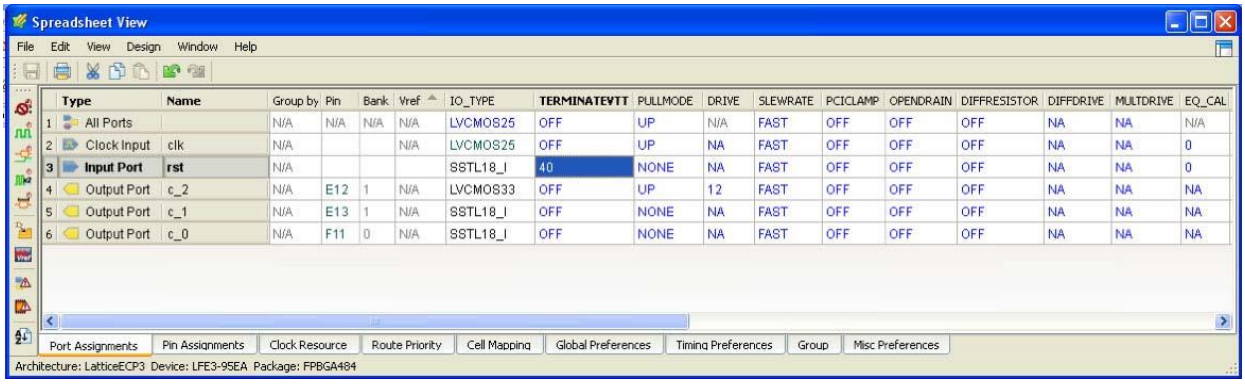

Figure C.1. Port Attributes Tab of SpreadSheet View

Users can create a V_{REF} pin using the Spreadsheet view as shown in Figure C.2 and then assign V_{REF} for a bank using the V_{REF} Column in the Ports Assignment Tab of the Spreadsheet View as show in Figure C.3. See the Diamond online help for a more detailed description of this setting.

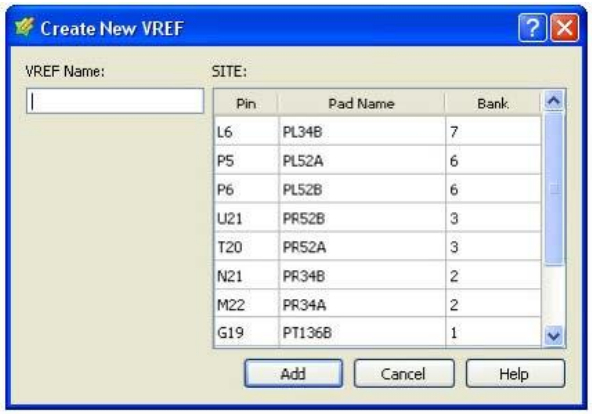

Figure C.2. Creating a VREF in Spreadsheet View

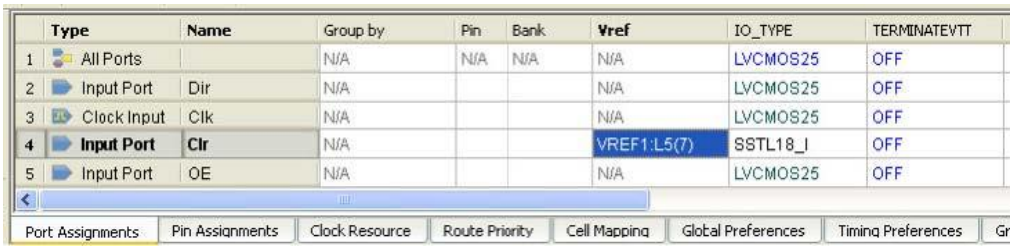

Figure C.3. Assigning a VREF for an Input Port in Spreadsheet View

References

- LatticeECP3 Family Devices web page
- Boards, Demos, IP Cores, and Reference Designs for LatticeECP3 Family Devices web page
- Lattice Diamond Software web page
- Lattice Insights for Lattice Semiconductor Training Series and Learning Plans

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, refer to the Lattice Answer Database at www.latticesemi.com/Support/AnswerDatabase.

Revision History

Revision 2.3, March 2024

Section	Change Summary
All	• Changed document number from *TN1177* to *FPGA-TN-02194*. • Updated document template.
Disclaimers	Added this section.
Acronyms in This Document	Added this section.
References	Added this section.
Technical Support Assistance	Added the link to Lattice Answer Database.

Revision 2.2, August 2013

Section	Change Summary
Software sysIO Attributes	Updated DRIVE Settings table.
Technical Support Assistance	Updated Technical Support Assistance information.

Revision 2.1, March 2013

Section	Change Summary
sysIO Banking Scheme	Mixed Voltage Support in Top Banks table – Updated footnote 2.

Revision 2.0, June 2012

Section	Change Summary
Supported sysIO Standards	• Supported Input Standards table – Updated VCCIO column and removed GTL+ row. • Supported Output Standards table – Updated VCCIO information for Point-to-Point LVDS.
sysIO Banking Scheme	• Mixed Voltage Support in Top Banks table – Updated footnote 2. • Mixed Voltage Support in Left and Right Banks table – Updated footnote 1.

Revision 1.9 March 2012

Section	Change Summary
Appendix A	Verilog Synplicity Attribute Syntax table – Corrected information in the Syntax column.

Revision 1.8 March 2012

Section	Change Summary
All	Updated document with new corporate logo.

Revision 1.7 April 2011

Section	Change Summary
All	Updated to clarify PCICLAMP programmability and DRIVE settings availably with and without OPENDRAIN.

Revision 1.6 March 2011

Section	Change Summary
sysIO Buffer Configurations	Added support for GTL+ input standard using HSTL input buffer.

Revision 1.5 November 2010

Section	Change Summary
Supported sysIO Standards	Updated Supported Input Standards table.
sysIO Banking Scheme	• Updated Hot Socketing Support text section • Updated Hot Socketing row of the I/O Standards Supported per Bank table. • Updated first footnote in the Mixed Voltage Support in Left and Right Banks table.

Revision 1.4 June 2010

Section	Change Summary
Appendix C	Added Appendix C - sysIO Attributes Using the Diamond Spreadsheet View User Interface.

Revision 1.3 April 2010

Section	Change Summary
All	Removed support for programmable PCICLAMP, equalization and VREF pins in Bank 8.

Revision 1.2 August 2009

Section	Change Summary
sysIO Buffer Configurations	Updated On-Chip Termination text section
Software sysIO Attributes	Updated DIFFRESISTOR text section.
Design Considerations and Usage	Updated Banking Rules bullets.

Revision 1.1 May 2009

Section	Change Summary
sysIO Banking Scheme	• Updated Mixed Voltage Support in Top Banks table. • Updated Mixed Voltage Support in Left and Right Banks table.
Software sysIO Attributes	Added FIXEDDELAY attribute support for SDR registers.

Revision 1.0 February 2009

Section	Change Summary
All	Initial release.

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