



# Power Consumption and Management for LatticeECP3 Devices

## Technical Note

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## 1. Introduction

A key requirement for designers using FPGA devices is the ability to calculate the power dissipation of a particular device used on a board. LatticeECP3™ devices bring together the lowest-power FPGA with SERDES and the state-of-the-art ispLEVER® Power Calculator tool. This technical note provides information on power supply considerations and the power calculations that the Power Calculator tool provides. Also included are some guidelines to reduce power consumption.

## 2. Power Supply Sequencing and Hot Socketing

LatticeECP3 devices have been designed to ensure predictable behavior during power-up and power-down. During power-up and power-down sequences, the I/Os remain in tri-state until the power supply voltage is high enough (VCCMIN) to ensure reliable operation. In addition, leakage into I/O pins is controlled to within the limits specified in the [LatticeECP3 Family Data Sheet](#), allowing for easy integration with the rest of the system.

These capabilities, along with lowest-power FPGA with SERDES, makes the LatticeECP3 the ideal choice for many low-power, high-speed SERDES, multiple power supply and hot-swap applications.

## 3. Recommended Power-up Sequence

Refer to the DC and Switching Characteristics section of the [LatticeECP3 Family Data Sheet](#) for more information on any power-up sequence for LatticeECP3 family.

## 4. Power Calculator Hardware Assumptions

Power consumption for a device can be coarsely broken down into the static (or DC) element and the dynamic (or AC) element. These elements have the following dependencies with respect to the junction temperature (T<sub>J</sub>) of the die.

- Static power is a result of the leakage associated with the transistors. There are two types of static leakage.
  - Static leakage which has a strong temperature dependency
  - DC bias which is fairly constant across temperature
- Dynamic power is caused by the toggling of signals in the transistor.
  - Dynamic power is fairly constant across temperature

Each component in an FPGA (e.g., LUT, register, EBR block, I/O etc.) has its own coefficients for static and dynamic positions. Certain selections in the Power Calculator tool affect some of these coefficients which are discussed in the Power Calculator section.

## 5. Power Calculator

Power Calculator is the fastest power simulation tool available in the industry. The tool offers Estimation Mode for “what-if” analysis, and also allows designers to import NCD design files to accurately estimate power for their designs. The background engine performs each calculation quickly and accurately.

When running the Power Calculator tool in Estimation mode, designers provide estimates of the utilization of various components and the tool provides an estimate of the power consumption. This is a good start, especially for what-if analyses and device selection.

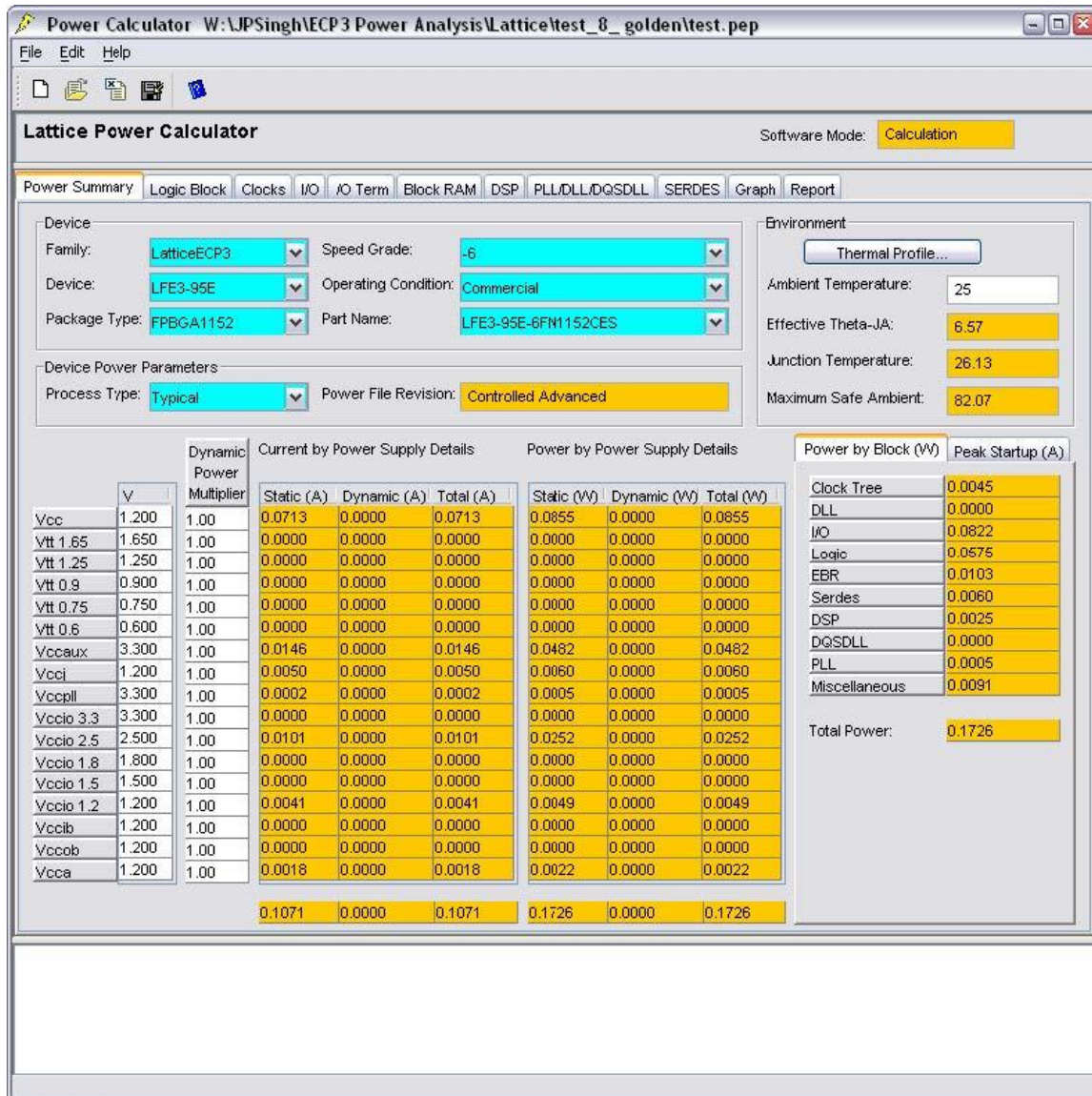
Calculation mode is a more accurate approach, where the designer imports the actual device utilization by importing the post place and route netlist design file (or NCD) file.

Users can also import a Trace Report (or TWR) file where the frequencies for various clocks are also imported. Note that the Trace Report only includes frequencies of the clocks nets that are constrained in the Preference file.

The default Activity Factor (AF%) for dynamic power calculation is set to 10% in the Power Calculator. Users can change the default AF for the entire project or for each clock net individually. Activity Factor is discussed in more detail later in this document.

## 5.1. Power Calculator and Power Equations

Please refer to the ispLEVER Tutorial for launching and using the Power Calculator tool under **Help > ispLEVER Help**. Once you step through the procedure, you will see a window that looks like [Figure 5.1](#).



**Figure 5.1. Power Calculator Main Window**

It is important to understand how the options available with Power Calculator affects the power. For example, if the ambient temperature is changed, it affects the junction temperature, according to the following equation:

$$T_J = T_A + \Theta_{JA\_EFFECTIVE} * P$$

Where  $T_J$  and  $T_A$  are the junction and ambient temperatures, respectively, and  $P$  is the power.

$\Theta_{JA\_EFFECTIVE}$  is the effective thermal impedance between the die and its environment.

The junction temperature is directly proportional to the ambient temperature. An increase in  $T_A$  will increase  $T_J$  and result in an increase of the static leakage component.

Selecting the Process Type again affects the static leakage; in particular the static leakage coefficient changes.

The DC Bias component is constant across the range.

For dynamic power, increasing the frequency of toggling will increase the dynamic component of power.

## 5.2. Typical and Worst Case Process Power/ICC

Another factor that affects DC power is process variation. This variation, in turn, causes variation in quiescent power.

Power Calculator takes these factors into account and allows designers to specify either a typical process or a worst case process.

## 5.3. Junction Temperature

Junction temperature is the temperature of the die during operation. It is one of the most important factors that affects the device power. For a fixed junction temperature, voltage and device package combination, quiescent power is fixed.

Ambient temperature affects the junction temperature as shown in Equation 1. Devices operating in a high-temperature environment have higher leakage since their junction temperature will be higher. Power Calculator models this ambient to junction temperature dependency. When the user provides an ambient temperature, it is rolled into an algorithm that calculates the junction temperature and power through an iterative process to find the thermal equilibrium of the system (device running with the design) with respect to its environment ( $T_A$ , airflow etc.).

## 5.4. Maximum Safe Ambient Temperature

Max. Safe Ambient Temperature is one of the most important numbers displayed in the Summary tab of the Power Calculator. This is the maximum ambient temperature at which the design can run without violating the junction temperature limits for commercial or industrial devices.

Power Calculator uses an algorithm to accurately predict this temperature. The algorithm adjusts itself as the user changes options such as voltage, process, frequency, AF% etc. (or any factor that may affect the power dissipation of the device).

## 5.5. Operating Temperature Range

When designing a system, engineers must make sure a device operates at specified temperatures within the system environment. This is particularly important to consider before a system is designed. With Power Calculator, users can predict device thermodynamics and estimate the dynamic power budget. The ability to estimate a device's operating temperature prior to board design also allows the designer to better plan for power budgeting and airflow.

Although total power, ambient temperature, thermal resistance and airflow all contribute to device thermodynamics, the junction temperature (as specified in the [LatticeECP3 Family Data Sheet](#)) is the key to device operation. The allowed junction temperature range is 0°C to 85°C for commercial devices and -40°C to 100°C for industrial devices. Anytime the junction temperature of the die falls out of these ranges, the performance and reliability of the device's operation must be evaluated. The reliability limit of junction temperature, on the other hand, for this generation of device technology is 125°C.

## 5.6. Dynamic Power Multiplier (DPM)

It is difficult to estimate the temperature dependence of dynamic power due to various ways in which a design can be placed and routed. The user-defined frequency of operation makes this problem even more complex. To help resolve this issue, the Dynamic Power Multiplier provides some guard bands for system and board designers.

The Dynamic Power Multiplier is defaulted to "1" which means the dynamic power is what it is. If the user wishes to add 20% additional dynamic power, the DPM can be set to 1.2 (1 + 20%) and it can be placed against the appropriate power supply. This increases the dynamic power for that supply by 20% and provides users with some guard band (if needed).

## 5.7. Power Budgeting

Power Calculator provides the power dissipation of a design under a given set of conditions. It also predicts the junction temperature ( $T_J$ ) for the design. Any time this junction temperature is outside the limits specified in the LatticeECP3 Family Data Sheet, the viability of operating the device at this junction temperature must be re-evaluated.

A commercial device is likely to show speed degradation with a junction temperature above 85°C and an industrial device at a junction temperature will degrade above 100°C. It is required that the die temperature be kept below these limits to achieve the guaranteed speed operation.

Operating a device at a higher temperature also means a higher SICC. The difference between the SICC and the total ICC (both Static ICC and Dynamic ICC) at a given temperature provides the dynamic budget available. If the device runs at a dynamic ICC higher than this budget, the total ICC is also higher. This causes the die temperature to rise above the specified operating conditions.

There are a number of ways to handle this situation. Some of these are discussed in the Power Management section of this document.

The four factors of power, ambient temperature, thermal resistance and airflow, can also be varied and controlled to reduce the junction temperature of the device. Power Calculator is a powerful tool to help system designers to properly budget the FPGA power that, in turn, helps improve overall system reliability.

## 6. Activity Factor Calculation

The Activity Factor % (or AF%) is defined as the percentage of frequency (or time) that a signal is active or toggling the output. Most resources associated with a clock domain are running or toggling at some percentage of the frequency at which the clock is running. Users must provide this value as a percentage under the AF% column in the Power Calculator tool.

Another term for I/Os is the I/O Toggle Rate. The AF% is applicable to the PFU, Routing, and Memory Read Write Ports, etc. The activity of I/Os is determined by the signals provided by the user (in the case of inputs) or as an output of the design (in the case of outputs). The rates at which the I/Os toggle define their activity. The I/O Toggle Rate or the I/O Toggle Frequency is a better measure of their activity.

The Toggle Rate (or TR) in MHz of the output is defined in the following equation:

$$\text{Toggle Rate (MHz)} = 1/2 * f * \text{AF\%} \quad (5)$$

Users are required to provide the TR (MHz) value for the I/O instead of providing the frequency and AF% for other resources. AF can be calculated for each routing resource, output or PFU. However, this involves long calculations. The general recommendation for a design occupying roughly 30% to 70% of the device is an AF% between 15% and 25%. This is an average value. The accurate value of an AF depends upon clock frequency, stimulus to the design and the final output.

### 6.1. Thermal Impedance and Airflow

A common method for characterizing a packaged device's thermal performance is with "Thermal Resistance",  $\Theta$ . For a semiconductor device, thermal resistance indicates the steady state temperature rise of the die junction above a given reference for each watt of power (heat) dissipated at the die surface. Its units are °C/W.

The most common examples are  $\Theta_{JA}$ , Thermal Resistance Junction-to-Ambient (in °C/W) and  $\Theta_{JC}$ , Thermal Resistance Junction-to-Case (also in °C/W). Another factor is  $\Theta_{JB}$ , Thermal Resistance Junction-to-Board (in °C/W).

Knowing the reference (i.e. ambient, case, or board) temperature, the power, and the relevant  $\Theta$  value, the junction temperature can be calculated per following equations.

$$T_J = T_A + \Theta_{JA} * P \quad (6)$$

$$T_J = T_C + \Theta_{JC} * P \quad (7)$$

$$T_J = T_B + \Theta_{JB} * P \quad (8)$$

Where  $T_J$ ,  $T_A$ ,  $T_C$  and  $T_B$  are the junction, ambient, case (or package) and board temperatures (in °C), respectively.  $P$  is the total power dissipation of the device.

$\Theta_{JA}$  is commonly used with natural and forced convection air-cooled systems.  $\Theta_{JC}$  is useful when the package has a high conductivity case mounted directly to a PCB or heatsink. And  $\Theta_{JB}$  applies when the board temperature adjacent to the package is known.

Power Calculator utilizes the ambient temperature (°C) to calculate the junction temperature (°C) based on the  $\Theta_{JA}$  for the targeted device. Users can also provide the airflow values (in LFM) to obtain a more accurate junction temperature value.

To improve airflow effectiveness, it is important to maximize the amount of air that flows over the device or the surface area of the heat sink. The airflow around the device can be increased by providing an additional fan or increasing the output of the existing fan. If this is not possible, baffling the airflow to direct it across the device may help. This means the addition of sheet metal or objects to provide the mechanical airflow guides to guide air to the target device. Often the addition of simple baffles can eliminate the need for an extra fan. In addition, the order in which air passes over devices can impact the amount of heat dissipated.

## 7. Reducing Power Consumption

One of the most critical challenges for designers today is reducing the system power consumption. A low-order reduction in power consumption goes a long way, especially in modern hand-held devices and electronics. There are several design techniques that can be used to significantly reduce overall system power consumption. Some of these include:

1. Reducing operating voltage.
2. Operating within the specified package temperature limitations.
3. Using optimum clock frequency reduces power consumption, as the dynamic power is directly proportional to the frequency of operation. Designers must determine if some portions of the design can be clocked at a lower rate that will reduce power.
4. Reducing the span of the design across the device. A more closely-placed design uses fewer routing resources and therefore less power.
5. Reducing the voltage swing of the I/Os where possible.
6. Using optimum encoding where possible. For example, a 16 bit binary counter has, on average, only 12% activity factor and a 7-bit binary counter has an average of 28% activity factor. On the other hand, a 7-bit LFSR counter will toggle at an activity factor of 50%, which causes higher power consumption. A gray code counter, where only one bit changes at each clock edge will use the least amount of power, as the activity factor is less than 10%.
7. Minimizing the operating temperature by the following methods:
  - Use packages that can better dissipate heat, such as ceramic packages.
  - Placing heat sinks and thermal planes around the device on the PCB.
  - Use better airflow techniques, such as mechanical airflow guides and fans (both system fans and device mounted fans).



## 8. Power Calculator Assumptions

The following are the assumptions made by the Power Calculator.

1. The Power Calculator tool uses equations with constants based on a room temperature of 25°C.
2. Users can define the ambient temperature ( $T_A$ ) for device junction temperature ( $T_J$ ) calculation based on the power estimation.  $T_J$  is calculated from the user-entered  $T_A$  and the power calculation of typical room temperature.
3. I/O power consumption is based on an output loading of 5 pF. Users have the ability to change this capacitive loading.
4. Users can estimate power dissipation and current for each type of power supply ( $V_{CC}$ ,  $V_{CCIO}$ ,  $V_{CCI}$  and  $V_{CCAUX}$ ). For  $V_{CCAUX}$ , only static  $I_{CCAUX}$  values are provided in the Power Calculator.
5. Additional  $V_{CCAUX}$  contributions due to differential output buffers, differential input buffers and reference input buffers must be added per pair for differential buffers or per pin for reference input buffers, according to the user's design. See the equation given in this technical note for Total DC Power ( $I_{CCAUX}$ ).
6. The nominal  $V_{CC}$  is used by default to calculate power consumption. A lower or higher  $V_{CC}$  can be chosen from a list of available values.
7. Users can enter Airflow in Linear Feet per Minute (LFM) along with a Heat Sink option to calculate the junction temperature.
8. The default value of the I/O types for LatticeECP3 devices is LVCMOS25, 12 mA.
9. The activity factor (AF) is defined as the toggle rate of the registered output. For example, assuming that the input of a flip-flop is changing at every clock cycle, 100% AF of a flip-flop running at 100 MHz is 50 MHz.

## Technical Support Assistance

Submit a technical support case through [www.latticesemi.com/techsupport](http://www.latticesemi.com/techsupport).

For frequently asked questions, refer to the Lattice Answer Database at [www.latticesemi.com/Support/AnswerDatabase](http://www.latticesemi.com/Support/AnswerDatabase).

## Revision History

### Revision 1.2, May 2023

Section	Change Summary
All	<ul style="list-style-type: none"><li>Changed document number from TN1181 to FPGA-TN-02189.</li><li>Updated document template.</li></ul>
Disclaimers	Added this section.
Power Calculator	In the <a href="#">Operating Temperature Range</a> section, updated the allowed junction temperature range for industrial devices from $-40\text{ }^{\circ}\text{C}$ to $105\text{ }^{\circ}\text{C}$ to $-40\text{ }^{\circ}\text{C}$ to $100\text{ }^{\circ}\text{C}$ .
Technical Support Assistance	Added a link to the Lattice Answer Database.

### Revision 1.1, February 2011

Section	Change Summary
All	Updated document with new corporate logo.

### Revision 1.0, February 2009

Section	Change Summary
All	Initial release.



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