LatticeECP3 Hardware Checklist

Technical Note

FPGA-TN-02183-2.2

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Acronyms in This Document

A list of acronyms used in this document.

Abbreviation	Definition
DDR	Double Data Rate
DLL	Delay-Locked Loop
HSTL	High-Speed Transceiver Logic
LUT	Look-Up Table
LVDS	Low-Voltage Differential Signaling
PCS	Physical Coding Sublayer
PLL	Phase-Locked Loop
SERDES	Serializer/Deserializer
SSTL	Stub Series Terminated Logic

1. Introduction

When designing complex hardware using the LatticeECP3™ FPGA, designers must pay special attention to critical hardware configuration requirements. This technical note steps through these critical hardware implementation items relative to the LatticeECP3 device. The document does not provide detailed step-by-step instructions but gives a high-level summary checklist to assist in the design process.

The device family consists of FPGA LUT densities ranging from 17K to150K. This technical note assumes that the reader is familiar with the LatticeECP3 device features as described in the LatticeECP3 Family Data Sheet (FPGA-DS-02074). The data sheet includes the functional specification for the device. Topics covered in the data sheet include but are not limited to the following:

- High-level functional overview
- Pinouts and packaging information
- Signal descriptions
- Device-specific information about peripherals and registers
- Electrical specifications

Please refer to the LatticeECP3 Family Data Sheet for the device-specific details.

- LatticeECP3 Family Data Sheet (FPGA-DS-02074)

The critical hardware areas covered in this technical note are:

- Power supplies as they relate to the LatticeECP3 power supply rails and how to connect them to the PCB and the associated system
- Configuration mode selection for proper power-up behavior
- Device I/O interface and critical signals

Important: Users should refer to the following documents for detailed recommendations.

- Electrical Recommendations for Lattice SERDES (FPGA-TN-02077)
- LatticeECP3 sysIO Usage Guide (FPGA-TN-02194)
- LatticeECP3 sysCONFIG™ Usage Guide (FPGA-TN-02192)
- LatticeECP3 High-Speed I/O Interface (FPGA-TN-02184)
- High-Speed PCB Design Considerations (FPGA-TN-02178)
- LatticeECP3 SERDES/PCS Usage Guide (FPGA-TN-02190)
- Decoupling and Bypass Filtering for Programmable Devices (FPGA-TN-02115)
- LatticeSC SERDES Jitter (TN1084)
- LatticeECP3 SERDES Characterization Report (TN1195)(available under NDA, contact your local Lattice sales representative)
- HSPICE SERDES CML simulation package and die models in RLGC format (available under NDA, contact the license administrator at lic_admin@latticesemi.com)
- LatticeECP3-related pinout information can be found on the Lattice web site.

2. Power Supplies

All supplies including V_{CC}, V_{CCAUX} and V_{CCIO8} power supplies determine the LatticeECP3 internal "power good" condition. These supplies need to be at a valid and stable level before the device can become operational. Several other supplies including V_{CCPLL}, V_{CCIB}, and V_{CCOB} are used in conjunction with on-board SERDES and phase-locked loops. Table 2.1. shows the power supplies and the appropriate voltage levels for each supply.

Table 2.1. LatticeECP3 FPGA Power Supplies

Supply	Voltage (Nominal Value)	Description
VCC	1.2V	FPGA core power supply.
VCCA	1.2V	Power supplies analog SERDES blocks. Should be isolated and "clean" from excessive noise.
VCCPLL[L:R]	3.3V	Power supply for PLL. Should be isolated and "clean" from excessive noise.
VCCAUX	3.3V	Auxiliary power supply
		I/O power supply. Seven general-purpose I/O banks and each bank has its own supply V_{CCIO0} to V_{CCIO3} and V_{CCIO6} to V_{CCIO8}.
VCCIO[0-3][1] & VCCIO[6-8][1]	1.2V to 3.3V	V_{CCIO8} is used in conjunction with the pins dedicated and shared with device configura- tion.
		V_{CCIO0} to V_{CCIO3} and V_{CCIO6} to V_{CCIO8} are optionally used based on per bank usage of I/O
VCCJ	1.2V to 3.3V	JTAG power supply for the TAP controller port.
VCCIB	1.2V to 1.5V	CML input termination voltage
VCCOB	1.2V to 1.5V	CML output termination voltage

Note: Banks 4 and 5 do not exist on the LatticeECP3. Therefore, VCCIO4 and VCCIO5 are not available.

The LatticeECP3 FPGA device has a power-up reset state machine that depends on various power supplies.

These supplies should come up monotonically. A power-up reset counter will begin to count after all of the approximate conditions are met:

- VCC reaches 0.8V or above
- VCCAUX reaches 2.7V or above
- VCCIO[8] reaches 0.8V or above

Initialization of the device will not proceed until the last power supply has reached its minimum operating voltage.

3. LatticeECP3 SERDES/PCS Power Supplies

Supplies dedicated to the operation of the SERDES/PCS include VCCA, VCCIB, VCCOB. All VCCA supply pins must always be powered to the recommended operating voltage range regardless of the SERDES use.

VCCIB and VCCOB can be left floating for unused SERDES channels. Unused channel outputs are tristated, with approximately 10 KOhm internal resistor connecting between the differential output pair.

When using the SERDES with 1.5 V VCCIB or VCCOB, the SERDES should not be left in a steady state condition with the 1.5 V power applied and the VCCA 1.2 V power not applied. Both the 1.2 V and the 1.5 V power should be applied to the SERDES at nominally the same time. The normal variation in ramp-up times of power supplies and voltage regulators is not a concern.

It is very important that the VCCA supply be low-noise and isolated from heavily loaded switching supplies. Please refer to Electrical Recommendations for Lattice SERDES (FPGA-TN-02077), for recommendations.

4. Power Estimation

Once the LatticeECP3 device density, package and logic implementation is decided, power estimation for the system environment should be determined based on the software Power Calculator provided as part of the ispLEVER®design tool. When estimating power, the designer should keep two goals in mind:

1. Power supply budgeting should be based on the maximum of the power-up in-rush current, configuration current or maximum DC and AC current for the given system's environmental conditions.
2. The ability for the system environment and LatticeECP3 device packaging to be able to support the specified maximum operating junction temperature. By determining these two criteria, LatticeECP3 power requirements are taken into consideration early in the design phase.

5. Configuration Considerations

The LatticeECP3 includes provisions to program the FPGA via a JTAG interface or though several modes utilizing the sysCONFIG port. The JTAG port includes a 4-pin interface. The interface requires the following PCB considerations.

Table 5.1. JTAG Pin Recommendations

JTAG Pin	PCB Recommendation
TDI	4.7K Pull-up to VCCJ
TMS	4.7K Pull-up to VCCJ
TDO	4.7K Pull-up to VCCJ
TCK	4.7K Pull-down

Every PCB should have easy access to FPGA JTAG pins. This enables debugging in the final system. For best results, route the TCK, TMS, TDI and TDO signals to a common test header along with VCCJ and ground.

Using other programming modes requires the use of the CFG[2:0] input pins. For JTAG, the MODE pins are not used. The CFG[2:0] pins include weak internal pull-ups. It is recommended that 5-10K external resistors be used when using the sysCONFIG modes. Pull-up resistors should be connected to VCCIO8.

The use of external resistors is always needed if the configuration signals are being used to handshake to other devices. Recommended 4.7K pull-up resistors to VCCIO8 and pull-down to board ground should be used on the following pins.

Table 5.2. Pull-up/Pull-down Recommendations for Configuration Pins

Pin	PCB Connection
PROGRAMN	Pull-up
INITN	Pull-up
CCLK	Pull-down
CFG[0:2]	See Table 5.3 1 = 4.7K pull-up, 0 = GND.

Table 5.3. Configuration Pins Needed per Programming Mode

Configuration Mode	Bus Size	Dedicated CFG[0:2]	sysCONFIG Pin Mapping + Dedicated Pins			Dedicated Pins
			Clock Pin	I/O	Shared Pins	
SPI Master (Fast/Slow)	1 bit	000	MCLK	O	SPISD0, CSSPIN, SPISI, DOUT, D0, CONT1N, CONT2N	PROGRAMN, INITN, DONE
		010	MCLK	O	SPISD[0,1], CSSPI[0,1]N, SPISI, D0, CONT1N, CONT2N	
Burst Flash	16 bits	001	MCLK	O	D[0:7], XD[8:15], AVDN, OEN, RDY	PROGRAMN, INITN, DONE
MPCM	8 bits	011	MCLK	O	D[0:7], CSN, CS1N, WRITEN, BUSY	PROGRAMN, INITN, DONE
Slave SPI	1 bit	100	CCLK	I	SO, SN, SI, DOUT,HOLDN	PROGRAMN, INITN, DONE
SCM	1 bit	101	CCLK	I	DI and DOUT	PROGRAMN, INITN, DONE
Parallel	8 bits	111	CCLK	I	D[0:7], CSN, CS1N, WRITEN, BUSY	PROGRAMN, INITN, DONE
JTAG	1 bit	XXX	TCK	I	NA	TCK, TMS, TDI, TDO

6. I/O Pin Assignments

The VCCA provides a “quiet” supply for the internal PLLs and critical SERDES blocks. For the best jitter performance, careful pin assignment will keep “noisy” I/O pins away from “sensitive” pins. The leading causes of PCB related SERDES crosstalk is related to FPGA outputs located in close proximity to the sensitive SERDES power supplies. These supplies require cautious board layout to insure noise immunity to the switching noise generated by FPGA outputs. Guidelines are provided to build quiet filtered supplies for the VCCA, however robust PCB layout is required to insure that noise does not infiltrate into these analog supplies.

Although coupling has been reduced in the device packages of the LatticeECP3 devices where little crosstalk is generated, the PCB board can cause significant noise injection from any I/O pin adjacent to SERDES data, reference clock, and power pins as well as other critical I/O pins such as clock signals. Electrical Recommendations for Lattice SERDES (FPGA-TN-02077), provides detailed guidelines for optimizing the hardware to reduce the likelihood of crosstalk to the analog supplies. PCB traces running in parallel for long distances need careful analysis. Simulate any suspicious traces using a PCB crosstalk simulation tool to determine if they will cause problems.

It is common practice for designers to select pinouts for their system very early in the design cycle. For the FPGA designer, this requires a detailed knowledge of the targeted FPGA device. Designers often use a spreadsheet program to initially capture the list of the design I/Os. Lattice provides detailed pinout information that can be downloaded from the Lattice website in .csv format for designers to use as a resource to create pinout information. For example, by navigating to www.latticesemi.com/documents/ecp3_17_pinout.csv the user can gather the pinout details for all the different package offerings of the ECP3-17 device family, including I/O banking, differential pairing, and input and output details.

7. Dedicated FPGA Inputs (Non-configuration)

Pins annotated E_A/B/C/D (example PR43E_A, PR43E_B, etc.) are dedicated input pins. The primary purpose of these pins is to provide a dedicated input to the FPGA PLLs. They are also available for use as general inputs into the FPGA fabric when not used with a PLL. However, they are available as inputs only. These pins cannot be an output or bidirectional.

8. Pinout Considerations

The LatticeECP3 supports many applications with high-speed interfaces. These include various rule-based pinouts that need to be understood prior to implementation of the PCB design. The pinout selection must be completed with an understanding of the interface building blocks of the FPGA fabric. These include IOLOGIC blocks such as DDR, clock resource connectivity, and PLL and DLL usage. Refer to LatticeECP3 High-Speed I/O Interface (FPGA-TN-02184) for rules pertaining to these interface types.

9. LVDS Pin Assignments

True-LVDS outputs are available on I/O pins on the left and right sides of the device. LVDS output differential drivers are not supported in banks on the top and bottom. Emulated LVDS outputs are available on any A and B pair around the device, but this will require external termination resistors. This is described in LatticeECP3 sysIO Usage Guide (FPGA-TN-02194).

LVDS inputs are available on any A and B pair of all I/O cells around the entire device. The LatticeECP3 device includes differential input terminations with a common mode connection to the bank VTT pin which must be left floating.

10. HSTL and SSTL Pin Assignments

These externally referenced I/O standards require an external reference voltage. The VREF pin(s) should get high priority when assigning pins on the PCB. Each bank includes a separate VREF voltage. VREF1 sets the threshold for the referenced input buffers. In the LatticeECP3 devices, any I/O pin in a bank can also be configured to be a dedicated reference voltage supply pin. However, the predefined VREF pins provide the best case. Each I/O is individually configurable based on the bank's supply and reference voltages.

In addition, there are dedicated Terminating Supply (VTT) pins to be used as terminating voltage for one of the two ways to perform parallel terminations. These VTT pins are located in banks 2, 3, 7 and 6 and may not be available in some packages. Unused VTT pins should be left not connected.

A calibration resistor is used to compensate output drivers. A 10Kohm +/-1% resistor connected between the XRES pin and PCB ground is needed.

11. XRES Pin

The XRES pin provides a PCB connected resistor (10K-ohm +/-1%) reference to the internal band gap circuit used by PLLs. Careful routing of the XRES pin is required to maintain a stable current source. The PCB should maintain a very short connection to the XRES resistor which must be connected directly to the PCB ground plane.

This XRES pin can also be protected by careful pin selection of adjacent signals in the design. Any "switching or noisy" signals on adjacent pins can increase the PLL output jitter due to cross coupling noise from the aggressor pin to the XRES pin.

It is strongly recommended to tie aggressor pins to PCB ground. If the user has to assign a function due to pin constraints, it is recommended that the pin should be a static or low-frequency control signal as opposed to a high-speed data signal. These aggressor pins are defined in Table 11.1.

Table 11.1. XRES Aggressor Pin Listing

Package	XRES Aggressor Pins
1156-ball BGA	AN29, AM31

12. SERDES Pin Considerations

High-speed signaling requires careful PCB design. Maintaining good transmission line characteristics is a requirement. A continuous ground reference should be maintained with high-speed routing. This includes tightly matched differential routing with very few discontinuities. Please refer to High-Speed PCB Design Considerations (FPGA-TN-02178), for suggested methods and guidance.

When operating at 2.5 Gpbs or above, use of the following FPGA I/O pins can cause increased jitter. Extra care must be given to these pins when used in combination with the high-speed SERDES interface. High-speed switching output assignments should be minimized or avoided on these pins when the SERDES interface is in use. Only static output or input configuration is recommended.

If using the PCSC quad on the 1156 package (for either LatticeECP3-70, LatticeECP3-95 or LatticeECP3-150), the following pins are affected: AE26, AF26, AG26, AH26, AH27, AJ27, AK27, AL27, AM27, AN27, AP27, AH28, AJ28, AK28, AL28, AM28, AN28, AP28, AK29, AL29, AM29, AN29, AP29.

If using the PSCD quad on the 1156 package (for LatticeECP3-150), the following pins are affected: AE9, AF9, AG9, AH9, AJ8, AK8, AL8, AM8, AN8, AP8, AH7, AJ7, AK7, AL7, AM7, AN7, AP7, AJ6, AK6, AL6, AM6, AN6, AP6.

The above mentioned aggressor pin list can only impact SERDES quads PCSC and PCSD. Quads PCSA and PCSB have no suggested aggressor pins due to the physical layout of the device.

There are no known aggressor I/O pins for any other LatticeECP3 device/package combinations other than the beforementioned devices.

Table 12.1. Hardware Checklist

	Item	OK	NA
1	**FPGA Power Supplies**		
1.1	VCC core @ 1.2V +/-5%		
1.1.1	Use a PCB plane for VCC core with proper decoupling		
1.1.2	VCC core sized to meet power requirement calculation from software		
1.2	VCCA @ 1.2V +/-5%		
1.2.1	VCCA “quiet” and isolated”		
1.2.2	VCCA pins should be ganged together and a solid PCB plane is recommended. This plane should not have adjacent non-SERDES signals passing above or below. It should also be isolated from the VCC core power plane.		
1.3	All VCCIO[1-8] 1.2V to 3.3V		
1.3.1	VCCIO8 used with configuration interfaces (i.e. memory devices). Need to match specifications.		
1.3.2	VCCIO[1:7] used based on user design		
1.4	VCCAUX @ 3.3V +/-5%		
1.4.1	VCCPLL @ 3.3V +/-5%		
1.4.2	VCCPLL “quiet” and isolated” @ 3.3V +/-5%		
1.5	VCCJ 1.2V to 3.3V		
1.6	Power estimation		
1.7	10K-ohm +/-1% pull-down on XRES pin		
1.7.1	XRES pin uses short connection to resistor. Resistor connected directly to PCB ground plane.		
1.7.2	Follow XRES aggressor pin recommendation.		
2	**SERDES Power Supplies**		
2.3	VCCIB and VCCOB connected for USED SERDES channels		
2.3.1	VCCIB and VCCOB 1.2V-1.5V nominal +/-5%		
3	**Configuration**		
3.1	Pull-ups and pull-downs on configuration specific pins		
3.2	VCCIO8 bank voltage matches sysCONFIG peripheral devices such as SPI Flash		
3.3	Pull-up or pull-down on SPIFASTN pin		
4	**SERDES**		
4.1	Dedicated reference clock input from clock source meets the DC and AC requirements		
4.1.1	External AC coupling caps may be required for compatibility to common-mode levels		
4.1.2	Ref clock termination resistors may be needed for compatible signaling levels		
4.2	Maintain good high-speed transmission line routing		
4.2.1	Continuous ground reference plane to serial channels		
4.2.2	Tightly length matched differential traces		
4.2.3	Do not pass other signals on the PCB above or below the high-speed SERDES without isolation.		
4.2.4	Keep non-SERDES signal traces from passing above or below the 1.2V VCCA power plane without isolation.		
4.2.5	Avoid the aggressor pins mentioned previously in this document.		
5	**Special Pin Assignments**		
5.2	VREF assignments followed for single-ended HSTL or SSTL inputs		
5.2.1	Properly decouple the VREF source		
5.3	VTT pins needed for on-die termination for HSTL or SSTL terminated I/O		
5.3.1	All VTT need to be connected to termination power supply if used for VTT. VTT pins do not need to be connected if ODT (on-die termination) is not used in the design. VTT pins can be left floating when not used for ODT.		
5.3.2	VTT power connections (for SSTL or HSTL terminations) needs to be a low-impedance PCB plane and properly decoupled.		

	Item	OK	NA
5.3.3	The bank VTT pin must float when using differential input terminations.		
6	**Critical Pinout Selection**		
6.1	Pinout has been chosen to address FPGA resource connections to I/O logic and clock resources per LatticeECP3 High-Speed I/O Interface (FPGA-TN-02184).		
6.2	Dedicated FPGA inputs are used as inputs only to the FPGA PLL or fabric. Not output or bi-directional.		
7	**JTAG**		
7.1	Pulldown on TCK. See Table 5.1.		
7.2	Pullups on TDI, TMS, TDO. See Table 5.1.		
8	**DDR3 Interface Requirements**		
8.1	DQ, DM, and DQS signals should be routed in a data group and should have similar routing and matched via counts. Using more than three vias is not recommended in the route between the FPGA controller and memory device.		
8.2	Maintain a maximum of ±50 mil between any DQ/DM and its associated DQS strobe within a DQ group. Use careful serpentine routing to meet this requirement.		
8.3	All data groups must reference a ground plane within the stack-up.		
8.4	DDR trace reference must be solid without slots or breaks. It should be continuous between the FPGA and the memory.		
8.5	Provide a separation of 3W spacing between a data group and any other unrelated signals to avoid crosstalk issues. Use a minimum of 2W spacing between all DDR traces excluding differential CK and DQS signals.		
8.6	Assigned FPGA I/O within a data group can be swapped to allow clean layout. Do not swap DQS assignments.		
8.7	Differential pair of DQS to DQS_N trace lengths should be matched at ±10 mil.		
8.8	Resistor terminations (DQ) placed in a fly-by fashion at the FPGA is highly recommended. Stub fashion terminations, if used, should not include a stub longer than 600 mil.		
8.9	LDQS/LDQS_N and UDQS/UDQS_N trace lengths should be matched within ±100 mil.		
8.10	Address/control signals and the associated CK and CK_N differential FPGA clock should be routed with a control trace matching ±100 mil.		
8.11	CK to CK_N trace lengths must be matched to within ±10 mil.		
8.12	Address and control signals can be referenced to a power plane if a ground plane is not available. Ground reference is preferred.		
8.13	Address and control signals should be kept on a different routing layer from DQ, DQS, and DM to isolate crosstalk between the signals.		
8.14	Differential terminations used by the CLK/CLKN pair must be located as close as possible to the memory.		
8.15	Address and control terminations placed after the memory component using a fly-by technique are highly recommended. Stub fashion terminations, if used, should not include a stub longer than 600 mils.		

References

- LatticeECP3 Family Devices web page
- Boards, Demos, IP Cores, and Reference Designs for LatticeECP3 Family Devices web page
- Lattice Diamond Software web page
- Lattice Insights for Lattice Semiconductor Training Series and Learning Plans

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, refer to the Lattice Answer Database at www.latticesemi.com/Support/AnswerDatabase.

Revision History

Revision 2.2, March 2024

Section	Change Summary
All	• Changed document number from *TN1189* to *FPGA-TN-02183*. • Updated document template.
Disclaimers	Added this section.
Acronyms in This Document	Added this section.
References	Added this section.
Technical Support Assistance	Added the link to Lattice Answer Database.

Revision 2.1, February 2012

Section	Change Summary
Disclaimers	Updated document with new corporate logo.

Revision 2.0, July 2011

Section	Change Summary
XRES Pin	Added XRES pin information.

Revision 1.9, July 2011

Section	Change Summary
SERDES Pin Considerations	Added DDR3 Interface Requirements section to Hardware Checklist.

Revision 1.8, June 2011

Section	Change Summary
SERDES Pin Considerations	Added Pull-up or pull-down on SPIFASTN pin to Hardware Checklist.

Revision 1.7, December 2010

Section	Change Summary
SERDES Pin Considerations	Updated Hardware Checklist.

Revision 1.6, March 2010

Section	Change Summary
All	Updated reference documents list.

Revision 1.5, November 2009

Section	Change Summary
Introduction	Updated FPGA LUT densities in this section.
SERDES Pin Considerations	Updated this text section.

Revision 1.4, August 2009

Section	Change Summary
SERDES Pin Considerations	Updated this text section with information regarding pins that can cause increased jitter when operating at 2.5 Gpbs and above.

Revision 1.3, July 2009

Section	Change Summary
Power Supplies	LatticeECP3 FPGA Power Supplies table - Updated voltage values for VCCIB and VCCOB supplies.

Revision 1.2, July 2009

Section	Change Summary
SERDES Pin Considerations	• Added Dedicated FPGA Inputs (Non-configuration) and Pinout Considerations text sections. • Added Critical Pinout Selection section to Hardware Checklist table.

Revision 1.1, March 2009

Section	Change Summary
SERDES Pin Considerations	Updated Hardware Checklist table.

Revision 1.0, February 2009

Section	Change Summary
All	Initial release.

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