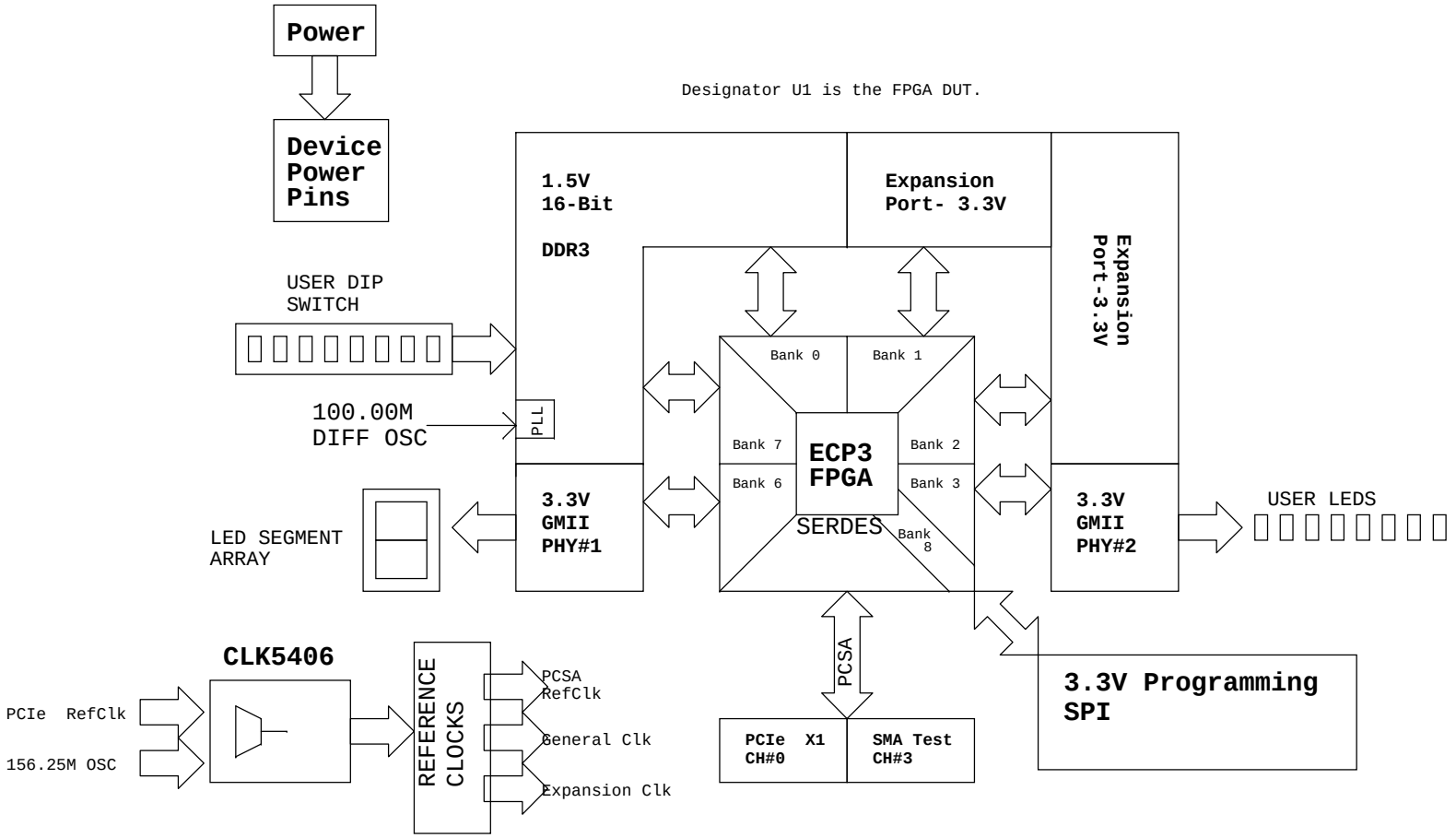
Revision History:

| | | |
|---|---|---|
| February 9, 2011 | Rev A Final Design | JPS |
| February 24, 2011 | Rev B | JPS |



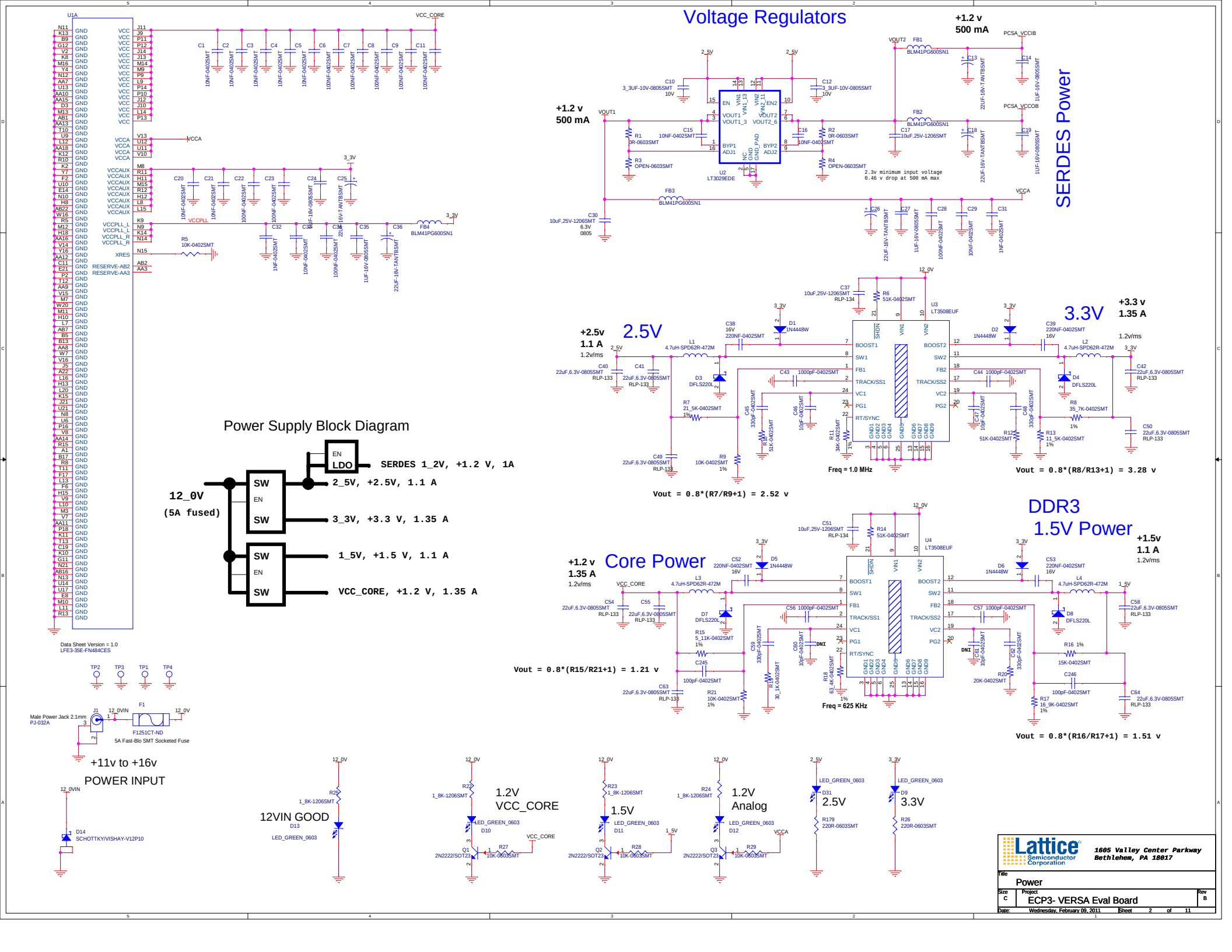


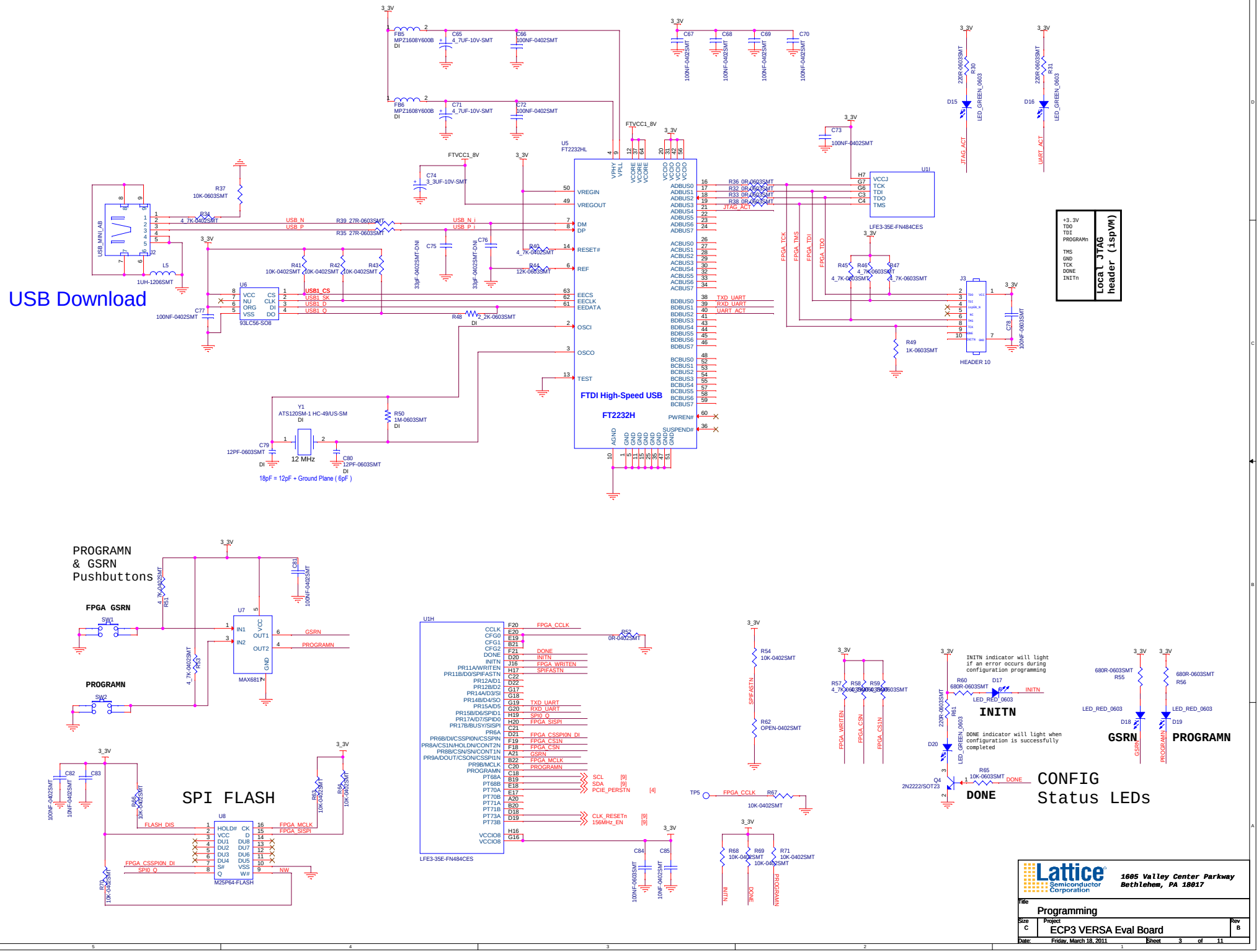
Lattice Semiconductor Corporation
1605 Valley Center Parkway
Bethlehem, PA 18017

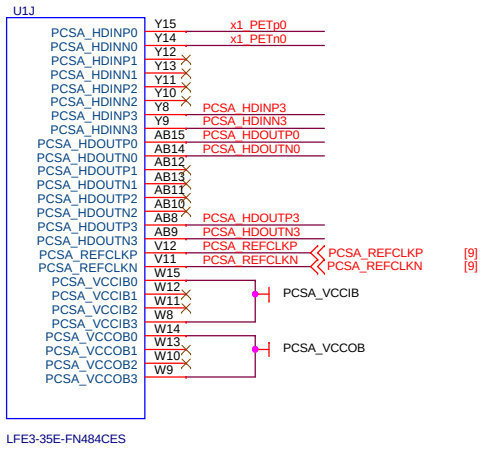

Title: Cover Page

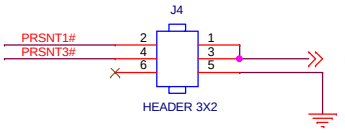
Size: B | Project: ECP3 VERSA Eval Board | Rev: B

Date: Monday, March 14, 2011 | Sheet 1 of 11

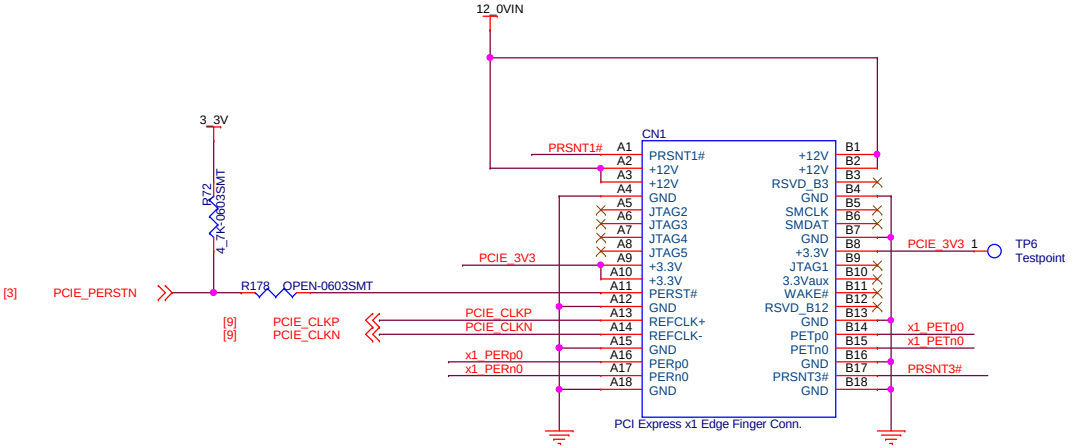

Voltage Regulators
SERDES Power
+1.2 v
500 mA
PCSA_VCCIB
PCSA_VCCOB
VCCA
VCC_CORE
2.5V
+2.5v
1.1 A
1.2v/ms
Vout = 0.8*(R7/R9+1) = 2.52 v
Freq = 1.0 MHz
3.3V
+3.3 v
1.35 A
1.2v/ms
Vout = 0.8*(R8/R13+1) = 3.28 v
DDR3
1.5V Power
+1.5v
1.1 A
1.2v/ms
Core Power
+1.2 v
1.35 A
1.2v/ms
Vout = 0.8*(R15/R21+1) = 1.21 v
Freq = 625 KHz
Vout = 0.8*(R16/R17+1) = 1.51 v
Power Supply Block Diagram
12_0V
(5A fused)
SW
EN
LDO
SERDES 1_2V, +1.2 V, 1A
2_5V, +2.5V, 1.1 A
3_3V, +3.3 V, 1.35 A
1_5V, +1.5 V, 1.1 A
VCC_CORE, +1.2 V, 1.35 A
Data Sheet Version = 1.0
LFE3-35E-FN484CES
Male Power Jack 2.1mm
PJ-032A
5A Fast-Blo SMT Socketed Fuse
+11v to +16v
POWER INPUT
SCHOTTKY/VISHAY-V12P10
12VIN GOOD
1.2V
VCC_CORE
1.5V
1.2V
Analog
2.5V
3.3V
LED_GREEN_0603
2.5v minimum input voltage
0.46 v drop at 500 mA max
Lattice Semiconductor Corporation
1605 Valley Center Parkway
Bethlehem, PA 18017
Title
Power
Size
C
Project
ECP3- VERSA Eval Board
Rev
B
Date:
Wednesday, February 09, 2011
Sheet
2
of
11

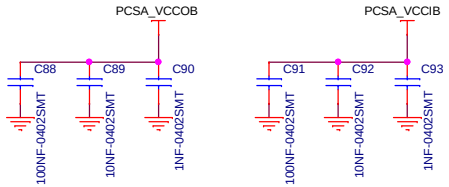

USB Download
FTDI High-Speed USB
FT2232H
U5
FT2232HL
USB_MINI_AB
93LC56-SO8
LFE3-35E-FN484CES
HEADER 10
Local JTAG header (ispVM)
+3.3V
TDO
TDI
PROGRAMn
TMS
GND
TCK
DONE
INITn
PROGRAMN & GSRN Pushbuttons
FPGA GSRN
PROGRAMN
MAX6817
SPI FLASH
M25P64-FLASH
INITN indicator will light if an error occurs during configuration programming
DONE indicator will light when configuration is successfully completed
INITN
DONE
GSRN
PROGRAMN
CONFIG Status LEDs
Lattice Semiconductor Corporation
1605 Valley Center Parkway
Bethlehem, PA 18017
Programming
ECP3 VERSA Eval Board
Friday, March 18, 2011





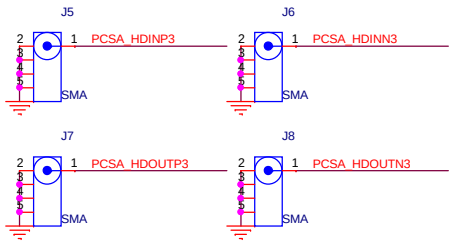



## X1 PCIe Board Fingers

**B side = Primary Component Side(TOP)**
**A side = Secondary Component Side(BOTTOM)**

All Nets are 85-ohm differential pairs.
The P and N traces shall be <20mil matched in length




All Nets to SMAs are 100-ohm differential pairs.
The P and N traces shall be <20mil matched in length

Lattice Semiconductor Corporation
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Title: SERDES
Size: B
Project: ECP3 VERSA Eval Board
Rev: B
Date: Wednesday, February 09, 2011
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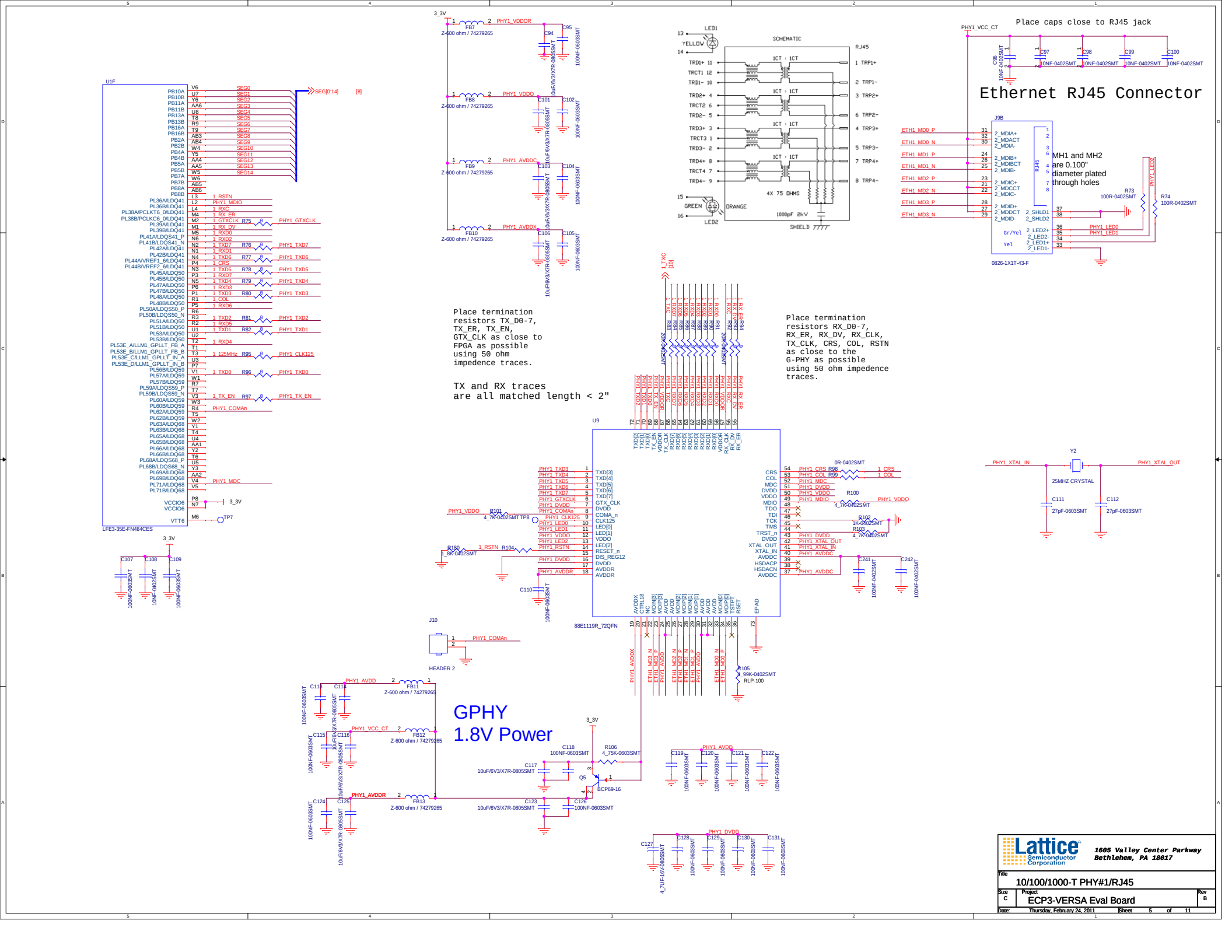
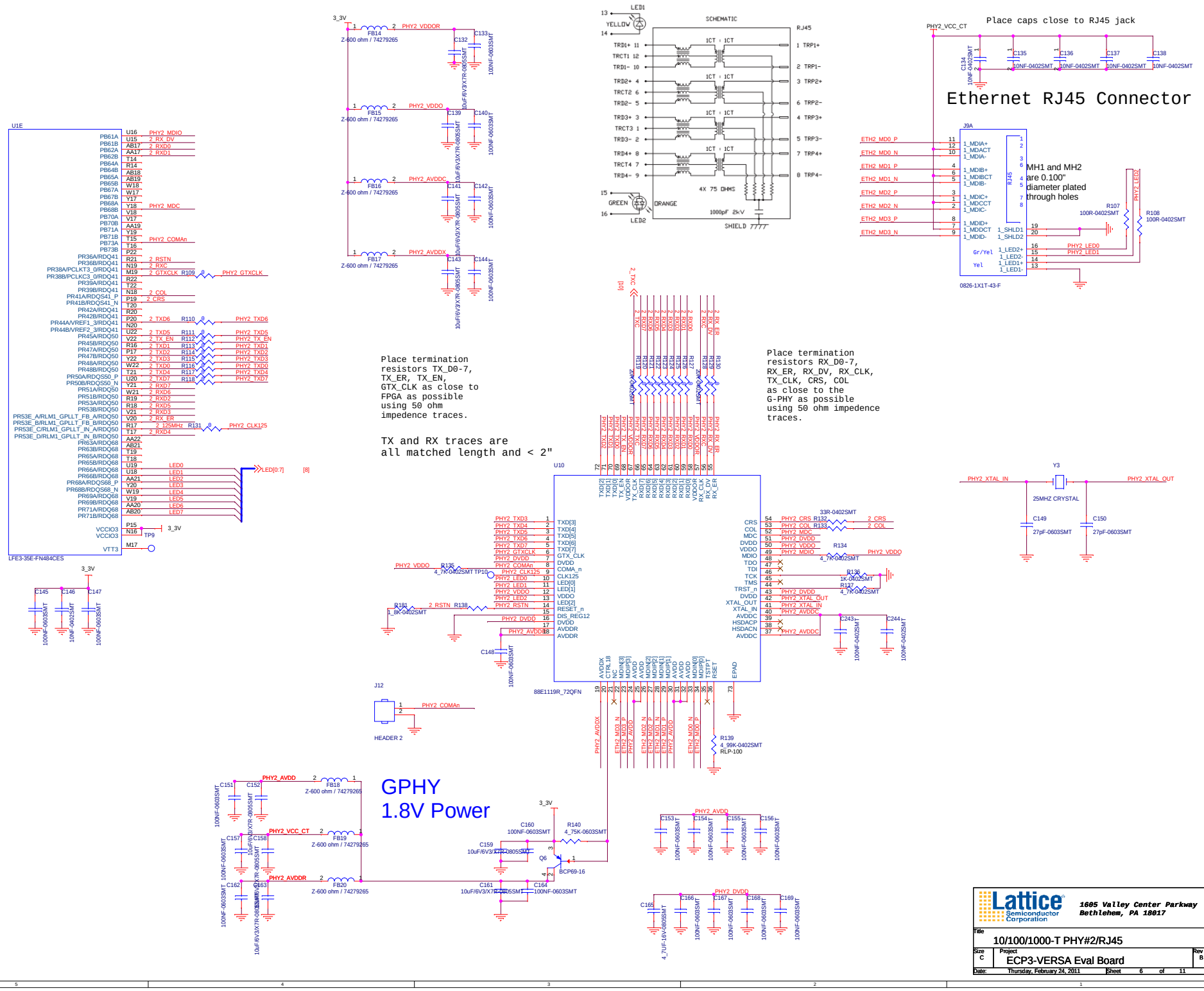

Ethernet RJ45 Connector
Place caps close to RJ45 jack
SCHEMATIC
MH1 and MH2 are 0.100" diameter plated through holes
Place termination resistors TX_D0-7, TX_ER, TX_EN, GTX_CLK as close to FPGA as possible using 50 ohm impedence traces.
TX and RX traces are all matched length < 2"
Place termination resistors RX_D0-7, RX_ER, RX_DV, RX_CLK, TX_CLK, CRS, COL, RSTN as close to the G-PHY as possible using 50 ohm impedence traces.
GPHY
1.8V Power
88E1119R_72QFN
LFE3-35E-FN484CES
0826-1X1T-43-F
Lattice Semiconductor Corporation
1605 Valley Center Parkway
Bethlehem, PA 18017
10/100/1000-T PHY#1/RJ45
ECP3-VERSA Eval Board
Thursday, February 24, 2011
Sheet 5 of 11


Ethernet RJ45 Connector
Place caps close to RJ45 jack
MH1 and MH2 are 0.100" diameter plated through holes
Place termination resistors TX_D0-7, TX_ER, TX_EN, GTX_CLK as close to FPGA as possible using 50 ohm impedence traces.
TX and RX traces are all matched length and < 2"
Place termination resistors RX_D0-7, RX_ER, RX_DV, RX_CLK, TX_CLK, CRS, COL as close to the G-PHY as possible using 50 ohm impedence traces.
GPHY
1.8V Power
LFE3-35E-FN484CES
88E1119R_72QFN
0826-1X1T-43-F
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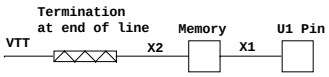
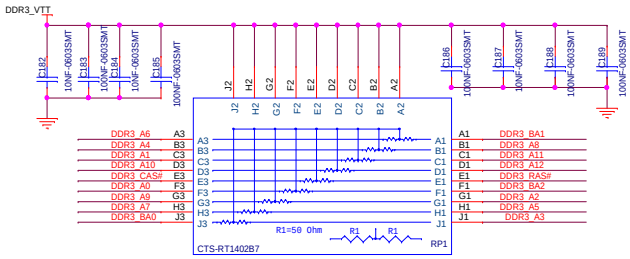
Bethlehem, PA 18017
10/100/1000-T PHY#2/RJ45
ECP3-VERSA Eval Board
Thursday, February 24, 2011

**ALL Memory controller buses, clocks, and control traces must be 50 Ohm Transmission lines**

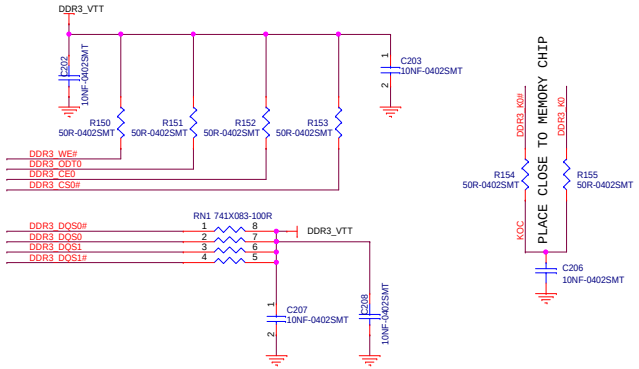
**MEMORY DEVICE TERMINATION for ADDRESS/ CONTROL SIGNALS**



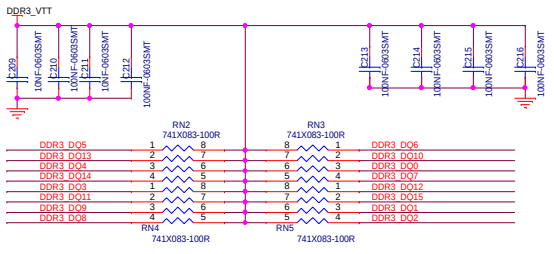

**X1 needs to be matched length for all traces**




**Place Address/Control Termination Resistors as close as possible to Memory Chip U7**

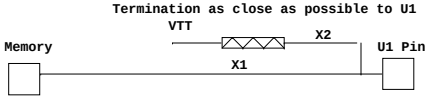



**Place DDR3_DQ/DQS Termination Resistors as close as possible to U1**

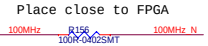


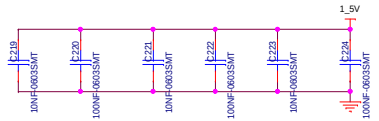

**FPGA DEVICE TERMINATION for DQ/DQS SIGNALS**

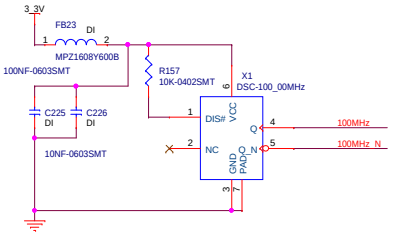
**Termination as close as possible to U1**

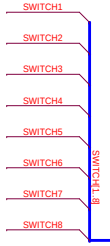



**Place close to FPGA**



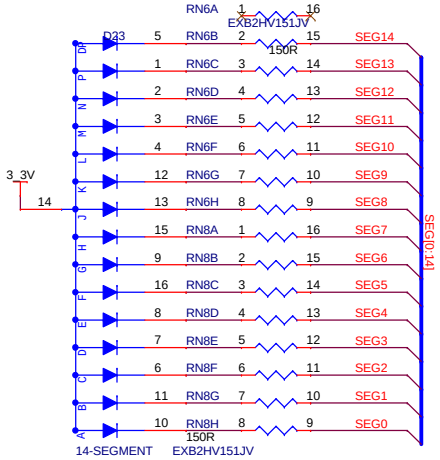


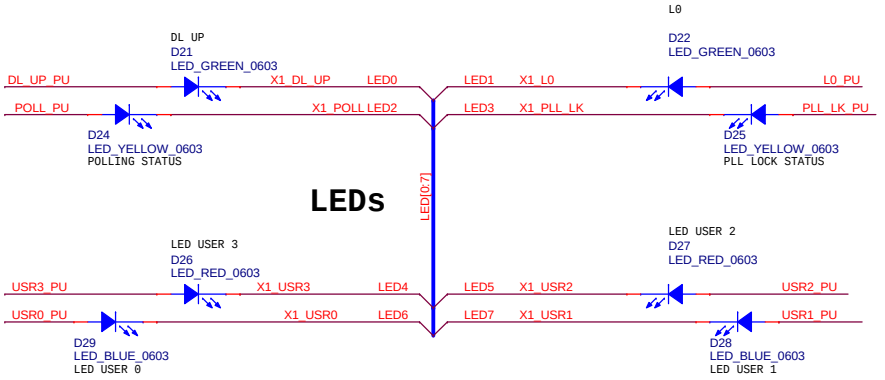

SWITCH[1:8] [8]

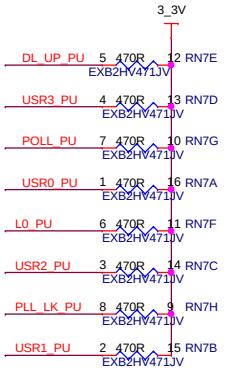
| | | | |
|---|---|---|---|
| Lattice Semiconductor Corporation | | 1605 Valley Center Parkway Bethlehem, PA 18017 | |
| Title: DDR3 Memory | | | |
| Size: C | Project: ECP3 VERSA Eval Board | | Rev: B |
| Date: Wednesday, February 09, 2011 | | Sheet 7 of 11 | |

# 14-SEGMENT DISPLAY



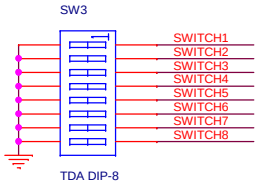

# LEDs

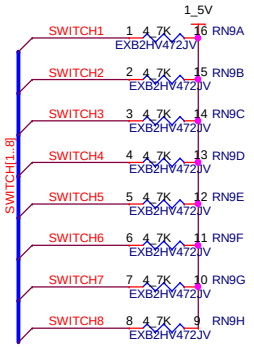




# DIP SWITCH/BANK=1.5V




Lattice Semiconductor Corporation
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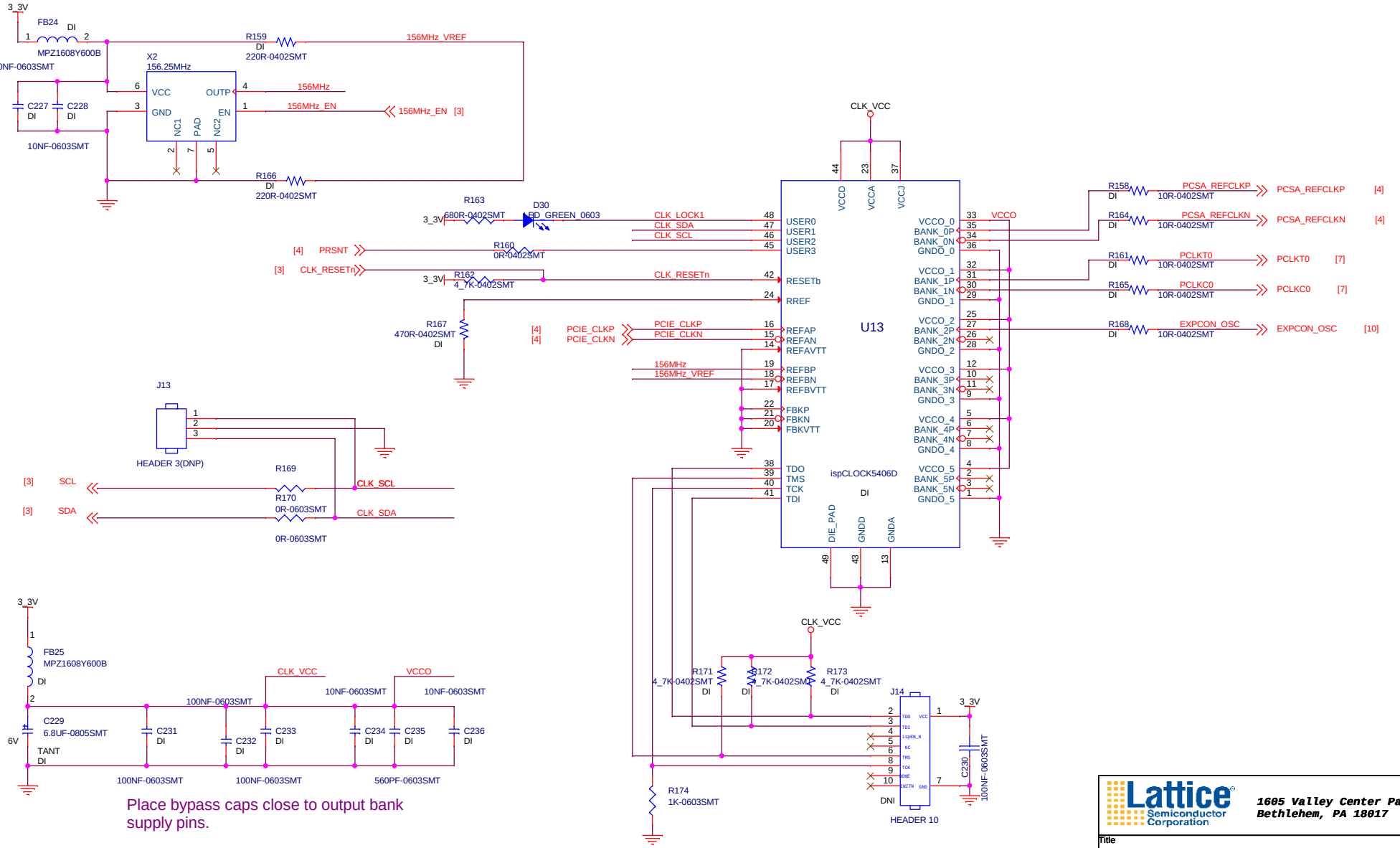
Bethlehem, PA 18017

Title: LEDs & Switches

Size: B | Project: ECP3 VERSA Eval Board | Rev: B

Date: Wednesday, February 09, 2011 | Sheet 8 of 11




Lattice Semiconductor Corporation
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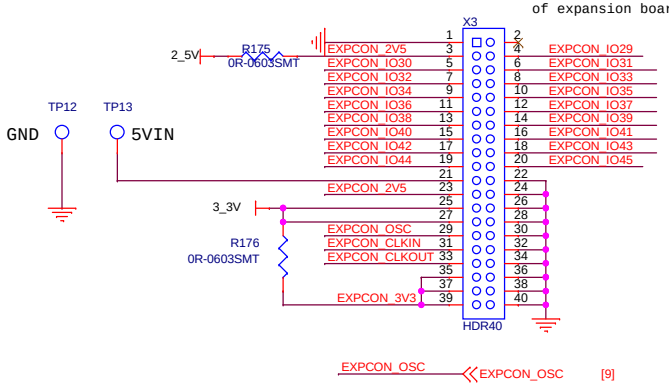
Bethlehem, PA 18017

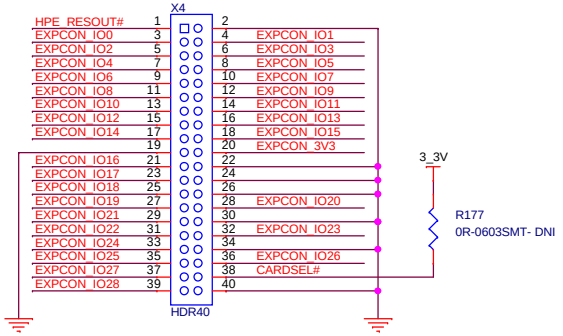
Title: REF CLOCK GEN

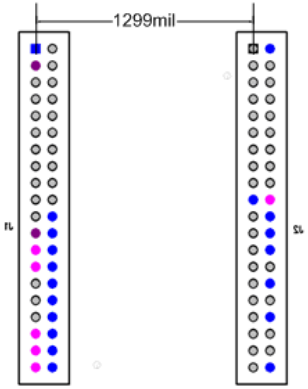
| Size | Project | Rev |
|---|---|---|
| B | ECP3 VERSA Eval Board | B |

Date: Tuesday, February 22, 2011 Sheet 9 of 11

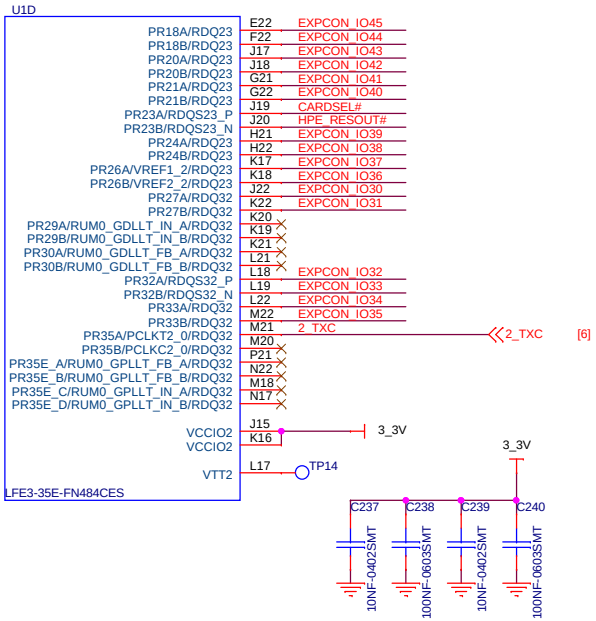
Pin 2 removed for coding
of expansion board

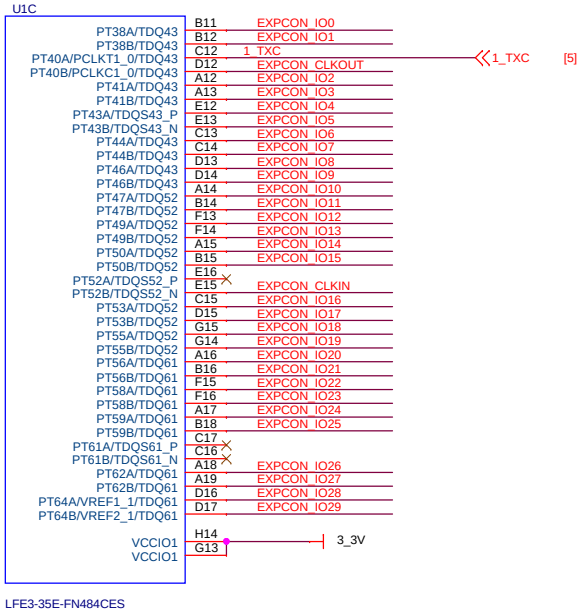



EXPCON_OSC — EXPCON_OSC [9]





Lattice Semiconductor Corporation
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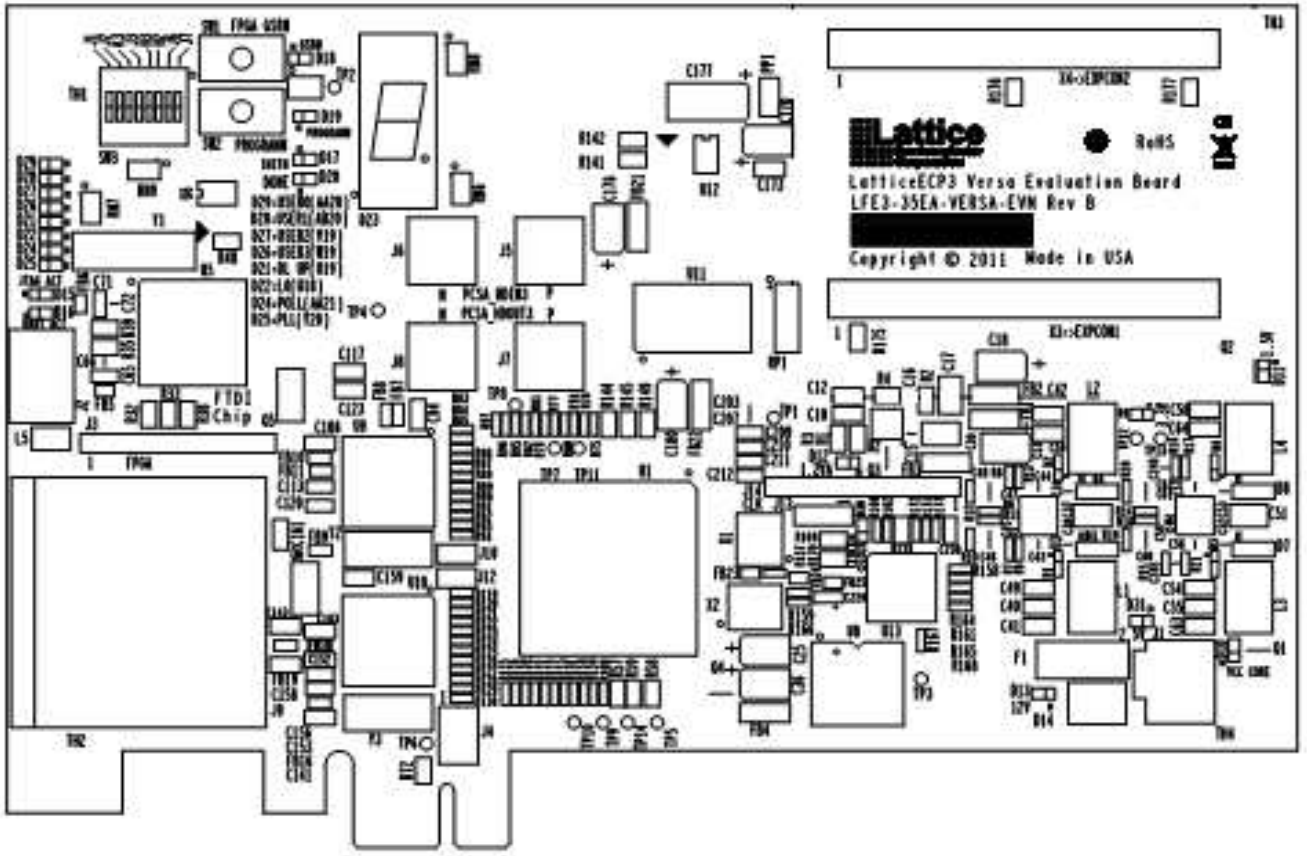
Bethlehem, PA 18017


Title: Expansion Connector

Size: B | Project: ECP3 VERSA Eval Board | Rev: B

Date: Friday, March 18, 2011 | Sheet 10 of 11




4.75" x 6.6in
Dimensions are approximations only.
Refer to the PCIe Card Electromechanical Spec Rev 1.1/2.0

TH1 ThruHole
TH3 ThruHole
TH4 ThruHole
TH2 ThruHole

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Bethlehem, PA 18017

Title: Mechanical

| Size | Project | Rev |
|---|---|---|
| A | ECP3 VERSA Eval Board | B |

Date: Friday, March 18, 2011 Sheet 11 of 11