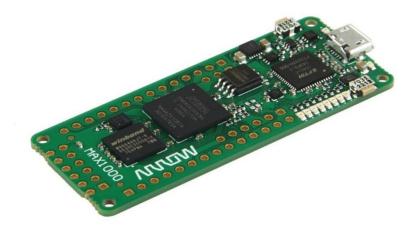
MAX1000

Timing Closure Lab



Software and hardware requirements to complete all exercises Software Requirements: Quartus® Prime Lite or Standard Edition version 18.0 or 18.1 Hardware Requirements: ARROW MAX1000 Board

1. Introduction

This tutorial provides comprehensive information to help you understand how to set and use your FPGA design environment to ensure that your design meets the timing requirements. The TimeQuest timing analyzer is a powerful ASIC-style timing analysis tool that validates the timing performance of all logic in a design using industry standard constraint, analysis, and reporting methodology.

Lab Notes: Many of the names that the lab asks you to choose for files, components, and other objects in this exercise must be spelled exactly as directed. This nomenclature is necessary because the pre-written software application includes variables that use the names of the hardware peripherals. Naming the components differently can cause errors. There are also other similar dependencies within the project that require you to enter the correct names.

2. Getting Started

The first objective is to ensure that you have all the necessary hardware items and software installed so that the lab can be completed successfully. Below is a list of items required to complete this lab:

- MAX1000 Board (10M08SAU169C8G)
- USB Cable
- Lab files: Timing_Closure_lab_template: Template files are required to complete the lab. Includes: top.vhd, fibonacci.vhd, timing_closure_lab_pinout.csv
- Quartus Prime 18.0 Lite was used for this lab. Previous/newer versions should work (If no Quartus Prime is installed, refer to MAX1000 User Guide for instructions)
- Installed Arrow USB Drivers (If not, refer to MAX1000 User Guide for instructions)
- Personal computer or laptop running 64-bit Linux / Windows 7 or later with at least an Intel i3 core (or equivalent), 4GB RAM and 12 GB of free hard disk space
- Basic knowledge of VHDL
- A desire to learn!

3. Project with MAX1000

3.1 Quartus Prime project

3.1.1 Create a new Quartus Prime project

- 3.1.1.1 If not already open, from the Start menu or the Desktop, open the Quartus Prime 18.0 Lite software.
- 3.1.1.2 Create a new project using the New Project Wizard: **File** → **New Project Wizard**.

New Project Wizard	×
Introduction	
The New Project Wizard helps you create a new project and preliminary project settings, including the following:	
 Project name and directory Name of the top-level design entity Project files and libraries Target device family and device EDA tool settings 	
You can change the settings for an existing project and specify additional project-wide settings with the Settings command (Assignments menu). You can use the various pages of the Settings dialog box to add functionality to the project.	
Don't show me this introduction again	
< Back Next > Finish Cancel Help	,

3.1.1.3 Click Next.

- 3.1.1.4 Configure the New Project Wizard directory, name and top-level entity information:
 - Enter a directory in which you will store your Quartus project files for this design, for example, C:/MAX1000/Timing_Closure_lab
 - Specify the name of the project: **timing_closure_lab**
 - Specify the name of the top-level entity: top



New Project Wizard	
)irectory, Name, Top-Level Entity	
/hat is the working directory for this project?	
:/MAX1000/Timing_Closure_lab	
/hat is the name of this project?	
iming_closure_lab	
/hat is the name of the top-level design entity for this project? This name is case sensitive and must exactly match the entity name ir esign file.	n the
op	
< Back Next > Finish Cancel	Help

3.1.1.5 Click Next.

3.1.1.6 On the Project Type page, select **"Empty project"** and click **Next**.

🛇 New Project Wizard	
Project Type	
Select the type of project to create.	
Empty project	
Create new project by specifying project files and libraries, target device family and device, and EDA	ool settings.
O Project template	
Create a project from an existing design template. You can choose from design templates installed v	ith the Quartus Prime
software, or download design templates from the Design Store.	
< Back Next > Finish	Cancel Help

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- 3.1.1.7 On the Add Files page, add source files to the project by clicking on the button and browse into the lab files folder where you will locate the provided design files and add:
 - top.vhd
 - fibonacci.vhd

-	-		lude in the project. Click Add A to the project later.	ll to add all desi	gn files in the project	directory to the project.	
ile name:	ways add des	ingri mes	to the project later.				Add
File Name top.vhd fibonaccl.vł	Type VHDL File		Design Entry/Synthesis Tool	HDL Version Default Default		X	Add All Remove Up Down Properties
pecify the path	names of an	y non-de	fault libraries. User Libraries				

- 3.1.1.8 Click Next.
- 3.1.1.9 Specify Family and Device Settings. Use pull-down menus to select MAX10 family or enter the part number in the Name Filter text box. The part number is **10M08SAU169C8G**.

New Project Wizard								
amily, Device 8	Board Settin	gs						
Device Board								
Select the family and o	device you want to t	arget for c	ompilation.					
You can install additio	onal device support	with the In	stall Devices com	mand on the	Tools n	nenu.		
To determine the vers	ion of the Quartus F	rime softw	vare in which you	r target devic	e is supp	orted, refe	r to the <u>Device Support List</u> webpage	2
Device family				Show in 'A	vailable	devices' list		
Family: MAX 10 (DA	VDF/DC/SA/SC)		•	Package:		UFBGA	•	
Device: All			•	Pin count:	n count: 169		•	
Target device				Core speed grade: 8		•		
O Auto device selec	ted by the Fitter			Name filter: 10M08SAU169C8G		J169C8G		
Specific device se	lected in 'Available	devices' list	t	Show advanced devices				
🔿 Other: n/a								
Available devices:								
Name	Core Voltage	LEs	Total I/Os	GPIOs	Me	no r y Bits	Embedded multiplier 9-bit eler	n
10M08SAU169C8G	3.3V	8064	130	130	38707	2	48	
10M08SAU169C8GE	S 3.3V	8064	130	130	38707	2	48	
<							>	
				< Back	Ne	xt >	Finish Cancel Help	

3.1.1.10 Click Finish. MAX1000 Timing Closure Lab

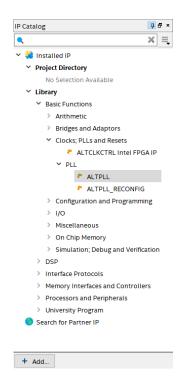
3.2 Design entry

Overview: In this module you will complete the design with missing components, elements.

3.2.1 Add PLL to the Quartus project

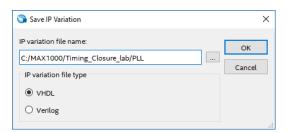
3.2.1.1 From the IP Catalog panel on the left side, expand the menus for the **Basic Functions** → **Clocks; PLLs and Resets** → **PLL** and double click on **ALTPLL**.

If the IP catalog is not visible, then right click on the toolbar and select IP catalog.



3.2.1.2 On the Save IP Variation window, enter the following information.

- IP variation file name: <project_directory>/PLL
- IP variation file type: VHDL

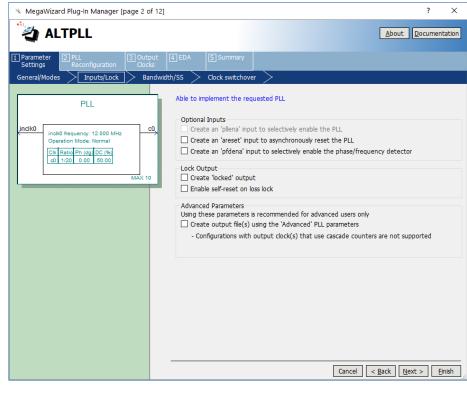


3.2.1.3 Click OK.

3.2.1.4 Under General/Modes tab (page 1 of 12) of PLL MegaWizard change the frequency of clock input to **12 MHz.** This source is provided by the internal oscillator in the MAX10 FPGA.

× MegaWizard Plug-In Manager [page 1 of 12]	? ×
altpll	About Documentation
Parameter 2 PLL 3 Output 4 Settings Reconfiguration Clocks 4	EDA 5 Summary
General/Modes $>$ Inputs/Lock $>$ Bandwidth/S	SS $>$ Clock switchover $>$
	Currently selected device family: MAX 10
PLL	Match project/default
inclik0 areset Cik Ratio Ph (dg) CC (%) d 1/1 0.00 00.00 MAX 10	Able to implement the requested PLL General Which device speed grade will you be using? Use military temperature range devices only What is the frequency of the inck0 input? Set up PLL in LVDS mode Data rate: Not Available Mbps PLL Type Which PLL type will you be using? Fast PLL Operation Mode How will the PLL outputs be generated?
	Use the feedback path inside the PLL

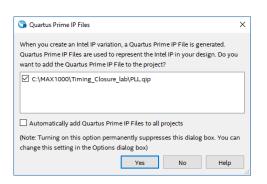
- 3.2.1.5 Click Next.
- 3.2.1.6 Under Input/Lock tab (page 2 of 12) uncheck 'areset' input and locked output option.



- 3.2.1.7 Click Next until you reach the Output Clocks tab (page 6 of 12).
- 3.2.1.8 Under the clk c0 tab (page 6 of 12) select "Enter output clock frequency" and enter **200 MHz**.

ℜ MegaWizard Plug-In Manager [page 6 of 12]		? ×
ALTPLL		<u>About</u> <u>D</u> ocumentation
1 Parameter 2 PLL 3 Output Settings dk c1 dk c2 dk c3	(4 EDA 5 Summary	
PLL icolk0 frequency: 12.000 MHz Operation Mode: Normal Cik Franci Phi (ag IOC (%) col 50/3 0.00 50.00 MAX 10	CO - Core/External Output Clo Able to implement the requested PLL Cuse this clock Clock Tap Settings Enter output clock frequency: Clock multiplication factor Clock division factor Clock phase shift Clock duty cycle (%) Note: The displayed internal settings of the	Requested Settings Actual Settings 200.00000000 MHz • 200.000000 1 • 50 1 • 0.00 • deg • 0.00 • 50.00 50.00 • 50.00
	PLL is recommended for use by advanced users only	Modulus for M counter 50 • • • • Per Clock Feasibility Indicators • c0 c1 c2 c3 c4

- 3.2.1.9 Click **Finish.** This will take you to the Summary tab (page 12 of 12). Click **Finish** again to close ALTPLL MegaWizard Manager.
- 3.2.1.10 In the pop-up Quartus Prime IP Files accept all defaults and click Yes.



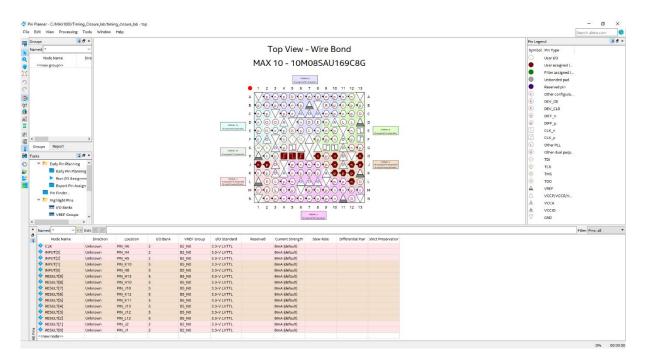
3.2.2 Import pin assignments

3.2.2.1 Select Assignments → Import Assignments...

3.2.2.2 Add source file by clicking on the <u>button</u> button and browse into the lab file folder where you will locate the provided design files and add **timing_closure_lab_pinout.csv**.

S Import Assignments	×
Specify the source and categories of assignments to import.	
File name: iming_Closure_lab/timing_closure_lab_pinout.csv Categories	
Copy existing assignments into top.qsf.bak before importing Advanced	
OK Cancel Help	

- 3.2.2.3 Press OK.
- 3.2.2.4 Open **Pin Planner** by clicking on ^I button on the toolbars, or **Assignments** → **Pin Planner** in order to check the import. In the Pin Planner you should see the following:



3.2.2.5 **Close** the Pin Planner.

3.3 Timing check

3.3.1 Compiling the design

3.3.1.1 Start Compilation by clicking on ► button on the toolbars, or Processing → Start Compilation.

There should be no errors. If there are errors, they should be fixed before re-compilating. The 100% in the lower right corner or a green checkmark next to the Compile Design in the Compilation task window indicates that the compilation was successful.

op りで (10 × 日 × 1				Search altera.com
ect Navigator		tion Report - top		IP Catalog
Entity.instance		Flow Summary		< ×
MAX 10: 10M08SAU169C8G	Flow Summary	< <filter>></filter>		Y 🧯 Installed IP
top to	Flow Settings	Flow Status	Successful - Thu Feb 07 16:29:38 2019	Project Directory
ter top the	Flow Non-Default Global Settings	Quartus Prime Version	18.0.0 Build 614 04/24/2018 5J Lite Edition	No Selection Available
	TT Flow Elapsed Time	Revision Name	top	~ Library
	Flow OS Summary	Top-level Entity Name	top	> Basic Functions
	E Flow Log	Family	MAX 10	> DSP
	Analysis & Synthesis	Device	10M08SAU169C8G	> Interface Protocols
	> Fitter	Timing Models	Final	> Memory Interfaces and Control
	> Assembler	Total logic elements	145 / 8,064 (2 %)	> Processors and Peripherals
	> Power Analyzer	Total registers	14	> University Program
	Flow Messages	Total pins	15/130(12%)	Search for Partner IP
	Flow Suppressed Messages	Total virtual pins	0	
	Timing Analyzer	Total memory bits	0/387,072 (0%)	
>		Embedded Multiplier 9-bit elements	0/48(0%)	
cs Compilation 💌 🚍 🗗 🛪		Total PLLs	1/1(100%)	
		UFM blocks	0/1(0%)	
Task		ADC blocks	0/1(0%)	
Y 🕨 Compile Design				
> Analysis & Synthesis				
> Fitter (Place & Route)				
> Assembler (Generate programmin)				
> Timing Analysis				
EDA Netlist Writer				
Edit Settings				
Program Device (Open Programmer)				+ Add
>	< >			T ADD.
	💏 Find., 🛤	Find Next		
	or max. or			
Type ID Message 332140 No Recovery paths to				
 332140 No Recovery paths to 332140 No Removal paths to 				
332146 Worst-case minimum	pulse width slack is 2.271			
	constrained for setup requirements			
	constrained for hold requirements g Analyzer was successful. 0 errors, 5 wa	roines		
	Compilation was successful. 0 errors, 24			
•		· · · · · · · · · · · · · · · · · · ·		
<				

3.3.2 Timing Analyzer report

3.3.2.1 In the Compilation Report window, expand Timing Analyzer folder. The red highlight shows the problematic areas, which are the unconstrained path and the operating frequency.



3.3.2.2 Expand **Slow 1200mV 85C Model** folder and click on **Setup Summary**. Here you can see the slack of clock-controlled signal.

The Slow 1200mV 85C timing model provides worst-case conditions for the FPGA operating. This condition is ideal for performing a setup check in static timing analysis.

Slo	Slow 1200mV 85C Model Setup Summary					
٩	< <filter>></filter>					
	Clock	Slack	End Point TNS			
1	clock altpll_component auto_generated pll1 clk[0]	-16.540	-142.030			

3.3.2.3 Click on **Fmax Summary** to see the maximum frequency for the current design. Our design should run on 200MHz, so we will fix it in in the following steps.

Slov	w 1200mV 85C I	Model Fmax Summa	у	
•	< <filter>></filter>			
	Fmax	Restricted Fmax	Clock Name	Note
1	46.43 MHz	46.43 MHz	clock altpll_component auto_generated pll1 clk[0]	

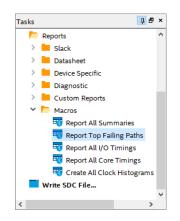
3.3.2.4 Open Timing Analyzer by clicking on ^{See} button on the toolbars, or Tools → Timing Analyzer.

Operating Conditions	₽ @ ×	Getting Started		
timing corners available		aun 9 anna	Welcome to the Quartus Prime Timing Analyzer	
			The Quarture three Timing Sentigers as assumental ASC style timing unalysis tool that valuate the importing methodology. You can see the Timing Andyres to constant, rus, and own-much for all timing paths up owners. The allowing methods are too the sentiger and the sentimeter of the sentimeter of the sentimeter of the sentimeter of the sentimeter of the sentimeter of	
ort Report not available	<u>q</u> 8		Number of the second	
			Lithis common for the second s	
ks 😽 Open Project	1 8 ×			
Netlist Setup	Ĩ			
 Create Timing Netlist Read SDC File 				
Update Timing Netlist				
Reset Design				
Set Operating Conditions				
Reports				
Y 芦 Slack				
Report Setup Summ	ary			
Report Hold Summa				
Report Recovery Sur Report Removal Sur				
Panort Minimum Pu	lea Widti			
number of the second	~			
I - Type "exit" t		list of Quartus Prime Tcl packages.		
O - Type "help <p< p=""></p<>	ackage n	ume>" to view a list of Tcl commands		
0 - Type "help -t	cl" to a	ified Quartus Prime Tcl package. t an overview on Quartus Prime Tcl usages.		
		MAX1000/Timing_Closure_lab/timing_closure_lab.gpf" -revision top		
teb		in a construction of the second		

- 3.3.2.5 Select **Netlist → Create Timing Netlist...** from the menu.
- 3.3.2.6 Make sure, that the **Post-fit** is chosen for Input netlist and check Specify Speed Grade. Set Speed Grade to **8**.

S Create Timing	Netlist X
Input netlist	Delay model
	Slow-corner
Post-fit	Specify Speed Grade
	Speed grade: 8 \checkmark
O Post-map	○ Fast-corner
	Zero IC delays
Tcl command:	create_timing_netlist -model slow -speed 8
	OK Cancel Help

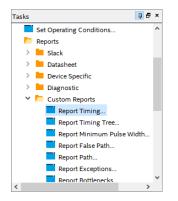
3.3.2.7 In the Task window, browse for **Reports\Macros** and double click on **Report Top Failing Path**.



3.3.2.8 In this report you can see the 200 worst-performing paths.

Slo	w 1200mV	85C Model						
	Slack	From Node	To Node	Launch Clock	Latch Clock	Relationship	Clock Skew	Data Delay
1	-16.540	iINPUT[3]	RESULT[9]~reg0	clock altpll_component auto_generated pll1 clk[0]	clock altpll_component auto_generated pll1 clk[0]	4.999	0.368	21.851
2	-16.521	IINPUT[2]	RESULT[9]~reg0	clock/altpll_component/auto_generated/pll1/clk[0]	clock/altpll_component/auto_generated/pll1/clk[0]	4.999	0.368	21.832
3	-16.493	iINPUT[3]	RESULT[9]~reg0	clock altpll_component auto_generated pll1 clk[0]	clock altpll_component auto_generated pll1 clk[0]	4.999	0.368	21.804
4	-16.474	iINPUT[2]	RESULT[9]~reg0	clock/altpll_component/auto_generated/pll1/clk[0]	clock/altpll_component/auto_generated/pll1/clk[0]	4.999	0.368	21.785
5	-16.447	IINPUT[3]	RESULT[9]~reg0	clock/altpll_component/auto_generated/pll1/clk[0]	clock/altpll_component/auto_generated/pll1/clk[0]	4.999	0.368	21.758
6	-16.428	iINPUT[2]	RESULT[9]~reg0	clock altpll_component auto_generated pll1 clk[0]	clock altpll_component auto_generated pll1 clk[0]	4.999	0.368	21.739
7	-16.400	iINPUT[3]	RESULT[9]~reg0	clock/altpll_component/auto_generated/pll1/clk[0]	clock/altpll_component/auto_generated/pll1/clk[0]	4.999	0.368	21.711
8	-16.396	IINPUT[3]	RESULT[9]~reg0	clock/altpll_component/auto_generated/pll1/clk[0]	clock/altpll_component/auto_generated/pll1/clk[0]	4.999	0.368	21.707
9	-16.382	iINPUT[3]	RESULT[9]~reg0	clock altpll_component auto_generated pll1 clk[0]	clock altpll_component auto_generated pll1 clk[0]	4.999	0.368	21.693
10	-16.381	IINPUT[2]	RESULT[9]~reg0	clock/altpll_component/auto_generated/pll1/clk[0]	clock/altpll_component/auto_generated/pll1/clk[0]	4.999	0.368	21.692
11	-16.380	IINPUT[3]	RESULT[9]~reg0	clock altpll_component auto_generated pll1 clk[0]	clock altpll_component auto_generated pll1 clk[0]	4.999	0.368	21.691
12	-16.377	iINPUT[2]	RESULT[9]~reg0	clock/altpll_component/auto_generated/pll1/clk[0]	clock/altpll_component/auto_generated/pll1/clk[0]	4.999	0.368	21.688
13	-16.364	IINPUT[3]	RESULT[9]~reg0	clock/altpll_component/auto_generated/pll1/clk[0]	clock/altpll_component/auto_generated/pll1/clk[0]	4.999	0.368	21.675
14	-16.363	iINPUT[2]	RESULT[9]~reg0	clock altpll_component auto_generated pll1 clk[0]	clock altpll_component auto_generated pll1 clk[0]	4.999	0.368	21.674
15	-16.361	iINPUT[2]	RESULT[9]~reg0	clock/altpll_component/auto_generated/pll1/clk[0]	clock altpll_component auto_generated pll1 clk[0]	4.999	0.368	21.672
16	-16.345	IINPUT[2]	RESULT[9]~reg0	clock/altpll_component/auto_generated/pll1/clk[0]	clock/altpll_component/auto_generated/pll1/clk[0]	4.999	0.368	21.656
17	-16.336	iINPUT[3]	RESULT[9]~reg0	clock altpll_component auto_generated pll1 clk[0]	clock altpll_component auto_generated pll1 clk[0]	4.999	0.368	21.647
18	-16.333	iINPUT[3]	RESULT[9]~reg0	clock altpll_component auto_generated pll1 clk[0]	clock altpll_component auto_generated pll1 clk[0]	4.999	0.368	21.644
19	-16.333	IINPUT[3]	RESULT[9]~reg0	clock altpll_component auto_generated pll1 clk[0]	clock altpll_component auto_generated pll1 clk[0]	4.999	0.368	21.644
20	-16.317	iINPUT[2]	RESULT[9]~reg0	clock altpll_component auto_generated pll1 clk[0]	clock altpll_component auto_generated pll1 clk[0]	4.999	0.368	21.628
21	-16.314	IINPUT[3]	RESULT[9]~reg0	clock altpll_component auto_generated pll1 clk[0]	clock altpll_component auto_generated pll1 clk[0]	4.999	0.368	21.625
22	-16.314	IINPUT[2]	RESULT[9]~reg0	clock altpll_component auto_generated pll1 clk[0]	clock altpll_component auto_generated pll1 clk[0]	4.999	0.368	21.625
23	-16.314	iINPUT[2]	RESULT[9]~reg0	clock altpll_component auto_generated pll1 clk[0]	clock altpll_component auto_generated pll1 clk[0]	4.999	0.368	21.625
24	-16.303	IINPUT[3]	RESULT[9]~reg0	clock altpll_component auto_generated pll1 clk[0]	clock altpll_component auto_generated pll1 clk[0]	4.999	0.368	21.614
25	-16.301	iINPUT[3]	RESULT[9]~reg0	clock altpll_component auto_generated pll1 clk[0]	clock altpll_component auto_generated pll1 clk[0]	4.999	0.368	21.612
26	-16.295	iINPUT[2]	RESULT[9]~reg0	clock altpll_component auto_generated pll1 clk[0]	clock altpll_component auto_generated pll1 clk[0]	4.999	0.368	21.606
27	-16.289	IINPUT[3]	RESULT[9]~reg0	clock altpll_component auto_generated pll1 clk[0]	clock altpll_component auto_generated pll1 clk[0]	4.999	0.368	21.600
28	-16.284	iINPUT[2]	RESULT[9]~reg0	clock altpll_component auto_generated pll1 clk[0]	clock altpll_component auto_generated pll1 clk[0]	4.999	0.368	21.595
29	-16.282	iINPUT[2]	RESULT[9]~reg0	clock/altpll_component/auto_generated/pll1/clk[0]	clock/altpll_component/auto_generated/pll1/clk[0]	4.999	0.368	21.593
30	-16.270	IINPUT[2]	RESULT[9]~reg0	clock/altpll_component/auto_generated/pll1/clk[0]	clock/altpll_component/auto_generated/pll1/clk[0]	4.999	0.368	21.581
31	-16.269	iINPUT[3]	RESULT[9]~reg0	clock altpll_component auto_generated pll1 clk[0]	clock/altpll_component/auto_generated/pll1/clk[0]	4.999	0.368	21.580

3.3.2.9 In the Tasks window browse for **Reports\Custom Reports** and double click on **Report Timing...** The Report Timing dialog box will appear.



3.3.2.10 Select clock altpll_component auto_generated pll1 clk[0] from the drop-down menu for the "To clock". In the target section type ***iINPUT*** for the "From" and set **50** the Report number of paths in the Paths section.

😂 Report Timing	×
Clocks	
From clock:	~
To clock:	clock altpll_component auto_generated pll1 clk[0] ~
Targets	
From: *iINPUT*	
Through:	
То:	
Analysis type Paths	
Setup Report	t number of paths: 50
O Hold Maxim	num number of paths per endpoint:
O Recovery Maxim	num slack limit: ns
🔿 Removal 🗌 Pa	irs only
Output	
Detail level:	Full path Set Default
	Show routing
Report panel name:	Report Timing
	Enable multi corner reports
File name:	
	File options Open Open
	Overwrite O Append
Console	
Tcl command: IPUT* -set	up -npaths 50 -detail full_path -panel_name {Report Timing} -multi_corner
4	Report Timing Close Help

3.3.2.11 Make sure that the Detail level is Full path and press Report Timing.

3.3.2.12 Here you can see the specific timing check report of the top 50 worst paths. The Data Path tab of detailed report gives the delay break-downs, but there is also useful information in the Path Summary and Statistic tabs, while the Waveform tab is useful to help visualize the Data Path analysis.

_															_	0-1
Slo	w 1200mV 8	35C Model														0-3
Co	mmand Info	Summan	r of Paths													
	Slack	From Node	To Node	Launch G	lock	Latch Clock		Relationship	Clock Skew	Data Delay						^
1	-16.540	iINPUT[3]	RESULT[9]~reg0	clock altpll_component auto	_generated pll1 clk[0]	clock/altpll_component/auto_generated/p	oll1 clk[0]	4.999	0.368	21.851						
2	-16.521	iINPUT[2]	RESULT[9]~reg0	clock altpll_component auto	_generated pll1 clk[0]	clock altpll_component auto_generated p	all1 clk[0]	4.999	0.368	21.832						
3	-16.493	iINPUT[3]	RESULT[9]~reg0	clock altpll_component auto	_generated pll1 clk[0]	clock altpll_component auto_generated p	oll1 clk[0]	4.999	0.368	21.804						
4	-16.474	iINPUT[2]	RESULT[9]~reg0	clock altpll_component auto	_generated pll1 clk[0]	clock altpll_component auto_generated p	oll1 clk[0]	4.999	0.368	21.785						
5	-16.447	iINPUT[3]	RESULT[9]~reg0	clock altpll_component auto	_generated pll1 clk[0]	clock altpll_component auto_generated p	oll1 clk[0]	4.999	0.368	21.758						
6	-16.428	iINPUT[2]	RESULT[9]~reg0	clock altpll_component auto	_generated pll1 clk[0]	clock altpll_component auto_generated p	oll1 clk[0]	4.999	0.368	21.739						
7	-16.400	iINPUT[3]	RESULT[9]~reg0	clock altpll_component auto	_generated pll1 clk[0]	clock altpll_component auto_generated p	oll1 clk[0]	4.999	0.368	21.711						
			0 (VIOLATED)					etup slack is -16								
Pat	h Summary	Statistics	Data Path War	veform			Path Sur	nmary Statisti	cs Data Path	Waveform	1					
	Prop	perty		Value												
1	From Node	ill ill	IPUT[3]													
2	To Node		ESULT[9]~reg0									10.805 ns				
3	Launch Clo			l auto_generated pll1 clk[0]			Launch C	Lock Launch					i í			^
4	Latch Clock			t auto_generated pll1 clk[0]								_		L		
5	Data Arriva		2.339				Setup Re	lationship	4.999 ns							
6	Data Requir		799							Latch			- r			
7	Slack	-1	6.540 (VIOLATED)				Latch Clo	xok		Laton				L		
							Data Arr:	luat								
							Data III.			_						
							Clock De	0.488 n	s							
												21.851 ns				
							Data Dela	ag				La loca in				•••••
							Slack						-16.54 ns			
							Data Req	uired		X						
										0.419 ns						
							Clock De	Lay								
																~

3.3.2.13 Select **Constraints** \rightarrow Write SDC File... from the menu.

3.3.2.14 Type **top.sdc** for SDC file name and press **OK**.

🚫 Write SDC Fi	le X
SDC file name:	top.sdc
Tcl command:	write_sdc -expand "top.sdc"
	OK Cancel Help

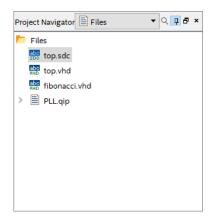
3.3.2.15 In Quartus Prime window, select Project → Add/Remove Files in Project...

3.3.2.16 Click on the ---- button and add **top.sdc** file to the project.

	General	iles						
	Files	Coloritation designs	filme		k Add All to add all design files i		at alter	
	Libraries	project.	files you want to include in t	ie project. Clici	k Add All to add all design files i	n the proje	ct dire	ctory to the
,	IP Settings	project						
	IP Catalog Search Locations	File name:						Add
	Design Templates	<hr/>					×	
	Operating Settings and Conditions	•					~	Add All
	Voltage	File Name	Туре	Library	Design Entry/Synthesis Tool	HDL Versi	ion	Remove
	Temperature	top.sdc	Synopsys Design Constrair	its File	<none></none>		1	
,	Compilation Process Settings	top.vhd	VHDL File		<none></none>	Default		Up
	Incremental Compilation	fibonacci.vho	VHDL File		<none></none>	Default		Down
	EDA Tool Settings	> PLL.gip	IP Variation File (.qip)		<none></none>			Down
	Design Entry/Synthesis	11						Properties
	Simulation							
	Board-Level							
	Compiler Settings							
	VHDL Input							
	Verilog HDL Input							
	Default Parameters							
	Timing Analyzer							
	Assembler							
	Design Assistant							
	Signal Tap Logic Analyzer							
	Logic Analyzer Interface							
	Power Analyzer Settings							
	SSN Analyzer							

3.3.2.17 Click Apply and OK.

3.3.2.18 Choose Files from the drop-down list in Project Navigator, and open top.sdc.

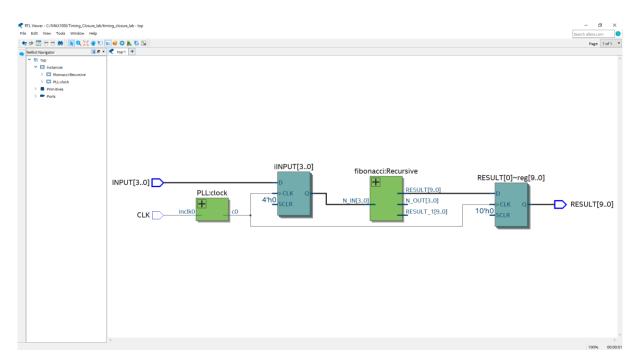


3.3.2.19 You should see that the Timing Analyzer automatically generated clock constrains for the input clock and for the PLL generated clock.

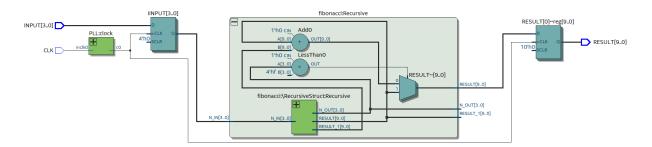
3.4 Design modification

3.4.1 RTL Viewer

3.4.1.1 Open RTL Viewer by selecting **Tools** \rightarrow **Netlist Viewers** \rightarrow **RTL Viewer**.



- 3.4.1.2 The Timing Analyzer indicates that path between iINPUT and RESULT does not meet with the requirement. Click on 🖶 button of Fibonacci:Recursive module to see the internal logic.
 - **Note:** Because this is a recursive component, it is enough to open it once. The internal modules contain the same logic.



3.4.1.3 In the current design you can see that a big combinatorial logic causes the negative path slack. In order to reduce the slack, we will move some registers into the design in the following steps.

3.4.1.4 **Close** RTL Viewer.

MAX1000 Timing Closure Lab

WUW

3.4.2 Code modification

3.4.2.1 Open fibonacci.vhd.

- 3.4.2.2 Comment from line 72 to line 74 by writing "--" at the beginning of the lines or select the lines and click on button.
- 3.4.2.3 Add the following output register in the architecture section after the word 'begin'.

3.4.2.4 Add the following connection to the Recursive : fibonacci association list, around line 66 after port map.

CLK => CLK,

3.4.2.5 Add the following port to the port list of fibonacci entity around line 34 and to the fibonacci component declaration, around line 54.

CLK : in std_logic;

- 3.4.2.6 Save the modification by clicking on \square button or File \rightarrow Save.
- 3.4.2.7 Open top.vhd.
- 3.4.2.8 Add the following connection to the Recursive : fibonacci association list, around line 72 after port map.

CLK => iCLK,

3.4.2.9 Add the following port to the fibonacci component declaration, around line 55.

CLK : in std_logic;

3.4.2.10 Save the modification by clicking on \blacksquare button or File \rightarrow Save.

```
MAX1000
Timing Closure Lab
```

3.4.3 Compiling the design

3.4.3.1 Start Compilation by clicking on ► button on the toolbars, or **Processing** → Start Compilation.

There should be no errors. If there are errors, they should be fixed before re-compilating.

			Closure_lab/timing_closure_lab - top essing Tools Window Help						Sear	- 0 ×
	0×000) (" top		÷ 😋 4 è 🙀 🔹						
Project	Navigator Elles	* Q 📮 🗗 ×	fibonacci.vhd E	3 💠 top.v	hd 🛛	\	Compilation Report - top	×	IP Catalog	- 8 -
File	5		Table of Contents	Flow Summary					۹.	×=
	top.sdc		Flow Summary	< <filter>></filter>					Y 🎎 Installed IP	
	top.vhd		Flow Settings	Flow Status	Successful - Fri Feb 08				Y Project Director	ny .
	fibonacci.vhd		Flow Non-Default Global Settings	Quartus Prime Version	18.0.0 Build 614 04/24j	2018 SJ Lite Ed	tion		No Selection	Available
	PLL-qip		TT Flow Elapsed Time	Revision Name	top				Y Library	
			Flow OS Summary	Top-level Entity Name	top				> Basic Functi	ons
			Flow Log	Family	MAX 10				> DSP	
			Analysis & Synthesis	Device	10M08SAU169C8G				> Interface Pro	
			Fitter	Timing Models Total logic elements	Final 247 / 8.064 (3 %)					rfaces and Controller
			Assembler Power Analyzer	Total logic elements Total registers	247 / 8,064 (3 %) 245				> Processors a	
			 Power Analyzer Flow Messages 	Total registers Total pins	245 15/130(12%)				> University Pr	
			Flow Plessages Flow Suppressed Messages	Total virtual pins	15/150(12-16)				Search for Partn	er IP
asks	Compilation	▼ ≡ 📮 🗗 ×	Timing Analyzer	Total memory bits	0/387.072(0%)					
	1	Task		Embedded Multiplier 9-bit element						
•	🛩 🕨 Compile Design			Total PLLs	1/1(100%)					
•	> 🕨 Analysis & Sj	ynthesis		UFM blocks	0/1(0%)					
1	> Fitter (Place 8	& Route)		ADC blocks	0/1(0%)					
1	> > Assembler (G	Senerate programmin								
,	> Timing Analy	ais								
	> EDA Netlist V									
	Edit Settings									
	Program Device	· · · · · · · · · · · · · · · · · · ·								
	 Program Device 	(Open Programmer)								
-			< >						+ Add	
	• •			JL						
A	t 🖸 🖄 🔺 /	Filter>>	68 Find 66	Find Next						
Т	ype ID Messa	age								
1	332140 No Re									
2			pulse width slack is 2.283 y: Found 4 synchronizer chains.							
Ľ	332102 Desig	n is not fully	constrained for setup requirements							
			constrained for hold requirements g Analyzer was successful. 0 errors, 1 wa							
•			g Analyzer was successful. O errors, 1 wa Compilation was successful. O errors, 12							
	-									
<									 	>
s	ystem Processing (1-	46)								
										100% 00:00

3.4.4 Timing Analyzer report

3.4.4.1 In the Compilation Report window, expand **Timing Analyzer\Slow 1200mV 85C Model** folder and click on **Fmax Summary** to see the maximum frequency for the modified design.

1	< <filter>></filter>			
	Emax	Restricted Emax	Clock Name	Note
	Fillax	Reserved Fillax	crock Marrie	Note
1	273.9 MHz	273.9 MHz	clock altpll_component auto_generated pll1 clk[0]	

Our project should run on 200MHz and a new frequency is 273.9MHz, so the code modification was successful. If you would like, you can check the design in the RTL Viewer and compare it with the previous version.

wow

3.4.4.2 The only problematic area is the unconstrained I/O. Expand **Unconstrained Paths** folder and click on **Summary**. In this report you can see how many I/O is not specified.

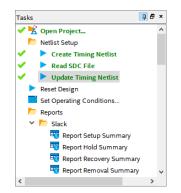
٩	< <filter>></filter>				
	Property	Setup	Hold		
1	Illegal Clocks	0	0		
2	Unconstrained Clocks	0	0		
3	Unconstrained Input Ports	4	4		
4	Unconstrained Input Port Paths	4	4		
5	Unconstrained Output Ports	10	10		
6	Unconstrained Output Port Paths	10	10		

3.4.4.3 To find more information about which I/O is affected and what is wrong, expand **Setup Analysis** folder and double click on **Unconstrained Input Ports**. With the **Unconstrained Output Ports** report you can see the affected output ports.

< <filter>></filter>										
	Input Port	Comment								
1	INPUT[0]	No input delay, min/max delays, false-path exceptions, or max skew assignments found								
2	INPUT[1]	No input delay, min/max delays, false-path exceptions, or max skew assignments found								
3	INPUT[2]	No input delay, min/max delays, false-path exceptions, or max skew assignments found								
4	INPUT[3]	No input delay, min/max delays, false-path exceptions, or max skew assignments found								

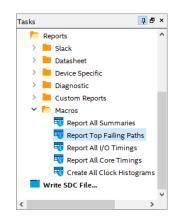
We will constrain these I/Os later.

- 3.4.4.4 Open Timing Analyzer window.
- 3.4.4.5 Double click on **Update Timing Netlist** in the Task window.

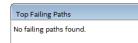


wow

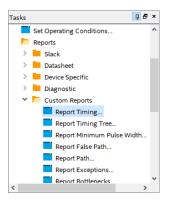
3.4.4.6 In the Task window, browse for **Reports\Macros** and double click on **Report Top Failing Path**.



3.4.4.7 You should see "No failing paths found", which means all the paths meet the timing.



3.4.4.8 In the Tasks window browse for **Reports\Custom Reports** and double click on **Report Timing...** The Report Timing dialog box will appear.



3.4.4.9 Select clock altpll_component auto_generated pll1 clk[0] from the drop-down menu for the "To clock". In the target section type ***iINPUT*** for the "From" and set **50** the Report number of paths in the Paths section.

Seport Timing	×
Clocks	
Г	
From clock:	~
To clock:	clock altpll_component auto_generated pll1 clk[0]
Targets	
From: *iINPUT*	
Through:	
To:	
Analysis type Paths	
Setup Report	t number of paths: 50
O Hold Maxim	num number of paths per endpoint:
O Recovery Maxim	num slack limit: ns
O Removal D Pa	irs only
Output	
Detail level:	Full path Set Default
	Show routing
Report panel name:	Report Timing
	Inable multi corner reports
File name:	
	File options
	Overwrite O Append
Console	
	tup -npaths 50 -detail full_path -panel_name {Report Timing} -multi_corner
P	Report Timing Close Help

3.4.4.10 Make sure that the Detail level is Full path and press Report Timing.

3.4.4.11 In the specific timing check report, you should see that there is not any negative slack, the data arrive in time.

perating Conditions	×	ow 1200mV 85C M	Model														
Slow 1200mV 85C Model	_	ommand Info		f Paths													
Slaw 1200mV OC Madel			rom Node		o Node		Launch Cloc	k	Latch Clock	Relationship	Clock Skew	Data Delay					
	1					clocklaft	pll componentjauto ge		clock[altpll component[auto generated]pll1]		-0.071	0.988					
Fast 1200mV 0C Model	2				COUT[0]		pll_component auto_ge		clock/altpll component/auto generated/pli1		-0.071	0.805					
	3	4.067 IINP			cOUT[2]		pll_component[auto_ge		clock[altpll_component]auto_generated[pl1]	[clk[0] 4.999	-0.071	0.805					
	4	4.068 iINP	PUT[3]	fibonac	OUT[3]	clock alt	pll_component auto_ge	merated pll1 clk[0]	clock/altpll_component/auto_generated/pll1	[clk[0] 4.999	-0.071	0.804					
	Pat	h #1: Setup slack	is 3.884						P	Path #1: Setup slack is 3J	184						
rt a		ath Summary	Statistics	Data P	lath Wa	veform				Path Summary Statis	tics Data Pati	Waveform					
	Dat	ta Arrival Path															
Timing Analyzer Summary		Total	Incr	RF	Type	Fanout	Location		Element ^								
SDC File List	1	0.000	0.000					launch edge time									
Top Failing Paths	2	Y 0.539	0.539					clock path		Launch Clock Launch							
Report Timing	1	0.000	0.000					source latency		_							-
Slow 1200mV 85C Model	2	0.000	0.000			1	PIN_H6	CLK		Setup Relationship			4.3	999 ns			
Slow 1200mV OC Model	3	0.000	0.000	RR		1	IOIBUF_X0_Y7_N22			Latch Clock			-	-		Lato	*
	× 4	0.841	0.841	RR		1	IOIBUF_X0_Y7_N22			Laton Liock							
	^ 5 ^ 6	3.679	2.838	RR	IC COMP	1	PLL_1 PLL_1		onent auto_generated pll1 inclk[0]	Data Arrival		X					
Slack	<pre></pre>	-5.720	-7.599	RR	COMP	1	PLL	clocklatibil comb	>	_	0.539 ns						
Datasheet	Dat	ta Required Path								Clock Delay	******						
Device Specific		Total	Incr	RF	Type	Fanout	Location		Element 1	Data Delau		988 ns					
Diagnostic	1	4,999	4,999					latch edge time									
Custom Reports	2	¥ 5.467	0.468					clock path	S	Slack.		•			3.884 ns		_
	1	4.999	0.000					source latency		Data Required				-			
	2	4.999	0.000			1	PIN_H6	CLK		baca required		_					
Report Timing Tree Report Minimum Pulse Width	4		0.000	RR	IC	1	IOIBUF_X0_Y7_N22	CLK~input[i		Clock Delay						0.	.031 ns
Report Timing Tree Report Minimum Pulse Width Report False Path	3	4.999		RR	CELL	1	IOIBUF_X0_Y7_N22										0.437 ns
Report Timing Tree Report Minimum Pulse Width Report False Path Report Path		5.840	0.841	RK					onent/auto_generated/pli1/inclk[0] 0	Clock Pessinism							01437 110
Report Timing Tree Report Minimum Pulse Width Report False Path			0.841	RR	IC COMP	1	PLL_1 PLL_1		onentjauto_generatedipli1iobservablev								

3.4.5 Constrain I/O

- 3.4.5.1 Open top.sdc in Quartus Prime.
- 3.4.5.2 Search for the Create Clock section which is indicated in the commented area, right click in the text editor and select Insert Constraint → Create Clock...

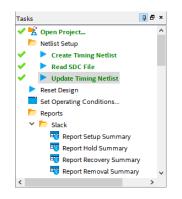
#***********	***	************		
<pre>create_clock -name {CLK} -period 8</pre>	3.3	33 -waveform { 0.000 41.666 }	[get_ports	{CLK}]
#*****	り	Undo		
<pre># Create Generated Clock #************************************</pre>	C	Redo		
create_generated_clock -name {clo	÷	Cut)]} -source [get_pins {clo
	D.	Сору		
#*************************************	n	Paste		
#*************	×	Delete		
		Locate Node	•	
#*************************************				
#**********	•	Increase Indent		
Set_crock_uncertainty -rise_rion	•	Decrease Indent	Shift+Tab	<pre>rated(pll1(clk[0])] -rise</pre>
<pre>set_clock_uncertainty -rise_from set_clock_uncertainty -fall_from</pre>	a,	Find Matching Delimiter	Ctrl+M	rated p]11 c]k[0]}] -rise rated p]11 c]k[0]}] -fall. rated p]11 c]k[0]}] -rise rated p]11 c]k[0]}] -fall.
<pre>set_clock_uncertainty -fall_from</pre>				<pre>erated(p)(1)(c)k[0]}] -fa()</pre>
#*****	U	Insert File	Ctrl+E	
# Set Input Delay	2	Insert Template		
		Insert Constraint	•	Create Clock
#********		Open Selected Entity		Create Generated Clock
# Set Output Delay #************************************		Open Symbol File		Set Clock Latency
"		Open AHDL Include File		Set Clock Uncertainty
#*********		Duplicate View		Set Clock Groups Remove Clock
# Set Clock Groups				

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3.4.5.3 In the Create Clock dialog box, type **in_vir_clock** for the Clock name and set the period to **5** ns.

💠 Create Cl	lock				×
Clock name: Period:	in_vir_clock	ns			
Waveform	edges				
Rising:		ns			
Falling:		ns	0.00	2.50	5.00
Targets:					
	Don't overwrite	existing c	locks on target	nodes	
SDC comma	and: create_clock -nam	e in_vir_c	lock -period 5		
			Insert	Cancel	Help

- 3.4.5.4 Click **Insert** and a new SDC command will be added to your SDC file.
- 3.4.5.5 Repeat the previous steps from 3.4.5.2 and add a new clock which name is **out_vir_clock**. Its period is **5 ns**.
- 3.4.5.6 Save the modification by clicking on \blacksquare button or File \rightarrow Save.
- 3.4.5.7 Open **Timing Analyzer** window and double click on **Update Timing Netlist** in the Task window.



3.4.5.8 Go back to the **top.sdc** file and search for the Set Input Delay section. Right click in the text editor and select **Insert Constraint** → **Set Input Delay...**

3.4.5.9 In the dialog box, select **in_vir_clock** from the drop-down menu for Clock name and set **1 ns** for the Delay value. Type **[get_ports INPUT*]** for the Targets.

🥸 Set Input De	-	
Clock name:	in_vir_clock	
	Use falling clock edge	
Input delay o	ptions	
	m	○ Rise
O Maximu	ım	⊖ Fall
Both		Both
Delay value:	1	ns 🗌 Add delay
Targets:	[get_ports INPUT*]	
SDC command	l: set_input_delay -clock { ir	_vir_clock } 1 [get_ports INPUT*]
		Insert Cancel Help

3.4.5.10 Click Insert.

- 3.4.5.11 Search for the Set Output Delay section, right click in the text editor and select Insert Constraint → Set Output Delay...
- 3.4.5.12 In the dialog box, select **out_vir_clock** from the drop-down menu for Clock name and set **1 ns** for the Delay value. Type **[get_ports RESULT*]** for the Targets.

🚸 Set Output I	Delay	×
	Jelay	~
Clock name:	out_vir_clock	~
	Use falling clock edge	
Output delay	options	
O Minimu	m	○ Rise
🔿 Maximu	ım	○ Fall
Both		Both
Delay value:	1	ns 🗌 Add delay
Targets:	[get_ports RESULT*]	
SDC command	set_output_delay -clock { c	out_vir_clock } 1 [get_ports RESULT*]
		Insert Cancel Help

3.4.5.13 Click Insert.

3.4.5.14 Search for the Set False Path section, right click in the text editor and select Insert Constraint → Set False Path...

3.4.5.15 In the dialog box, click — button for the "From".

💠 Set False Path	l.					Х
From:						
Through:						
To:						
SDC command:	set_false_path					
		Insert	C	ancel	Help	•

3.4.5.16 In the Name Finder dialog box, make sure that the Collection is **get_clocks** and click on **List**.

3.4.5.17 Select **in_vir_clock** and click on button.

Collection	get_clocks	▼ Filter: *				
Options	Ber-clocks	Pitter.				
Case-	insensitive					
Hierar	rchical					
🗹 Comp	patibility mode					
No du	plicates					
Matches						
Matches						
List						
4 match	es found			1 selected name	•	
4 match	es found		>	1 selected name	•	
CLK	es found tpll_component aut	o_generated pll	1	, 	2	
CLK clock alt in_vir_cl	tpll_component aut	o_generated pll		, 	:	
CLK clock alt	tpll_component aut	o_generated pll	1	, 	2	
CLK clock alt in_vir_cl	tpll_component aut	o_generated pll	1 >>	, 	3	
CLK clock alt in_vir_cl out_vir_0	tpll_component aut		1 >>> < <	, 	3	
CLK clock alt in_vir_cl	tpll_component aut	o_generated pll	1 >>> < <	, 	:	

3.4.5.18 Press OK.

3.4.5.19 Click on ____ button for the "To" and like in the previous steps, add the clock|altpll_component|auto_generated|pll1|clk[0].

💠 Set False Pa	ath ×
From:	[get_clocks {in_vir_clock}]
Through:	
To:	[get_clocks {clock altpll_component auto_generated pl1 clk[0]}]
SDC comman	d: ock}] -to [get_clocks {clock altpll_component auto_generated pll1 clk[0]]]
	Insert Cancel Help

3.4.5.20 Click Insert. MAX1000 Timing Closure Lab

3.4.5.21 Repeat the previous steps from 3.4.5.14 and set false path from clock/altpll_component/auto_generated/pll1/clk[0] to out_vir_clock.

Set False F	?ath
From:	[get_clocks {clock altpll_component auto_generated pll1 clk[0]}]
Through:	
To:	[get_clocks {out_vir_clock}]
SDC comman	nd: ll_component auto_generated pll1 clk[0]}] -to [get_clocks {out_vir_clock;
	Insert Cancel Help

3.4.5.22 **Save** the modification by clicking on \square button or **File** \rightarrow **Save**.

3.4.6 Compiling the design

3.4.6.1 Start Compilation by clicking on ► button on the toolbars, or Processing → Start Compilation.

There should be no errors. If there are errors, they should be fixed before re-compilating.

top		- F K & © 7 # 28 •		
ect Navigator 📄 Files 🔹 🤉 🦉			Compliation Report - top	IP Catalog 📮 🖥
Files	Table of Contents	🖉 🗗 Flow Summary		< ×
🐯 top.sdc	Flow Summary	< <filter>></filter>		Y 🙀 Installed IP
top.vhd	Flow Settings	Flow Status	Successful - Fri Feb 08 17:32:06 2019	Project Directory
fibonacci.vhd	Flow Non-Default Global Settings	Quartus Prime Version	18.0.0 Build 614 04/24/2018 SJ Lite Edition	No Selection Available
PLL-gip	Flow Elapsed Time	Revision Name	top	✓ Library
	Flow OS Summary	Top-level Entity Name	top	> Basic Functions
	Flow Log	Family	MAX 10	> DSP
	Analysis & Synthesis	Device	10M08SAU169C8G	> Interface Protocols
	> Fitter	Timing Models	Final	> Memory Interfaces and Controlle
	> Assembler	Total logic elements	247 / 8,064 (3 %)	> Processors and Peripherals
	Power Analyzer	Total registers	245	> University Program
	Flow Messages	Total pins	15/130(12%)	Search for Partner IP
s Compilation • =		Total virtual pins	0	
Task	> Timing Analyzer	Total memory bits	0/387,072(0%)	
		Embedded Multiplier 9-bit element		
Y 🕨 Compile Design		Total PLLs	1/1(100%)	
> 🕨 Analysis & Synthesis		UFM blocks	0/1(0%)	
> Fitter (Place & Route)		ADC blocks	0/1(0%)	
> 🕨 Assembler (Generate prog	ammin			
Timing Analysis				
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332101 Design is full	y constrained for setup requirements			
	y constrained for hold requirements			
	Timing Analyzer was successful. O error Full Compilation was successful. O erro			
•	Furr compriation was successful. 0 erro	no, 12 Marinings		
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With this compilation all timing problem was resolved, our design meets with the timing requirements and there is no unconstrained path in the reports.

3.5 Design Test (optional)

Note: This section is optional, and only uses Quartus environment for the internal testing. If you have an external device, for example logic analyzer, you can use it after the configuration and skip the following steps.

3.5.1 VHDL code modification

3.5.1.1 Modify the io_reg process in top.vhd in order to able to generate input data

3.5.1.2 Save the modification by clicking on \square button or File \rightarrow Save.

3.5.2 JTAG Signal Constraints

3.5.2.1 Many in-system debugging tools use the JTAG interface in Intel FPGAs. When you debug your design with the JTAG interface, the JTAG signals are implemented as part of the design. Because of this, the Timing Analyzer flags these signals as unconstrained when an unconstrained path report is generated. In order to avoid this in reports, add the following lines to the **top.scd**.

3.5.2.2 **Save** the modification by clicking on \square button or **File** \rightarrow **Save**.

3.5.3 SignalTap setup

3.5.3.1 Select from the menu **Tools** → **Signal Tap Logic Analyzer**.

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- 3.5.3.2 Double click in the Setup tab to add nodes.
- 3.5.3.3 In the Node Finder make sure, that **Signal Tap: post-fitting** is selected for the Filter and click on **List**.

Named:	*			```````````````````````````````````````	🖌 List 🔶
Options	;				
Filter:	Signal Tap: post-	-fitting			 Customize
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- i - i - inpu - i - i - i - i - i - i - i - i	INPUT[1]-feeder INPUT[2]-feeder INPUT[3]-feeder IT NPUT[0]-input NPUT[2]-input NPUT[2]-input RESULT[0]-reg0 RESULT[0]-reg0	Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned Unassigned	>>> <		

3.5.3.4 Expand "iINPUT" and select from **iINPUT[0]** to **iINPUT[3]** and click on > button.

3.5.3.5 Select from **RESULT[0]~reg0** to **RESULT[9]~reg0** and lick on button.

Named: *			✓ List
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Filter: Signal Tap: post-fitti	ng		 Customize
Look in: top		✓ … ✓ Include suben	tities 🗹 Hierarchy view
fatching Nodes:		Nodes Found:	
Name	Assignmen ^ 🕈	Name	Assignments
✓ iINPUT		👆 iINPUT[0]	Unassigned
👆 iinput[0]	Unassigned	🖕 iINPUT[1]	Unassigned
linput[1]	Unassigned	👆 iinput[2]	Unassigned
linput[2]	Unassigned	👆 iINPUT[3]	Unassigned
👆 IINPUT[3]	Unassigned	RESULT[0]~reg0	Unassigned
🖕 IINPUT[1]~feeder	Unassigned	RESULT[1]~reg0	Unassigned
🦕 iINPUT[2]~feeder	Unassigned >3	RESULT[2]~reg0	Unassigned
🦕 iINPUT[3]~feeder	Unassigned <	RESULT[3]~reg0	Unassigned
> INPUT	<-		Unassigned
Sinput [0]~input	Unassigned	RESULT[5]~reg0	Unassigned
Sinput [1]~input	Unassigned	RESULT[6]~reg0	Unassigned
SINPUT[2]~input	Unassigned	RESULT[7]~reg0	Unassigned
🖕 INPUT[3]~input	Unassigned	RESULT[8]~reg0	Unassigned
👆 RESULT[0]~reg0	Unassigned 🗸	RESULT[9]~reg0	Unassigned
< [^]	>	4 <	2

3.5.3.6 Click Insert.

3.5.3.7 On the pop-up window, click **Yes** and **close** the Node Finder window.

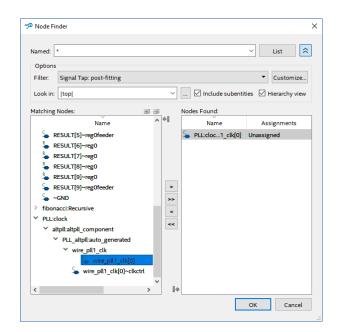


- 3.5.3.8 Select from **iINPUT[0]** to **iINPUT[3]**, right click on them and choose **Group**.
- 3.5.3.9 Select from **RESULT[0]~reg0** to **RESULT[9]~reg0**, right click on them and choose **Group**.
- 3.5.3.10 Select **iINPUT[0..3]** and **RESULT[0..9]** node group, right click on them and select **Bus Display Format** → **Unsigned Decimal**.
- 3.5.3.11 Uncheck Trigger Enable for **RESULT[0..9]**.
- 3.5.3.12 Double click in Trigger Conditions cell of **iINPUT[0..3]** and type **0**.

auto_	auto_signaltap_0 Lock mode: 🥌 Allow all changes		ges		
		Node	Data Enable	Trigger Enable	Trigger Conditions
Туре	Alias	Name	14	4	1 🗹 Basic AND 🔻
-			\checkmark		0
-			\checkmark		

3.5.3.13 In the Signal Configuration window on the right side, click on the button to browse the clock signal.

- 3.5.3.14 In the Node Finder window, make sure, that the **Signal Tap: post-fitting** is selected for the Filter, and click on the **List** button.
- 3.5.3.15 In the Matching Nodes window expand PLL:clock\altpl1:altpl1_component\ PLL_altpl1:auto_generated\wire_pll1_clk and select wire_pll1_clk[0]. Click on button.

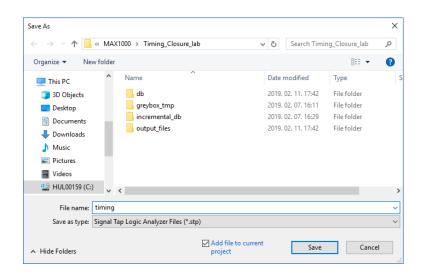


3.5.3.16 Click **OK** to close window.

3.5.3.17 Set Sample depth to 64 under Data and leave the other parameters by default.

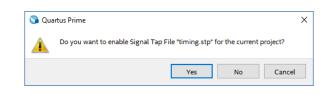
ignal Configu	ration:	
lock: PLL:clo	ck altpll:altpll_component PLL_altpll:auto_generate	
Data		
Sample dept	h: 64 🔻 RAM type: Auto	•
Segment	ed: 2 32 sample segments	7
Nodes Alloca	ated: Auto O Manual: 14	*
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- 3.5.3.18 Save the analyzer setting by clicking on \Box button or **File** \rightarrow **Save** and enter the following information:
 - File name: timing
 - Save as type: Signal Tap Logic Analyzer Files (*.stp)
 - Make sure that "Add file to current project" option is checked.



3.5.3.19 Click Save.

3.5.3.20 In the Quartus Prime pop-up window click Yes to add this file to the current project.



3.5.4 Compiling the Design

3.5.4.1 Before the compilation, make sure, that auto_signaltap_0 instance is enabled in SignalTap.

Instance	Status	Enabled	LEs: 541	Memory: 896	Small: 0/0	Medium: 1/42	Large: 0/0
🔝 auto_signaltap_0	Not running		541 cells	896 bits	0 blocks	1 blocks	0 blocks

3.5.4.2 Start Compilation by clicking on \triangleright button on the toolbars, or **Processing** \rightarrow Start Compilation.

There should be no errors. If there are errors, they should be fixed before re-compilating.

If you check the compilation report, there should be no timing issues. If you expand Timing Analyzer \rightarrow Slow 1200mV 85C Model and open Fmax Summary, you should see, that the minimum frequency is still higher than the requested 200 MHz.

Table of Contents		Slo	w 1200mV 85C	Model Fmax Summa	ry		
> Partition Merge			< <filter>></filter>				
> 📙 Fitter			Fmax	Restricted Fmax	Clock Name	Note	
> 📙 Assembler		1	32.08 MHz	32.08 MHz	altera reserved tck		
> 🧧 Power Analyzer		2	218.25 MHz	204.04 MHz	clock/altpll_component/auto_generated/pll1/clk[0]	limit due to minimum period restriction (tmin)	
I Flow Messages							
Flow Suppressed Messages							
✓ ► Timing Analyzer							
Summary							
Parallel Compilation							
📅 SDC File List							
E Clocks							
Y 芦 Slow 1200mV 85C Model							
📅 Fmax Summary							
📰 Setup Summary							
== Hold Summary							
📰 Recovery Summary							
📰 Removal Summary							
📅 Minimum Pulse Width Summary							
Metastability Summary							
> 📕 Slow 1200mV 0C Model							
> Fast 1200mV 0C Model							
📅 Multicorner Timing Analysis Summary							
> Advanced I/O Timing							
Clock Transfers							
Report TCCS							
Report RSKM							
Unconstrained Paths						riods. FMAX is only computed for paths where the source and	
Messages	~					r paths between a clock and its inversion, FMAX is computed a	
<	>	sca	led along with F	MAX, such that the d	uty cycle (in terms of a percentage) is maintained. Alter	a recommends that you always use clock constraints and other	slack reports for sign-off analysis.

3.5.5 Configuration

3.5.5.1 Connect your MAX1000 board to your PC using an USB cable. Since the Arrow USB Blaster should be already installed, the Window's Device Manager should display the following entries are highlighted in red (port number may differ depending on your PC):



WUW

3.5.5.2 Open the SignalTap window and click on the **Setup...** button in the top right corner.

JTAG Chai	n Configuration: No devi	ces detected	×
Hardware:		7	Setup
Device:	None Detected	~	Scan Chain
>> SOF	Manager: 👗 🕕		

3.5.5.3 Double click **Arrow-USB-Blaster** entry in the Hardware Setup tab. The Currently selected hardware should now show Arrow-USB-Blaster [USB0] (depending on your PC, the USB port number may variant).

Hardware Settings JTAG S	Settings		
elect a programming hardwa hardware setup applies only t			
Currently selected hardware: Available hardware items	Arrow-USB-BI	aster [USB0]	•
Hardware Arrow-USB-Blaster	Server Local	Port USB0	Add Hardware Remove Hardware

3.5.5.4 Click Close.

3.5.5.5 The hardware configuration window should be updated as follows.

JTAG Chain Configuration: JTAG ready ×							
Hardware:	Arrow-USB-Blaster [USB0]	Setup					
Device:	@1: 10M08SA(. ES)/10M08SC (🔻	Scan Chain					
>> SOF Manager:							

- 3.5.5.6 Click on button to choose the programming file.
- 3.5.5.7 Navigate to <project_directory>/output_files/ and select the top.sof file.
- 3.5.5.8 Click **Open**.

3.5.5.9 Click on key button to program the board. When the configuration is complete, the message box of the Instance Manages should write "Ready to acquire".

Instance Manager. 📉 😥 🔳 🔯 Ready to acquire							
Instance	Status	Enabled	LEs: 541	Memory: 896	Small: 0/0	Medium: 1/42	Large: 0/0
🕄 auto_signaltap_0	Not running	\checkmark	541 cells	896 bits	0 blocks	1 blocks	0 blocks

3.5.6 Analyze the design

3.5.6.1 Click on to run single acquisition analysis. On the waveform you can see that the logic generates the correct value of Fibonacci numbers. Because of the registers between the components, there is a latency on the line and its value is 17 clock period.

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CONGRATULATIONS! YOU HAVE SUCCESSFULLY COMPLETED THE TIMING CLOSURE LAB!

5 Revision History

Version	Change Log	Date of Change
V1.0	Initial Version	12/02/2019

6 Legal Disclaimer

ARROW ELECTRONICS

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