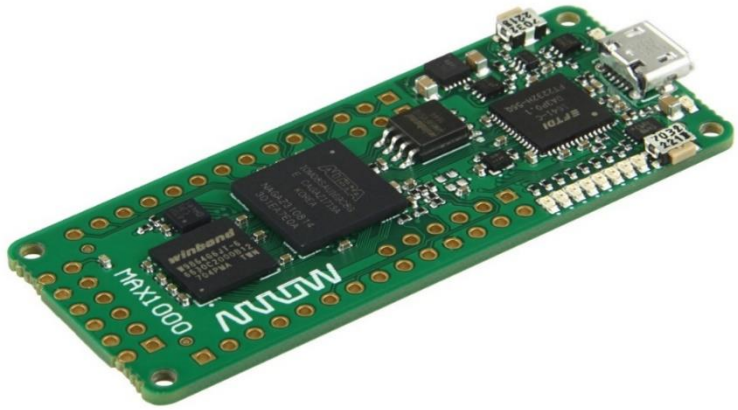
MAX1000

In-System Sources & Probes Lab



Software and hardware requirements to complete all exercises

Software Requirements: Quartus® Prime Lite or Standard Edition version 18.0 or 18.1

Hardware Requirements: ARROW MAX1000 Board

Revision 1.0

1. Introduction

The In-System Sources & Probes Editor allows you to easily control any internal signal and provides you with a completely dynamic debugging environment. Traditional debugging techniques often involve using an external pattern generator to exercise the logic and a logic analyzer to study the output waveform during runtime. You can make the debugging cycle more efficient when you can drive any internal signal manually within your design. This feature can be especially helpful for prototyping your design, such as creating a virtual interface, emulating external data and monitoring, changing run time constant on the fly.

Lab Notes: Many of the names that the lab asks you to choose for files, components, and other objects in this exercise must be spelled exactly as directed. This nomenclature is necessary because the pre-written software application includes variables that use the names of the hardware peripherals. Naming the components differently can cause errors.

2. Getting Started

The first objective is to ensure that you have all the necessary hardware items and software installed so that the lab can be completed successfully. Below is a list of items required to complete this lab:

- MAX1000 Board **(**10M08SAU169C8G)
- USB Cable
- Lab files: InSystem_Debug_lab_template: Template files are required to complete the lab. Includes: insystem_debug_lab.vhd, insystem_debug_lab.sdc, insystem_debug_lab_pinout.csv
- Quartus Prime 18.0 Lite was used for this lab. Previous/newer versions should work (If no Quartus Prime is installed, refer to MAX1000 User Guide for instructions)
- Installed Arrow USB Drivers (If not, refer to MAX1000 User Guide for instructions)
- Personal computer or laptop running 64-bit Linux / Windows 7 or later with at least an Intel i3 core (or equivalent), 4GB RAM and 12 GB of free hard disk space
- A desire to learn!

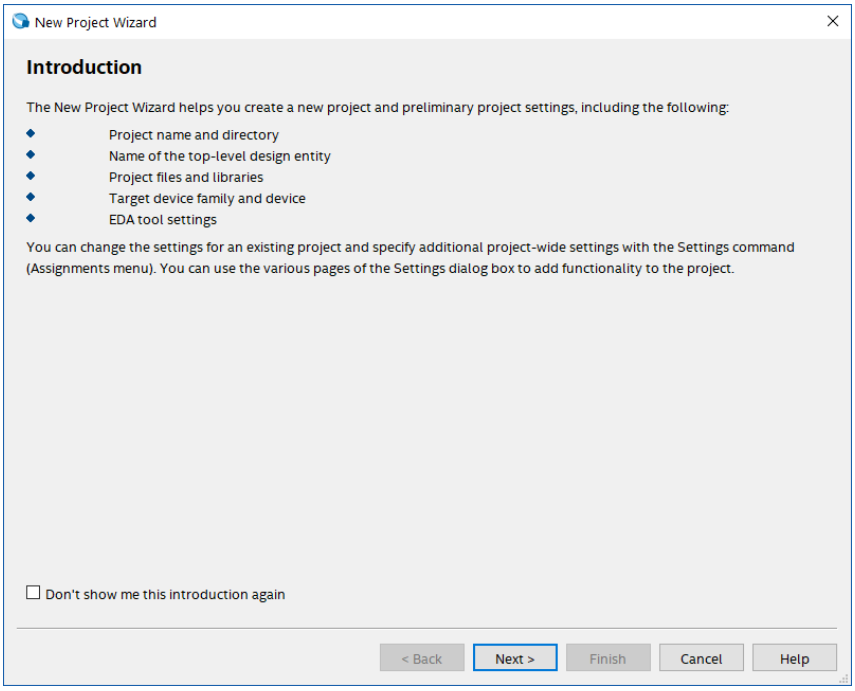
3. Project with MAX1000

3.1 New Quartus Prime project

3.1.1 New project creation

3.1.1.1 If not already open, from the Start menu or the Desktop, open the Quartus Prime 18.0 Lite software.

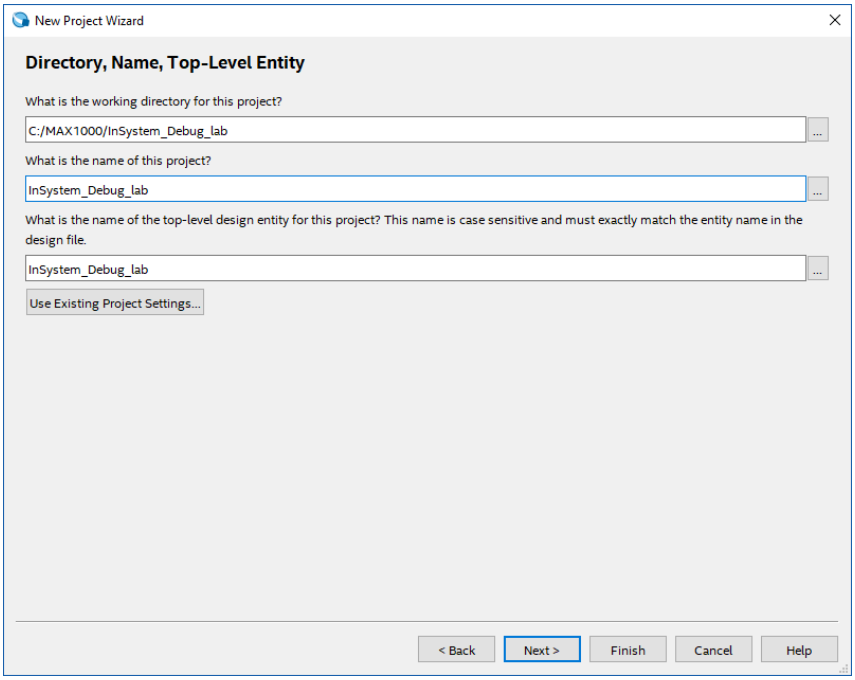
3.1.1.2 Create a new project using the New Project Wizard: **File → New Project Wizard**.



3.1.1.3 Click **Next**.

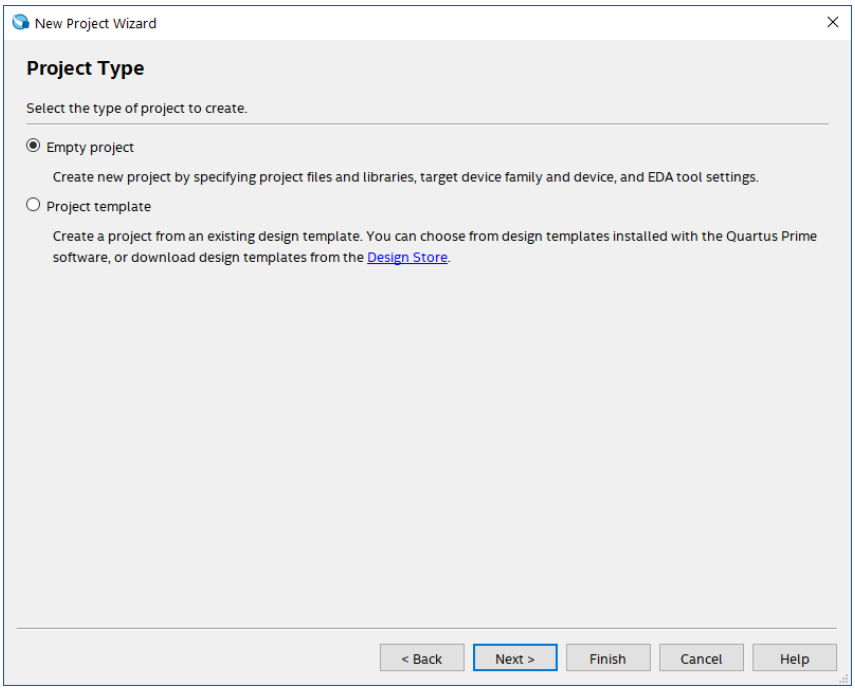
3.1.1.4 Configure the New Project Wizard directory, name and top-level entity information:

- Enter a directory in which you will store your Quartus project files for this design, for example, **C:/MAX1000/InSystem_Debug_lab**
- Specify the name of the project: **InSystem_Debug_lab**
- Specify the name of the top-level entity: **InSystem_Debug_lab**



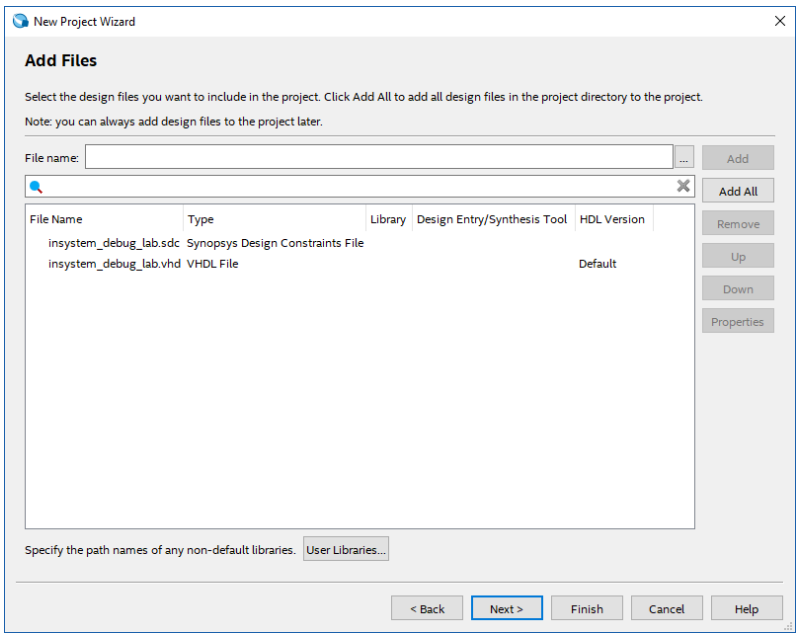
3.1.1.5 Click **Next**.

3.1.1.6 On the Project Type page, select **"Empty project"** and click **Next**.



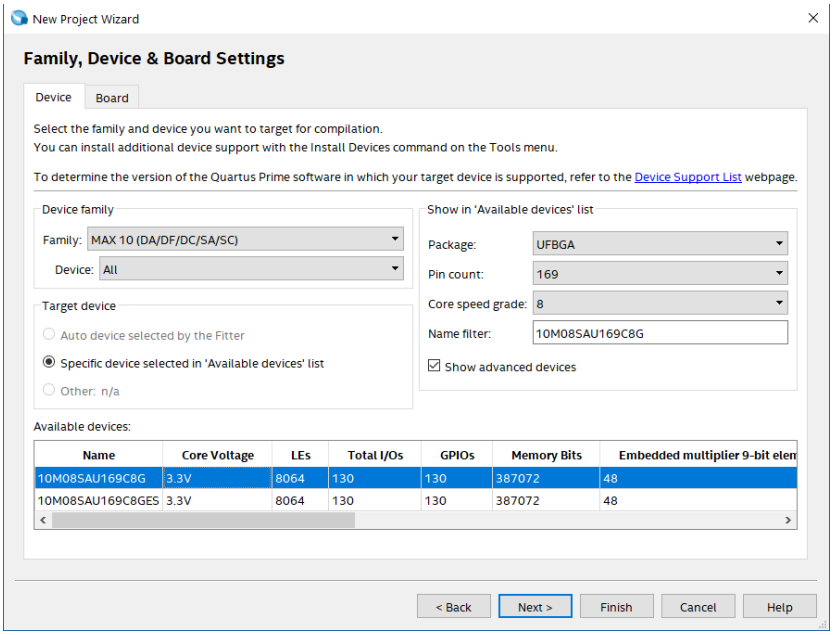
4.1.1.1 On the Add Files page, add source files to the project by clicking on the ... button and browse into the lab files folder where you will locate the provided design files and add:

- **insystem_debug_lab.vhd**
- **insystem_debug_lab.sdc**



3.1.1.7 Click **Next**.

3.1.1.8 Specify Family and Device Settings. Use pull-down menus to select MAX10 family or enter the part number in the Name Filter text box. The part number is **10M08SAU169C8G**.



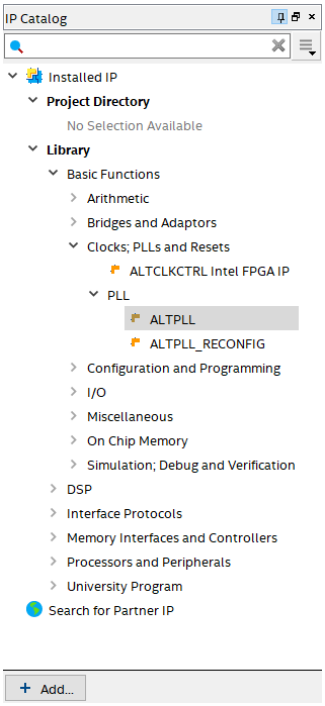
3.1.1.9 Click **Finish**.

3.2 Design entry

3.2.1 Add PLL to the Quartus Project

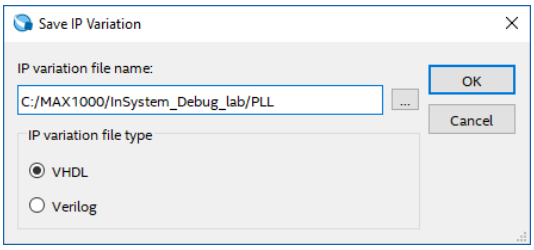
3.2.1.1 From the IP Catalog panel on the left side, expand the menus for the **Basic Functions → Clocks; PLLs and Resets → PLL** and double click on **ALTPLL**.

If the IP catalog is not visible, then right click on the toolbar and select IP catalog.



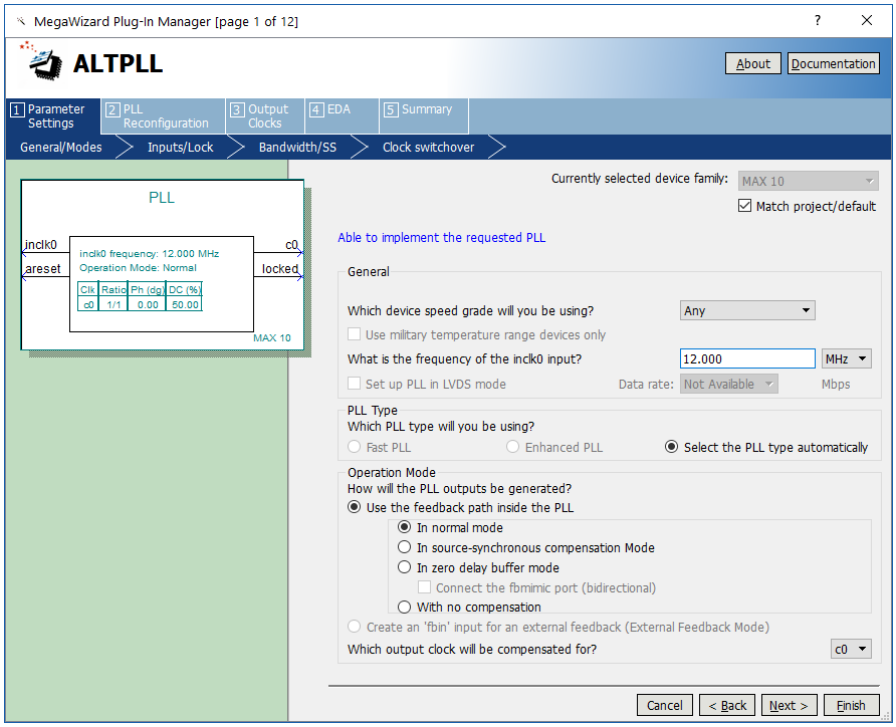
3.2.1.2 On the Save IP Variation window, enter the following information.

- IP variation file name: **<project_directory>/PLL**
- IP variation file type: **VHDL**



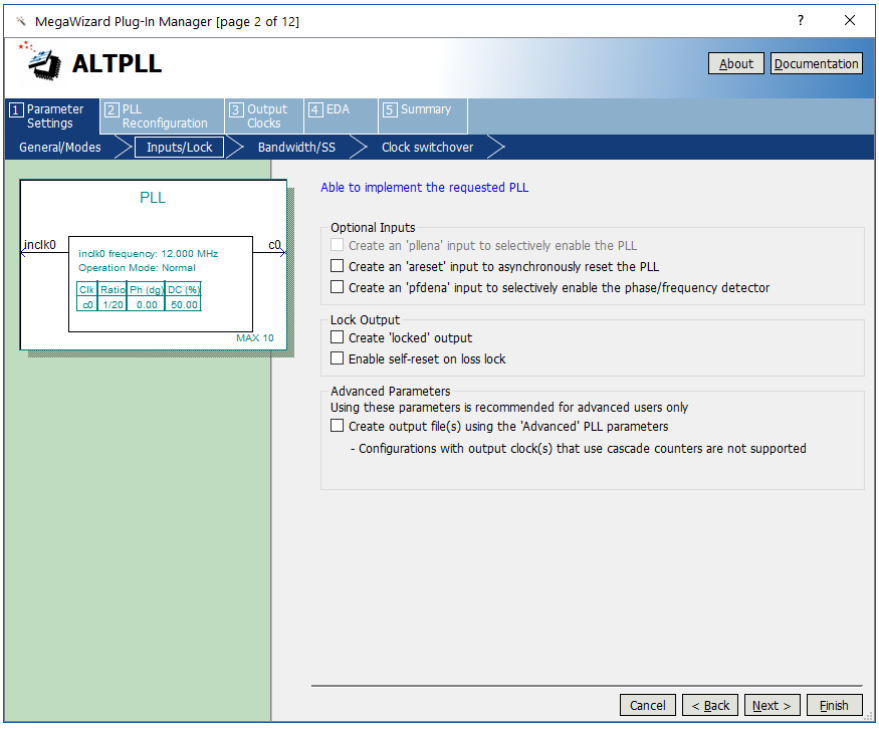
3.2.1.3 Click **OK**.

3.2.1.4 Under General/Modes tab (page 1 of 12) of PLL MegaWizard change the frequency of clock input to **12 MHz.** This source is provided by the internal oscillator in the MAX10 FPGA.



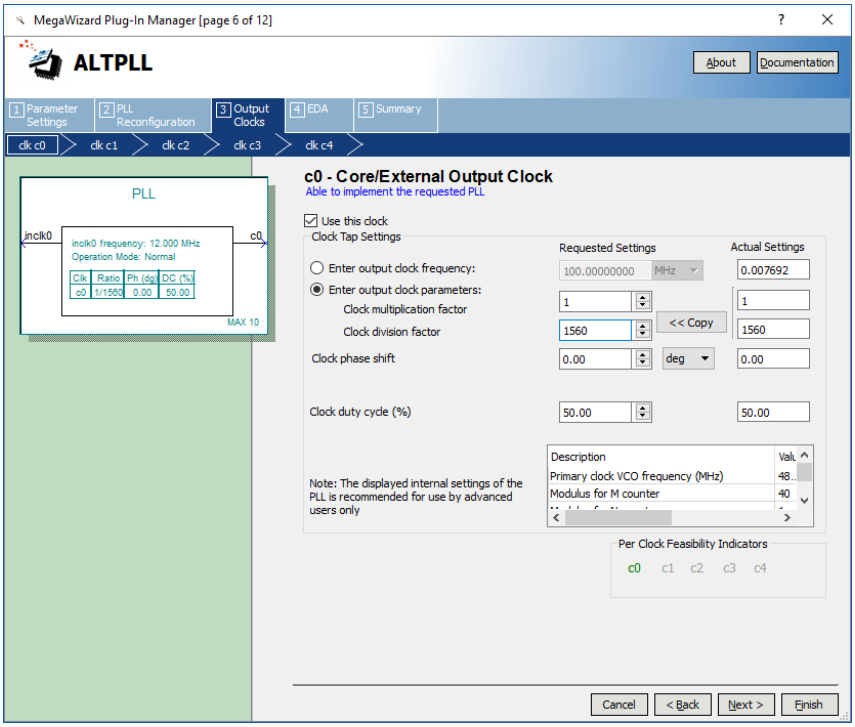
3.2.1.5 Click **Next**.

3.2.1.6 Under Input/Lock tab (page 2 of 12) uncheck ‘areset’ input and locked output option.



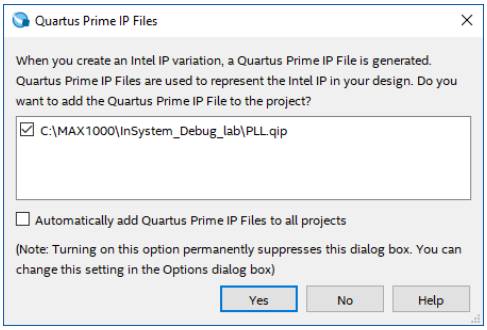
3.2.1.7 Click **Next** until you reach the **Output Clocks** tab (page 6 of 12).

3.2.1.8 Under the clk c0 tab (page 6 of 12) select “Enter output clock parameters” and set Clock division factor to **1560**. Leave the rest as default.



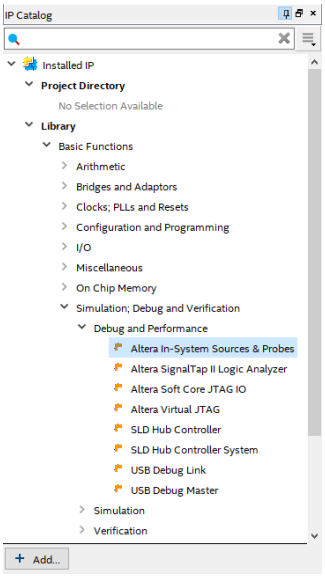
3.2.1.9 Click **Finish.** This will take you to the **Summary** tab (page 12 of 12). Click **Finish** again to close ALTPLL MegaWizard Manager.

3.2.1.10 In the pop-up Quartus Prime IP Files accept all defaults and click **Yes**.

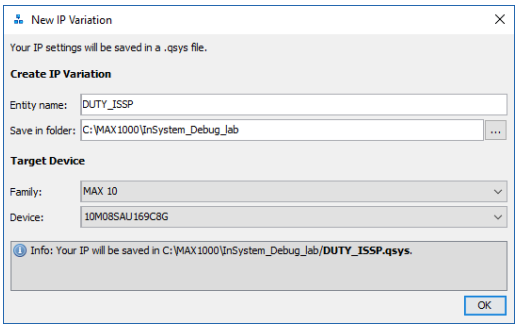


3.2.2 Add 1. In-System Sources & Probes to the Quartus Project

3.2.2.1 From the IP Catalog panel, expand the menus for the **Basic Functions → Simulation; Debug and Verification → Debug and Performance** and add **Altera In-System Sources & Probes**.

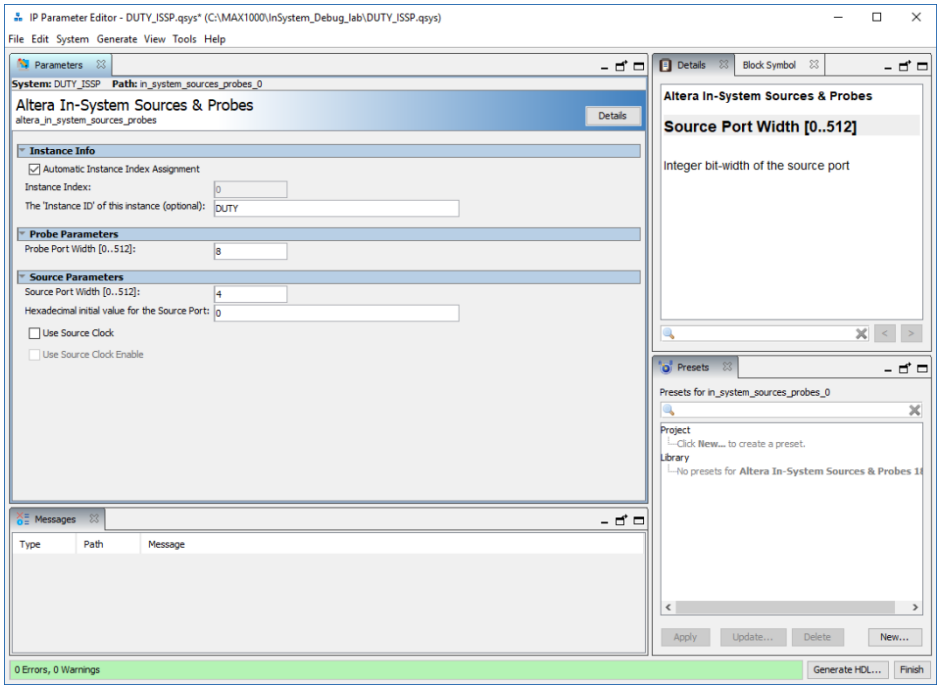


3.2.2.2 In the New IP Variation window enter **DUTY_ISSP** for the Entity name and leave the rest as default.



3.2.2.3 Press **OK**.

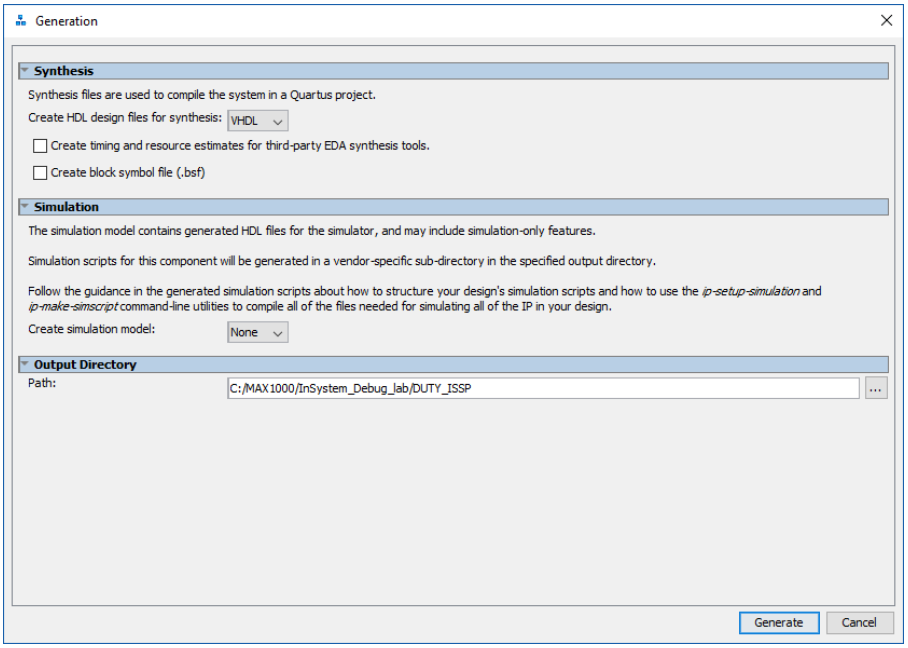
3.2.2.4 Enter **DUTY** for the Instance ID. Set **8** for the Probe Port Width and **4** for the Source Port Width.



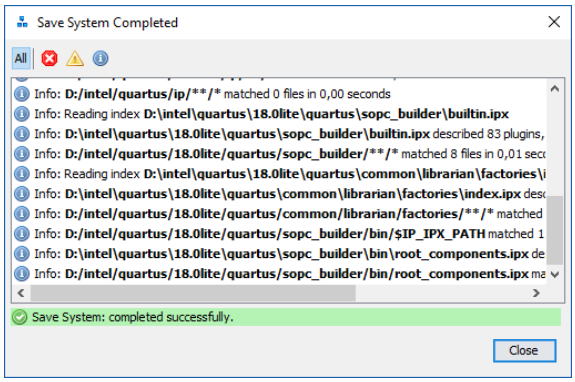
3.2.2.5 Click **Generate HDL…** button on the bottom right of Parameter Editor window.

3.2.2.6 On the Generation window, enter the following information.

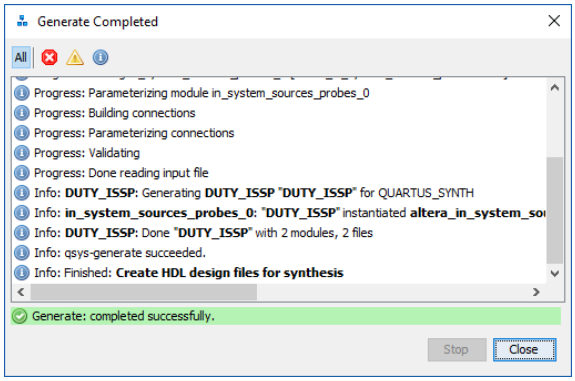
- Create HDL design files for synthesis: **VHDL**
- Uncheck Create timing and resource estimates for third-party EDA synthesis tools.
- Uncheck Create block symbol file (.bsf)
- Create simulation model: **None**



3.2.2.7 Click **Generate** and when the Save System is completed, click **Close**.

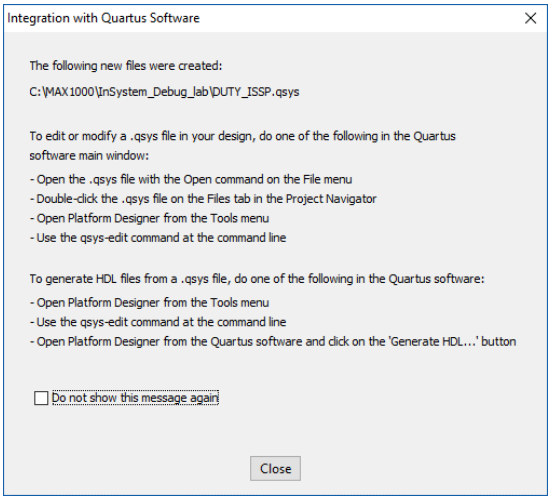


3.2.2.8 When the generate process completed, click **Close**.

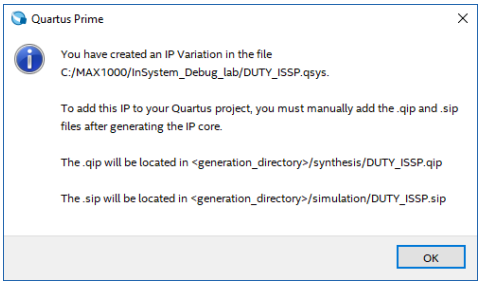


3.2.2.9 Click **Finish** button to close Parameter Editor window.

3.2.2.10 Click **Close** on pop-up window.

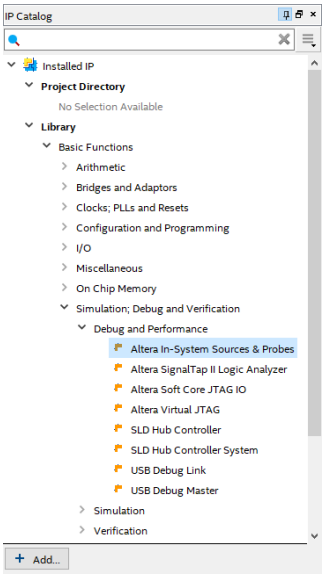


3.2.2.11 It generates IP pointer files for both synthesis (.qip) and simulation (.sip) that will point Quartus to all the necessary design files needed to synthesize or simulate the Platform Designer system. Press **OK** to close as the .qip file will be added to the project later. The In-System Sources and Probes Editor does not support simulation, so no need to add the .sip file.

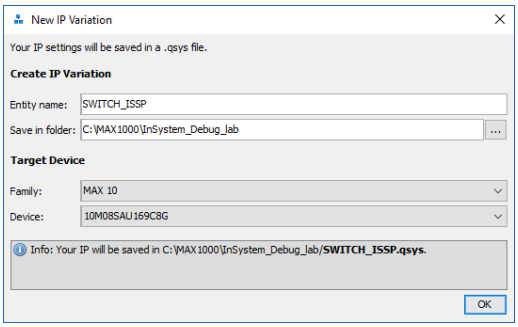


3.2.3 Add 2. In-System Sources & Probes to the Quartus Project

3.2.3.1 From the IP Catalog panel, expand the menus for the **Basic Functions → Simulation; Debug and Verification → Debug and Performance** and add **Altera In-System Sources & Probes**.

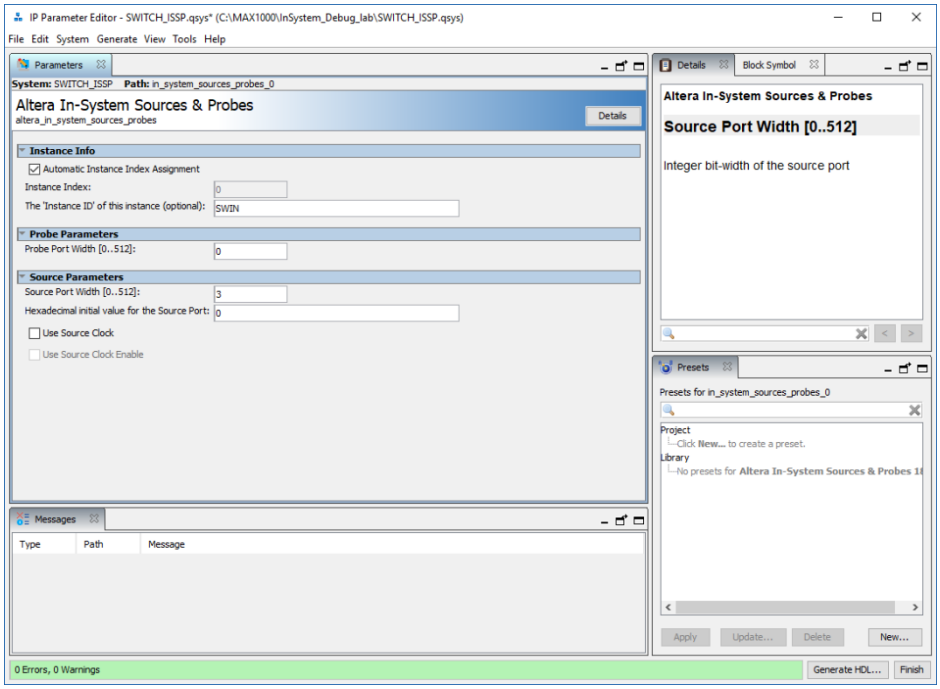


3.2.3.2 In the New IP Variation window enter **SWITCH_ISSP** for the Entity name and leave the rest as default.



3.2.3.3 Press **OK**.

3.2.3.4 Enter **SWIN** for the Instance ID. Set **0** for the Probe Port Width and **3** for the Source Port Width.



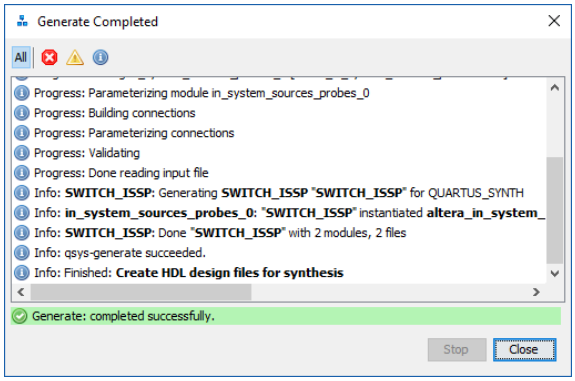
3.2.3.5 Click **Generate HDL…** button on the bottom right of Parameter Editor window.

3.2.3.6 On the Generation window, enter the following information and click **Generate**.

- Create HDL design files for synthesis: **VHDL**
- Uncheck Create timing and resource estimates for third-party EDA synthesis tools.
- Uncheck Create block symbol file (.bsf)
- Create simulation model: **None**

3.2.3.7 Click **Close** when the Save System completed.

3.2.3.8 When the generate process completed, click **Close**.



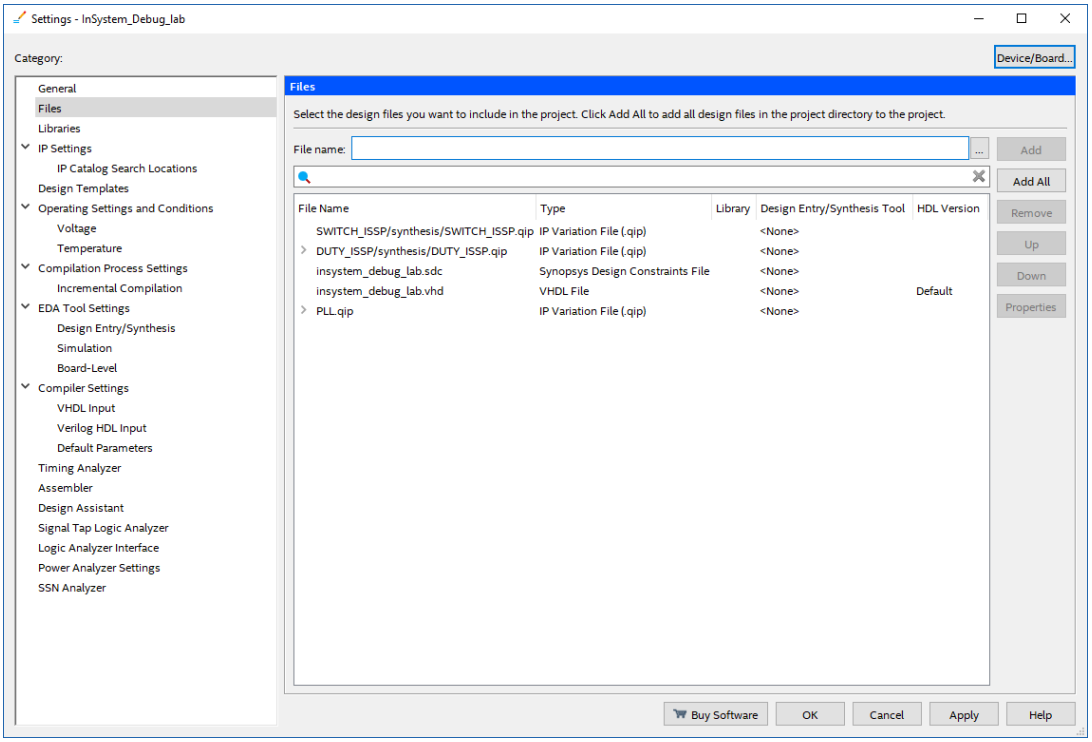
3.2.3.9 Click **Finish** button to close Parameter Editor window.

3.2.3.10 **Close** both pop-up windows.

3.2.3.11 Choose **Project → Add/Remove Files in Project...** from the Quartus Prime menu.

3.2.3.12 Click on the ... button and browse through the synthesis directories: **<project_directory>/DUTY_ISSP/synthesis/** and open **DUTY_ISSP.qip**.

3.2.3.13 Add **SWITCH_ISSP.qip** to the project from **<project_directory>/SWITCH_ISSP/synthesis**



3.2.3.14 Click **Apply** and **OK**.

3.2.4 Design modification

Notes: Up to this point, the original design is done. If you want, you can continue with 3.3 point with pin assignment, compilation and programming the board for the testing purpose in order to see the original function of the project, and then come back to continue with this 3.2.4 point.

3.2.4.1 Open **insystem_debug_lab.vhd**.

3.2.4.2 Uncomment line 44-46, line 113-115 and line 123 by deleting "--" characters at the beginning of the lines or select the desired lines and click on button on the toolbar of text editor.

3.2.4.3 Comment line 98 and line 103 by writing "--" at the beginning of the lines or select the lines and click on button.

3.2.4.4 Add the following component declarations in the architecture section. There should be a commented area indicating where exactly around line 59.

```
component DUTY_ISSP
port( probe       : in std_logic_vector(7 downto 0);
      source      : out std_logic_vector(3 downto 0));
end component;


component SWITCH_ISSP
port( source      : out std_logic_vector(2 downto 0));
end component;
```

3.2.4.5 Add the following component instantiations in the architecture section after the word 'begin'. There should be a commented area where exactly around line 78.

```
pwm_debug : DUTY_ISSP
port map(   probe => probe,
            source => source);


sw : SWITCH_ISSP
port map(source => iSW);
```

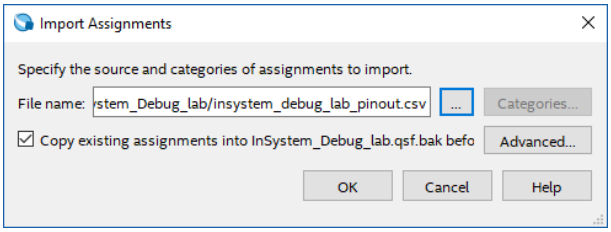
3.2.4.6 Save the modification by clicking on button or **File → Save**.

3.3 Compile design

3.3.1 Import pin assignments

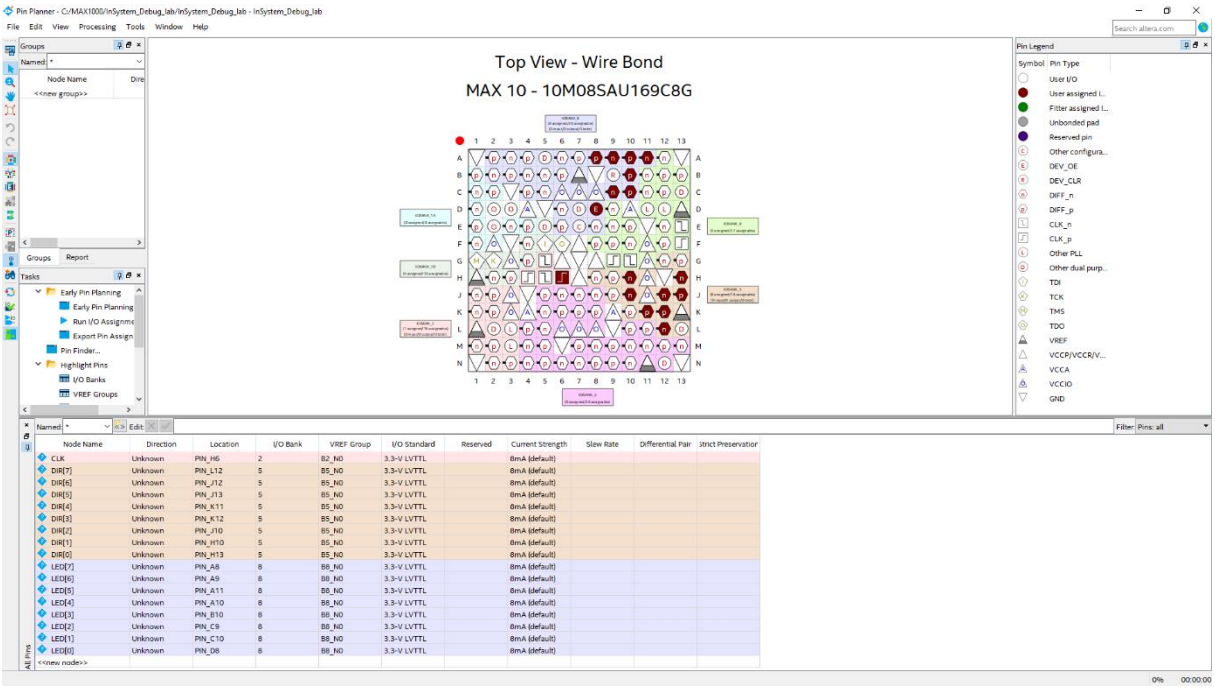
3.3.1.1 Select **Assignments → Import Assignments…**

3.3.1.2 Add source file by clicking on the ... button and browse into the lab file folder where you will locate the provided design files and add **insystem_debug_lab_pinout.csv**.



3.3.1.3 Press **OK**.

3.3.1.4 Open **Pin Planner** by clicking on button on the toolbars, or **Assignments → Pin Planner** in order to check the import. In the Pin Planner you should see the following:

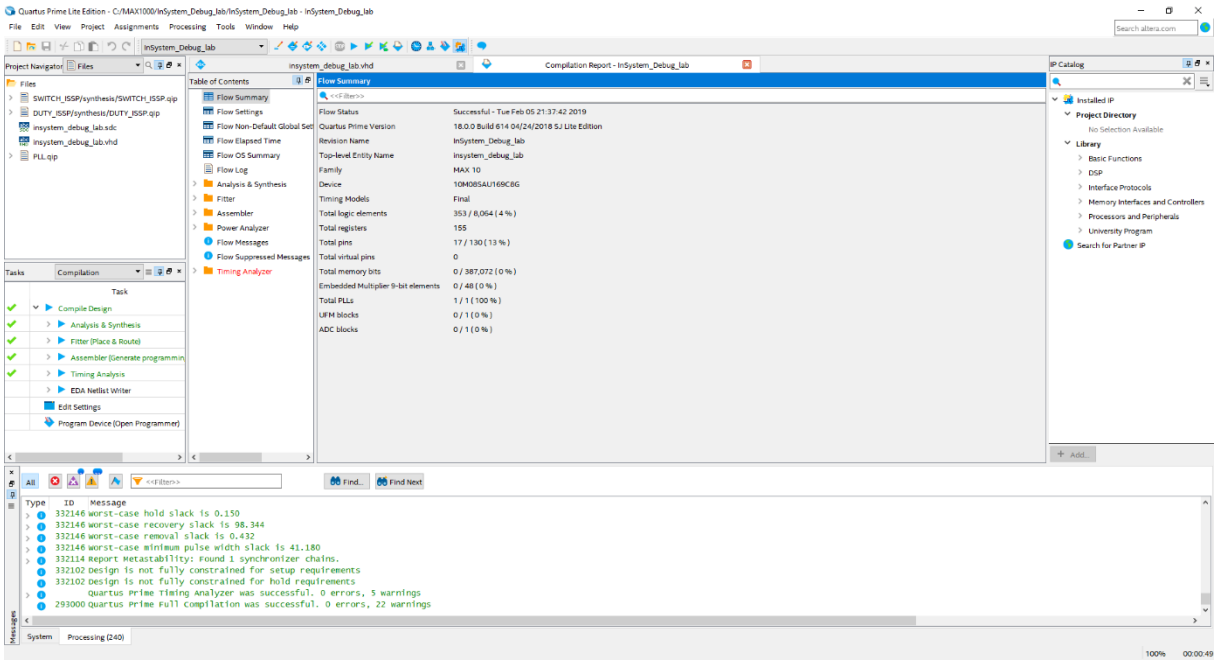


3.3.1.5 **Close** the Pin Planner.

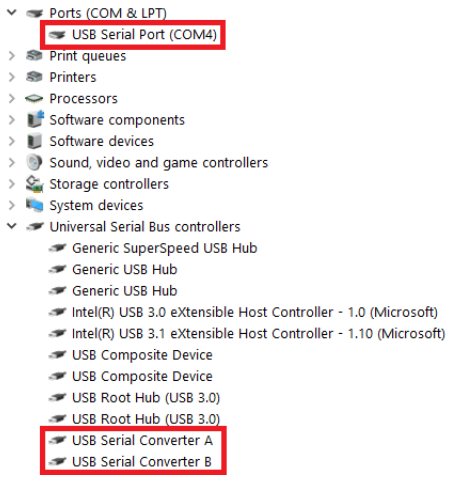
3.3.2 Compiling the Design

3.3.2.1 Start Compilation by clicking on  button on the toolbars, or **Processing → Start Compilation**.

There should be no errors. If there are errors, they should be fixed before re-compilating. The 100% in the lower right corner or a green checkmark next to the Compile Design in the Compilation task window indicates that the compilation was successful.



3.3.2.2 Connect your MAX1000 board to your PC using an USB cable. Since the Arrow USB Blaster should be already installed, the Window's Device Manager should display the following entries are highlighted in red (port number may differ depending on your PC):

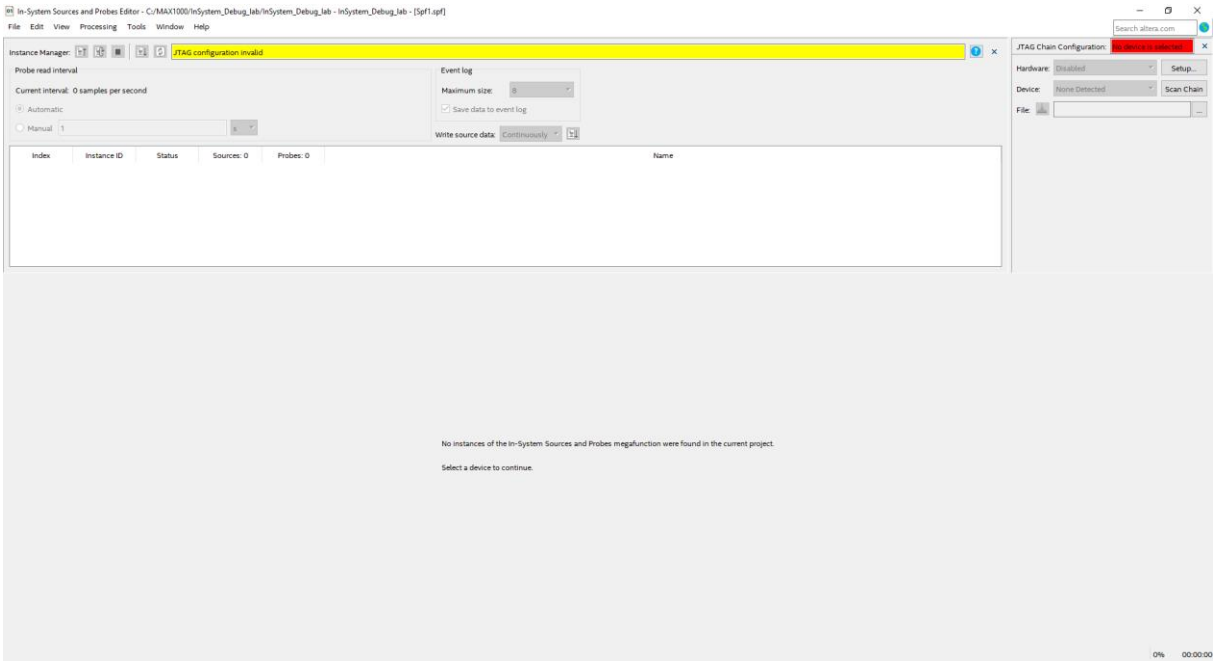


3.4 In-System Sources and Probes

3.4.1 Editor setup

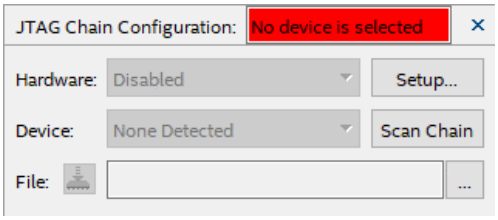
3.4.1.1 Select **Tools → In-System Sources and Probes Editor** from the menu.

3.4.1.2 The In-System Sources and Probes Editor will open. Click **OK** to close the pop-up window.

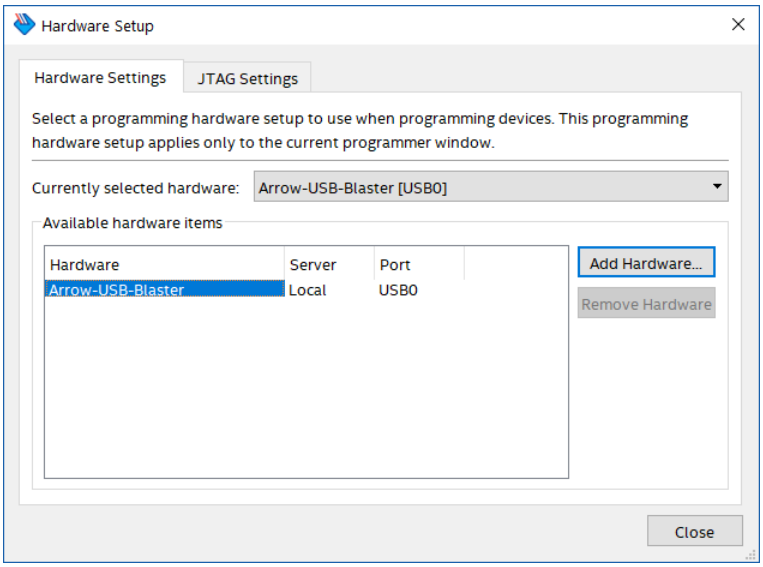


3.4.1.3 If your board is automatically detected, then you can skip the following steps and continue with the 3.4.1.7 point.

3.4.1.4 Click on the **Setup…** button in the top right corner.

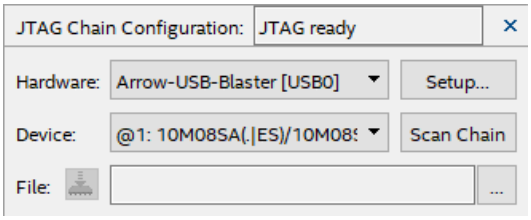


3.4.1.5 Double click **Arrow-USB-Blaster** entry in the Hardware Setup tab. The Currently selected hardware should now show Arrow-USB-Blaster [USB0] (depending on your PC, the USB port number may variant).



3.4.1.6 Click **Close** and press **OK** to close the pop-up windows.

3.4.1.7 The hardware configuration window should be updated as follows.

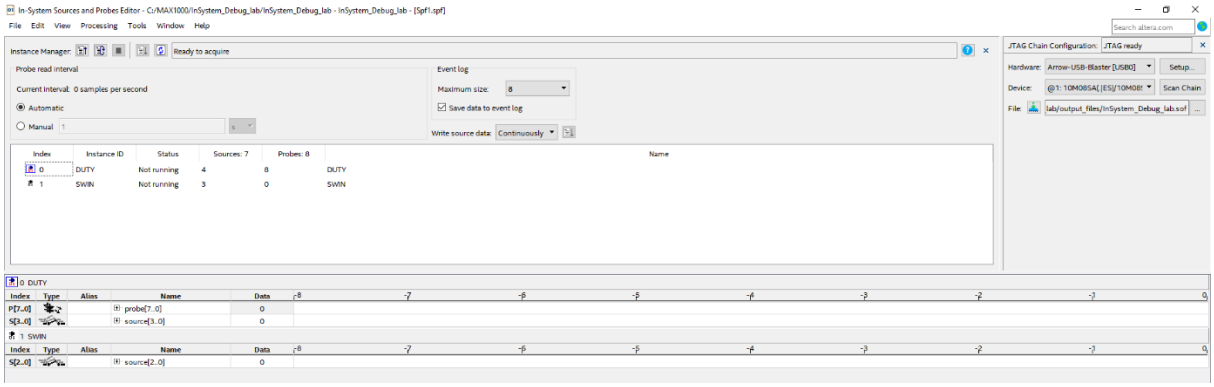


3.4.1.8 Click on  button to choose the programming file.

3.4.1.9 Navigate to **<project_directory>/output_files/** and open the **InSystem_Debug_lab.sof** file.

3.4.1.10 Click **OK** to close pop-up window.

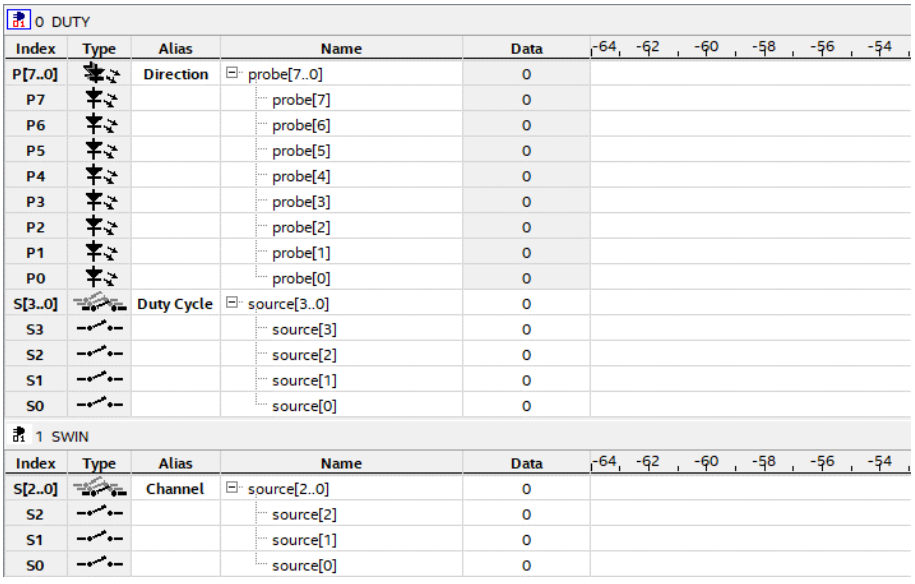
3.4.1.11 Click on  button to program the board. When the configuration is complete, the message box in the middle should write “Ready to acquire” and update the Instance Manager window.



3.4.1.12 Choose **Manual** for Probe read interval and leave the default **1 s** value.

3.4.1.13 Change the maximum size of Event log to **64** and leave **Continuously** for Write source data.

3.4.1.14 In the waveform window, type **Direction** in the alias cell of P[7..0], **Duty Cycle** for S[3..0] and **Channel** for S[2..0]. Expand the nodes.



3.4.2 Testing the board

3.4.2.1 Select DUTY and SWIN instance and click  on button to run. The status should be "Unloading data" for both instances and starts to draw the waveform.

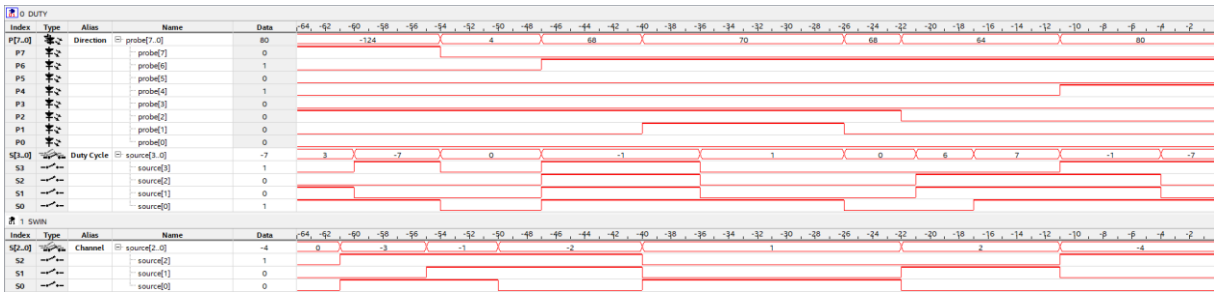
Index	Instance ID	Status	Sources: 7	Probes: 8	
0	DUTY	Unloading data	4	8	DUTY
1	SWIN	Unloading data	3	0	SWIN

3.4.2.2 Set all source node of Duty Cycle to 1 by clicking on the Data cell next to them. After this one LED is lighting on the MAX1000 board and you should see the following waveform.

3.4.2.3 Repeat the previous step with any value you like and observe that the brightness of LED will change.

3.4.2.4 By setting a value for Channel, you can change the channel of Duty Cycle input, and in this way, you can set different value for the PWMs. Set different values for Channel and Duty Cycle and observe the change on the board.

3.4.2.5 The Direction output only changes, when you set b1111 or b0000 for Duty Cycle. If you set b1111, the belonged output will be '1' until you set b0000 and vice versa.



3.4.2.6 Click  button to stop running.

CONGRATULATIONS! YOU HAVE SUCCESSFULLY COMPLETED THE IN-SYSTEM SOURCES & PROBES LAB!

5 Revision History

Version	Change Log	Date of Change
V1.0	Initial Version	06/02/2019

6 Legal Disclaimer

ARROW ELECTRONICS

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