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# <u>MAX1000</u>

# In-System Sources & Probes Lab



Software and hardware requirements to complete all exercises Software Requirements: Quartus<sup>®</sup> Prime Lite or Standard Edition version 18.0 or 18.1 Hardware Requirements: ARROW MAX1000 Board

### 1. Introduction

The In-System Sources & Probes Editor allows you to easily control any internal signal and provides you with a completely dynamic debugging environment. Traditional debugging techniques often involve using an external pattern generator to exercise the logic and a logic analyzer to study the output waveform during runtime. You can make the debugging cycle more efficient when you can drive any internal signal manually within your design. This feature can be especially helpful for prototyping your design, such as creating a virtual interface, emulating external data and monitoring, changing run time constant on the fly.

Lab Notes: Many of the names that the lab asks you to choose for files, components, and other objects in this exercise must be spelled exactly as directed. This nomenclature is necessary because the pre-written software application includes variables that use the names of the hardware peripherals. Naming the components differently can cause errors.

### 2. Getting Started

The first objective is to ensure that you have all the necessary hardware items and software installed so that the lab can be completed successfully. Below is a list of items required to complete this lab:

- MAX1000 Board (10M08SAU169C8G)
- USB Cable
- Lab files: InSystem\_Debug\_lab\_template: Template files are required to complete the lab.
   Includes: insystem\_debug\_lab.vhd, insystem\_debug\_lab.sdc,
   insystem\_debug\_lab\_pinout.csv
- Quartus Prime 18.0 Lite was used for this lab. Previous/newer versions should work (If no Quartus Prime is installed, refer to MAX1000 User Guide for instructions)
- Installed Arrow USB Drivers (If not, refer to MAX1000 User Guide for instructions)
- Personal computer or laptop running 64-bit Linux / Windows 7 or later with at least an Intel i3 core (or equivalent), 4GB RAM and 12 GB of free hard disk space
- A desire to learn!

### 3. Project with MAX1000

### 3.1 New Quartus Prime project

### 3.1.1 New project creation

- 3.1.1.1 If not already open, from the Start menu or the Desktop, open the Quartus Prime 18.0 Lite software.
- 3.1.1.2 Create a new project using the New Project Wizard: **File** → **New Project Wizard**.

🕽 New F	roject Wizard	×
Intro	duction	
The Ne	w Project Wizard helps you create a new project and preliminary project settings, including the following:	
•	Project name and directory	
•	Name of the top-level design entity	
•	Project files and libraries	
•	Target device family and device	
•	EDA tool settings	
You car	change the settings for an existing project and specify additional project-wide settings with the Settings command	
(Assign	ments menu). You can use the various pages of the Settings dialog box to add functionality to the project.	
Don	t show me this introduction again	
	< Back Next > Finish Cancel Hel	n

#### 3.1.1.3 Click Next.

- 3.1.1.4 Configure the New Project Wizard directory, name and top-level entity information:
  - Enter a directory in which you will store your Quartus project files for this design, for example, C:/MAX1000/InSystem\_Debug\_lab
  - Specify the name of the project: InSystem\_Debug\_lab
  - Specify the name of the top-level entity: InSystem\_Debug\_lab



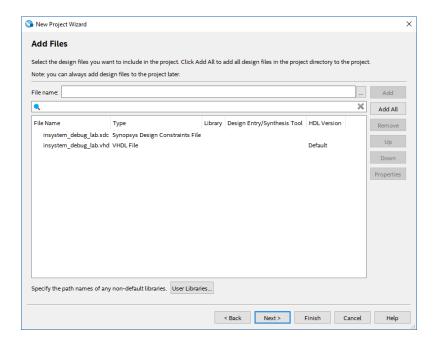
New Project Wizard					
irectory, Name, Top-Level Entity					
'hat is the working directory for this project?					
:/MAX1000/InSystem_Debug_lab					
'hat is the name of this project?					
nSystem_Debug_lab					
hat is the name of the top-level design entity for this project? This esign file.	name is case sei	nsitive and mu	ist exactly matc	h the entity nam	e in the
nSystem_Debug_lab					

#### 3.1.1.5 Click Next.

3.1.1.6 On the Project Type page, select **"Empty project"** and click **Next**.

New Project Wizard					
Project Type					
Select the type of project to create.					
Empty project					
Create new project by specifying project files and lib	raries, target d	evice family an	d device, and I	EDA tool settings.	
○ Project template					
Create a project from an existing design template. Yo		from design ter	nplates install	ed with the Quar	tus Prime
software, or download design templates from the D	<u>esign Store</u> .				
	< Back	Next >	Finish	Cancel	Help
	< Back	Next >	FILISH	Cancel	негр

- 4.1.1.1 On the Add Files page, add source files to the project by clicking on the button and browse into the lab files folder where you will locate the provided design files and add:
  - insystem\_debug\_lab.vhd
  - insystem\_debug\_lab.sdc



#### 3.1.1.7 Click Next.

3.1.1.8 Specify Family and Device Settings. Use pull-down menus to select MAX10 family or enter the part number in the Name Filter text box. The part number is **10M08SAU169C8G**.

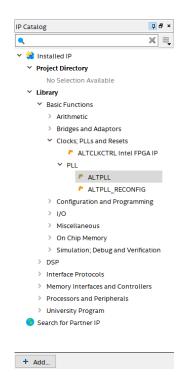
	Descuel Castin							
amily, Device &	Board Settin	gs						
Device Board								
elect the family and d								
/ou can install additio	nal device support	with the In	stall Devices com	imand on the	Tools m	ienu.		
o determine the versi	ion of the Quartus P	rime softw	are in which you	r target devic	e is supp	orted, refer	to the <u>Device Support List</u> webp	age.
Device family				Show in 'A	vailable	devices' list		
Family: MAX 10 (DA/DF/DC/SA/SC)				Package:		UFBGA		•
Device: All			•	Pin count:	5			•
Torrest devides								•
Target device				Core speed grade: 8		-		
<ul> <li>Auto device selection</li> </ul>	ted by the Fitter			Name filter: 10M08SAU169C8G				
Specific device sel	lected in 'Available o	devices' list	r -	Show a	dvanced	devices		
Other: n/a								
vailable devices:								
Name	Core Voltage	LEs	Total I/Os	GPIOs	Mer	no <b>ry</b> Bits	Embedded multiplier 9-bit	elen
10M08SAU169C8G	3.3V	8064	130	130	38707	2	48	
10M08SAU169C8GES	5 3.3V	8064	130	130	38707	2	48	
<								>

### 3.2 Design entry

### 3.2.1 Add PLL to the Quartus Project

3.2.1.1 From the IP Catalog panel on the left side, expand the menus for the **Basic Functions** → **Clocks; PLLs and Resets** → **PLL** and double click on **ALTPLL**.

If the IP catalog is not visible, then right click on the toolbar and select IP catalog.



3.2.1.2 On the Save IP Variation window, enter the following information.

- IP variation file name: <project\_directory>/PLL
- IP variation file type: VHDL

Save IP Variation	×
IP variation file name:	ОК
C:/MAX1000/InSystem_Debug_lab/PLL	
IP variation file type	Cancel
• VHDL	
○ Verilog	
	.:

3.2.1.3 Click OK.

# WUW

3.2.1.4 Under General/Modes tab (page 1 of 12) of PLL MegaWizard change the frequency of clock input to **12 MHz.** This source is provided by the internal oscillator in the MAX10 FPGA.

🌂 MegaWizard Plug-In Manager [page 1 of	12] ? X
altpll	About Documentation
Parameter         2 PLL         3 Output           Settings         Reconfiguration         Clocks	t 4 EDA 5 Summary
General/Modes Inputs/Lock Ban	lwidth/SS > Clock switchover >
PLL inclk0 areset Coperation Mode: Normal Coperation M	Which device speed grade will you be using? Any
	PLL Type         Which PLL type will you be using?         Fast PLL         Operation Mode         How will the PLL outputs be generated?         Image: Select the PLL type automatically         Operation Mode         How will the PLL outputs be generated?         Image: Select the PLL type automatically         Image: Select the PLL type automatically         Operation Mode         How will the PLL outputs be generated?         Image: Select the PLL type automatically         Image: Select the PLL type automatically

#### 3.2.1.5 Click Next.

3.2.1.6 Under Input/Lock tab (page 2 of 12) uncheck 'areset' input and locked output option.

🔨 MegaWizard Plug-In Manager [page 2	f 12]	? ×
altpll		<u>About</u> <u>Documentation</u>
Parameter 2 PLL 3 Out Settings Reconfiguration Cloce	ut 4 EDA 5 Summary	
General/Modes Inputs/Lock Bi	ndwidth/SS > Clock switchover >	
PLL	Able to implement the requested PLL	
incik0 Operation Mode: Normal Cite Ratio Philos DC (%) c0 1120 0.00 50.00 MAX 1	Enable self-reset on loss lock  Advanced Parameters Using these parameters is recommended for advanced u     Create output fie(5) using the 'Advanced' PLL param     - Configurations with output clock(s) that use cascade	PLL ase/frequency detector

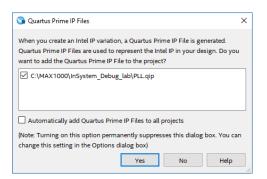
3.2.1.7 Click Next until you reach the Output Clocks tab (page 6 of 12).MAX1000Page | 7In-System Sources & Probes LabIn System Sources & Probes Lab

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3.2.1.8 Under the clk c0 tab (page 6 of 12) select "Enter output clock parameters" and set Clock division factor to **1560**. Leave the rest as default.

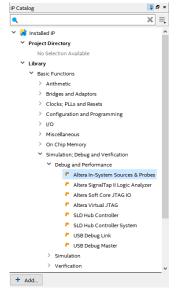
☆ MegaWizard Plug-In Manager [page 6 of 12]		? ×
altpll		About Documentation
Settings Reconfiguration Clocks	EDA 5 Summary	
PLL incik0 molk0 frequency: 12.000 MHz Operation Mode: Normal	CO - Core/External Output Clov Able to implement the requested PLL Use this dock Clock Tap Settings O Enter output dock frequency:	Requested Settings Actual Settings
Cik Ratio Ph (dg) DC (%) c0 1/1503 0.00 50.00 MAX 10	Enter output dock parameters: Clock multiplication factor Clock division factor Clock phase shift	1         ↓           1560         ↓           0.00         ↓             0.00         ↓
	Clock duty cycle (%)	50.00 🕏 50.00
	Note: The displayed internal settings of the PLL is recommended for use by advanced users only	Description Val.  Primary clock VCO frequency (MHz) Modulus for M counter 40  K
		Per Clock Feasibility Indicators C0 c1 c2 c3 c4
		Cancel < Back Next > Einish

- 3.2.1.9 Click **Finish.** This will take you to the **Summary** tab (page 12 of 12). Click **Finish** again to close ALTPLL MegaWizard Manager.
- 3.2.1.10 In the pop-up Quartus Prime IP Files accept all defaults and click Yes.



### 3.2.2 Add 1. In-System Sources & Probes to the Quartus Project

3.2.2.1 From the IP Catalog panel, expand the menus for the Basic Functions → Simulation; Debug and Verification → Debug and Performance and add Altera In-System Sources & Probes.



3.2.2.2 In the New IP Variation window enter **DUTY\_ISSP** for the Entity name and leave the rest as default.

👗 New IP Va	riation	×
Your IP setting	s will be saved in a .qsys file.	
Create IP Va	riation	
Entity name:	DUTY_ISSP	
Save in folder:	C:\MAX1000\InSystem_Debug_lab	
Target Devic	e	
Family:	MAX 10	~
Device:	10M08SAU169C8G	~
🕕 Info: Your	IP will be saved in C:\MAX1000\UnSystem_Debug_lab/ <b>DUTY_ISSP.qsys</b> .	
		OK

3.2.2.3 Press OK.

3.2.2.4 Enter **DUTY** for the Instance ID. Set **8** for the Probe Port Width and **4** for the Source Port Width.

IP Parameter Editor - DUTY_ISSP.qsys* (C:\MAX1000\InSystem_Debug_Iab\DUTY_ISSP.qsys)	- 🗆 X
ile Edit System Generate View Tools Help	
Parameters 82	_ d" 🗖 🖸 Details 💠 Block Symbol 🕸 _ d" d
System: DUTY_ISSP Path: in_system_sources_probes_0	Altera In-System Sources & Probes
Altera In-System Sources & Probes altera_in_system_sources_probes	Details Detail
* Instance Info	
Automatic Instance Index Assignment	Integer bit-width of the source port
Instance Index:	
The 'Instance ID' of this instance (optional): DUTY	
* Probe Parameters	
Probe Port Width [0512]: 8	
* Source Parameters	
Source Port Width [0512]: 4	
Hexadecimal initial value for the Source Port:	
Use Source Clock	
Use Source Clock Enable	
	🐻 Presets 💠 🗕 🖬 🗖
	Presets for in_system_sources_probes_0
	Project
	-Cick New to create a preset.
	Library -No presets for Altera In-System Sources & Probes 10
Kan and a state of the state o	
Type Path Message	
	< >
	Apply Update Delete New
0 Errors, 0 Warnings	Generate HDL Finish

- 3.2.2.5 Click **Generate HDL...** button on the bottom right of Parameter Editor window.
- 3.2.2.6 On the Generation window, enter the following information.
  - Create HDL design files for synthesis: VHDL
  - Uncheck Create timing and resource estimates for third-party EDA synthesis tools.
  - Uncheck Create block symbol file (.bsf)
  - Create simulation model: None

Synthesis		
Synthesis files are used to com	pile the system in a Quartus project.	
Create HDL design files for syn	thesis: VHDL 🗸	
Create timing and resource	e estimates for third-party EDA synthesis tools.	
Create block symbol file (.t	vsf)	
Simulation		
The simulation model contains of	generated HDL files for the simulator, and may include simulation-only features.	
Simulation scripts for this comp	onent will be generated in a vendor-specific sub-directory in the specified output directory.	
	erated simulation scripts about how to structure your design's simulation scripts and how to use the ip-setup-simulation and	
	e utilities to compile all of the files needed for simulating all of the IP in your design.	
Create simulation model:	None 🗸	
Output Directory		
Path:	C:/MAX1000/InSystem_Debug_lab/DUTY_ISSP	
	Generate	Cancel

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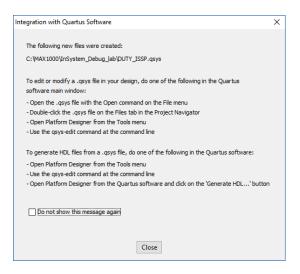
3.2.2.7 Click Generate and when the Save System is completed, click Close.

All 🚺 🔺 🕕	)			
Info: D:/inte	l/quartus/ip/**/* ma	 atched 0 files in 0,00 s	econds	,
<ol> <li>Info: Reading</li> </ol>	index D:\intel\quartu	s\18.0lite\quartus	s\sopc_builder\builtin.ip	x
Info: D:\inte	l\quartus\18.0lite\q	uartus\sopc_builde	er\builtin.ipx described 83	8 plugins,
1 Info: D:/inte	l/quartus/18.0lite/q	uartus/sopc_builde	er/**/* matched 8 files in (	0,01 secc
<ol> <li>Info: Reading</li> </ol>	index D:\intel\quartu	ıs\18.0lite\quartus	s\common\librarian\fac	tories\i
Info: D:\inte	l\quartus\18.0lite\q	uartus\common\li	brarian\factories\index	.ipx desc
🕕 Info: D:/inte	l/quartus/18.0lite/q	uartus/common/li	brarian/factories/**/*	matched
🕕 Info: D:/inte	l/quartus/18.0lite/q	uartus/sopc_builde	er/bin/\$IP_IPX_PATH ma	atched 1
🕕 Info: D:\inte	l\quartus\18.0lite\q	uartus\sopc_builde	er\bin\root_component	s.ipx de
🕕 Info: D:/inte	l/quartus/18.0lite/q	uartus/sopc_builde	er/bin/root_component	s.ipx ma
<				>
Save System:	completed successfully.			

3.2.2.8 When the generate process completed, click Close.

Senerate Completed	×
AI 😮 🛆 🕕	
Progress: Parameterizing module in_system_sources_probes_0     Progress: Building connections	^
Progress: Parameterizing connections     Progress: Validating	
Progress: Done reading input file     for OUTY_ISSP *DUTY_ISSP* for QUARTUS_SYNTH	
<ul> <li>Info: Insystem_sources_probes_0: "DUTY_ISSP" instantiated altera_in_system_s</li> <li>Info: DUTY_ISSP: Done "DUTY_ISSP" with 2 modules, 2 files</li> </ul>	501
Info: qsys-generate succeeded.	
Info: Finished: Create HDL design files for synthesis	> <sup>×</sup>
O Generate: completed successfully.	
Stop Clos	e

- 3.2.2.9 Click Finish button to close Parameter Editor window.
- 3.2.2.10 Click **Close** on pop-up window.

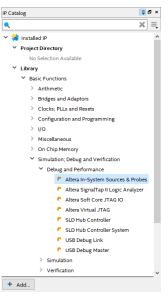


3.2.2.11 It generates IP pointer files for both synthesis (.qip) and simulation (.sip) that will point Quartus to all the necessary design files needed to synthesize or simulate the Platform Designer system. Press **OK** to close as the .qip file will be added to the project later. The In-System Sources and Probes Editor does not support simulation, so no need to add the .sip file.

🕥 Qua	irtus Prime X
i	You have created an IP Variation in the file C:/MAX1000/InSystem_Debug_lab/DUTY_ISSP.qsys.
	To add this IP to your Quartus project, you must manually add the .qip and .sip files after generating the IP core.
	The .qip will be located in <generation_directory>/synthesis/DUTY_ISSP.qip</generation_directory>
	The .sip will be located in <generation_directory>/simulation/DUTY_ISSP.sip</generation_directory>
	ок

### 3.2.3 Add 2. In-System Sources & Probes to the Quartus Project

3.2.3.1 From the IP Catalog panel, expand the menus for the **Basic Functions** → **Simulation**; Debug and Verification → Debug and Performance and add Altera In-System Sources & Probes.



3.2.3.2 In the New IP Variation window enter **SWITCH\_ISSP** for the Entity name and leave the rest as default.

👗 New IP Va	ariation	×
Your IP setting	s will be saved in a .qsys file.	
Create IP Va	riation	
Entity name:	SWITCH_ISSP	
Save in folder:	C:\MAX1000\InSystem_Debug_lab	
Target Devic	e	
Family:	MAX 10	~
Device:	10M08SAU 169C8G	~
🕕 Info: Your	IP will be saved in C:\MAX1000\[InSystem_Debug_lab/ <b>SWITCH_ISSP.qsys</b> .	
		ОК

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#### 3.2.3.3 Press OK.

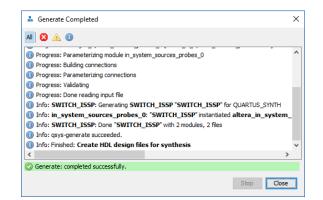
3.2.3.4 Enter **SWIN** for the Instance ID. Set **0** for the Probe Port Width and **3** for the Source Port Width.

IP Parameter Editor - SWITCH_ISSP.qsys* (C:\MAX1000\InSystem_Debug_lab\SWITCH_ISSP.qsys)	-
File Edit System Generate View Tools Help	
Parameters 🛛	_ 🗗 🗖 Details 💠 Block Symbol 🕸 🛛 _ 🗗
System: SWITCH_ISSP Path: in_system_sources_probes_0	Altera In-System Sources & Probes
Altera In-System Sources & Probes	Detais
altera_in_system_sources_probes	Source Port Width [0512]
Instance Info	
Automatic Instance Index Assignment	Integer bit-width of the source port
Instance Index:	
The 'Instance ID' of this instance (optional): SWIN	
V Probe Parameters	
Probe Port Width [0512]: 0	
Source Parameters	
Source Port Width [0512]: 3	
Hexadecimal initial value for the Source Port:	
Use Source Clock	🔍 🗙 < >
Use Source Clock Enable	
	🍯 Presets 💠 🗕 📑
	Presets for in_system_sources_probes_0
	A A A A A A A A A A A A A A A A A A A
	Project
	-Click New to create a preset.
	Library
	The presets for Altera In-System Sources a probes a
<mark>∦</mark> ≣ Messages ⊠	
Type Path Message	
	< >
	Apply Update Delete New
0 Errors, 0 Warnings	Generate HDL Finis

3.2.3.5 Click **Generate HDL...** button on the bottom right of Parameter Editor window.

3.2.3.6 On the Generation window, enter the following information and click **Generate**.

- Create HDL design files for synthesis: VHDL
- Uncheck Create timing and resource estimates for third-party EDA synthesis tools.
- Uncheck Create block symbol file (.bsf)
- Create simulation model: None
- 3.2.3.7 Click **Close** when the Save System completed.
- 3.2.3.8 When the generate process completed, click Close.



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3.2.3.9 Click Finish button to close Parameter Editor window.

3.2.3.10 **Close** both pop-up windows.

- 3.2.3.11 Choose **Project** → **Add/Remove Files in Project...** from the Quartus Prime menu.
- 3.2.3.12 Click on the button and browse through the synthesis directories: <project\_directory>/DUTY\_ISSP/synthesis/ and open DUTY\_ISSP.qip.
- 3.2.3.13 Add SWITCH\_ISSP.qip to the project from <project\_directory>/SWITCH\_ISSP/synthesis

Settings - InSystem_Debug_lab					-		×
Category:						Device/Bo	oard.
General	Files						
Files	Select the design files you want to include in	the project. Click Add All to add all de	sign files	in the project directory to the	project.		
Libraries			0				
✓ IP Settings	File name:					Add	
IP Catalog Search Locations					×	Add A	
Design Templates					1	Add A	.u
<ul> <li>Operating Settings and Conditions</li> </ul>	File Name	Туре	Library	Design Entry/Synthesis Tool	HDL Version	Remov	ve .
Voltage	SWITCH_ISSP/synthesis/SWITCH_ISSP.c	qip IP Variation File (.qip)		<none></none>			
Temperature	> DUTY_ISSP/synthesis/DUTY_ISSP.qip	IP Variation File (.qip)		<none></none>		Up	
<ul> <li>Compilation Process Settings</li> </ul>	insystem_debug_lab.sdc	Synopsys Design Constraints File		<none></none>		Down	
Incremental Compilation	insystem_debug_lab.vhd	VHDL File		<none></none>	Default		
<ul> <li>EDA Tool Settings</li> </ul>	> PLL.qip	IP Variation File (.qip)		<none></none>		Properti	ies
Design Entry/Synthesis							
Simulation							
Board-Level							
✓ Compiler Settings							
VHDL Input							
Verilog HDL Input							
Default Parameters							
Timing Analyzer							
Assembler							
Design Assistant							
Signal Tap Logic Analyzer							
Logic Analyzer Interface							
Power Analyzer Settings							
SSN Analyzer							
		🐨 Buy	Software	e OK Cancel	Apply	Hel	lp

3.2.3.14 Click Apply and OK.

### **3.2.4** Design modification

**Notes:** Up to this point, the original design is done. If you want, you can continue with 3.3 point with pin assignment, compilation and programming the board for the testing purpose in order to see the original function of the project, and then come back to continue with this 3.2.4 point.

#### 3.2.4.1 Open insystem\_debug\_lab.vhd.

- 3.2.4.2 Uncomment line 44-46, line 113-115 and line 123 by deleting "--" characters at the beginning of the lines or select the desired lines and click on  $\equiv$  button on the toolbar of text editor.
- 3.2.4.3 Comment line 98 and line 103 by writing "--" at the beginning of the lines or select the lines and click on button.
- 3.2.4.4 Add the following component declarations in the architecture section. There should be a commented area indicating where exactly around line 59.

```
component DUTY_ISSP
port( probe : in std_logic_vector(7 downto 0);
    source : out std_logic_vector(3 downto 0));
end component;

component SWITCH_ISSP
port( source : out std_logic_vector(2 downto 0));
end component;
```

3.2.4.5 Add the following component instantiations in the architecture section after the word 'begin'. There should be a commented area where exactly around line 78.

pwm\_debug : DUTY\_ISSP
port map( probe => probe,
 source => source);
sw : SWITCH\_ISSP
port map(source => iSW);

3.2.4.6 Save the modification by clicking on  $\Box$  button or File  $\rightarrow$  Save.

### 3.3 Compile design

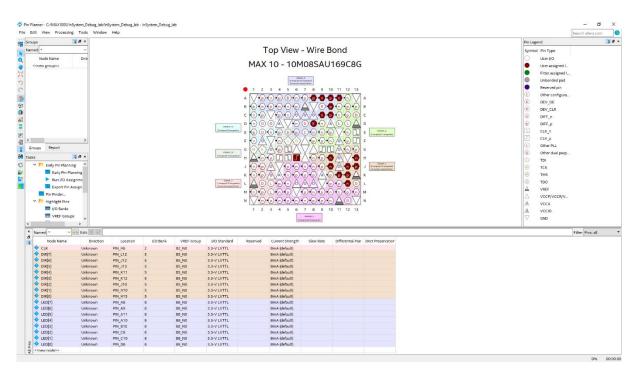
#### 3.3.1 Import pin assignments

- 3.3.1.1 Select Assignments → Import Assignments...
- 3.3.1.2 Add source file by clicking on the button and browse into the lab file folder where you will locate the provided design files and add **insystem\_debug\_lab\_pinout.csv**.

S Import Assignments	×
Specify the source and categories of assignments to import.	
File name: vstem_Debug_lab/insystem_debug_lab_pinout.csv	ries
Copy existing assignments into InSystem_Debug_lab.qsf.bak befo	ced
OK Cancel He	elp

3.3.1.3 Press OK.

3.3.1.4 Open **Pin Planner** by clicking on <sup>I define</sup> button on the toolbars, or **Assignments** → **Pin Planner** in order to check the import. In the Pin Planner you should see the following:



3.3.1.5 **Close** the Pin Planner.

### **3.3.2** Compiling the Design

3.3.2.1 Start Compilation by clicking on ► button on the toolbars, or **Processing** → Start Compilation.

There should be no errors. If there are errors, they should be fixed before re-compilating. The 100% in the lower right corner or a green checkmark next to the Compile Design in the Compilation task window indicates that the compilation was successful.

🗋 🔂 🚽 🖆 🛍 🏷 🗘 InSystem			- the state of the				
oject Navigator 📄 Files 🔹 🔍 🖬 🗗		m_debug_lab.vhd		Compilation Report - InSystem_Debug_lab		IP Catalog	<b>#</b> 1
Files		Flow Summary				٩	×
SWITCH_ISSP/synthesis/SWITCH_ISSP.q		< <filter>&gt;</filter>				🗸 🎽 Installed IP	
DUTY_ISSP/synthesis/DUTY_ISSP.qip	Flow Settings	Flow Status	Successful - Tue Feb			Y Project Directory	
insystem_debug_lab.sdc	Flow Non-Default Global Set			24/2018 SJ Lite Edition		No Selection Available	
insystem_debug_lab.vhd	Flow Elapsed Time	Revision Name	InSystem_Debug_lab			Library     Library	
PLL qip		Top-level Entity Name	insystem_debug_lab	•		> Basic Functions	
	Flow Log	Family Device	MAX 10 10M0854U169C8G			> DSP	
	Analysis & Synthesis     Fitter	Device Timing Models	10M08SAU169C8G Final			> Interface Protocols	
	Assembler	Timing Models Total logic elements	Final 353 / 8,064 (4%)			> Memory Interfaces and	
	Assembler     Power Analyzer	Total registers	353 / 8,064 (4 %) 155			Processors and Periph	ierals
	<ul> <li>Flow Messages</li> </ul>	Total pins	17/130(13%)			> University Program	
	<ul> <li>Flow Messages</li> <li>Flow Suppressed Messages</li> </ul>		0			Search for Partner IP	
ks Compilation - = 🕫 🗗		Total memory bits	0/387,072(0%)				
	Timing Analyzer	Embedded Multiplier 9-bit elements	0/48(0%)				
Task		Total PLLs	1/1(100%)				
Y 🕨 Compile Design		UFM blocks	0/1(0%)				
Analysis & Synthesis		ADC blocks	0/1(0%)				
Fitter (Place & Route)		ADC DOCKS	0,1(0.0)				
Assembler (Generate program)	nin						
> Timing Analysis							
EDA Netlist Writer							
	-						
Edit Settings	_						
Program Device (Open Programm)	n						
	> < >					+ Add	
All 🗿 🔬 👗 📐 🔻 < <filter< td=""><td>~</td><td>💏 Find 😽 Find Next</td><td></td><td></td><td></td><td></td><td></td></filter<>	~	💏 Find 😽 Find Next					
Type ID Message							
> 0 332146 worst-case hold s							
332146 worst-case recove 332146 worst-case remove							
	I STACK IS 0.432 m pulse width slack is 41.14	80					
5 5 332114 Report Metastabil	ity: Found 1 synchronizer cl	hains.					
	ly constrained for setup re						
	ly constrained for hold req						
	ing Analyzer was successful. l compilation was successfu						
		in the second second strings					

3.3.2.2 Connect your MAX1000 board to your PC using an USB cable. Since the Arrow USB Blaster should be already installed, the Window's Device Manager should display the following entries are highlighted in red (port number may differ depending on your PC):



### 3.4 In-System Sources and Probes

### 3.4.1 Editor setup

- 3.4.1.1 Select **Tools** → **In-System Sources and Probes Editor** from the menu.
- 3.4.1.2 The In-System Sources and Probes Editor will open. Click **OK** to close the pop-up window.

In-System Sources and Probes Editor - C:/MAX1000/InSystem_Debug_Jab/InSystem_Debug_Jab - InSystem_ ie Edit View Processing Tools Window Help			Search altera.com
stance Manager: 🔄 🛞 🔳 🛃 🖉 JTAG configuration invalid		0 ×	JTAG Chain Configuration: No device is selected
Probe read interval	Event log		Hardware: Disabled. To Set.
Current interval: 0 samples per second	Maximum size: 8 7		Device: None Detected * Scan
Automatic	Save data to event log		File 🔟
Manual 1 g. *	Write source data: Contrinuously *		
Index Instance D Status Source: 0 Problet: 0	None		
	No instances of the In-System Sources and Probes megafunction were found in the current project. Select a device to continue.		
			0% 0

- 3.4.1.3 If your board is automatically detected, then you can skip the following steps and continue with the 3.4.1.7 point.
- 3.4.1.4 Click on the **Setup...** button in the top right corner.

JTAG Chair	n Configuration:	No device is se	elected ×
Hardware:	Disabled	V	Setup
Device:	None Detected	7	Scan Chain
File:			

3.4.1.5 Double click **Arrow-USB-Blaster** entry in the Hardware Setup tab. The Currently selected hardware should now show Arrow-USB-Blaster [USB0] (depending on your PC, the USB port number may variant).

Hardware Settings	JTAG Set	tings			
Select a programming nardware setup applie				-	his programming
Currently selected har Available hardware if		Arrow-USB-Bl	aster [USB0]		•
Hardware Arrow-USB-Blaster		Server Local	Port USB0		Add Hardware Remove Hardware

- 3.4.1.6 Click **Close** and press **OK** to close the pop-up windows.
- 3.4.1.7 The hardware configuration window should be updated as follows.

JTAG Chair	n Configuration:	JTAG ready		×
Hardware:	Arrow-USB-Blast	er [USB0] 🔻	Setup	
Device:	@1: 10M08SA(. E	ES)/10M08: 🔻	Scan Cha	ain
File:				

- 3.4.1.8 Click on button to choose the programming file.
- 3.4.1.9 Navigate to <project\_directory>/output\_files/ and open the InSystem\_Debug\_lab.sof file.
- 3.4.1.10 Click **OK** to close pop-up window.

3.4.1.11 Click on is button to program the board. When the configuration is complete, the message box in the middle should write "Ready to acquire" and update the Instance Manager window.

volue read interval           Visite read         Event log         Visite read         Visi	stance Manager: 🗄 😟 🔳 🗄	S Ready to acquire							0 ×	JTAG Chain Co	onfiguration: JTAG read	ły
Advantate     Avanual     Avanual     Marker D     Status     Govers     Pother     S     O     Over     Nore     Over     Nore     Over     Nore     Over     Nore     Over     Nore     Over     Over	Probe read interval	(M2) received to activity		Event log						Hardware: Ar	row-USB-Blaster [USB0]	▼ Setup.
Manual     Image: Status     Source: 7     Pode:: 8       Mode:     Instance ID     Status     Source: 7       Mode:     Status     Source: 7       Status     Status     Status       Status     Status     Status       Status     Status	urrent interval: 0 samples per second			Maximum size:	8 *					Device: @	1: 10M085A[ E5]/10M0	81 👻 Scan Ch
Image       Intervention       Stature 10       Stature 10       Stature 10       Stature 10       Stature 10       Stature 10       Name         If 0       DUTY       Name       Name       Name       Name       Name         If 0       DUTY       Name       Name       Name       Name       Name         DUTY       Name       Name       Name       Name       Name       Name         DUTY       Name       Name       Name       Name       Name       Name         DUTY       Name       Name       Name       Name       Name       Name         0       DUTY       Name       Name       Name       Name       Name         0       Name       Name       Name       Name       Name       Name         0       Name       Name       Name       Name       Name       Name	Automatic			Save data to ev	vent log					File: 👗 🖬	/output_files/InSystem	Debug_lab.sof
B         DUTY         Networking         4         8         DUTY           R         1         SWN         References         SWN           DUTY         References         SWN	O Manual 1	5 V		Write source data:	Continuously *							
na Type Allen Wanne Date (* 7 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	0 DUTY Not	0										
	In o DUTY Nor In SWIN Nor	0				Hari 19						
	O DUTY	trunning 3 0	SWN	-7	4							
		trunning 3 0	SWN	-7	÷		-4	-3	-2		-1	
	0     DUTY     Nor       0     DUTY     Nor	Name         Data           .0]         0	SWN	7	÷		-4	÷	-2		-)	

- 3.4.1.12 Choose **Manual** for Probe read interval and leave the default **1 s** value.
- 3.4.1.13 Change the maximum size of Event log to **64** and leave **Continuously** for Write source data.

Instance Manager: 🛐 🛐 🔳 👔 🕼 Ready to acquire			
Probe read interval	Event log		
Current interval: 0 samples per second	Maximum size: 64 🔻		
O Automatic	Save data to event log		
Manual   1   s   ▼	Write source data: Continuously 👻 🗒		

3.4.1.14 In the waveform window, type **Direction** in the alias cell of P[7..0], **Duty Cycle** for S[3..0] and **Channel** for S[2..0]. Expand the nodes.

🚮 0 DI	UTY				
Index	Туре	Alias	Name	Data	-64 -62 -60 -58 -56 -54
P[70]	**	Direction	□ probe[70]	0	
P7	*∻		probe[7]	0	
P6	*₹		probe[6]	0	
P5	*∻		probe[5]	0	
P4	*∻		probe[4]	0	
P3	*∻		probe[3]	0	
P2	*∻		probe[2]	0	
P1	*∻		probe[1]	0	
PO	*∻		probe[0]	0	
S[30]		Duty Cycle	E source[30]	0	
<b>S</b> 3			source[3]	0	
<b>S2</b>			source[2]	0	
<b>S1</b>			source[1]	0	
<b>SO</b>			source[0]	0	
🕈 1 SV	MIN				
Index	Туре	Alias	Name	Data	-64 -62 -60 -58 -56 -54
S[20]		Channel	□ source[20]	0	
<b>S2</b>			source[2]	0	
<b>S1</b>			source[1]	0	
<b>SO</b>			source[0]	0	

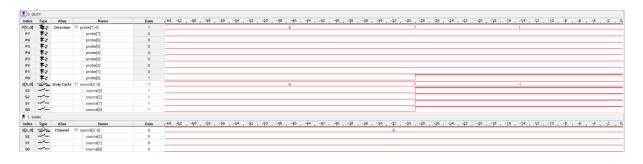
# wow

### **3.4.2** Testing the board

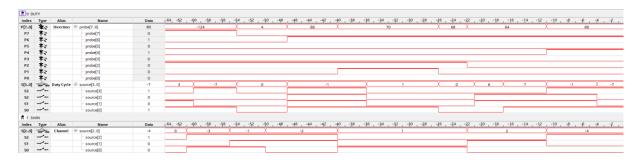
3.4.2.1 Select DUTY and SWIN instance and click 🗈 on button to run. The status should be "Unloading data" for both instances and starts to draw the waveform.

Index	Instance ID	Status	Sources: 7	Probes: 8	
a 0	DUTY	Unloading data	4	8	DUTY
1	SWIN	Unloading data	3	0	SWIN

3.4.2.2 Set all source node of Duty Cycle to 1 by clicking on the Data cell next to them. After this one LED is lighting on the MAX1000 board and you should see the following waveform.



- 3.4.2.3 Repeat the previous step with any value you like and observe that the brightness of LED will change.
- 3.4.2.4 By setting a value for Channel, you can change the channel of Duty Cycle input, and in this way, you can set different value for the PWMs. Set different values for Channel and Duty Cycle and observe the change on the board.
- 3.4.2.5 The Direction output only changes, when you set b1111 or b0000 for Duty Cycle. If you set b1111, the belonged output will be '1' until you set b0000 and vice versa.



3.4.2.6 Click 🔳 button to stop running.

### CONGRATULATIONS! YOU HAVE SUCCESSFULLY COMPLETED THE IN-SYSTEM SOURCES & PROBES LAB!

MAX1000 In-System Sources & Probes Lab

# 

### 5 Revision History

Version	Change Log	Date of Change
V1.0	Initial Version	06/02/2019

# wow

### 6 Legal Disclaimer

#### **ARROW ELECTRONICS**

#### **EVALUATION BOARD LICENSE AGREEMENT**

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#### RECYCLING

The Evaluation Board is not to be disposed as an urban waste. At the end of its life cycle, differentiated waste collection must be followed, as stated in the directive 2002/96/EC. In all the countries belonging to the European Union (EU Dir. 2002/96/EC) and those following differentiated recycling, the Evaluation Board is subject to differentiated recycling at the end of its life cycle, therefore: It is forbidden to dispose the Evaluation Board as an undifferentiated waste or with other domestic wastes. Consult the local authorities for more information on the proper disposal channels. An incorrect Evaluation Board disposal may cause damage to the environment and is punishable by the law.