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# <u>MAX1000</u>

# **Signal Probe Debugging Lab**



Software and hardware requirements to complete all exercises Software Requirements: Quartus<sup>®</sup> Prime Lite or Standard Edition version 18.0 or 18.1 Hardware Requirements: ARROW MAX1000 Board

### 1. Introduction

The Signal Probe feature allows you to route a user specified internal node to a top-level I/O without affecting the existing fitting in a design. Using the Signal Probe allows you to investigate internal device signals without performing a full compilation.

Lab Notes: Many of the names that the lab asks you to choose for files, components, and other objects in this exercise must be spelled exactly as directed. This nomenclature is necessary because the pre-written software application includes variables that use the names of the hardware peripherals. Naming the components differently can cause errors.

### 2. Getting Started

The first objective is to ensure that you have all the necessary hardware items and software installed so that the lab can be completed successfully. Below is a list of items required to complete this lab:

- MAX1000 Board (10M08SAU169C8G)
- USB Cable
- Quartus Prime 18.0 Lite was used for this lab. Previous/newer versions should work (If no Quartus Prime is installed, refer to MAX1000 User Guide for instructions)
- Installed Arrow USB Drivers (If not, refer to MAX1000 User Guide for instructions)
- Personal computer or laptop running 64-bit Linux / Windows 7 or later with at least an Intel i3 core (or equivalent), 4GB RAM and 12 GB of free hard disk space
- A desire to learn!

### 3. Project with MAX1000

### 3.1 New Quartus Prime project

### 3.1.1 New project creation

- 3.1.1.1 If not already open, from the Start menu or the Desktop, open the Quartus Prime 18.0 Lite software.
- 3.1.1.2 Create a new project using the New Project Wizard: File → New Project Wizard.

🕽 New F	roject Wizard	×
Intro	duction	
The Ne	w Project Wizard helps you create a new project and preliminary project settings, including the following:	
•	Project name and directory	
•	Name of the top-level design entity	
•	Project files and libraries	
•	Target device family and device	
•	EDA tool settings	
You car	change the settings for an existing project and specify additional project-wide settings with the Settings command	
(Assign	ments menu). You can use the various pages of the Settings dialog box to add functionality to the project.	
Don	t show me this introduction again	
	< Back Next > Finish Cancel Heli	n

#### 3.1.1.3 Click Next.

- 3.1.1.4 Configure the New Project Wizard directory, name and top-level entity information:
  - Enter a directory in which you will store your Quartus project files for this design, for example, C:/MAX1000/SignalProbe\_lab
  - Specify the name of the project: SignalProbe\_lab
  - Specify the name of the top-level entity: SignalProbe\_lab



New Project Wizard	
Directory, Name, Top-Level Entity	
What is the working directory for this project?	
C:/MAX1000/SignalProbe_lab	
What is the name of this project?	
SignalProbe_lab	
What is the name of the top-level design entity for this project? This name is case sensitive and must exactly match the entity name in design file.	the
SignalProbe lab	
Use Existing Project Settings	
	Lista

#### 3.1.1.5 Click Next.

3.1.1.6 On the Project Type page, select **"Empty project"** and click **Next**.

New Project Wizard					
Project Type					
Select the type of project to create.					
Empty project					
Create new project by specifying project files and li	ibraries, target d	levice family an	d device, and I	DA tool settings.	
O Project template					
Create a project from an existing design template. software, or download design templates from the	You can choose <u>Design Store</u> .	from design ter	nplates install	ed with the Quar	tus Prime

3.1.1.7 On the Add Files page, click Next.

New Project Wizard		
ielect the design files you want to include in the project. Click Add All to add all design files in the project.	project director	y to the
lote: you can always add design files to the project later.		
ile name:		Add
٩	×	Add All
File Name Type Library Design Entry/Synthesis Tool HDL Version		Remove
		Up
		Down
		Properties
pecify the path names of any non-default libraries. User Libraries		
< Back Next > Finish	Cancel	Help

3.1.1.8 Specify Family and Device Settings. Use pull-down menus to select MAX10 family or enter the part number in the Name Filter text box. The part number is **10M08SAU169C8G**.

Device Board							
bound bound							
Select the family and d You can install addition	levice you want to t nal device support	arget for o with the In	ompilation. stall Devices con	nmand on th	e Tools m	ienu.	
To determine the versi	on of the Quartus F	Prime softw	vare in which you	r target devi	ce is supp	orted refe	r to the Device Support List webpar
Device formily			,,	Chausia II			
Device family				Show in A	wallable	devices list	
Family: MAX 10 (DA)	/DF/DC/SA/SC)		•	Package:		UFBGA	•
Device: All			•	Pin count	:	169	•
Target device	Target device				Core speed grade:		•
O Auto device select	ed by the Fitter			Name filter: 10M08SAU169C8G			U169C8G
Specific device sel	ected in 'Available	devices' lis		Chave	a du a n co d	devices	
Other: n/a				E SHOW (	auvanceu	devices	
o other. hyu							
Available devices:							
Name	Core Voltage	LEs	Total I/Os	GPIOs	Mer	nory Bits	Embedded multiplier 9-bit ele
10M08SAU169C8G	3.3V	8064	130	130	38/0/	2	48
10M085A0109C8GE5	5.5V	0004	150	150	56707	2	40

3.1.1.9 Click Finish.

### 3.2 Design entry

### 3.2.1 Add PLL to the Quartus Project

3.2.1.1 From the IP Catalog panel on the left side, expand the menus for the **Basic Functions** → **Clocks; PLLs and Resets** → **PLL** and double click on **ALTPLL**.

If the IP catalog is not visible, then right click on the toolbar and select IP catalog.



3.2.1.2 On the Save IP Variation window, enter the following information.

- IP variation file name: <project\_directory>/PLL
- IP variation file type: VHDL

🕥 Save IP Variation	×
IP variation file name: C:/MAX1000/SignalProbe_lab/PLL	OK Cancel
IP variation file type <ul> <li>VHDL</li> </ul>	
○ Verilog	

3.2.1.3 Click OK.

# WUW

3.2.1.4 Under General/Modes tab (page 1 of 12) of PLL MegaWizard change the frequency of clock input to **12 MHz.** This source is provided by the internal oscillator in the MAX10 FPGA.

NegaWizard Plug-In Manager [page 1 of 12]	? ×
altpll	About Documentation
Parameter         PLL         Output         4           Settings         Reconfiguration         Clocks         4	]EDA []Summary
General/Modes > Inputs/Lock > Bandwidth,	/SS > Clock switchover >
PLL inclk0 inclk0 frequency: 12 000 MHz areset Operation Mode: Normal locked	Currently selected device family: MAX 10  MAX 10 Match project/default Able to implement the requested PLL General
MAX 10	Which device speed grade will you be using?       Any         Use military temperature range devices only         What is the frequency of the inck0 input?       12.000         Set up PLL in LVDS mode       Data rate:         PLL Type       Which PLL type will you be using?
	Operation Mode       • Enhanced PLL       • Select the PLL type automatically         Operation Mode       In select the PLL outputs be generated?       • Select the PLL type automatically         • Use the feedback path inside the PLL       • In normal mode       • In normal mode         • In source-synchronous compensation Mode       • In zero delay buffer mode       • Connect the forminic port (bidirectional)         • With no compensation       • With no compensation       • Create an 'fbin' input for an external feedback (External Feedback Mode)         Which output clock will be compensated for?       • • • • • • • • • • • • • • • • • • •

#### 3.2.1.5 Click Next.

3.2.1.6 Under Input/Lock tab (page 2 of 12) uncheck 'areset' input and locked output option.

🔌 MegaWizard Plug-In Manager [page 2 of	2]	? ×
altpll		<u>About</u> <u>Documentation</u>
Parameter         PLL         Output           Settings         Reconfiguration         Clocks	4 EDA 5 Summary	
General/Modes Inputs/Lock Band	width/SS Clock switchover >	
PLL incik0 frequency: 12.000 MHz Operation Mode: Normal Cis Ratio Ph (sg OC (6) (d 1/20 0.00 00.00) MAX 10	Optional Inputs Create an 'plena' input to selectively enable the PLL Create an 'areset' input to asynchronously reset the PL Create an 'pfdena' input to selectively enable the phase Lock Output Create 'locked' output Enable self-reset on loss lock Advanced Parameters Using these parameters is recommended for advanced use Create output file(s) using the 'Advanced' PLL parameter - Configurations with output clock(s) that use cascade	L ;/frequency detector rs only ers counters are not supported
	Cano	cel < <u>B</u> ack <u>N</u> ext > <u>Finish</u>

 3.2.1.7 Click Next until you reach the Output Clocks tab (page 6 of 12).

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3.2.1.8 Under the clk c0 tab (page 6 of 12) select "Enter output clock parameters" and set Clock division factor to **1000**. Leave the rest as default.

ℜ MegaWizard Plug-In Manager [page 6 of 12]		? ×
ALTPLL		About Documentation
Parameter     PLL     Settings     Clocks	EDA Summary	
PLL Incik0 Incik0 frequency: 12 000 MHz Operation Mode: Normal	c0 - Core/External Output Clov Able to implement the requested PLL ✓ Use this dock Clock Tap Settings	Ck Requested Settings Actual Settings
DR Ratio Ph (dg DC (%) c0 1/1000 0.00 50.00 MAX 10	Enter output dock frequency:     Enter output dock parameters:     Clock multiplication factor     Clock division factor     Clock phase shift	1         ↓           100.000000         MHz ∨           0.012000         1           1000         ↓           0.00         ↓           0.00         ↓
	Clock duty cycle (%)	50.00 🔅 50.00
	Note: The displayed internal settings of the PLL is recommended for use by advanced users only	Description Val. A Primary clock VCO frequency (MHz) 48. Modulus for M counter 40 C
		Per Clock Feesability Indicators c0 c1 c2 c3 c4
-		Cancel < Back Next > Finish

- 3.2.1.9 Click Finish. This will take you to the Summary tab (page 12 of 12).
- 3.2.1.10 Select PLL.bsf checkbox and click Finish.

🔨 MegaWizard Plug-In Manager [page 12 of 12]			? ×
altpll			About Documentation
Parameter         PLL         Output           Settings         Reconfiguration         Clocks	4 EDA 5 Summary		
PLL incik0 frequency: 12.000 MHz Operation Mode: Normal Cik Ratio Ph (dg OC fv) e0 1/1000 0.00 80.00 MAX 10	Turn on the files you wish tr green checkmark indicates i checkbox is maintaned in si the MegaWizard Plug-In Mi C: (MAX1000)SignalProbe_Le File PLL.pof PLL.pof PLL.inc PLL.opf PLL.bsf PLL_inst.vhd	o generate. A gray checkmark indicates a file that is an optional file. Click Finish to generate the selected block file of the selected files in the following dire block file of the selected files in the following dire block file of the selected files in the following dire block file of the selected files in the following dire block file of the selected file of the selected file of the selected file of the selected file of the selected file file of the selected file of the selected file of the selected file file file of the selected file of the sel	automatically generated, and a files. The state of each ctory:
		Cancel < <u>B</u>	ack Next > Finish

3.2.1.11 In the pop-up Quartus Prime IP Files accept all defaults and click **Yes**.



### 3.2.2 Add counter to the Quartus Project

3.2.2.1 In the search bar of the IP Catalog, type "counter", and double click on LPM\_COUNTER.

- 3.2.2.2 In the Save IP Variation window enter **COUNTER** for the IP variation file name and select **VHDL.**



3.2.2.3 Press OK.

3.2.2.5 Change the 'q' output bus to **3 bits**.

🔨 MegaWizard Plug-In M	anager [page 1 of 5]		? ×
👌 LPM_CO	DUNTER		About Documentation
1 Parameter 2 EDA Settings	3 Summary		
General Ceneral 2	Optional Inputs		
COUNTER	<b>→</b>	Currently selected device family:	MAX 10 Match project/default
	How wide should the 'q' output' What should the counter dire	bus be? 3 v bits ction be? port to allow me to do both (1 counts up	o; 0 counts down)
Resource Usage 3 lut + 3 reg		Cancel	dk Next > Finish

3.2.2.6 Click Finish. This will take you to the Summary tab (page 5 of 5).

3.2.2.7 Select COUNTER.bsf checkbox and click Finish.

r [page 5 of 5]		? ×
ITER	e e	bout Documentation
lummary		
Turn on the files you wish t generated, and a green ch The state of each checkbo The MegaWizard Plug-In M C:\MAX1000\SignalProbe_l	o generate. A gray checkmark indicates a file that eckmark indicates an optional file. Click Finish to ge is maintained in subsequent MegaWizard Plug-In anager creates the selected files in the following d ab\	is automatically merate the selected files. Manager sessions. rectory:
File	Description	
COUNTER.vhd	Variation file	
COUNTER.inc	AHDL Include file	
COUNTER.cmp	VHDL component declaration file	
COUNTER.bsf	Quartus Prime symbol file	
COUNTER_inst.vhd	Instantiation template file	
	Cancel < Back	Next > Finish
	r [page 5 of 5] ITER Ummary Turn on the files you wish t generated, and a green of The state of each checkbo The MegaWizard Plug-In M CVUNTER.vhd COUNTER.vhd COUNTER.inc COUNTER.inc COUNTER.ing COUNTER.ing COUNTER_inst.vhd	r [page 5 of 5]  ITER  Immory  Turn on the files you wish to generate. A gray checkmark indicates a file that generated, and a green checkmark indicates an optional file. Click Finish to ge The state of each checkbox is maintained in subsequent MegaVizard Plug-In The MegaVizard Plug-In Manager creates the selected files in the following d CVMAX1000(SignalProbe_Jab)  File COUNTER.whd Variation file COUNTER.inc AHDL Include file COUNTER.inf COUNTER COUNTER COUNTER COUNTER COUNTER COU

3.2.2.8 In the pop-up Quartus Prime IP Files accept all defaults and click Yes.



### **3.2.3** Add shift register to the Quartus Project

3.2.3.1 In the search bar of the IP Catalog, type "shift", and double click on LPM\_SHIFTREG.

IP Catalog	‡∂×
🔍 shift	≍ ≡
Y 🙀 Installed IP	
✓ Library	
✓ Basic Functions	
✓ Miscellaneous	
LPM_CLSHIFT	
LPM_SHIFTREG	
On Chip Memory	
Shift register (RAM-based)	
Search for Partner IP	

3.2.3.2 In the Save IP Variation window enter **DEBOUNCER** for the IP variation file name and select **VHDL.** 

🕥 Save IP Variation	×
IP variation file name:	ОК
C:/MAX1000/SignalProbe_lab/DEBOUNCER	Const
IP variation file type	Cancel
• VHDL	
○ Verilog	

3.2.3.3 Press OK.

3.2.3.5 Accept all defaults and press Finish.

				~
MegaWizard Plug-In N	lanager [page 1 of 4]		ŕ	×
🄄 LPM_SH	IFTREG	About	Document	tation
1 Parameter Settings	3 Summary			
General Optional In	puts >			
DEBOUNCER	Currently selected device family:	MAX 10	roject/defa	v
	How wide should the 'q' output bus be? 8 v bits			
	Which direction do you want the registers to shift? <ul> <li>Left</li> <li>Right</li> </ul> <li>Which outputs do you want (select at least one)?  <ul> <li>Data output</li> </ul></li>			
	Serial shift data output			
	Do you want any optional inputs?			
Resource Usage 8 lut	Cancel < Bac	k <u>N</u> ext	> Eir	nish

3.2.3.6 On the **Summary** tab (page 4 of 4) select **DEBOUNCER.bsf** and click **Finish**.

🐁 MegaWizard Plug-In Man	ager [page 4 of 4]		? ×
👌 LPM_SHI	FTREG		About Documentation
1 Parameter 2 EDA [ Settings	3 Summary		
DEBOUNCER left shift clock shiftin q[70]→	Turn on the files you wish t generated, and a green ch The state of each checkbox The MegaWizard Plug-In M C: \MAX1000\SignalProbe_l	o generate. A gray checkmark indicates a file eckmark indicates an optional file. Click Finish k is maintained in subsequent MegaWizard Plu anager creates the selected files in the followi ab\	that is automatically to generate the selected files. g-In Manager sessions. ing directory:
	File DEBOUNCER.vhd DEBOUNCER.inc DEBOUNCER.cmp DEBOUNCER.cbf DEBOUNCER_inst.vhd	Description Variation file AHDL Include file VHDL component declaration file Quartus Prime symbol file Instantiation template file	
Resource Usage 8 lut		Cancel	idk Next > Finish

3.2.3.7 In the pop-up Quartus Prime IP Files accept all defaults and click **Yes**.



### 3.2.4 Add comparator to the Quartus Project

3.2.4.1 In the search bar of the IP Catalog, type "compare", and double click on LPM\_COMPARE.



3.2.4.2 In the Save IP Variation window enter **COMPARATOR** for the IP variation file name and select **VHDL.** 

🕥 Save IP Variation	>
IP variation file name: C:/MAX1000/SignalProbe_lab/COMPARATOR	OK Cancel
VHDL     Verilog	

3.2.4.3 Press OK.

3.2.4.5 On the General tab set **3 bits** for the inputs and select **a >= b (greater than or equal)**.

× MegaWizard Plug-li	n Manager [page 1 of 5]		? ×
🍓 LPM_(		About Doc	umentation
1 Parameter Settings	3 Summary		
General General	2 > Pipelining >		
COMPARATOR unsigned compare dataa[20] datab[20] ageb	Currently selected device family: M ✓	AX 10 Match project	✓ t/default
	How many 'dataa' input bits do you want to compare to the 'datab' input bits?       3       >         Which outputs do you want?       (Select at least one)       a = b (equal)       a = b (equal)         a < b (not equal)       a > b (greater than)       >       >         a < b (greater than or equal)       a < b (less than or equal)       a < = b (less than or equal)	] bits	
Resource Usage	Cancel	Next >	Fjinish

#### 3.2.4.6 Press Finish.

3.2.4.7 On the Summary tab (page 5 of 5) select COMPARATOR.bsf and click Finish.



3.2.4.8 In the pop-up Quartus Prime IP Files accept all defaults and click Yes.



### 3.2.5 Creating schematic

3.2.5.1 Choose File → New → Block Diagram/Schematic File and click OK. A new schematic will be created, where the components can be added.



3.2.5.2 Right click in the schematic page, and select Insert → Symbol...

n Blo	ck1.bdf		×			
평 📘 🍳 👋 A 🕀 👺 🕶 🗖 🤼 🐂 🦷	15	. 🗆 O 🔪 へ 🖓 👯 🛝	4 ▲   日   🔶	⊬⊡∎!って		
	÷ (	Cut				
	0 (	Сору				
		Paste Delete				
	- -	Update Symbol or Block				
	9	Show	•			
	1	Insert	•	Symbol		
	<b>Q</b> 2	Zoom In	Ctrl+Space	Symbol as Block		
	<b>q</b> 7	Zoom Out	Ctrl+Shift+Space			
	2	Zoom				
		Fit in Window	Ctrl+Alt+W			
	R 1	Fit Selection in Window	Ctrl+Shift+W			

3.2.5.3 In the Symbol window, expand the "Project" folder and the four components that were created can now be seen.

ibraries:	
Y D Project	
다 PLL	
> 🗅 d:/intel/quartus/18.0lite/quartus/li	
< >	
lame:	
Repeat-insert mode	
Insert symbol as block	

#### 3.2.5.4 Select PLL and click OK.

3.2.5.5 The PLL component can be added by left clicking on the schematic page.

3.2.5.6 Just like in the steps from 4.2.3.2 to 4.2.3.5, do the same for 3 counters, comparator and debouncer to add them to the schematic.



- 3.2.5.7 Open again the Symbol window and expand the basic libraries.
- 3.2.5.8 Browse **megafunction** → **gates** and select **lpm\_and**.



3.2.5.9 Add it to the schematic.



3.2.5.10 Right click on the LPM\_AND and select Properties.

3.2.5.11 Choose Parameter tab and enter the following information. You can select the parameters from the drop-down menu if you double click on the cell.

Name	Value	Туре
LPM_SIZE	8	Unsigned Integer
LPM_WIDTH	1	Unsigned Integer

	eral Ports	Par	ameter Format		
	Name	Value	Туре	Description	
1	LPM_SIZE	8	Unsigned Integer	Number of inputs per gate, any integer > 0	
2	LPM_WIDTH	1	Unsigned Integer	Number of gates, any integer > 0	
3	<new></new>				

3.2.5.12 Click OK.

- 3.2.5.13 Open again the Symbol window and browse **primitives**  $\rightarrow$  **logic.**
- 3.2.5.14 Select **not** and add it to the schematic.



3.2.5.15 Click on the **Pin Tool** on the top button bar and select **Input**.



- 3.2.5.16 Add one input pin for **shiftin** of the DEBOUNCER, and an additional one input pin for **inclk0** of the PLL.
- 3.2.5.17 Click on the **Pin Tool** as before and select **Output**.
- 3.2.5.18 Add one output pin for the not gate.
- 3.2.5.19 Rename the pins by double clicking its current name.
  - pin\_name1 to CLK12M. This is going to be the clock signal coming into the FPGA.
  - pin\_name2 to BTN. This is going to be the signal of the button coming into the FPGA.
  - pin\_name3 to PWM. This is going to be the output signal.

3.2.5.20 At this point all components are added to the schematic and should look as follows:



#### 3.2.5.21 Select **Node Tool** on the top button toolbar.



#### 3.2.5.22 Connect the wires:

CLK12M	$\rightarrow$	PLL   inclk0
PLL   <b>c0</b>	$\rightarrow$	COUNTER(inst1)   clock
BTN	$\rightarrow$	DEBOUNCER   shiftin
DEBOUNCER   clock	$\rightarrow$	COUNTER(inst2)   clock
LPM_AND   result[]	$\rightarrow$	COUNTER(inst3)   clock
COMPARATOR   ageb	$\rightarrow$	NOT   input
NOT   output	$\rightarrow$	PWM



3.2.5.23 Select the **Bus Tool** on the top button toolbar.



3.2.5.24 Create the connections:

COUNTER(inst2)   <b>q[20]</b>	$\rightarrow$	COMPARATOR   dataa[20]
COUNTER(inst3)   <b>q[20]</b>	$\rightarrow$	COMPARATOR   datab[20]
DEBOUNCER   <b>q[70]</b>	$\rightarrow$	LPM_AND   data[][]

3.2.5.25 Using the bus tool create a connection coming out of the COUNTER (inst1).



3.2.5.26 Right click on the bus line of the COUNTER(inst1)'s output and select Properties.

3.2.5.27 Set the name of the bus to **clkout[2..0]**.

🔁 Bus Prop	operties	×
General	Font Format	
Name:	clkout[20]	
🗌 Hide	le name in block design file.	
	OK Cancel	Help

3.2.5.29 Right click on the wire of the DEBOUNCER clock and select **Properties**.

3.2.5.30 Set the name of the bus to clkout[2].

🔁 Bus Prop	perties	×
General	Font Format	
Name:	clkout[2]	
🗌 Hide	e name in block design file.	
	OK Cancel He	elp

#### 3.2.5.31 Click **OK**.

#### 3.2.5.32 Verify that your schematic is the same as below:



- 3.2.5.33 Save your design by clicking on  $\square$  button or **File**  $\rightarrow$  **Save** and enter the following information.
  - File name: SignalProbe\_lab
  - Save as type: Block Diagram/Schematic Files (\*.bdf)
  - Make sure that "Add file to current project" option is checked.

Save As							×
$\leftrightarrow$ $\rightarrow$ $\land$ $\uparrow$	« MAX1	000 → SignalProbe_lat	, v	v Ö	Search Signa	alProbe_lab	<i>م</i>
Organize 🔻 Ne	w folder					== -	?
💻 This PC	^	Name	^	Date	modified	Туре	1
3D Objects		db		2019.	01. 25. 16:06	File folder	
Desktop		greybox_tmp		2019.	01. 25. 16:40	File folder	
🔮 Documents	- 64						
🕹 Downloads							
👌 Music							
Pictures							
Videos							
🏪 HUL00159 (C:	) 🗸 .						>
File name:	SignalPri	be_lab					~
Save as type:	Block Dia	gram/Schematic Files (	*.bdf)				$\sim$
∧ Hide Folders			Add file to current project	t	Save	Canc	el

3.2.5.34 Click Save.

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### 3.3 Compile design

### 3.3.1 Analysis and Synthesis

3.3.1.1 Run Analysis and Synthesis by clicking on 💺 button on the toolbars, or **Processing** -> Start → Analysis and Synthesis.

There should be no errors. If there are errors, they should be fixed before continuing. If there are no errors the compilation task windows should look like this:



### 3.3.2 Pin Assignments

3.3.2.1 Open **Pin Planner** by clicking on <sup>4</sup>/<sub>2</sub> button on the toolbars, or **Assignments** -> **Pin Planner**.



3.3.2.2 In the bottom table, type **PIN\_H6** in Location column of the CLK12M.

Node Name	Direction	Location	I/O Bank	VREF Group	I/O Standard	Reserved	Current Strength	Slew Rate	Differential Pair	Strict Preservation
BTN	Input				2.5 V (default)		12mA (default)			
LLK12M	Input	PIN_H6	2	B2_N0	2.5 V (default)		12mA (default)			
PWM	Output				2.5 V (default)		12mA (default)	2 (default)		
< <new node="">&gt;</new>										

3.3.2.3 Repeat the previous step with the following assignments:

Node Name	Pin Location
BTN	PIN_E6
PWM	PIN_A8

Node Name	Direction	Location	I/O Bank	VREF Group	I/O Standard	Reserved	Current Strength	Slew Rate	Differential Pair	Strict Preservation
BTN	Input	PIN_E6	8	B8_N0	2.5 V (default)		12mA (default)			
ELK12M	Input	PIN_H6	2	B2_N0	2.5 V (default)		12mA (default)			
PWM	Output	PIN_A8	8	B8_N0	2.5 V (default)		12mA (default)	2 (default)		
< <new node="">&gt;</new>										

3.3.2.4 Double click in the I/O Standard column of BTN to open a drop-down list and change the 2.5V (Default) to **3.3 V Schmitt Trigger**.

3.3.2.5 Change the I/O Standard of CLK12M and PWM to **3.3-V LVTTL**.

Node Name	Direction	Location	I/O Bank	VREF Group	I/O Standard	Reserved	Current Strength	Slew Rate	Differential Pair	Strict Preservation
💾 BTN	Input	PIN_E6	8	B8_N0	3.3 V Schmitt Trigger		8mA (default)			
LK12M	Input	PIN_H6	2	B2_N0	3.3-V LVTTL		8mA (default)			
PWM	Output	PIN_A8	8	B8_N0	3.3-V LVTTL		8mA (default)	2 (default)		
< <new node="">&gt;</new>										

3.3.2.6 Close the Pin Planner, the settings are automatically saved.

### 3.3.3 Compiling the Design

3.3.3.1 Start Compilation by clicking on ► button on the toolbars, or Processing → Start Compilation.

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There should be no errors. If there are errors, they should be fixed before re-compilating. The 100% in the lower right corner or a green checkmark next to the Compile Design in the Compilation task window indicates that the compilation was successful.

😘 Quartus Prime Lit	te Edition - C:/MAX1000/SignalProbe_la	b/SignalProbe_lab - SignalProbe_lab					×
File Edit View	Project Assignments Processing	Tools Window Help				Search altera.com	.m 🌖
🗋 🗖 🖬 🗠 (	) 🗈 つ C SignalProbe_lab	- 260	💿 🕨 📉 🥂 🔶 🚫 🕈 🔌 😽	9			
Project Navigator	A Hierarchy 🔹 🤉 🛱 🛪	🔁 Sign	alProbe_lab.bdf		Compilation Report - SignalProbe_lab	IP Catalog	₽ð×
	Entity:Instance	Table of Contents	P Flow Summary			<u> </u>	×≡
AX 10: 10M08	SAU169C8G	Flow Summary	< <filter>&gt;</filter>			Y 🙀 Installed IP	
> 🛃 SignalProbe	lab 🐴	Flow Settings	Flow Status	Successful - Mon	Jan 28 14:39:35 2019	Project Directory	
		Flow Non-Default Global Se	et Quartus Prime Version	18.0.0 Build 614	04/24/2018 SJ Lite Edition	No Selection Available	
		Flow Elapsed Time	Revision Name	SignalProbe_lab		✓ Library	
		Elevice	Top-level Entity Name	SignaProbe_tab		> Basic Functions	
		Anabaria & Suptheria	Device	1040854115971		> DSP	
		> Eller	Timing Models	Final		> Interface Protocols	
		Assembler	Total logic elements	22 / 8.054 ( < 1 %	1	Memory Interfaces and C Descences and Descences	ontrollers
		> Power Analyzer	Total registers	17		<ul> <li>Processors and Peripher</li> <li>University Descent</li> </ul>	10
		Flow Messages	Total pins	3/130(2%)		Search for Pastner IP	
		Flow Suppressed Messager	s Total virtual pins	0			
		> 🖿 Timing Analyzer	Total memory bits	0/387,072(0%	)		
<	· · · · · · · · · · · · · · · · · · ·		Embedded Multiplier 9-bit elements	0/48(0%)			
Tasks	Compilation 💌 🗏 📮 🗗 🗶		Total PLLs	1/1(100%)			
	Task	1	UFM blocks	0/1(0%)			
🗸 🗸 🕨 Com	pile Design		ADC blocks	0/1(0%)			
> > > A	nalvsis & Svnthesis						
🗸 🔷 🕨 F	itter (Place & Route)						
> > > A	asembler (Generate programming files)						
✓ > ► T	iming Analysis						
	DA Netlict Writer						
Edes	Lettines						
Edit	secongs						
Progr	ram Device (Open Programmer)						
<	,					+ Add	
×	Î 🔊 💌 contras		n real and real year				
	Structure		oo Find Next				
Type ID	Message						^
3321	46 worst-case minimum puls	e width slack is -1.000					
0 3321	02 Design is not fully con-	strained for setup require	ements				
3321	02 Design is not fully con: Quartus Prime Timing An	strained for hold require alvzer was successful 0.0	ments errors 5 warnings				
2930	00 Quartus Prime Full Comp	ilation was successful. O	errors, 24 warnings				- 10
5 c							×
Sustem Pr	ocassing (169)						
2						-61, -42 100%	00:00:42

### 3.3.4 Configuration

3.3.4.1 Connect your MAX1000 board to your PC using an USB cable. Since the Arrow USB Blaster should be already installed, the Window's Device Manager should display the following entries are highlighted in red (port number may differ depending on your PC):



3.3.4.2 Open the Quartus Prime Programmer from **Tools** → **Programmer** or double click on Program Device (Open Programmer) from the Task window.

Programmer - C:/ File Edit View	/MAX1000/SignalProbe_lab/ Processing Tools Win	SignalProbe_lab - Sigr dow Help	nalProbe_lab - [Si	gnalProbe_lal	o.cdf]*						Search al	era.com	×
🔔 Hardware Setup.	No Hardware				Mode:	JTAG		•	Progress				
Enable real-time I	ISP to allow background pro	gramming when avai	lable										
<sup>≥1</sup> Start	File	Device	Checksum	Usercode	Program/ Configure	Verify	Blank- Check	Examine	Security Bit	Erase	ISP CLAMP		
Stop													
Auto Detect													
🗙 Delete													
膧 Add File													
Change File													
Save File													
Add Device													
1 <sup>₩</sup> Up													
<sup>∥v</sup> b Down													

3.3.4.3 Click **Hardware Setup...** and double click **Arrow-USB-Blaster** entry in the Hardware Setup tab. The Currently selected hardware should now show Arrow-USB-Blaster [USB0] (depending on your PC, the USB port number may variant).

lardware Settings	JTAG Sett	ings			
elect a programming ardware setup appli	g hardware s es only to th	etup to use i ne current pr	when progran ogrammer wir	nming devices. T ndow.	his programming
urrently selected ha Available hardware	rdware: A	rrow-USB-Bl	aster [USB0]		
Hardware Arrow-USB-Blaster		Server Local	Port USB0		Add Hardware Remove Hardware

3.3.4.4 Click Close.

3.3.4.5 Make sure the hardware setup is Arrow-USB-Blaster [USB0] and the mode is JTAG. Click **Auto Detect**.

Programmer - C:, File Edit View	Programmer - Cr/MAX1000/SignalProbe_Jab/SignalProbe_Jab - SignalProbe_Jab - [SignalProbe_Jab.cdf]* Edit View Processing Tools Window Help												
Aardware Setup	Arrow-USB-Blaster [USB	30]			Mode:	JTAG		Ť	Progress	s:			
Enable real-time	ISP to allow background pro	gramming when ava	ilable										
⊨ <sup>1</sup> b Start	File	Device	Checksum	Usercode	Program/ Configure	Verify	Blank- Check	Examine	Security Bit	Erase	ISP CLAMP		
Stop													
× Delete													
Add File													
Save File													
Add Device													
<sup>1</sup> <sup></sup>													

- 3.3.4.6 If the configuration has been added by default, you can skip the following steps and continue with the 3.3.4.11 point.
- 3.3.4.7 Select **10M08SA** device and click **OK** in the pop-up window.



- 3.3.4.8 Click **Change File...** or double click <none> to choose the programming file.
- 3.3.4.9 Navigate to <project\_directory>/output\_files/ and select the SignalProbe\_lab.sof file.
- 3.3.4.10 Click **Open**.

3.3.4.11 Make sure the Programmer shows the correct file and the correct part in the JTAG chain and check the Program/Configure checkbox.

Programmer - C://MAX1000/SignalProbe_lab/SignalProbe_lab - SignalProbe_lab.cdf]*         —         —         X           File         Edit         View         Processing         Tools         Window         Hein												×
File Edit View	Processing Tools Window H	lelp								Search	altera.com	<b>(</b>
🔔 Hardware Setup.	Arrow-USB-Blaster [USB0]				Mode: JTAG			▼ Pro	gress:			
Enable real-time I	ISP to allow background programm	ing when available										
Mu Start	File	Device	Checksum	Usercode	Program/ Configure	Verify	Blank- Check	Examine	Security Bit	Erase	ISP CLAMP	
in Stop	output_files/SignalProbe_lab.sof	10M08SAU169	00084521	00084521								
💏 Auto Detect												
🗙 Delete												
🟓 Add File												
隆 Change File												
Save File												
P <sup>th</sup> Add Device የ <sup>th</sup> Up ያኑስ Down												

3.3.4.12 Click **Start** to program the board. When the configuration is complete, the Progress bar should show 100% (Successful).

Progress:	100% (Successful)

3.3.4.13 After the programming, when you press the user button, the duty cycle of PWM will change, and accordingly, you can check it visually on LED[0].

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### 3.4 Signal Probe

### 3.4.1 Signal Probe setup

- 3.4.1.1 In the Quartus Prime, select Assignments → Device... and click on the Device and Pin Options... button.
- 3.4.1.2 Choose the **Voltage** category.
- 3.4.1.3 Set the Default I/O standard to **3.3-V LVTTL** from the drop-down menu.

ieneral	Voltage		
onfiguration	Specify voltage options fo	r the device.	
rogramming Files		· · · · · · · · · · · · · · · · · · ·	
Inused Pins	Default I/O standard:	3.3-V LVTTL	
Jual-Purpose Pins	VCCIO I/O bank1 voltage:	n/a in MAX 10 use Pin Planner to adjust VCCIO voltage	
apacitive Loading			
oard Trace Model	VCCIO I/O bank2 voltage:	n/a in MAX 10 use Pin Planner to adjust VCCIO voltage	
o Timing	Core voltage: 1.2V		
in Placement			
ror Detection CRC			
/P Settings			
artial Reconfiguration			
and a recombing a ration			
	Description:		
	Description:		
	Description:	standard to be used for pins on the target device.	
	Description: Specifies the default I/O :	standard to be used for pins on the target device.	
	Description: Specifies the default I/O t	standard to be used for pins on the target device.	
	Description: Specifies the default I/O :	standard to be used for pins on the target device.	
	Description:	standard to be used for pins on the target device.	

3.4.1.4 Press **OK** to close Device and Pin Options window. Press again **OK** to close Device window.

3.4.1.5 Select **Tools** → **Signal Probe Pins...** from the menu.

3.4.1.6 Click on Add... button.

	Node Name	Pin Location	Pin Name	Registers	Clock	Register Reset	Add.
							Delet
							Enable
							Calification
							Disable
anal Braha car	noilation						1
share robe con	inpliation						

MAX1000 Signal Probe Debugging Lab

3.4.1.7 Click on the ---- button to browse source node.

Source node name:				
Pin location:	PIN_A10	 		
Signal Probe pin name	c .			
Pipeline registers				
Number of registers:	D			
Clock signal:				
Reset signal:				

3.4.1.8 In the Node Finder window set the Filter to **SignalProbe** and click on the **List** button.

🕥 Node Fi	nder				>	<
Named:	*			~	List	
Filter:	SignalProbe				<ul> <li>Customize</li> </ul>	
Look in:	SignalProbe_lab			✓ ✓ Include subentities	Hierarchy view	
Matching	Nodes:	*: -:		Nodes Found:		
	Name	Assignments		Name	Assignments	
			>			
			>>			
			<<			
<		>		<	>	
				OK	Cancel	

3.4.1.9 From the Matching Nodes window expand **lpm\_and:inst6** → **and\_node[0]** and select **and\_node[0][7]**.

Node Finder				
lamed: *			~	List
Options				
Filter: SignalProbe				<ul> <li>Customize</li> </ul>
Look in: SignalProbe_lab			✓ ✓ Include subentities	Hierarchy view
fatching Nodes:	41 -	1	Nodes Found:	
Name	Assignments	ф	Name	Assignments
SignalProbe_lab				
BTN	PIN_E6			
STN~input	Unassigned			
🖕 ~QUARTUS_CREATED_GND~I	Unassigned			
✓ lpm_and:inst6				
Y and_node[0]				
and_node[0][7]	Unassigned			
🖕 and_node[0][7]~0	Unassigned			
and_node[0][7]~1	Unassigned	<		
and_node[0][7]~clkctrl	Unassigned	<<		
DEBOUNCER:inst5				
PLL:inst				
COUNTER:inst1				
COUNTER:inst2				
> COUNTER:inst3				
COMPARATOR:inst4	>	I	<	
		_ ···		
			Ok	Cancel

3.4.1.10 Click on the button and click **OK**.

3.4.1.11 In the Add Signal Probe Pin window set the Pin location to **PIN\_D8** and leave the rest as default.

Source node name:	lpm_and:inst6 and_node[0][7]
Pin location:	PIN_D8
Signal Probe pin nam	e: lpm and:inst6land node[0][7] signalProbe
Number of registers	0
Clock signal:	
0	

#### 3.4.1.12 Click OK.

3.4.1.13 Click again on the Add... button in the Signal Probe Pins window.

Enabled	Source Node Name	Pin Location	Pin Name	Number of Registers	Register Clock	Register Reset	Add.
1	lpm_and:inst6	PIN_D8	lpm_and:inst6	0			Delet
							Enable
							Disable
						>	
ignal Probe c	ompilation						
ignal Probe pin: heck & Save	s are created using eng All Netlist Changes.	ineering change ord	lers (ECOs). To create	e a new Signal Probe p	in or change an exis	ting Signal Probe pin yo	u must did

MAX1000 Signal Probe Debugging Lab

- 3.4.1.14 Click on the ---- button to browse source node in the Add Signal Probe Pin window.
- 3.4.1.15 In the Node Finder window make sure that the Filter is **SignalProbe** and click on the **List** button.
- 3.4.1.16 From the Matching Nodes window expand **COMPARATOR:inst4** → Ipm\_compare:LPM\_COMPARE\_component → cmpr\_n3g:auto\_generated and select ageb~1

Node Finder				
amed: *				✓ List 2
Options				
Filter: SignalProbe				<ul> <li>Customize.</li> </ul>
Look in: SignalProbe_lab			✓ … ✓ Include suber	ntities 🗹 Hierarchy view
latching Nodes:			Nodes Found:	
Name	Assignme	ф <b> </b>	Name	Assignments
SignalProbe_lab				
BTN	PIN_E6			
STN~input	Unassigned			
~QUARTUS_CREATED_GND~I	Unassigned			
Ipm_and:inst6				
> DEBOUNCER:inst5		>		
> PLL:inst		>>		
> COUNTER:inst1				
COUNTER:inst2		<		
COUNTER:inst3		<<		
COMPARATOR:inst4				
Ipm_compare:LPM_COMPARE_compon	ent			
cmpr_n3g:auto_generated				
- ageb~U	Unassigned			
le allen, i	onassigned			
c	>	[+	<	

- 3.4.1.17 Click on the button and click **OK**.
- 3.4.1.18 In the Add Signal Probe Pin window set the Pin location to **PIN\_C10** and leave the rest as default.

Source node name:	IPARATOR:inst4 lpm_compare:LPM_COMPARE_component cmpr_n3g:auto_generated ageb	<b>~</b> 1
Pin location:	PIN_C10	
Signal Probe pin nan	ne: Rinst4llpm compare:LPM COMPARE componenticmpr n3g:auto generatediageb~1 signa	alPro
Pipeline registers		
Pipeline registers Number of registers:	0	
Pipeline registers Number of registers: Clock signal:	0	

3.4.1.19 Click OK.

3.4.1.20 Make sure that both nodes are enabled and click **Start Check & Save all Netlist Changes**.

nal Probe pin	s allow you to pull or	ut an internal signa	al to a pin without	changing your design	n or running a full	compilation.	
Enabled	Source Node Name Ipm_and:inst6  COMPARATOR:	Pin Location PIN_D8 PIN_C10	Pin Name lpm_and:inst6  COMPARATOR	Number of Registers 0	Register Clock	Register Reset	Add Delete Enable
ignal Probe c	ompilation					>	
ignal Probe pin heck & Save	s are created using eng All Netlist Changes	ineering change ord	lers (ECOs). To crea	ite a new Signal Probe p	in or change an exis	ting Signal Probe pin y	rou must click
					all a set		

3.4.1.21 When the ECO fitting is complete, click **close**.

### 3.4.2 Reconfiguration

- 3.4.2.1 Open Quartus Programmer window.
- 3.4.2.2 Click **Start** to program the board.

The SignalProbe compilation generated a new programming file (.sof) which is automatically updated in the Programmer. You do not need to add again.

#### 3.4.3 Testing

The LED[7] are driven by the debounced user button. When you press it, the LED will blink accordingly to this.

The LED[6] are driven by the noninverted PWM output. The brightness will change inversely as the original, LED[0] output. Please note, because the comparator is set to a  $\geq$  b, the high value will appear on the output in every counting period. So, in contrast to LED[0], this LED will never turn off completely.



### CONGRATULATIONS! YOU HAVE SUCCESSFULLY COMPLETED THE SIGNAL PROBE DEBUGGING LAB!

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## 

### 5 Revision History

Version	Change Log	Date of Change
V1.0	Initial Version	28/01/2019

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