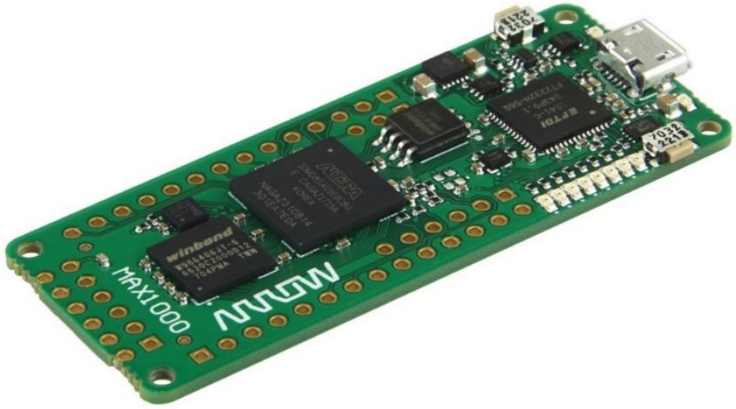
MAX1000

First MAX1000 Design Lab



Software and hardware requirements to complete all exercises

Software Requirements: Quartus® Prime Lite or Standard Edition version 18.0 or 18.1

Hardware Requirements: ARROW MAX1000 Board

Revision 1.0

1. Introduction

This tutorial provides comprehensive information to help you understand how to create a simple Intel FPGA Design and run it on your MAX1000 board. This lab will not make you an expert, but at the end, you will understand basic concepts about Quartus Prime projects, such as entering a design using a schematic editor, compiling your design, and downloading it into the FPGA on your development board.

Lab Notes: Many of the names that the lab asks you to choose for files, components, and other objects in this exercise must be spelled exactly as directed. This nomenclature is necessary because the pre-written software application includes variables that use the names of the hardware peripherals. Naming the components differently can cause errors.

2. Getting Started

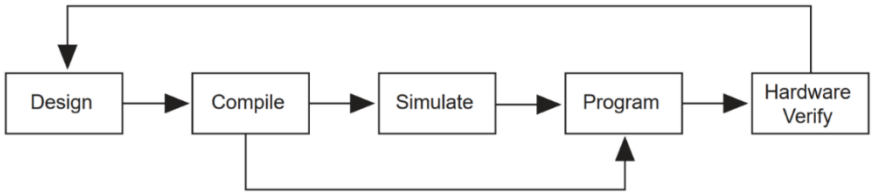
The first objective is to ensure that you have all the necessary hardware items and software installed so that the lab can be completed successfully. Below is a list of items required to complete this lab:

- MAX1000 Board **(**10M08SAU169C8G)
- USB Cable
- Quartus Prime 18.0 Lite was used for this lab. Previous/newer versions should work (If no Quartus Prime is installed, refer to MAX1000 User Guide for instructions)
- Installed Arrow USB Drivers (If not, refer to MAX1000 User Guide for instructions)
- Personal computer or laptop running 64-bit Linux / Windows 7 or later with at least an Intel i3 core (or equivalent), 4GB RAM and 12 GB of free hard disk space
- A desire to learn!

3. Design Flow

The Quartus Prime design software provides a complete, multiplatform design environment that easily adapts to your specific design needs. It is a comprehensive environment for system-on-a-programmable-chip (SOPC) design. The Quartus Prime software includes solutions for all phases of FPGA and CPLD design.

The standard FPGA design flow starts with design entry using schematics or hardware description language (HDL), such as Verilog HDL or VHDL. In this step, you create the digital circuit that is implemented inside the FPGA. The flow then proceeds through compilation, simulation, programming, and verification in the FPGA hardware.



This tutorial guides you through all of the steps except for simulation. Although it is not covered in this document, simulation is very important to learn, and there are entire applications devoted to simulating hardware design.

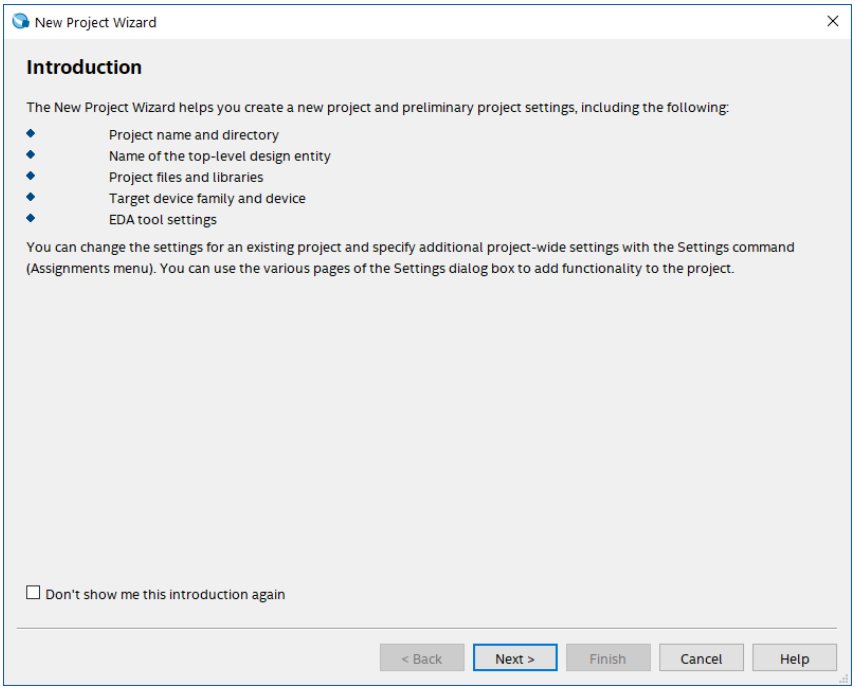
4. Project with MAX1000

4.1 New Quartus Prime project

4.1.1 New project creation

4.1.1.1 If not already open, from the Start menu or the Desktop, open the Quartus Prime 18.0 Lite software.

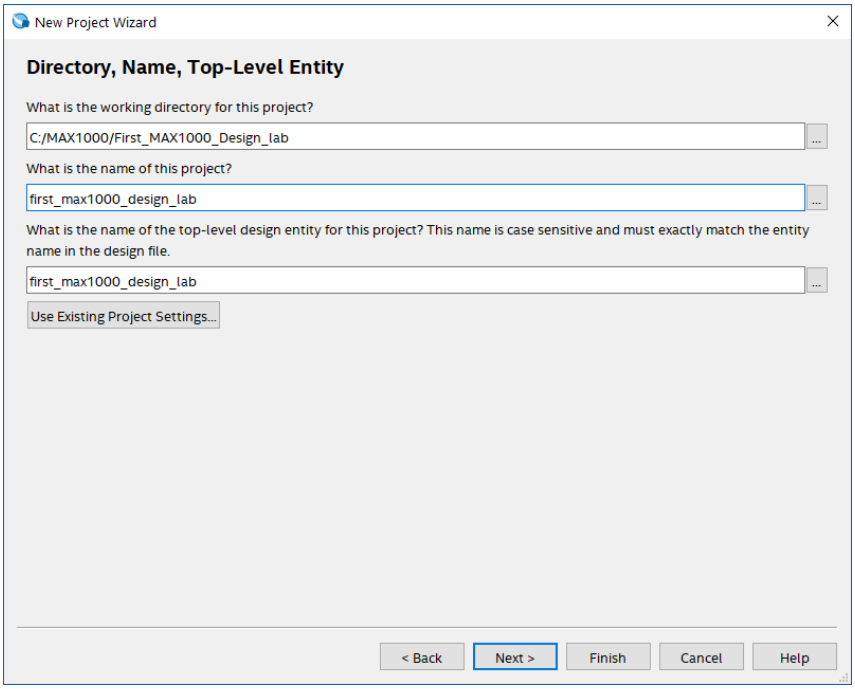
4.1.1.2 Create a new project using the New Project Wizard: **File → New Project Wizard**.



4.1.1.3 Click **Next**.

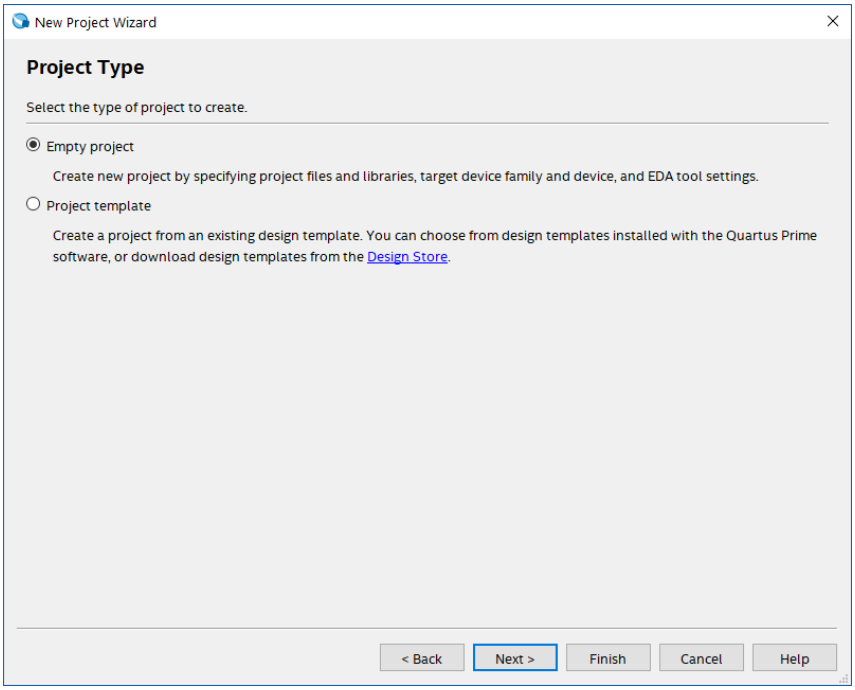
4.1.1.4 Configure the New Project Wizard directory, name and top-level entity information:

- Enter a directory in which you will store your Quartus project files for this design, for example, **C:/MAX1000/First_MAX1000_Design_lab**
- Specify the name of the project: **first_max1000_design_lab**
- Specify the name of the top-level entity: **first_max1000_design_lab**

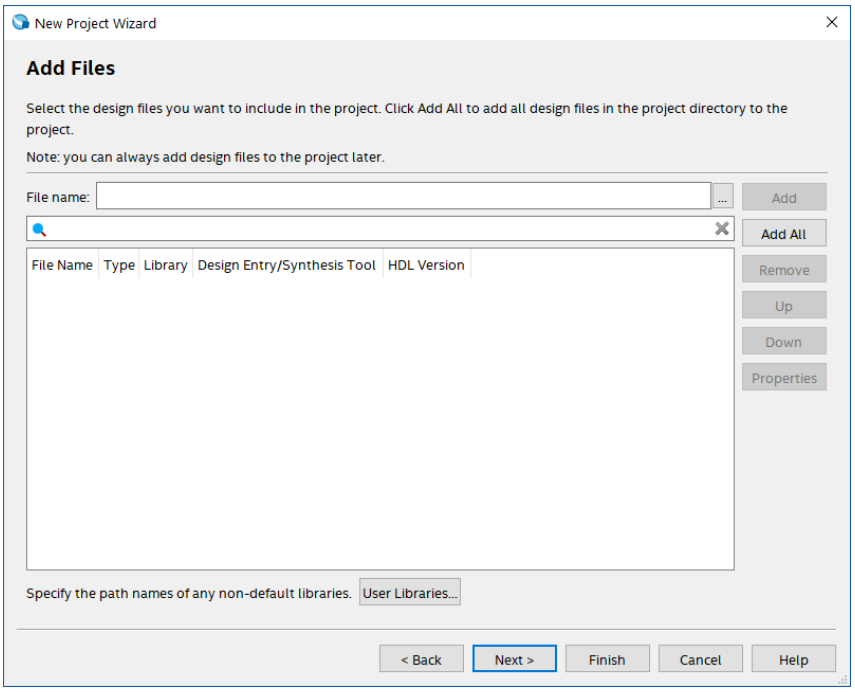


4.1.1.5 Click **Next**.

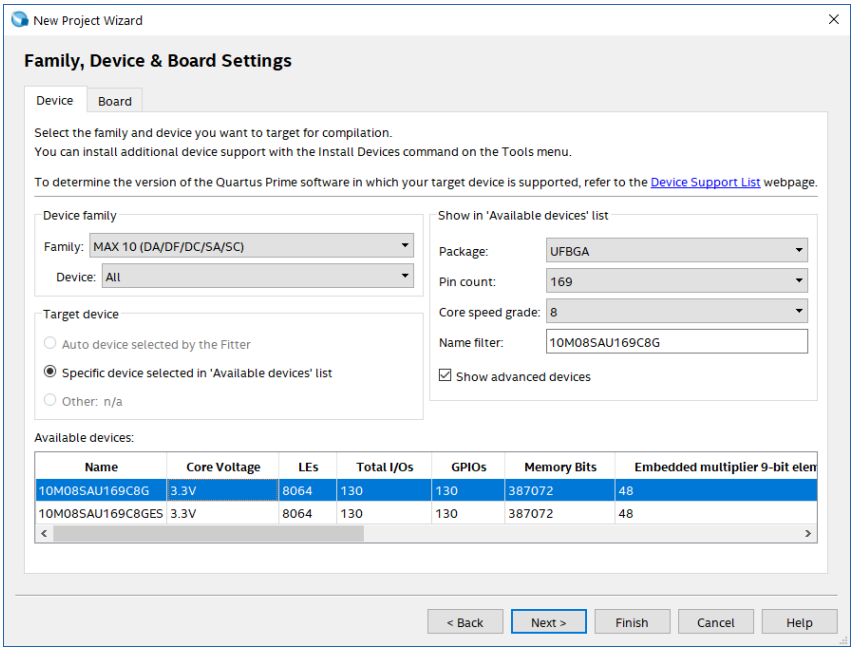
4.1.1.6 On the Project Type page, select **"Empty project"** and click **Next**.



4.1.1.7 On the Add Files page, click **Next**.



4.1.1.8 Specify Family and Device Settings. Use pull-down menus to select MAX10 family or enter the part number in the Name Filter text box. The part number is **10M08SAU169C8G**.



4.1.1.9 Click **Finish**.

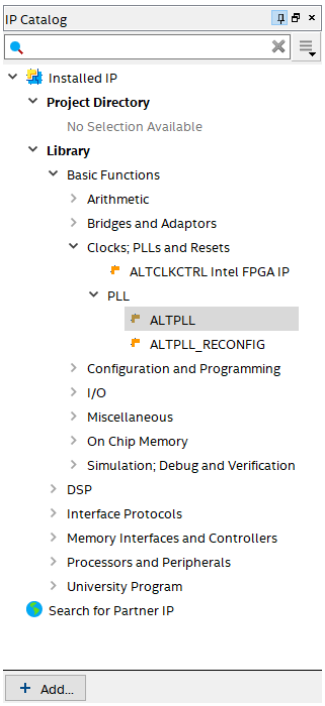
4.2 Design entry

Overview: In this module you will use schematic entry to create the components to design. You will also make connections, set the pin assignments, and compile a project.

4.2.1 Add PLL to the Quartus Project

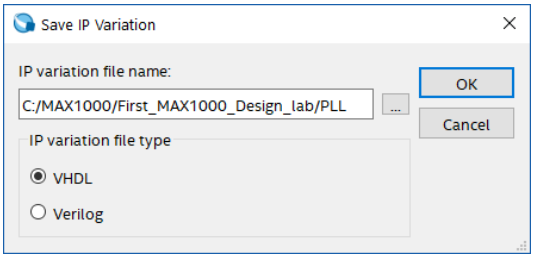
4.2.1.1 From the IP Catalog panel on the left side, expand the menus for the **Basic Functions → Clocks; PLLs and Resets → PLL** and double click on **ALTPLL**.

If the IP catalog is not visible, then right click on the toolbar and select IP catalog.



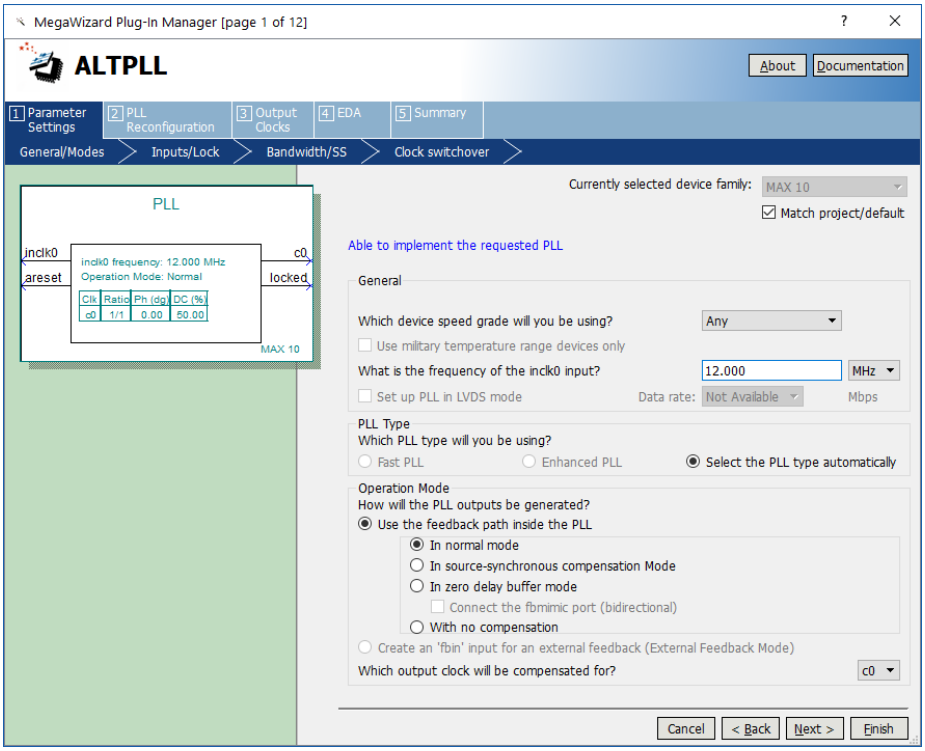
4.2.1.2 On the Save IP Variation window, enter the following information.

- IP variation file name: **<project_directory>/PLL**
- IP variation file type: **VHDL**



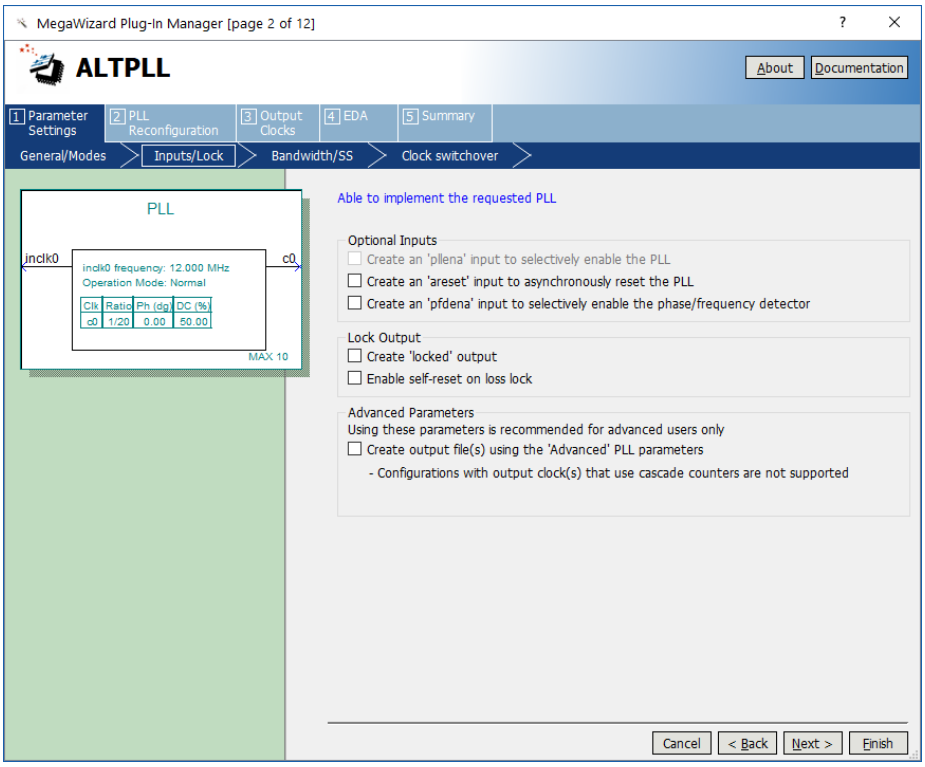
4.2.1.3 Click **OK**.

4.2.1.4 Under General/Modes tab (page 1 of 12) of PLL MegaWizard change the frequency of clock input to **12 MHz.** This source is provided by the internal oscillator in the MAX10 FPGA.



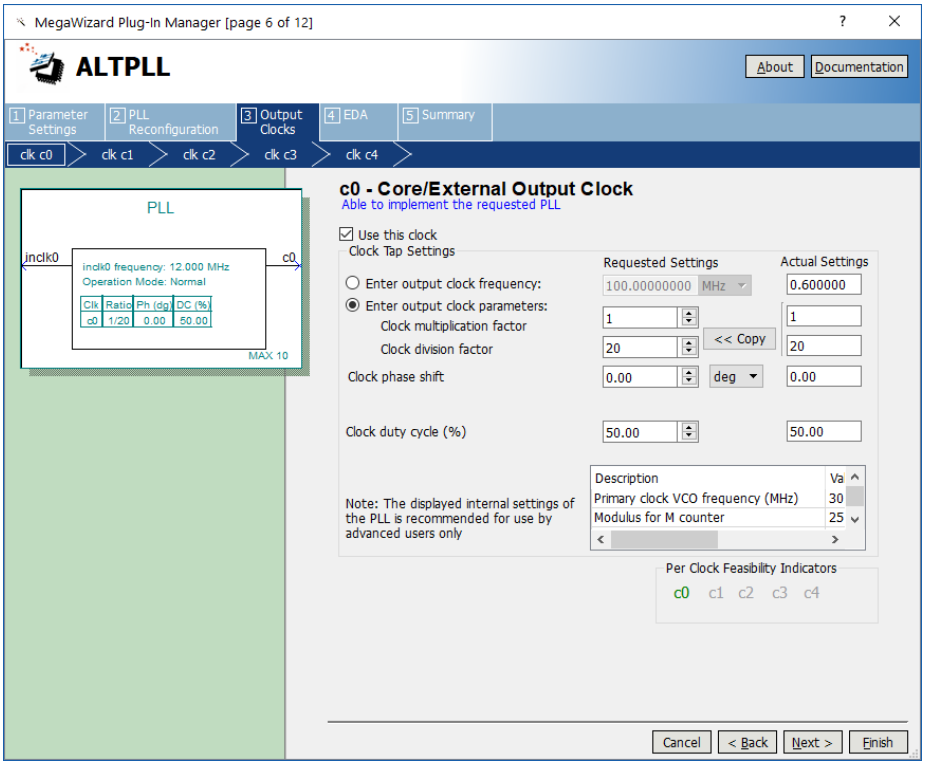
4.2.1.5 Click **Next**.

4.2.1.6 Under Input/Lock tab (page 2 of 12) uncheck ‘areset’ input and locked output option.

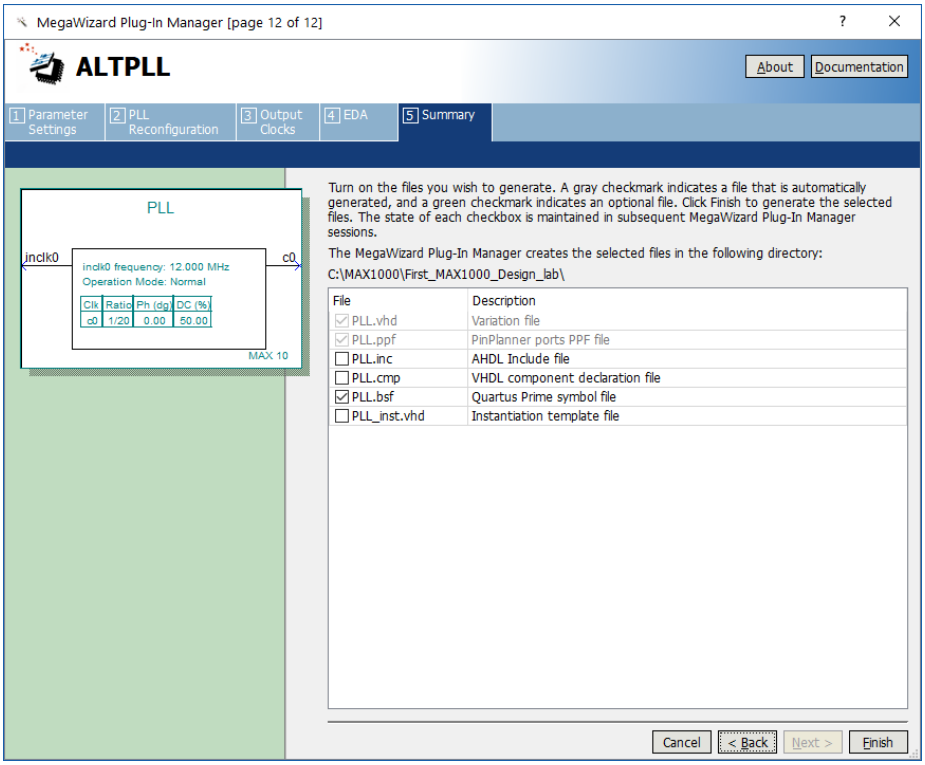


4.2.1.7 Click **Next** until you reach the **Output Clocks** tab (page 6 of 12).

4.2.1.8 Under the clk c0 tab (page 6 of 12) select “Enter output clock parameters” and set Clock division factor to **20**. Leave the rest as default.

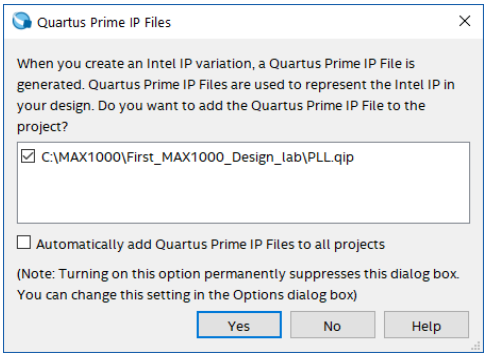


4.2.1.9 Click **Next** until you reach the **Summary** tab (page 12 of 12) and select **PLL.bsf** checkbox.



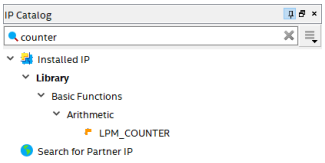
4.2.1.10 Click **Finish**.

4.2.1.11 In the pop-up Quartus Prime IP Files accept all defaults and click **Yes**.

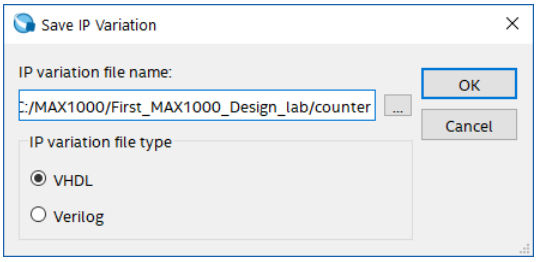


4.2.2 Add counter to the Quartus Project

4.2.2.1 In the search bar of the IP Catalog, type “counter”, and double click on **LPM_COUNTER**.

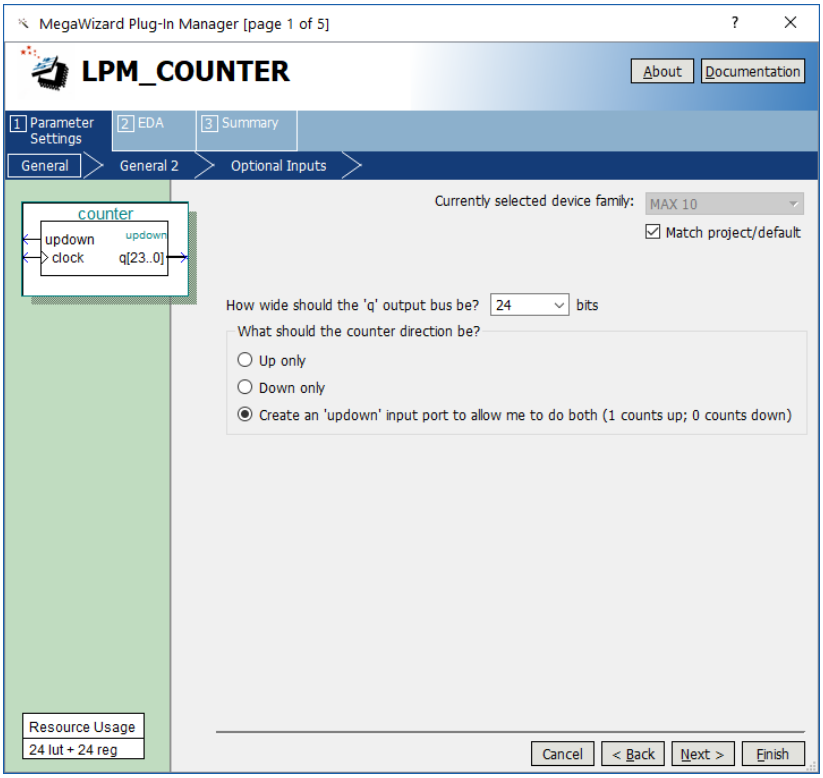


4.2.2.2 In the Save IP Variation window enter **counter** for the IP variation file name and select **VHDL.**



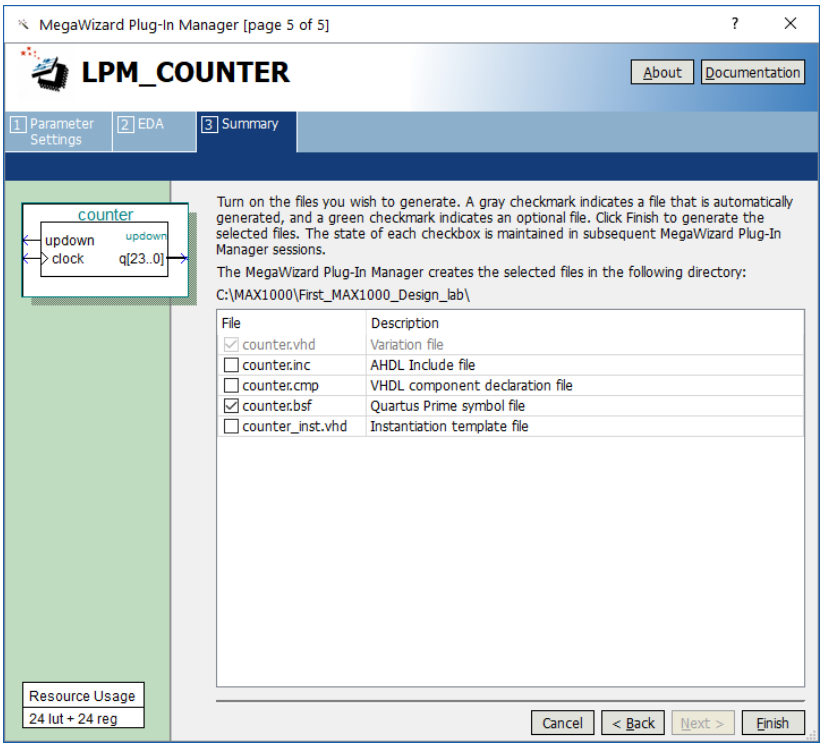
4.2.2.3 Press **OK**.

4.2.2.5 Change the ‘q’ output bus to **24 bits** and select “Create an ‘updown’ input port to allow me to do both”.

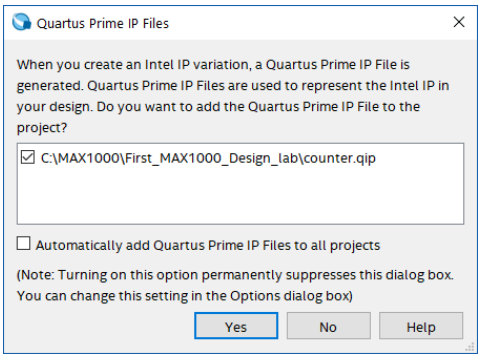


4.2.2.6 Click **Next** until reaching the **Summary** tab (page 5 of 5).

4.2.2.7 Select **counter.bsf** checkbox and click **Finish**.

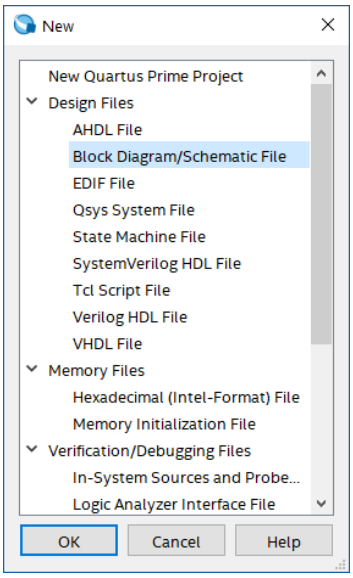


4.2.2.8 In the pop-up Quartus Prime IP Files accept all defaults and click **Yes**.

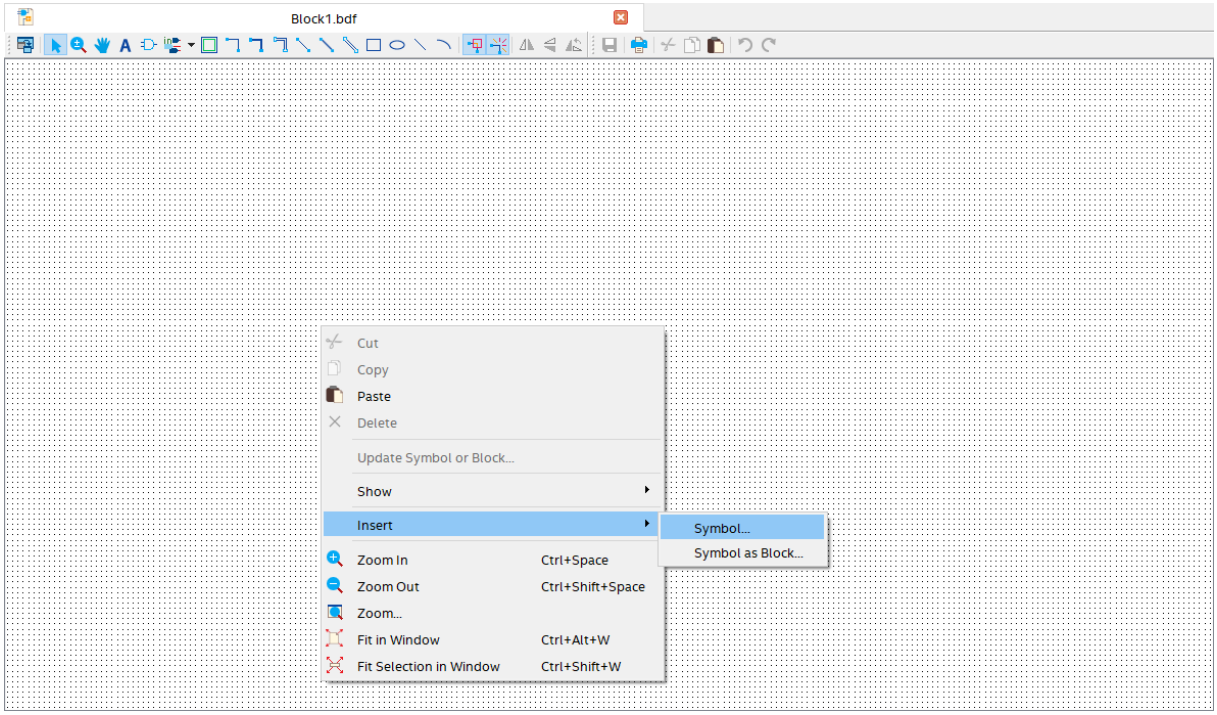


4.2.3 Creating schematic

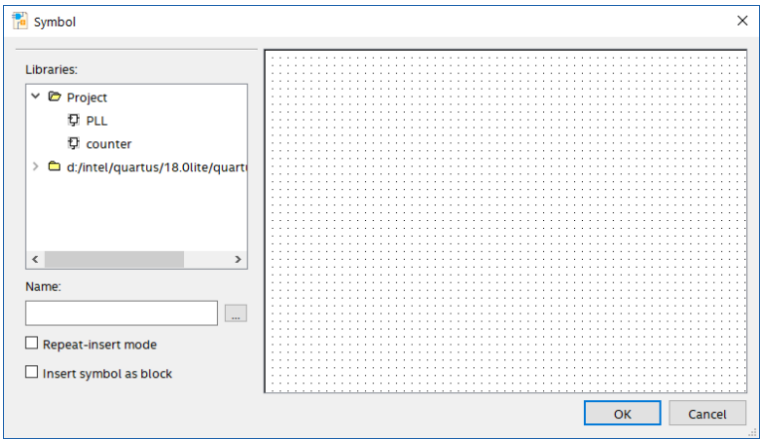
4.2.3.1 Choose **File → New → Block Diagram/Schematic File** and click **OK**. A new schematic will be created, where the components can be added.



4.2.3.2 Right click in the schematic page, and select **Insert → Symbol…**



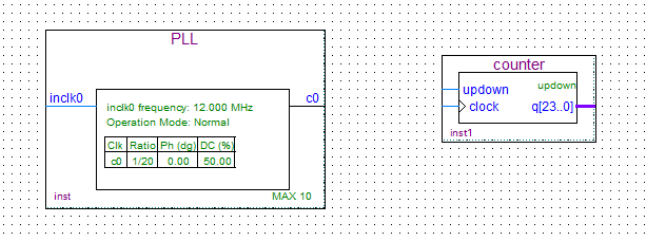
4.2.3.3 In the Symbol window, expand the “Project” folder and both components that were created can now be seen.



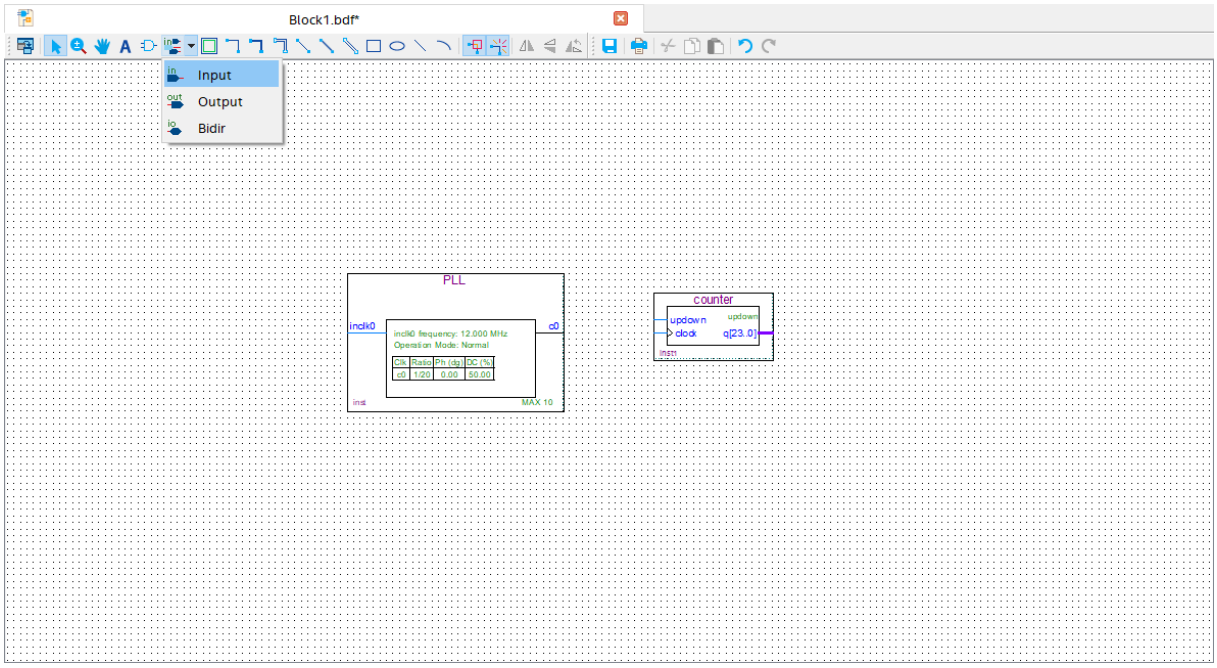
4.2.3.4 Select **PLL** and click **OK**.

4.2.3.5 The PLL component can be added by left clicking on the schematic page.

4.2.3.6 Just like in the steps from 4.2.3.2 to 4.2.3.5, do the same for counter to add it to the schematic.



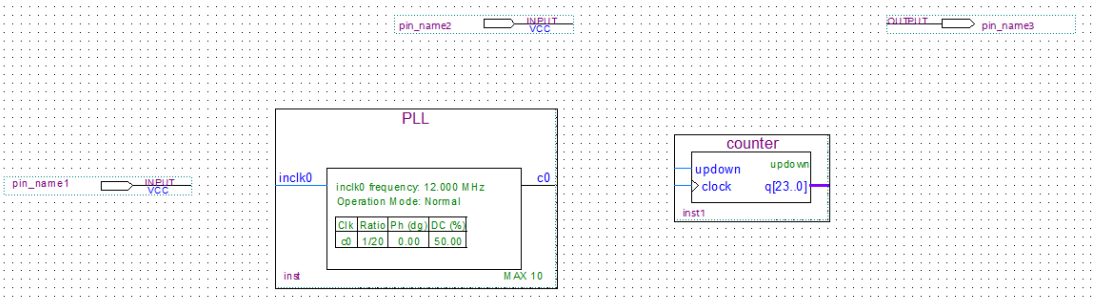
4.2.3.7 Click on the **Pin Tool** on the top button bar and select **Input**.



4.2.3.8 Add one input pin for **updown** of the counter, and an additional one input pin for **inclk0** of the PLL.

4.2.3.9 Click on the **Pin Tool** as before and select **Output**.

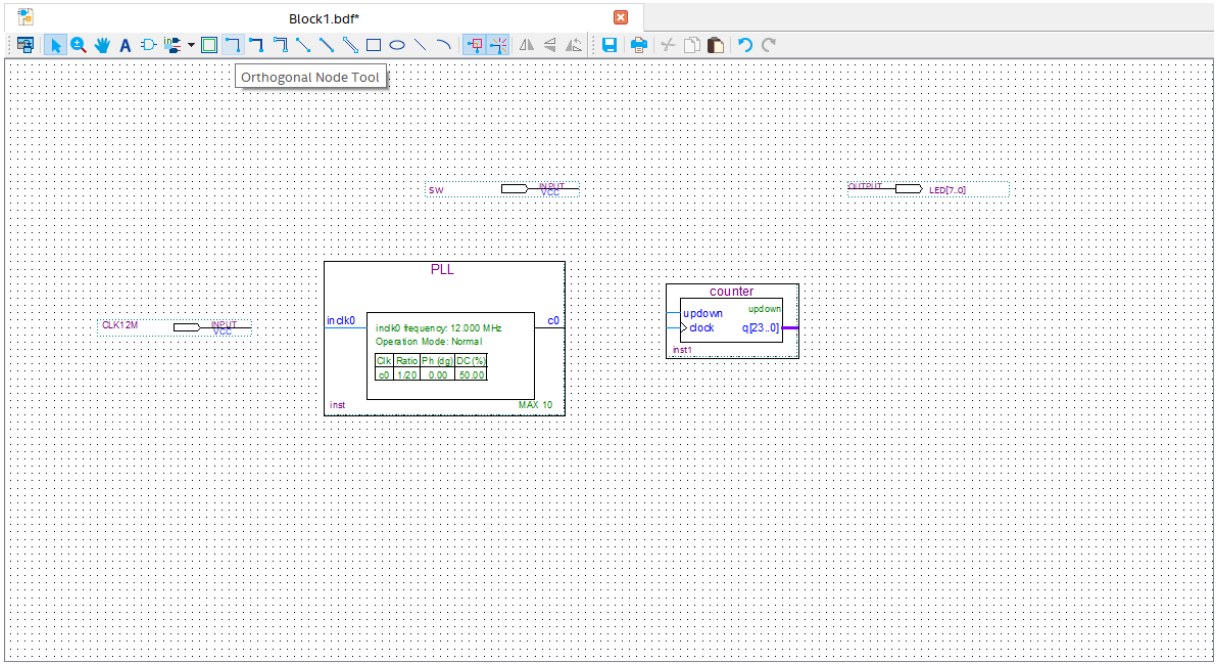
4.2.3.10 Add one output pin for the LEDs.



4.2.3.11 Rename the pins by double clicking its current name.

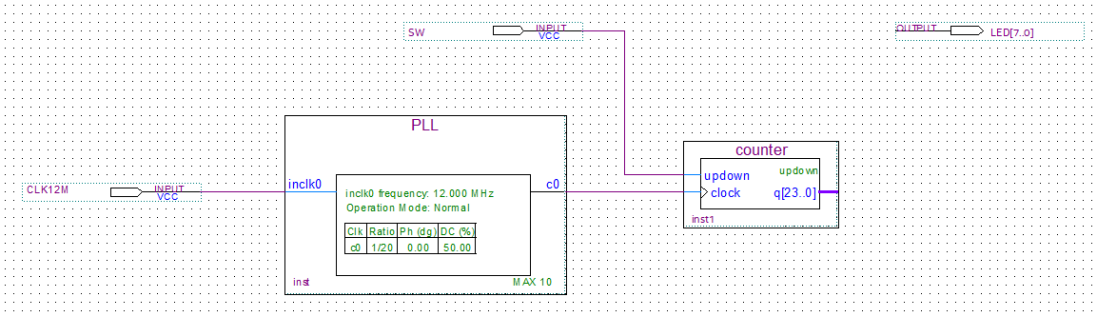
- pin_name1 to **CLK12M**. This is going to be the clock signal coming into the FPGA.
- pin_name2 to **SW**. This is going to be the signal of the button coming into the FPGA.
- pin_name3 to **LED[7..0]**. This is going to be the output signal for the LEDs.

4.2.3.12 Select **Node Tool** on the top button toolbar.

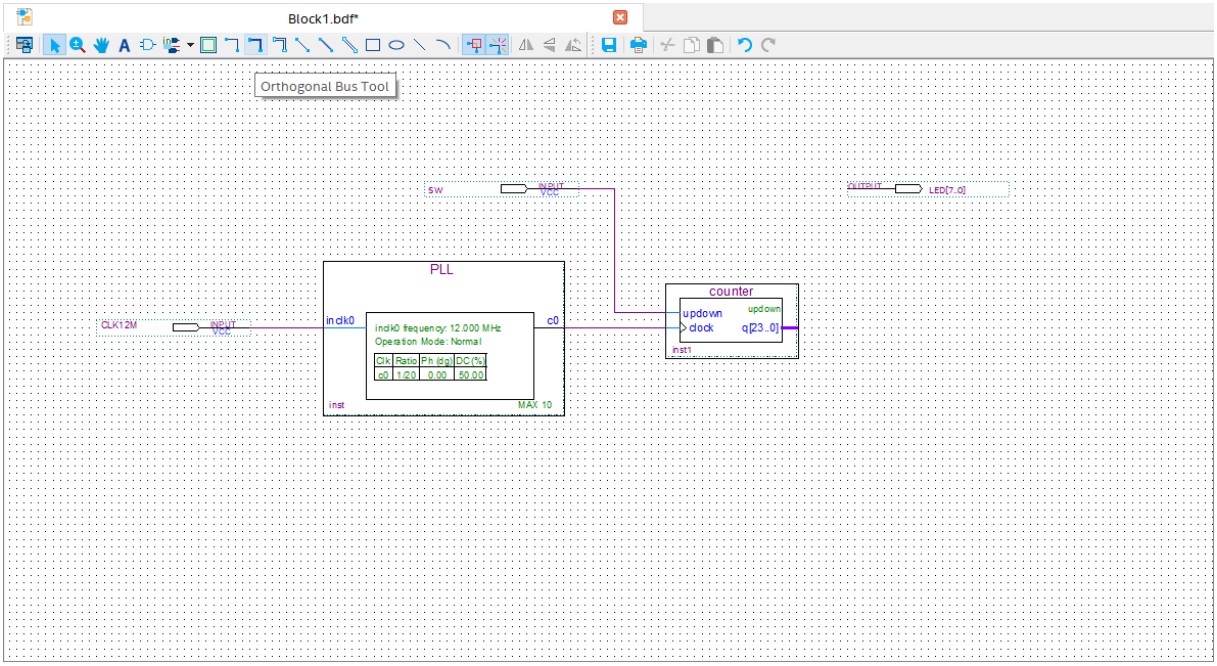


4.2.3.13 Connect the wires:

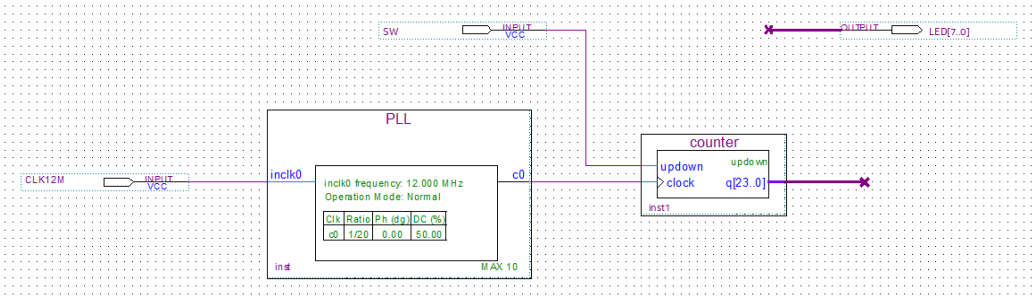
CLK12M	→	PLL | **inclk0**
SW	→	counter | **updown**
PLL | **c0**	→	counter | **clock**



4.2.3.14 Select the **Bus Tool** on the top button toolbar.

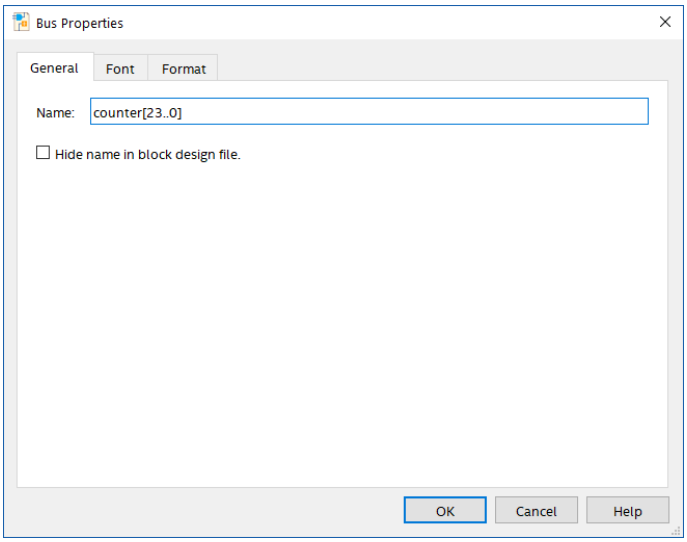


4.2.3.15 Using the bus tool create a connection coming out of the counter and one connection for the LEDs.



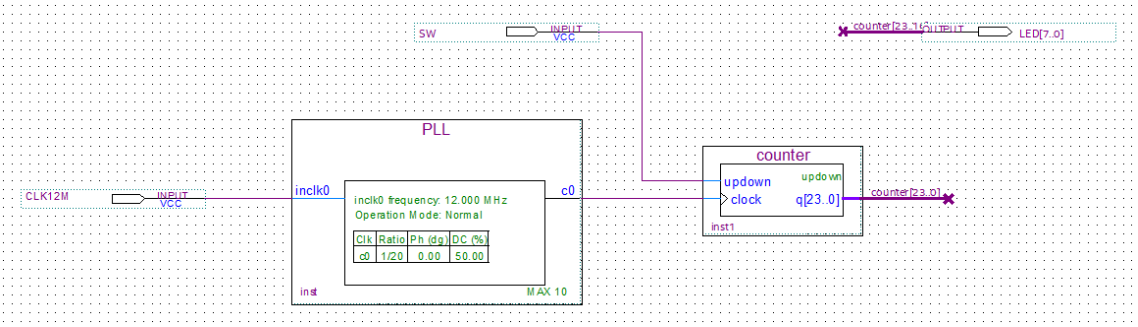
4.2.3.16 Right click on the bus line of the counter's output and select **Properties**.

4.2.3.17 Set the name of the bus to **counter[23..0]**.



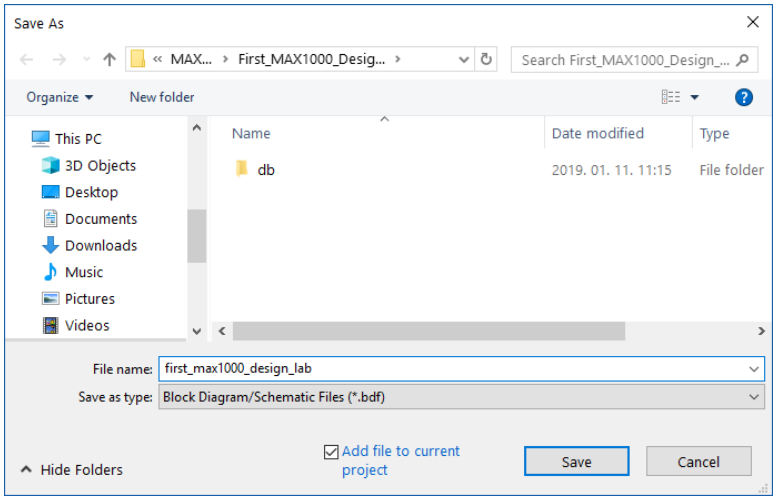
4.2.3.18 Click **OK**.

4.2.3.19 Do the same from 4.2.3.18 to 4.2.3.20 for the bus of the LED. The name of this bus is **counter[23..16]**.



4.2.3.20 Save your design by clicking on  button or **File → Save** and enter the following information.

- File name: **first_max1000_design_lab**
- Save as type: **Block Diagram/Schematic Files (*.bdf)**
- Make sure that **"Add file to current project"** option is checked.



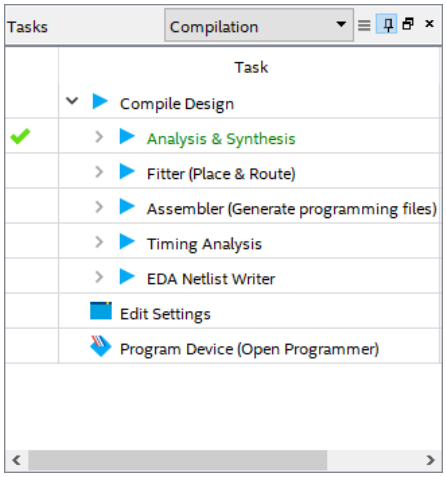
4.2.3.21 Click **Save**.

4.3 Compile design

4.3.1 Analysis and Synthesis

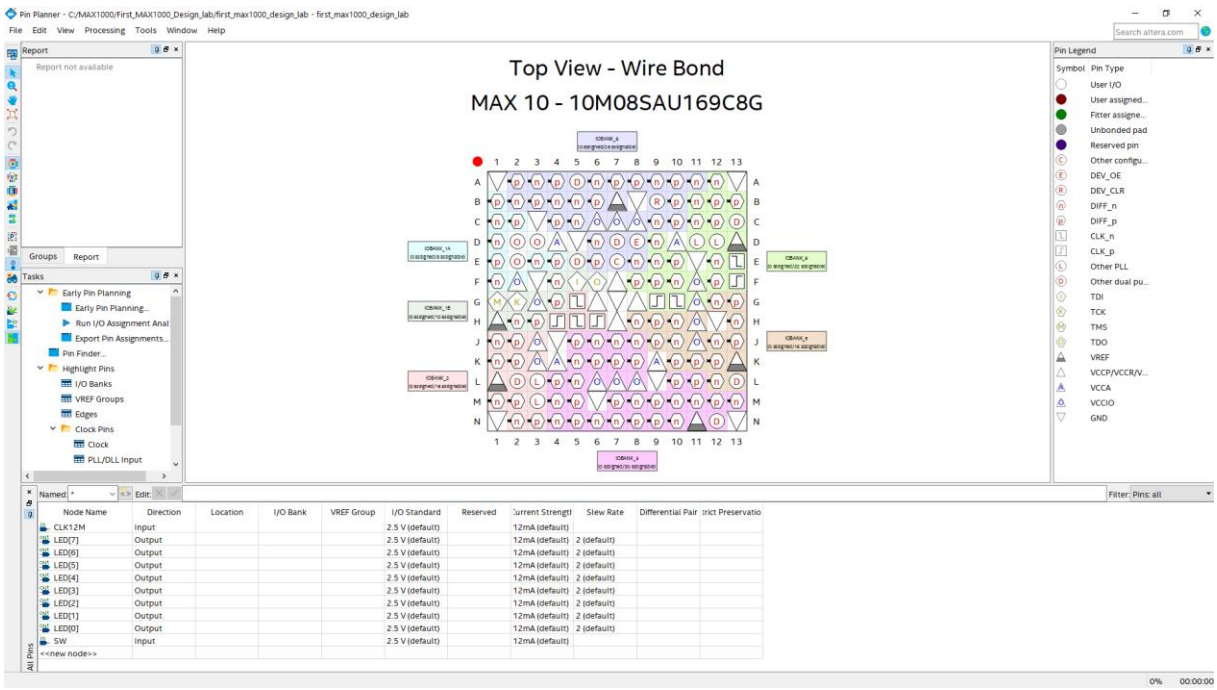
4.3.1.1 Run Analysis and Synthesis by clicking on button on the toolbars, or **Processing → Start → Analysis and Synthesis**.

There should be no errors. If there are errors, they should be fixed before continuing. If there are no errors the compilation task windows should look like this:



4.3.2 Pin Assignments

4.3.2.1 Open **Pin Planner** by clicking on button on the toolbars, or **Assignments → Pin Planner**.



4.3.2.2 In the bottom table, type **PIN_H6** in Location column of the CLK12M.

Node Name	Direction	Location	I/O Bank	VREF Group	I/O Standard	Reserved	Current Strengtl	Slew Rate	Differential Pair	trict Preservatio
CLK12M	Input	PIN_H6	2	B2_N0	2.5 V (default)		12mA (default)			
LED[7]	Output				2.5 V (default)		12mA (default)	2 (default)		
LED[6]	Output				2.5 V (default)		12mA (default)	2 (default)		
LED[5]	Output				2.5 V (default)		12mA (default)	2 (default)		
LED[4]	Output				2.5 V (default)		12mA (default)	2 (default)		
LED[3]	Output				2.5 V (default)		12mA (default)	2 (default)		
LED[2]	Output				2.5 V (default)		12mA (default)	2 (default)		
LED[1]	Output				2.5 V (default)		12mA (default)	2 (default)		
LED[0]	Output				2.5 V (default)		12mA (default)	2 (default)		
SW	Input				2.5 V (default)		12mA (default)			
<<new node>>										

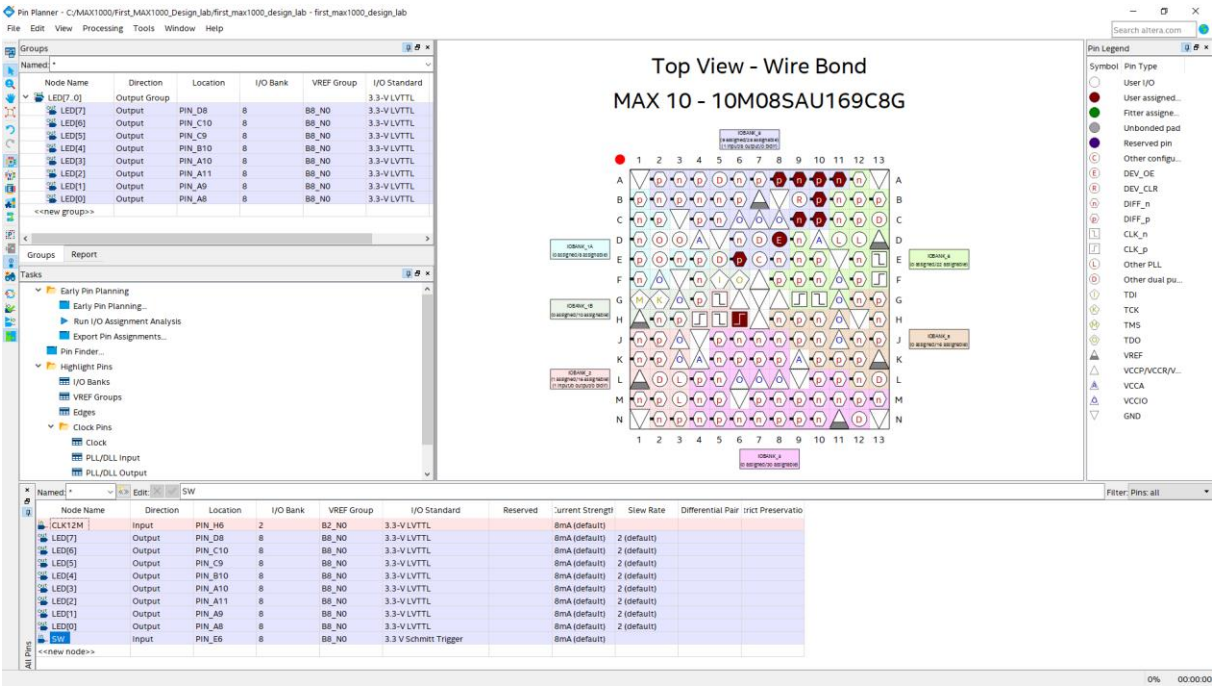
4.3.2.3 Repeat the previous step with the following assignments:

Node Name	Pin Location
LED[7]	PIN_D8
LED[6]	PIN_C10
LED[5]	PIN_C9
LED[4]	PIN_B10
LED[3]	PIN_A10
LED[2]	PIN_A11
LED[1]	PIN_A9
LED[0]	PIN_A8
SW	PIN_E6

Node Name	Direction	Location	I/O Bank	VREF Group	I/O Standard	Reserved	Current Strengtl	Slew Rate	Differential Pair	trict Preservatio
CLK12M	Input	PIN_H6	2	B2_N0	2.5 V (default)		12mA (default)			
LED[7]	Output	PIN_D8	8	B8_N0	2.5 V (default)		12mA (default)	2 (default)		
LED[6]	Output	PIN_C10	8	B8_N0	2.5 V (default)		12mA (default)	2 (default)		
LED[5]	Output	PIN_C9	8	B8_N0	2.5 V (default)		12mA (default)	2 (default)		
LED[4]	Output	PIN_B10	8	B8_N0	2.5 V (default)		12mA (default)	2 (default)		
LED[3]	Output	PIN_A10	8	B8_N0	2.5 V (default)		12mA (default)	2 (default)		
LED[2]	Output	PIN_A11	8	B8_N0	2.5 V (default)		12mA (default)	2 (default)		
LED[1]	Output	PIN_A9	8	B8_N0	2.5 V (default)		12mA (default)	2 (default)		
LED[0]	Output	PIN_A8	8	B8_N0	2.5 V (default)		12mA (default)	2 (default)		
SW	Input	PIN_E6	8	B8_N0	2.5 V (default)		12mA (default)			
<<new node>>										

4.3.2.4 Double click in the I/O Standard column for any ten pins to open a drop-down list and change the 2.5V (default) to the specific I/O standard.

Node Name	Pin I/O Standard
CLK12M	3.3-V LVTTL
LED[7]	3.3-V LVTTL
LED[6]	3.3-V LVTTL
LED[5]	3.3-V LVTTL
LED[4]	3.3-V LVTTL
LED[3]	3.3-V LVTTL
LED[2]	3.3-V LVTTL
LED[1]	3.3-V LVTTL
LED[0]	3.3-V LVTTL
SW	3.3-V Schmitt Trigger

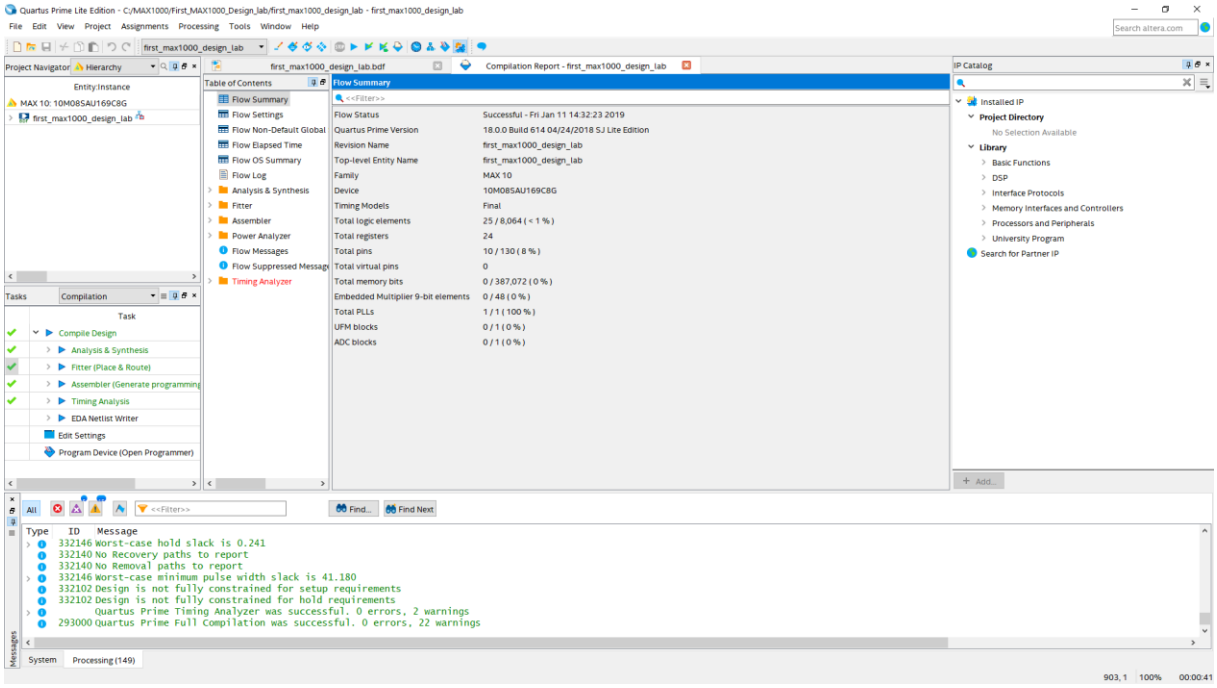


4.3.2.5 Close the Pin Planner, the settings are automatically saved.

4.3.3 Compiling the Design

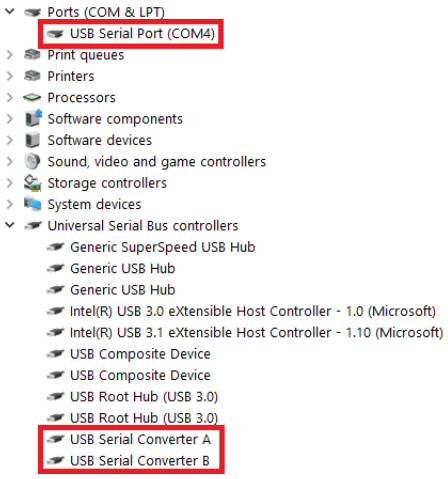
4.3.3.1 Start Compilation by clicking on button on the toolbars, or **Processing → Start Compilation**.

There should be no errors. If there are errors, they should be fixed before re-compilating. The 100% in the lower right corner or a green checkmark next to the Compile Design in the Compilation task window indicates that the compilation was successful.

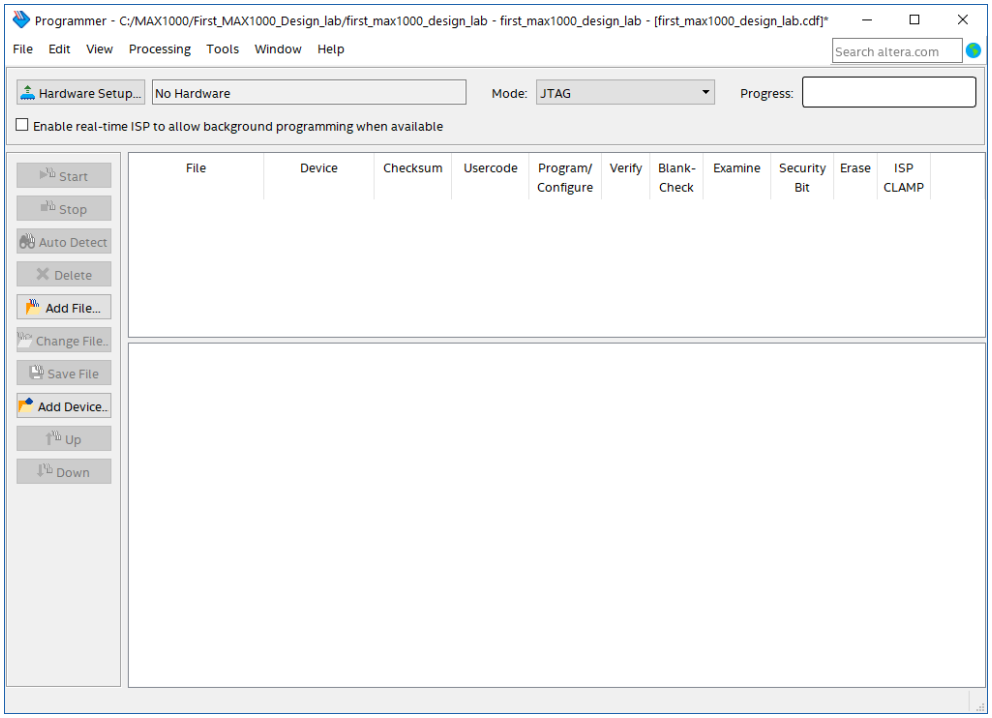


4.3.4 Configuration

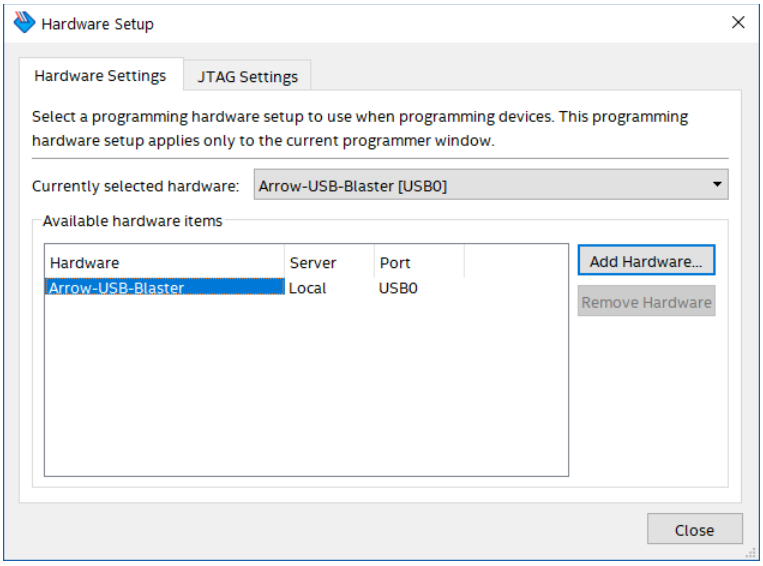
4.3.4.1 Connect your MAX1000 board to your PC using an USB cable. Since the Arrow USB Blaster should be already installed, the Window's Device Manager should display the following entries are highlighted in red (port number may differ depending on your PC):



4.3.4.2 Open the Quartus Prime Programmer from **Tools → Programmer** or double click on Program Device (Open Programmer) from the Task window.

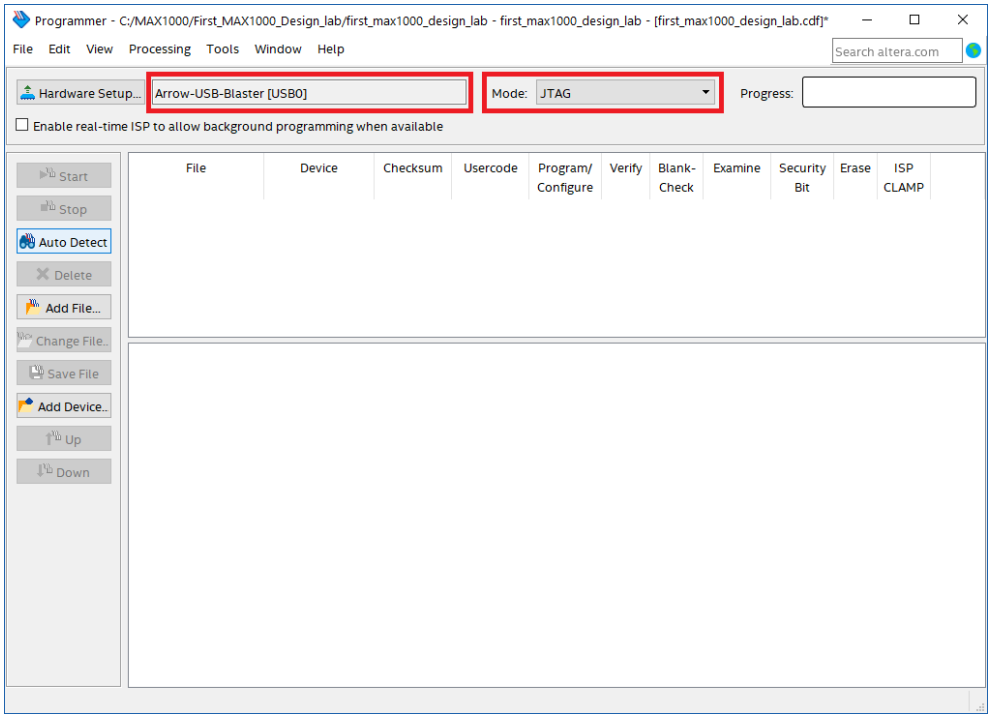


4.3.4.3 Click **Hardware Setup…** and double click **Arrow-USB-Blaster** entry in the Hardware Setup tab. The Currently selected hardware should now show Arrow-USB-Blaster [USB0] (depending on your PC, the USB port number may variant).



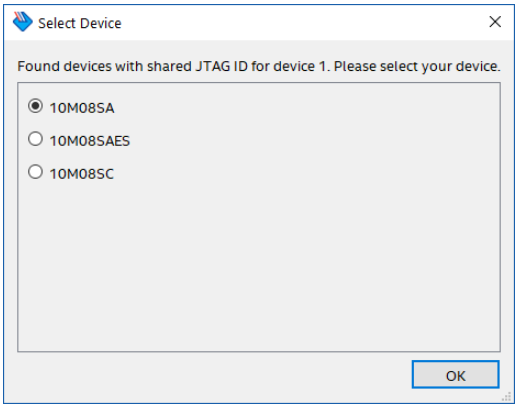
4.3.4.4 Click **Close**.

4.3.4.5 Make sure the hardware setup is Arrow-USB-Blaster [USB0] and the mode is JTAG. Click **Auto Detect**.



4.3.4.6 If the configuration has been added by default, you can skip the following steps and continue with the 4.3.4.11 point.

4.3.4.7 Select **10M08SA** device and click **OK** in the pop-up window.

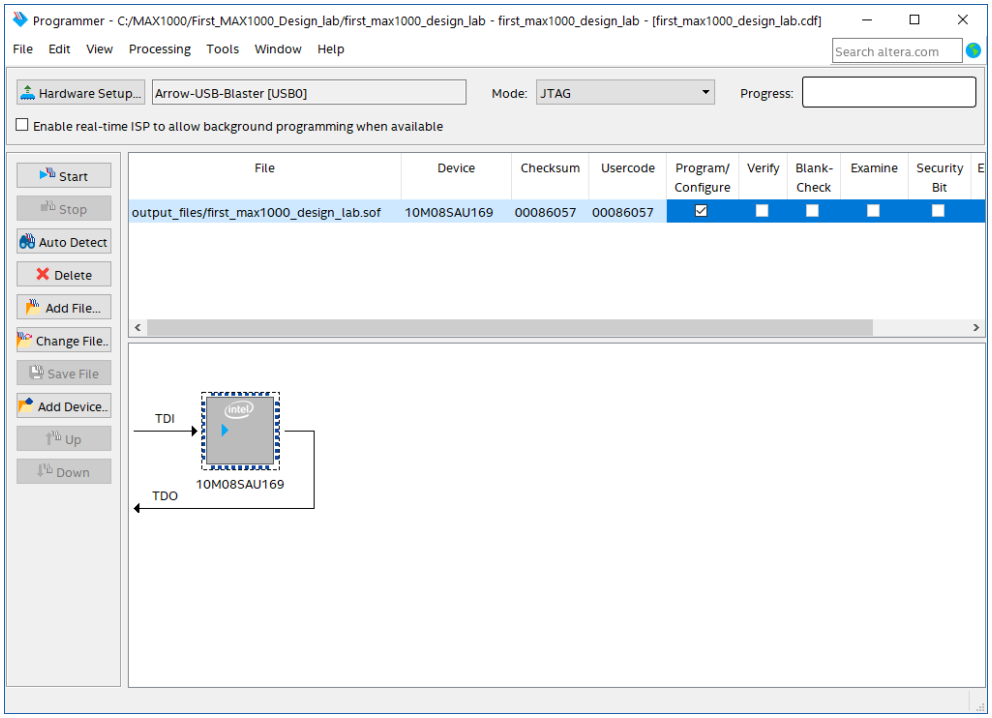


4.3.4.8 Click **Change File...** or double click <none> to choose the programming file.

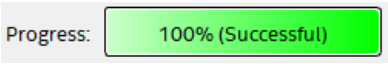
4.3.4.9 Navigate to **<project_directory>/output_files/** and select the **first_max1000_design_lab.sof** file.

4.3.4.10 Click **Open**.

4.3.4.11 Make sure the Programmer shows the correct file and the correct part in the JTAG chain and check the Program/Configure checkbox.



4.3.4.12 Click **Start** to program the board. When the configuration is complete, the Progress bar should show 100% (Successful).



4.3.5 Testing the design

4.3.5.1 On the board by default, the LEDs should now toggle in a counting sequence.

4.3.5.2 Push and hold the user, SW button to see that the LEDs counting sequence will be reserved.

4.3.5.3 Releasing the button, the direction of counting will be the same as before.

CONGRATULATIONS! YOU HAVE SUCCESSFULLY COMPLETED THE FIRST DESIGN LAB!

5 Revision History

Version	Change Log	Date of Change
V1.0	Initial Version	11/01/2019

6 Legal Disclaimer

ARROW ELECTRONICS

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