MAX® 10 Device Errata

2016.05.16

ES-1054 Subscribe Send Feedback

This errata sheet provides information about known device issues affecting MAX® 10 production devices.

Table 1: Issues

Issue	Affected Devices	Planned Fix
Configuration Failure on page 1 Intermittent configuration failure when configured to start up in fast or slow POR delay mode	All MAX 10 devices with date code prior to 1625	All MAX 10 devices with date code 1625 or later

Configuration Failure

Description

MAX 10 production devices shipped prior to date code 1625 may experience intermittent configuration failures. They may fail to enter user mode if the Power On Reset (POR) scheme is configured to operate in either **Fast POR delay** or **Slow POR delay** mode. When observed, devices may be power cycled to reconfigure or pulse low either the `nCONFIG` or the `nSTATUS` pins.

Designs configured to use the **Instant ON** mode of operation are not affected by this issue and will continue to operate without any problems.

Workaround

If your existing design POR scheme is configured to use either **Fast POR delay** or **Slow POR delay** modes, you need to modify it to **Instant ON** mode. Ensure your board power design meets the power up requirements listed below.

Table 2: Power Up Requirements for MAX 10 Devices

Power Supply Device Options	Power Rails	Maximum Ramp Rate Requirement (t_{RAMP})
Single Supply Devices	V_{CC_ONE}/V_{CCA}	3 ms
Dual Supply Devices	V_{CC}, V_{CCINT}, V_{CCD_PLL}, V_{CCA}, V_{CCA_ADC}	3 ms

For both options, ensure that all IO banks are powered up to nominal operating voltage when configuration completes. Refer to the *MAX 10 FPGA Configuration User Guide* for minimum configuration time specifications. If your board power design cannot meet the stated t_{RAMP} requirement, contact **Intel® Premier Support**.

Long Term Solution

Starting with shipments with date code 1625, MAX 10 devices have a modified power on configuration scheme that enables a simplified power on scheme. This gives you an easier method of configuring MAX 10 devices with the following benefits:

- Single power up scheme
- No power up sequencing requirements
- Maximum power supply rail ramp time increased from 3 ms to 10 ms
- Minimum power supply rail ramp time of 200 µs is now a recommendation rather than an absolute minimum
- No changes to either the die or the ordering part number (OPN)

Quartus® Prime Update

From Quartus® Prime software version 16.0 and onwards, the POR scheme option will be unavailable. This option will be removed in subsequent Quartus Prime software versions when a single, simplified power on scheme is introduced.

Note: Ensure that you select the **Instant ON** POR scheme if you are using a Quartus Prime software version prior to 16.0. If you select **Fast POR delay** or **Slow POR delay**, this may result in failure even if the device has a date code of 1625 or later.

Status

Affects: All MAX 10 devices with date code prior to 1625

Status: Planned configuration setting update in all MAX 10 devices with date code 1625 or later

Related Information

MAX 10 FPGA Configuration User Guide

Revision History for MAX 10 Device Errata

Date	Version	Changes
May 2016	2016.05.16	Clarified the workaround in the "Configuration Failure" section.
May 2016	2016.05.03	Initial release