Guide to Passing LVS (Layout vs. Schematic)
A Cadence Help Document

Document Contents

Introduction

Cadence Tutorial B describes the steps for running an LVS (Layout vs. Schematic) comparison to verify the layout and schematic for a cell exactly match. This document describes techniques for tracking down and fixing problems that cause LVS to fail or not pass. Passing LVS for a circuit is critical to ensure the physical design will perform as intended when the circuit is fabricated. However, passing LVS can be one of the most difficult and time consuming tasks of the design flow because often the problems are hard to track down. The Cadence LVS tool provides several sources of information which can be used to find and debug the problems that caused LVS to fail or not pass. This document briefly describes some of these information sources and provides some techniques for solving common LVS problems.

Golden Rules

- Always verify the operation of a circuit via simulations at the schematic level before attempting to layout the cell. LVS only verifies the schematic and layout match, so if the schematic does not work the layout will not either. If the schematic does not function properly, there is no reason to spend time debugging the LVS.
- Always design in a hierarchical fashion, building smaller (lower level) cells before constructing larger circuit blocks from the lower level cells.
- Always pass LVS on lower level cells before attempting to check LVS on a higher-level cell. If the lower level cells do not pass LVS, it is much easier to debug them on their own than after you have added the cell to a higher level circuit.
- Always re-check LVS on a cell if you make any changes to the schematic or layout.
- If you modify a layout to correct a problem found in an LVS check, always re-extract the layout and save it before running the LVS checker again.

Understanding the LVS Output File

The LVS Output File provides a lot of useful information about a cell, including the number of devices, nets, etc. within the cell. It also lists some results that can be useful in tracking down errors that caused LVS not to pass. An example LVS Output File for a cell that has passed LVS is given below. The five color-coded and numbered subsections of the LVS output file are:

1. The Netlist summary for the layout and the schematic.

- This is a very important indicator of problems. If the netlists match, as they do above, you will notice that the numbers for the Nets, Terminals, NMOS, and PMOS all match. A quick description of these:
    - NETS – These are the wires or connections in a device. In your inverter the output which connects the drain of you PMOS to the drain of your NMOS is considered an NET.
    - Terminals – These are the pins in your design. These Numbers must always match completely.
    - NMOS – The number of NMOS transistors in your design
    - PMOS – The number of PMOS transistors in your design

2. Terminal correspondence points.
    - A list of the terminals that match in your Layout and your schematic. **ALL Pins including vdd! and gnd! must show up.** If all pins are not showing, your LVS probably will not show a match.

3. Netlist Summary
    - Provides a basic comparison summary of the netlists for your layout and schematic.

4. Probe file output for your schematic.
    - Provides information about your schematic if there is not a match. If the netlists do match, the file will look like the example given above.

5. Probe file output for your layout.
    - Provides information about your layout if there is not a match. If the netlists do match, the file will look like the example given above.

Example: Passed LVS Output File

```
@(#)$CDS: LVS version 4.4.6
08/30/2001 16:57 (cds11612) $

Like matching is enabled.
Net swapping is enabled.
Using terminal names as
correspondence points.
Compiling Diva LVS rules...

1.
    Net-list summary for
/egr/classes/ece410/dotsonna/caden
ce/LVS/layout/netlist
       count
      24          nets
      7           terminals
      17          pmos
      17          nmos

    Net-list summary for
/egr/classes/ece410/dotsonna/caden
ce/LVS/schematic/netlist
       count
      24          nets
      7           terminals
      17          pmos
      17          nmos

2.
Terminal correspondence points
        1   CLK
        2   D
        3   Q
        4   QBAR
        5   R
        6   gnd!
        7   vdd!

3.
The net-lists match.

                        layout
schematic
                        instances
      un-matched        0     0
      rewired           0     0
```

```
size errors          0     0
pruned               0     0
active               34    34
total                34    34

                       nets
un-matched           0     0
merged               0     0
pruned               0     0
active               24    24
total                24    24

                     terminals
un-matched           0     0
matched but
different type       0     0
total                7     7
```

4.

```
Probe files from
/egr/classes/ece410/dotsonna/caden
ce/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:
```

5.

```
Probe files from
/egr/classes/ece410/dotsonna/caden
ce/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:
```

Solutions to Common LVS Problems

LVS Fails

A very common problem is that your LVS will fail. If this happens you will need to know why. The following steps will help you to identify the issue.

1. Once the LVS comparison fails, click OK on the window that pops up.

2. Click the Output button on the LVS window.

3. Click OK in the next window that pops up.

4. Next a “Display Run Information” window will pop up. In this window, click the LogFile button.

5. A LogFile will then pop up. This file contains some information about the LVS run and why it failed. The reason for failure is listed towards the bottom of the file. Many times, a schematic or a layout was not saved or needs to be in order for the comparison to complete.

Number of Terminals do not Match

The number of terminals in your layout does not match the numbers for your schematic. (This can be seen at the top of the output file in the netlist summary section). Below are some possible conditions and solutions.

1. You forgot to include jumper pins for your vdd! and gnd! Rails. In this case your LVS will still pass, but your extracted circuit will not function correctly in simulations, so this problem must be fixed.
2. You forgot to include all pins in your layout. Maybe one of the inputs or outputs was not made in the layout or it was made improperly.
3. You did not name the pins in your layout ***EXACTLY*** the same as their counterparts in the schematic. For example, a pin called Vdd! in the layout view will not match a pin called vdd! in the schematic view.

Number of Nets do not Match

The number of nets in your layout does not match the number for your schematic. (This can be seen at the top of the output file in the netlist summary section)

1. If the number of nets given for your layout is higher than that for your schematic, then there are some connections between points in your layout that need to be made. Fixing this can sometimes be very difficult. The "Layout Probe File Output" section in your output file usually contains some useful information on this.

   - The first scenario for this situation is that your probe file output will say something like **"? Net /net 027 merged with /R."** These problems are usually very easy to fix. What the above line means is that net 027, which is some internal connection in the circuit, needs to be connected to terminal R. This can be confusing because you might assume *merged* means they are already connected, but in the Cadence LVS output file this means they need to be connected.

   - The second scenario for this situation is that your probe file output will say something like **"terminal gnd! in layout fails to match any terminal in the schematic"** These problems are usually not so easy to fix, if more than one terminal is not matching. In the given case, a transistor that should be connected to gnd! probably is not connected, so you would need to inspect your layout and find where a connection needs to be made. If you have multiple terminals that are not matching, inspect each terminal listed very carefully to ensure that all connections are made to the appropriate points in your layout. This is never an easy task and can be quite time consuming, so use patience and try and locate your mistake.

2. If the number of nets given for your layout is lower than that for your schematic, then there are some connections between points in your layout that are made and should not be. Fixing this can again be very difficult. The "Schematic Probe File Output" and "Layout Probe File Output" sections in your output file usually contain some useful information on this.

   - The first scenario for this situation is that your **Schematic** probe file output will say something like **"? Net /net 027 merged with /R."** As above, these problems are usually very easy to fix. What the above line means is that net 027, which is some internal connection in the circuit, needs to be connected to terminal R in your schematic view. **However, remember that we are assuming that you have a correct functioning schematic, so the issue is still with the layout.** You need to go into your layout and find the connection that you made between these points and then delete it.

- The second scenario for this situation is that your Layout and Schematic probe file outputs will say something like **"terminal gnd! in layout fails to match any terminal in the schematic"** Again, these problems are usually not so easy to fix, if more than one terminal is not matching. In the given case, a transistor that should be connected to gnd! probably is not connected, so you would need to inspect your layout and find where a connection needs to be made. If you have multiple terminals that are not matching, inspect each terminal listed very carefully to ensure that all connections are made to the appropriate points in your layout.

Tools and Techniques for Passing LVS

If you have taken care while laying out your circuits, problems usually fall under the scenarios given above. But sometimes certain errors are still difficult to find from the information in the LVS Output File, so below are a list of tools to help you locate other problems in your layout.

LVS Error Display

If you have a netlist that does not match, you can visually show the errors on your extracted layout view. This can help you find the error so you can fix the problem in your layout.

1. To see this option, click LVS Error Display button in the LVS window.
2. This is a tip that will help you to see the errors on your extracted view. Change the Error color to be highlighted, by clicking on that button, to white. This will make it much easier to see the errors on your extracted view. The default color is pink and that is sometimes hard to see.
3. After you have set this up, click the next button and your errors will be listed in the Error display window and highlighted on your extracted window at the same time.

Shorts Locator

Many times the Output file will let you know that either connections are made that should not be or connections should be made. Most of the time some net name is given and you have no idea what that net is or how to find it, so this tool can be quite helpful.

1. Open the Extracted view for the cell on which you are running LVS.
2. In the extracted view window, click verify on the menu bar and then click on Shorts in this menu.
3. The Shorts Locator window will then pop up. If it does not pop up immediately, click OK on any small pop-ups until it does appear.
4. In the shorts locator window, type in the number of the net you wish to find and click the run button. On your extracted view, the net will be highlighted in orange so you will be able to see it pretty easily. If you wish to find a different net when you are finished looking at the first, click the finish button in the shorts locator window and then just type in the number of the next net you wish to find and click the run button.