Cadence Tutorial B: Layout, DRC, Extraction, and LVS
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Introduction

This document is one of a three-part tutorial for using CADENCE Custom IC Design Tools (ver: IC445) for a typical bottom-up digital circuit design flow with the AMI06 process technology and NCSU design kit. This tutorial demonstrates how to complete the physical design (layout), design rule check (DRC), parameter extraction, and layout vs. schematic (LVS) using the Cadence tools. These operations are performed step-by-step to complete the design of an inverter cell, began in Tutorial A, using the design rules for the AMI C5N (λ=0.3) fabrication process. Techniques and tips for using Cadence layout tools are presented.

It is important that you always have a verified functional schematic before beginning layout. If the schematic is not correct, the layout will also be incorrect. As shown in the figure below, the layout should contain the same pin names and the transistors must be made the same size as those in the schematic. In this tutorial the nMOS and pMOS transistors both use the minimum size transistor dimensions (W = 1.5um and L = 0.6um) for the AMI C5N process.

Design rule illustrations for the AMI C5N process can be found at:
http://www.mosis.org/Technical/Layermaps/lm-scmos_scn3m.html
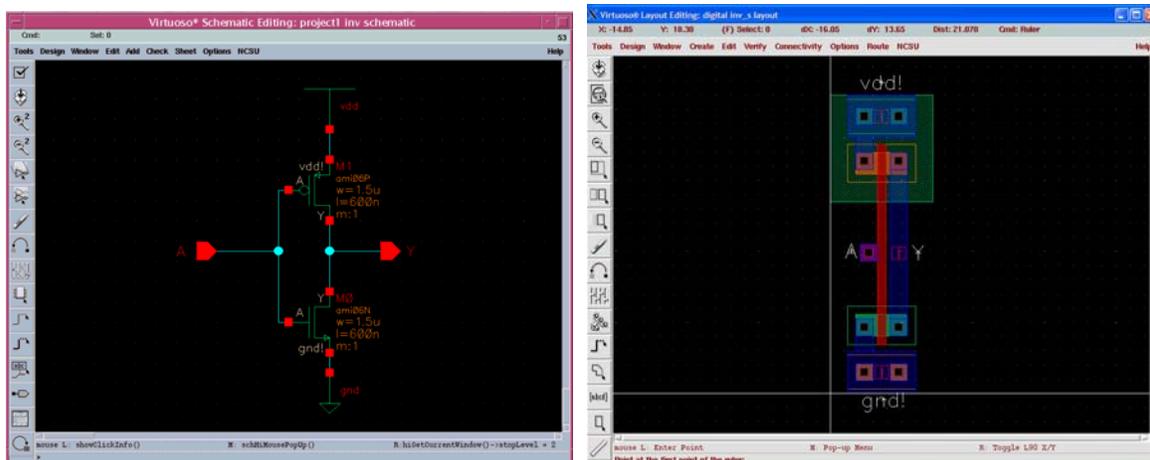
Create Layout Cellview

The custom design process is discussed briefly in Tutorial A. We will assume that you have logged on and started Cadence Design Tools, and that you already have created a design library and the schematic of the inverter. Please refer to Tutorial A if you have not done so.

STEP 1: Create a new layout view

- From the Library Manager window, Select File => New => Cellview.
- A dialog box will appear prompting you for the library, cell, and view names. Make sure that the library name corresponds to your design library that you have used in Tutorial A. Enter *inv* as the *Cell Name* and choose **Virtuoso** as the *Design Tool*. The View Name will be automatically set to *layout*.

Two design windows (Virtuoso and LSW) will pop-up. The Layer Selection window (LSW) (small window on the left in the figure below) lets the user select different layers of the mask layout. Virtuoso will always use the layer selected in the LSW for editing. The LSW can also be used to determine which layers will be visible and which layers will be selectable. To select a layer, simply click on the desired layer within the LSW.

Virtuoso is the main layout editor of Cadence design tools. Commonly used functions can be accessed by pressing the buttons/icons of the *toolbar* on the left side of this window. There is an *information line* at the top of the window which shows (from left to right) the X and Y coordinates of the cursor, number of selected objects, the distance traveled in the X and Y directions, the total distance, and the command currently in use. This information can be very handy while editing. At the bottom of the window, another line shows the function of each mouse button. Note that the mouse button functions will change according to the command you are currently executing. The default mouse mode is *selection*, and as long as you do not choose a new mode you will remain in that mode. To quit from any mode or command and return to the default selection mode, the 'ESC' key can be used.
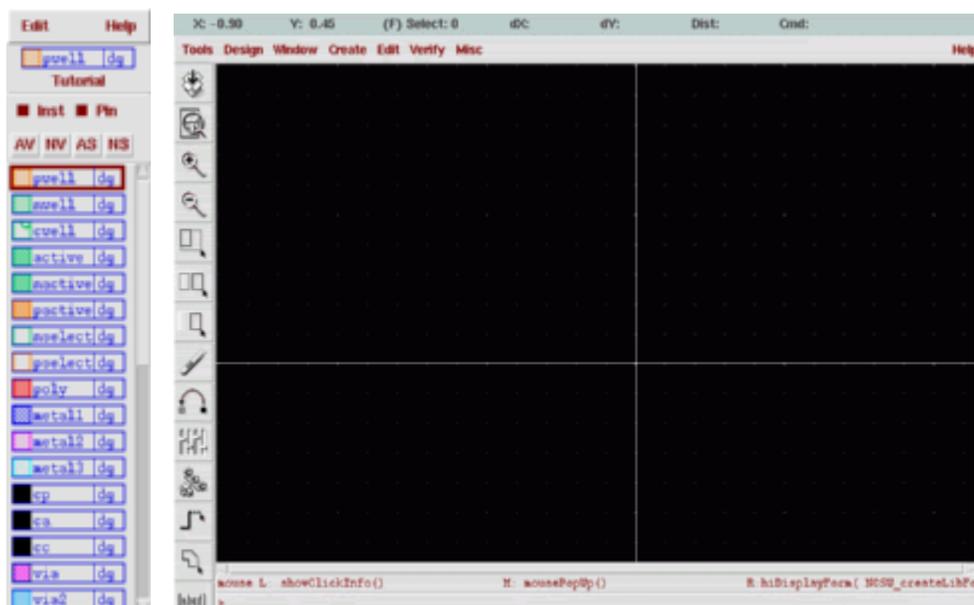
STEP 2: Display Setup

Before drawing on a new cell you should always setup the grid properties.

- In the Virtuoso Layout Editing window, select Options => Display (or type 'e') to bring up the Display Options window shown below.

- Type in the following settings: *Minor Spacing* **0.3**, *Major Spacing* **1.5**, *X Snap Spacing* **0.15**, *Y Snap Spacing* **0.15**, then click OK. It is also very important to note that the grid spacing is in micrometers (um) and not in lambda (λ).
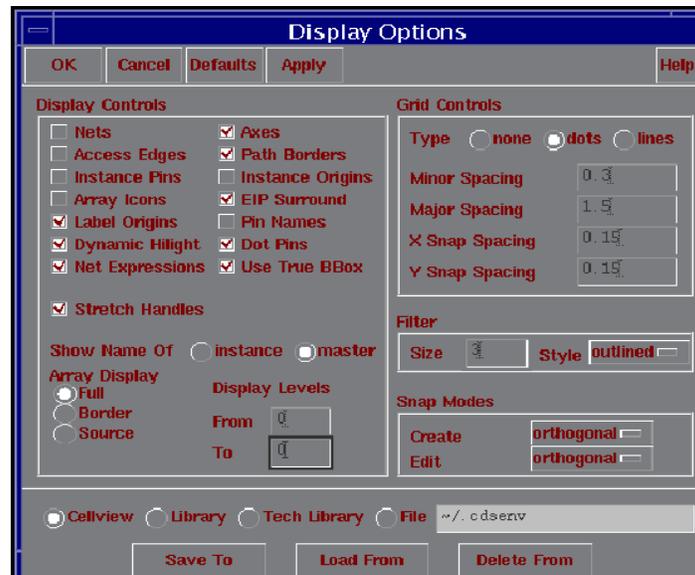
STEP 3: Creating VDD (Power) and GND Rails

Now we are ready to start laying out our design. The first parts we will create are the power and ground rails for our inverter. Usually a circuit will consist of a large number of cells, all of which need power and ground connections. Therefore it is common to design cells with the same spacing between the power and ground so that they can easily be connected together when the cells are placed side by side. This vertical spacing is called the cell *pitch* and it is generally standardized for all cells in the same library to facilitate combining cells in higher-level circuits. For this tutorial the power and ground rails will be made 3um (10 lambda) wide using the Metal-1 layer and the standard cell pitch (height from bottom of the GND rail to top of the VDD rail) will be 21um (70 lambda).

Now draw the Power Rail and the Ground Rail in Metal-1 as shown below.
- Select *metal1 dg* layer from the LSW. In the rest of the tutorial, always use the *dg* layers for your layouts unless otherwise specified.
- In the Virtuoso Layout Editing window click Create => Rectangle (or select the *create rectangle* tool from the toolbar).
- Move your mouse to the *cell origin*, where the horizontal and vertical guidelines intersect. Check the information bar at the top of the screen to make sure you are at the right location (0,0). **Click** on this point.
- **Move** the mouse up and right to create a rectangle. Use the data in the information bar to move your mouse to the point that is 4.8um horizontal and 3um vertical from the origin (4.8 x 3 um is always in the X direction by the Y direction, respectively). **Click** on this point to create the Metal-1 rectangle which will be your ground rail.
- Repeat these steps to draw the VDD rail 21um (70 lambda), top to bottom, above the GND rail. Read the *Useful Editing Tools* section below.
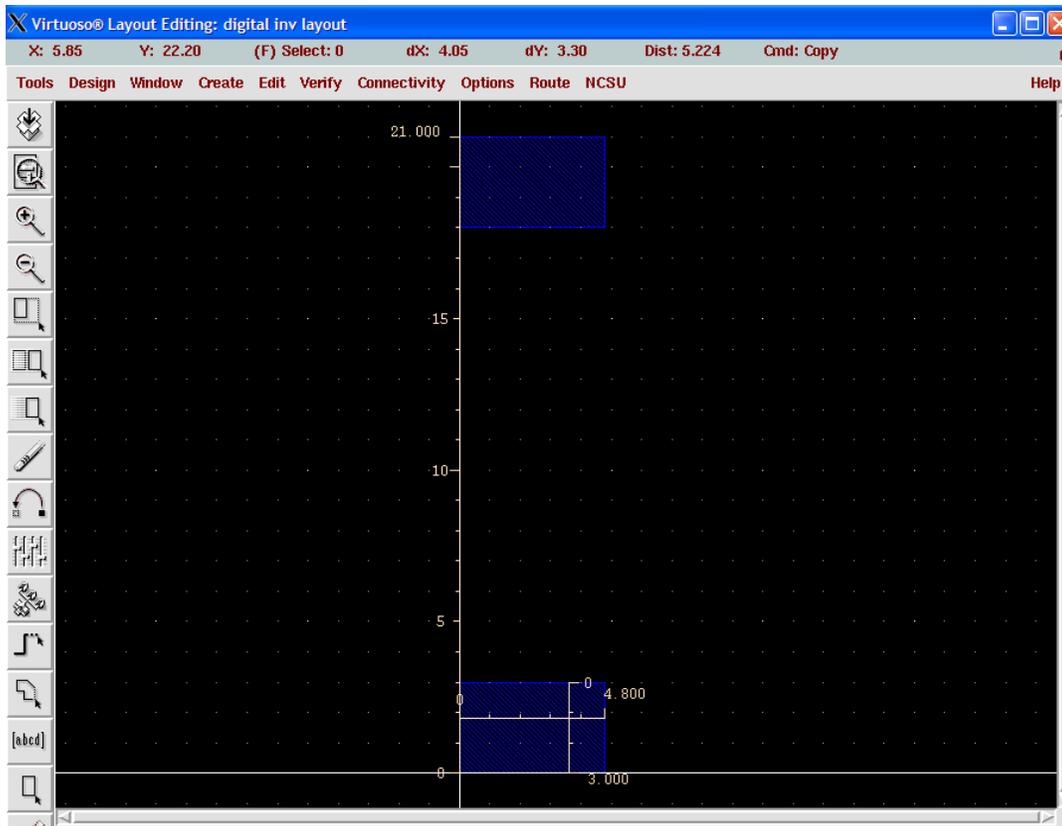
Useful Editing Tools

Ruler: The *ruler* is very useful to place objects and measure the distance between the objects.

- To start the ruler, **click** on the *ruler* icon at the bottom of the toolbar (shortcut key is 'k').
- Click the start and end point in the window; a ruler is created showing the distance between the two points.
- Hit the 'ESC' key to exit the ruler command.
- To remove all ruler markers on your layout, press 'Shift+k'.

Move: If you place the objects on the wrong place, you can use ***move*** function to adjust the location of the object.

- Select Edit => Move (or click on the *move* icon on the toolbar), (shortcut key is 'm').
- A window will pop-up. The *Snap Mode* is an interesting option. When this is in *orthogonal* setting, the copied objects will move only along one axis. This is a good feature to help you avoid alignment problems.
- When you have finished the move operation, hit the 'ESC' key to exit the move command.

Copy: If you want to create the same object repeatedly, you can use the ***copy*** function.

- Select Edit => Copy and the copy dialog box will pop-up (shortcut key is 'c').
- Click in an object. Notice that an outline of the object will attach to your mouse cursor. Move our mouse and click when you are satisfied with the location to place a copy of the object.

Delete: If you want to delete an object you have drawn:
- Place your mouse over the object and left-click to select it.
- Press the ***Delete*** key on the keyboard.

Undo: When you make a mistake (accidentally delete a component, etc.), you can undo the action by click on the Undo icon in the toolbar (shortcut key is 'u').

STEP 4: Draw an nMOS Active Layer
Now we need to add an nMOS transistor to the layout of the CMOS inverter. Normally the pMOS transistors are at the top near the VDD rail and the nMOS transistors are at the bottom of the layout near the GND rail. From the schematic we know that the nMOS transistor has a channel *width* of 1.5um. The width of the transistor (W) will correspond to the width of the active area. We want to draw a horizontal transistor so the channel width will be measured top-to-bottom of the active layer (Y-dimension of the information bar).
- Select ***nactive*** layer from the **LSW.**
- In the Virtuoso Layout Editing window select Create => Rectangle
- Draw a rectangle that is 3.6um x 1.5um. Place the left bottom corner of the box at (0.6, 3.9) and click once. Then move the cursor to (4.2, 5.4) and click again.

STEP 5: The Gate Poly
We will use a vertical polysilicon rectangle to create the gate of the nMOS transistor. Note that the *length* of the transistor channel (L) will be determined by the width of this poly rectangle.
- Select ***poly*** layer from the **LSW.**
- In the Virtuoso Layout Editing window draw poly rectangle that is 0.6 x 2.7 um over the center of the *nactive* as shown in the figure below. Start drawing the poly rectangle 1.5um from the left side and 0.6um above the top of the active layer.
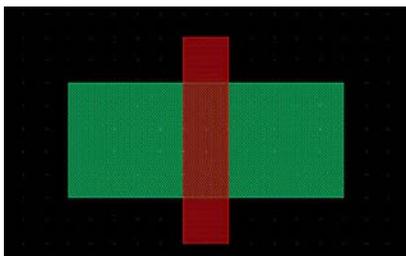
STEP 6: Making Active Contacts
Active Contacts provide a connection between the Metal-1 layer and the Active layer, which in this case is the drain and source regions of the nMOS transistor.

- Select the *cc* layer from the LSW**.**
- In the Virtuoso Layout Editing window draw a box that is 0.6x 0.6 um within the active area. Start drawing the contact at 0.3um away from the bottom-left corner of the *nactive* layer.
- Draw the second contact on the right side of the *nactive* layer as shown below. As set by the Design Rules, the contacts must be at least 0.3um from the edge of the active layer. You might want to use the Copy command (see *Useful Editing Tools* section above) to simplifiy this procedure.
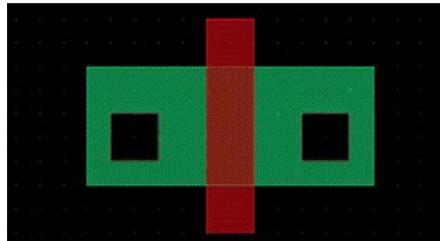
STEP 7: Covering Contacts with Metal-1

The Active Contact layer defines where a hole will be formed in the oxide that separates the active region from the Metal-1 layer. To complete the contact, we must ALWAYS cover the contact with a Metal-1 layer.

- Select layer *Metal-1* from the **LSW.**
- In the Virtuoso Layout Editing window draw a 1.2um square to cover each contact.
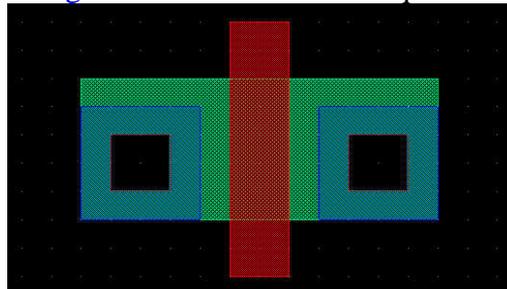
> **Note**: Metal-1 must extend over the contact in all directions by at least 0.3um (1 lambda).

STEP 8: Create N-Select Layer

Each diffusion (active) area must be specified as being of n-type or p-type. This is accomplished by a defining the window of n-select (or p-select) around each n-type (or p-type) transistor. Since we are making an nMOS right now, we will choose the *nselect* layer.

- Select *nselect* layer from the **LSW.**
- Draw a rectangle extending over the active area by 0.6um (2 lambda) in all directions.

This completes the nMOS transistor, which should look like the following figure.
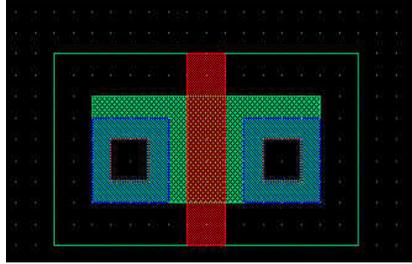
STEP 9: Drawing PMOS

Repeat steps 4-8 to make a pMOS transistor at the top of your cell, just below the VDD power rail. The only difference between drawing nMOS and pMOS is that you will be using *pactive* and *pselect* layers in place of the n-type layers specified in steps 4-8. Place the pMOS active the same distance from the VDD rail as your nMOS active was from the GND rail.

STEP 10: Drawing the N-Well

The selected process, AMI C5N, uses a p-type substrate, where nMOS transistors can be formed, and requires an n-well, where pMOS transistors can be formed. We must add an n-well to our cell to form an local n-type substrate (body terminal) for pMOS transistors.

- Select the *nwell* layer from the **LSW.**
- Draw a large n-well rectangle around the *pactive* area. The n-well must extend over the pMOS active area by a large margin, at least 1.8um (6 lambda). Align the top side of the nwell to the top of the VDD rail, as shown below.
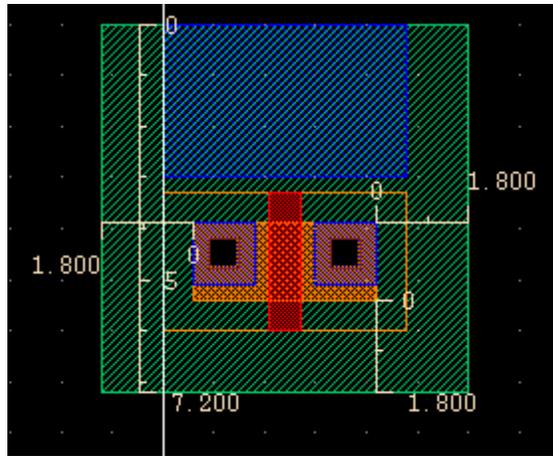
STEP 11: Create Substrate/Well Contacts (plugs)

The body terminals of the nMOS and pMOS transistors are the substrate and n-well, respectively. These terminals must be tied to the proper supply rail, substrate to GND and n-well to VDD. To simplify this connection, we can place Active Contacts directly on the existing supply rails. This will require adding active, contact, and select layers on top of the existing metal-1 layer as shown in the figure below.

- Select the *pactive* layer from the **LSW**
- Draw a 1.2um x 1.2um square placed in the center of the GND rail directly beneath the Active contact on the nMOS transistor. Repeat to add a contact beneath the second nMOS active contact.
- Select the *cc* layer from the **LSW** and place 0.6um x 0.6um contacts inside the pactive squares.
- Select *pselect* layer from the LSW and draw a box extending over both *pactive* squares by 0.6um on each side.
- Repeat this process using complementary layers (nactive, nselect) to add n-type active contacts to the VDD power rail.

Notice the active contacts on the GND rail are p-type since they connect to the p-type substrate and they are n-type on the VDD rails since they connect to the n-type n-well. If we were to switch these layers we would make diodes rather than ohmic (low resistance) contacts.
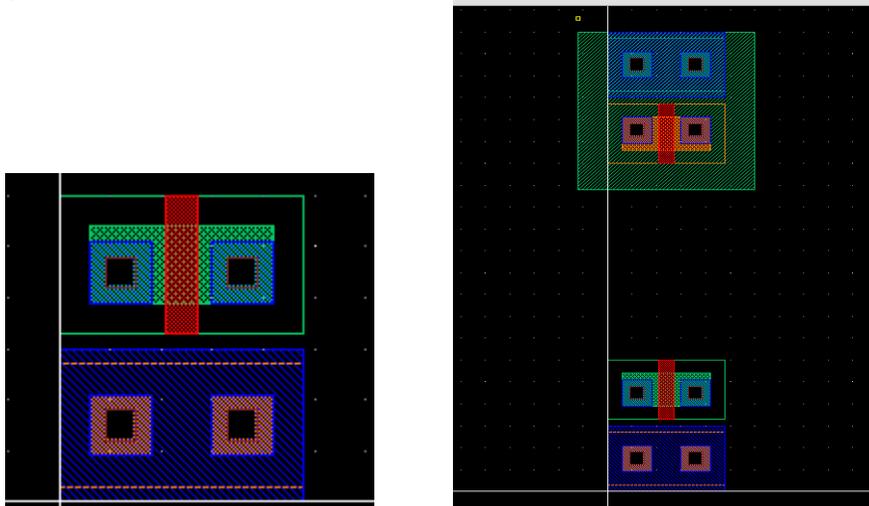
STEP 12: Connect Transistor Nodes to Match Schematic and Form the Inverter
- Select *poly* layer from the **LSW**.
- Draw a rectangle to connect the poly gate inputs of nMOS and pMOS transistors.

Note: To connect polygons of the same layer (eg., poly) you simply need to add another polygon that makes contact to each of the original layers. If the layers touch or overlap, they will form a continuous shape for fabrication.
- Select layer *Metal-1* from the **LSW**.
- Draw a rectangle to connect the source of the nMOS to GND rail. In this tutorial, the left side of the MOS is the source, and the right side is drain.
- Draw a rectangle to connect the source of the pMOS to VDD rail.
- Draw a rectangle to connect the drains of the nMOS and pMOS transistors together. This is the inverter output node.

STEP 13: Make All I/O Nodes Available in Metal-1
As a standard practice that will help when connecting multiple cells (logic gates), we need to ensure that all of our input and output nodes have a connection in *Metal-1*. For our inverter, the output is already in Metal-1, but the input (the node that links the gates of both transistors) is only in poly. We will make a connection to Metal-1 on the input by adding a poly-to-metal contact.
- Draw a 1.2 x 1.2 um square of *poly* extended from the existing poly away from the output metal (see figure below).
- Add a contact (0.6um x 0.6um square in the *cc* layer) in the center of the new poly square.
- Draw a *Metal-1* square (about 1.2 x 1.2 um) that overlaps the poly box.
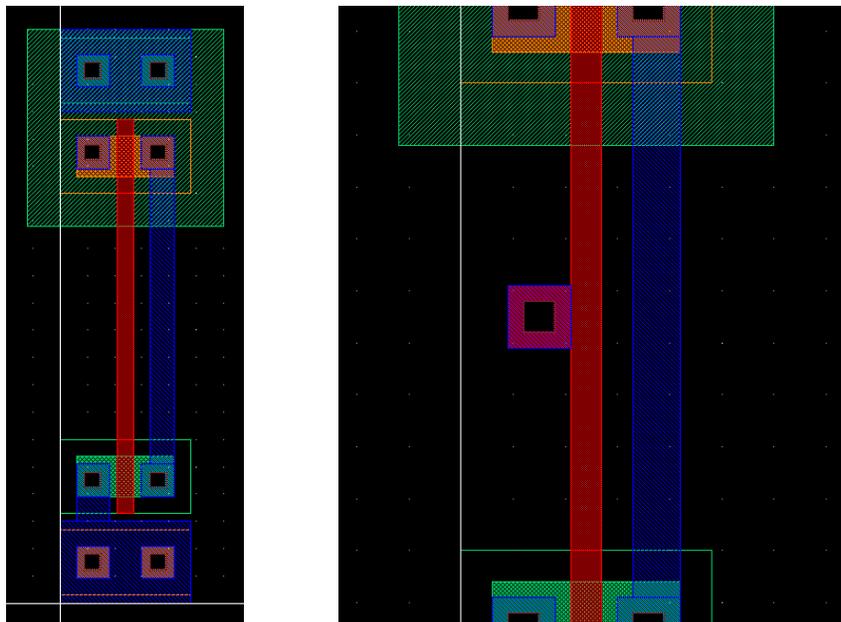
(left) Connected input and output nodes and (right) Poly-to-Metal contact on the inverter input.

STEP 14: Add Pins to the I/O Nodes
Now we need to assign pin names to the power, input, and output nodes.

- In the Virtuoso Layout Editing window select Create => Pin to open the Create Symbolic Pin window. Using this window we will first set the global power pins then the input and output.
- In the *Terminal Names* field, enter **vdd! gnd!** which are the names of the two global power pins. Put both names in this field, separate by a space, and be sure to include the '!'.
- Check **sym pin** and **Display Pin Name**. In *I/O Type* select **jumper**. For *Pin Type* select **metal1**.
- In the Virtuoso Layout Editing window, move the mouse over the VDD rail of the inverter. Be sure to place your mouse over *metal-1* layer and not other layers (e.g., *active*) on the VDD rail. Click on the middle of the VDD rail to place the pin. Click again to place the symbol vdd! -- you may move the mouse prior to clicking to place the name in any location.
- Now move the mouse to the GND rail, place the gnd! pin the same way you placed vdd!. Note that because you entered both names (vdd! and gnd!) as Terminal Names, you can place both in the same order you entered the names. You can use this same procedure to place multiple pins OF THE SAME TYPE (power/jumper, input, output).
- Go back to the Create Symbolic Pin window and input pin name *A* in the *Terminal Names* field. Change the *I/O Type* to **input**.
- In the Virtuoso Layout Editing window, move the mouse over the middle of the input *poly* layer and place the pin.
- Repeat the process to place the output pin on the output *metal-1*. Use *Y* in *Terminal Names* and **output** in *I/O Type*.

Now we have the final layout of an inverter! See figure below.
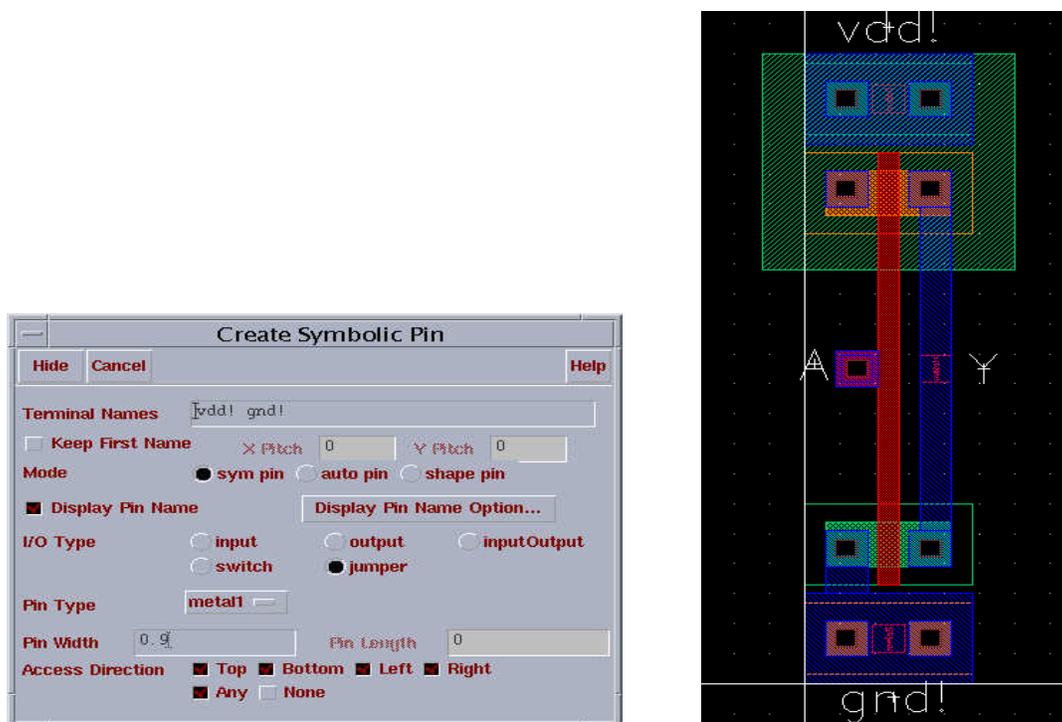
(left) Create pin window and (right) final inverter layout.

STEP 15: Minimize the Width of the layout

The width of a layout is defined as the distance from the left edge of VDD/GND rail to the right edge of that same rail. To ease the placement of cells in a row without violating the design rule, the VDD and GND rails need to extend beyond the outermost poly, active, or metal1 polygon in the layout by 2λ. nwell and select layers are not subject to this rule. As an example, in the inverter layout, the furthest features are the active regions transistors.

- In the Virtuoso Layout Editing window select Edit => Stretch to extend the VDD/GND rail.
- Select the edge (left or right side) of the VDD/GND rail and drag the edge to the proper place. Make sure they are just 2λ extend over the active layer.
- *Note: If you have followed this tutorial exactly, your inverter layout should already be sized correctly. In future layouts, you will need to carefully follow these guidelines to ensure that you have met the layout width requirements.*
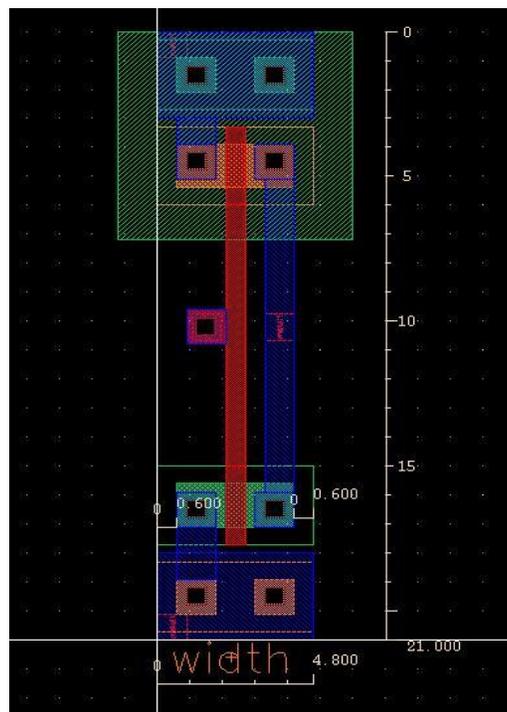
Useful skill: As layouts get more complex, you may find it useful to view only specific layers rather than all of them. This will allow you to see exactly what layers are present which can be difficult when many layers are placed on top of each other. Here's how this is done.

- From **LSW** select **Edit → Set Valid Layers**.
- Select the box on the right side of the layer(s) you want view in the layout. For example, to view only "metal1 pn" select the box on the right side of metal1 pn. Press **OK** and only the selected layers will be shown in the Virtuoso Layout Editing window.
- To make all layers visible again, press the **AV** button on the LSW.

Design Rule Checking

Layout must be drawn according to strict design rules. After you have finished your layout, an automatic program will check each and every polygon in your design against these design rules

and report violations. This process is called *Design Rule Checking* (DRC) and MUST be done for every layout to ensure it will function properly when fabricated.

Note: You are STRONGLY advised not to wait until your layout is completed to check for design rule violations. In future layouts, run DRC frequently as you add layers to your cell. If you wait until you are finished to check for errors, it will be much hard to track down and fix all your errors.

- In the Virtuoso Layout Editing window select **NCSU => Modify LVS Rules.** Make sure the option "Compare FET parameter" is checked. This will enable the crosschecking of transistor dimensions between your schematic and layout.
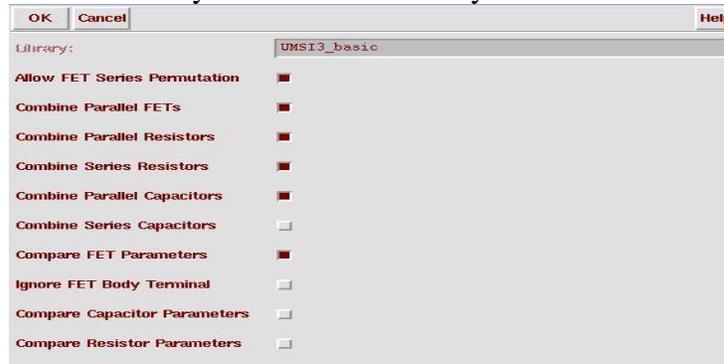
- In the Virtuoso Layout Editing window select **Verify => DRC.** This will open the DRC options dialog box. The default options for the DRC are adequate for most situations.
- Click **OK** to start DRC. DRC results and progress will be displayed in the CIW (Command Interpreter Window) (the main window when you start Cadence).
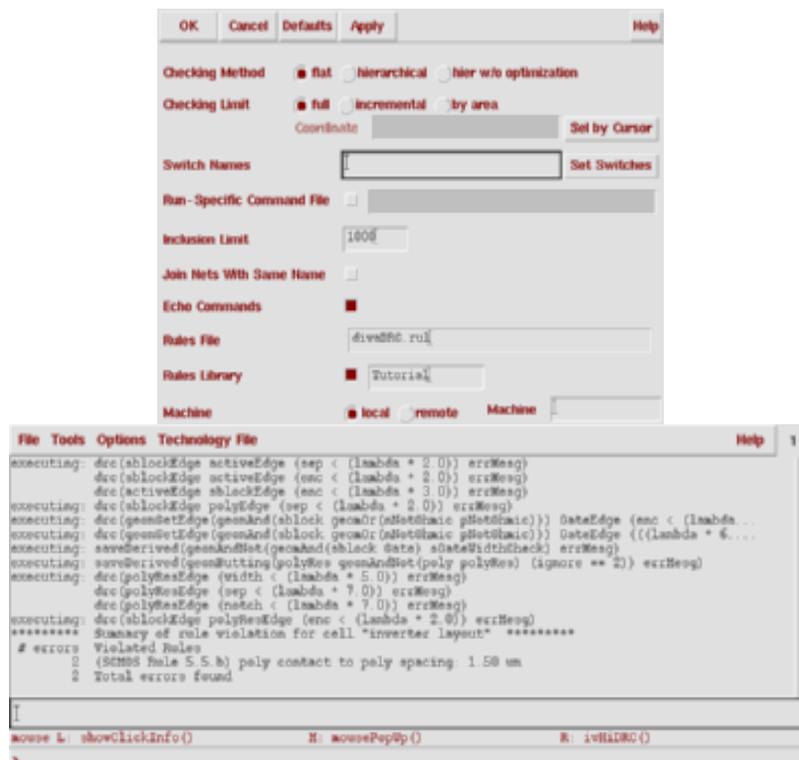
(top) DRC dialog window and (bottom) CIW showing DRC results.

- After the DRC is complete, the bottom line in the CIW will show "*# Total errors found*". If the number is greater than zero, any errors will be highlighted on the layout. Using the design rules as a guideline, correct all errors and perform another DRC until you get no errors.
- The DRC will be successful when you see the results saying "*0 Total errors found*", as shown above.

Layout Parameter Extraction

The mask layout contains only physical data. In fact it just contains coordinates of rectangles drawn in different colors (layers). The extraction process identifies the devices from the layout and generates a SPICE-like *netlist* and other files necessary to complete the design process.

Before beginning a layout extraction you must have the cell opened in the layout window and the layout should have already passed DRC.

- In the Virtuoso Layout Editing window select **Verify => Extract.** A new window (below) with extraction options will appear.
- Click on **Set Switches** and select *Extract_parasitic_caps*. This setting will extract parasitic elements from the layout. Click on **OK**.
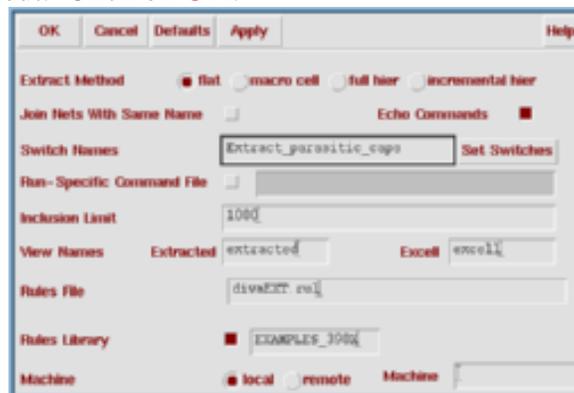
- After extraction check the Command Interpreter Window to make sure there are no errors.
- Following a successful extraction you will see a new cell view called *extracted* added to the Library Manager window.

The Extracted Cell View

- Load the extracted cellview from the Library Manager window. This will open up a layout that looks almost identical to the layout you produced earlier.

You will notice that only the I/O pins appear as solid blocks and all other shapes appear as outlines. The red rectangles indicate that there are a number of instances (electrical elements) within this hierarchy.

- Try pressing 'Shift+F' to view the complete hierarchy. A number of symbols are revealed. If you zoom in, you will be able to identify individual elements such as transistors and capacitors. You will notice that the parameters (e.g. channel dimensions) of these devices represent the values as they were drawn in the layout view.
- To disable this view, press 'Ctrl+F'
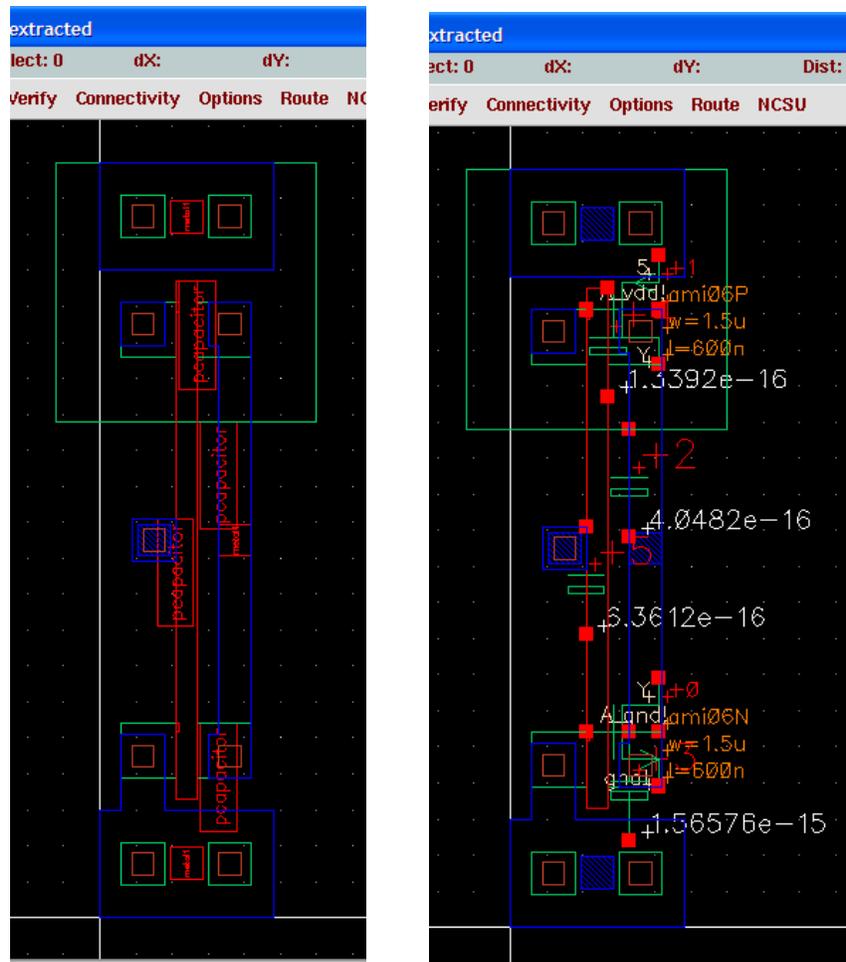
Extracted view (left) before and (right) after showing extracted devices.

In addition to the actual transistors you will notice a number of elements (mainly capacitors) in your extracted cell view. These are not actual devices. They are *parasitic* capacitances, which are side effects formed by different layers you used for your layout.

Layout vs. Schematic Comparison

The next step is to compare the netlist extracted from the layout with the schematic to ensure the layout you have drawn is an identical match to the cell schematic.

- In the Virtuoso Layout Editing window select Verify => LVS to open the LVS window.
  - If you had previously run an LVS check, this would open a small warning box. Make sure that the option Form Contents is selected in this box and click OK.
- The top half of the LVS options window is split into two parts, schematic and extracted. Make sure that the entries in the Library, Cell, and View boxes are correct for your circuit.
- Select **Run** to start the comparison. The comparison algorithm will run in the background, the result of the LVS run will be displayed in a message box. Be patient, even for a very small design the LVS run can take some time (minutes).

- When the LVS comparison is complete you will get a pop up window saying "*Job . . . has succeeded*". This does **NOT** necessarily mean the circuits match, just that the LVS operation is complete. Click OK to close this window.
- In the LVS window, click on the **Output** button (just right of the Run button) to display the LVS result. Scroll through this window and take a look at the LVS result. The most important part of the report tells if errors were found or if netlists did match ("The netlists match" as shown below).
- If there are no errors, your layout is complete and correct. If there are errors, you will have to reload the layout view, fix the problems, and re-run LVS until there are no errors. See the *Guide to Passing LVS* document for some tips on correcting LVS errors.
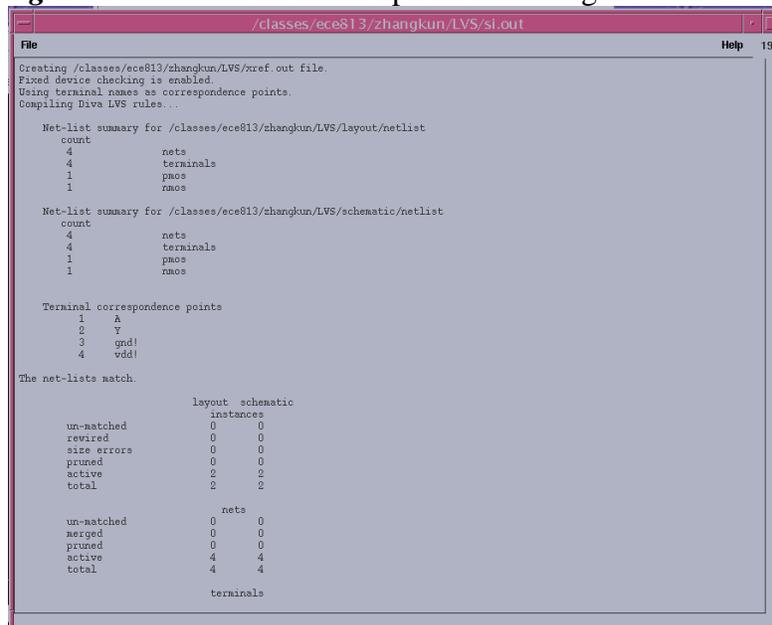
Successful LVS where the netlists match.

LVS Options

Some of the other options in the LVS window are for finding mismatches between two netlists and for generating netlists that include only parasitic effects relevant to one part of the circuit. Feel free to explore these options to learn more about the Cadence tools.

Series FETs

By default, LVS will allow FETs in series to be matched in any order. This can cause discrepancies between simulations of schematic and extracted cellviews, particularly in timing analysis. Therefore, it is generally preferable to modify this feature as follows for any cell that includes series transistors to ensure an exact match between schematic and layout.

- In the Virtuoso Layout Editing window select NCSU => Modify LVS Rules and uncheck the "Allow FET Series Permutation" checkbox.

You should confirm this setting before performing LVS on most logic gates that are more complex than the INV cell, including NAND and NOR gates.

Although this completes Tutorial B, in a normal design process you would follow a successful LVS with timing simulations of the *extracted* cellview. Such simulations provide a very accurate measurement of how the circuit would perform after fabrication by including the parasitic elements in the simulations. This procedure will be covered in Tutorial C.