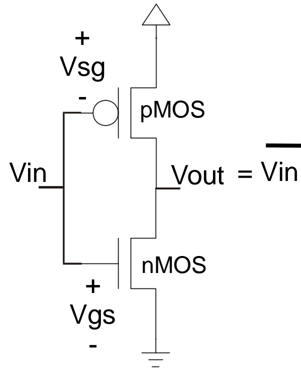
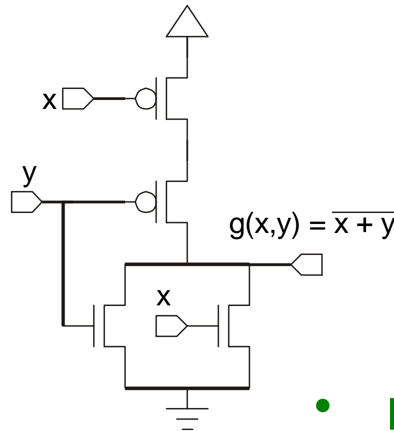
Review: CMOS Logic Gates

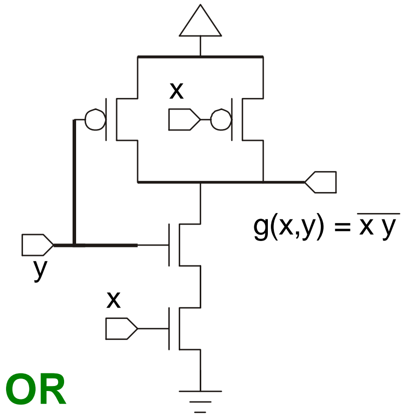
- INV Schematic



- NOR Schematic

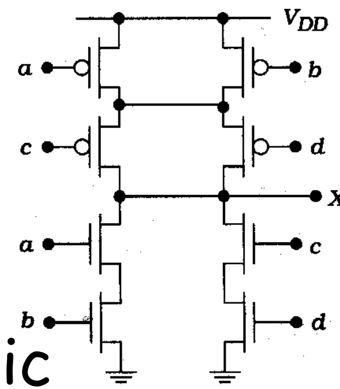


- NAND Schematic

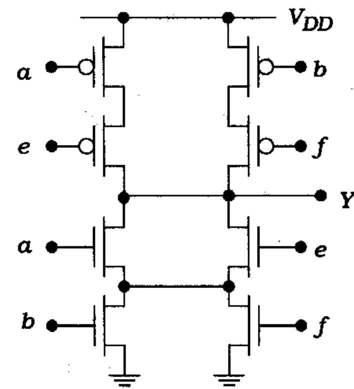


- **CMOS inverts functions**
- **parallel for OR**
- **series for AND**

- CMOS Combinational Logic
  - use DeMorgan relations to reduce functions
    - remove all NAND/NOR operations
  - implement nMOS network
  - create pMOS by complementing operations
- AOI/OAI Structured Logic
- XOR/XNOR using structured logic



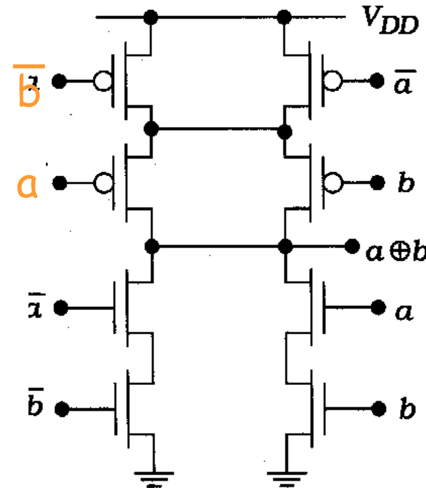
(a) AOI circuit



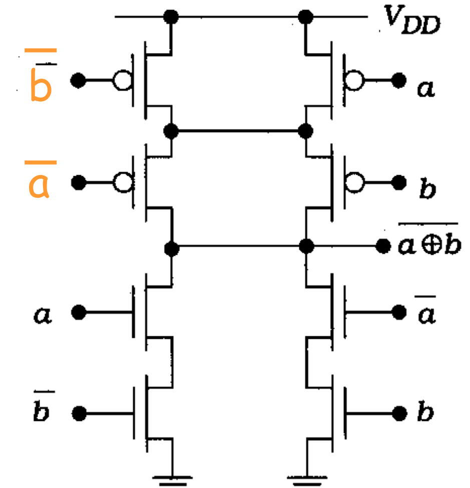
(b) OAI circuit

Review: XOR/XNOR and TGs

- Exclusive-OR (XOR)
  - $a \oplus b = \overline{a} \cdot b + a \cdot \overline{b}$
- Exclusive-NOR
  - $\overline{a \oplus b} = a \cdot b + \overline{a} \cdot \overline{b}$



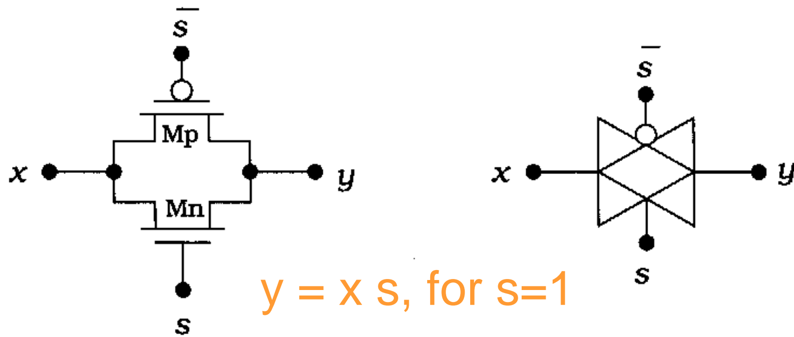
(a) Exclusive-OR



(b) Exclusive-NOR

XOR/XNOR in AOI Form

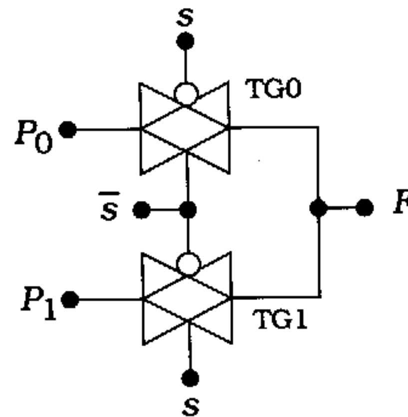
- Transmission Gates



y = x s, for s=1

- MUX Function using TGs

$F = Po \cdot \overline{s} + P1 \cdot s$



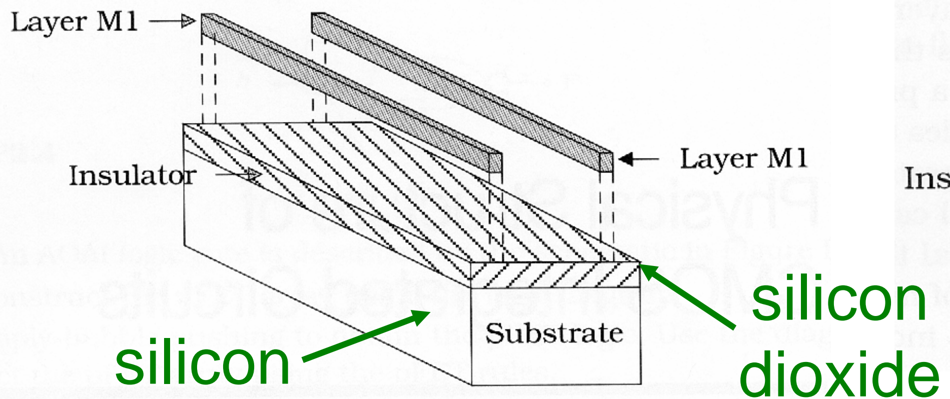
s	TG0	TG1	F
0	Closed	Open	P_0
1	Open	Closed	P_1

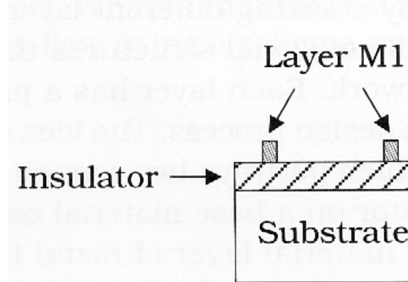
CMOS Technology

- Properties of microelectronic materials
  - resistance, capacitance, doping of semiconductors
- Physical structure of CMOS devices and circuits
  - pMOS and nMOS devices in a CMOS process
  - n-well CMOS process, device isolation
- Fabrication processes
- Physical design (layout)
  - layout of basic digital gates, masking layers, design rules
  - LOCOS process
  - planning complex layouts (Euler Graph and Stick Diagram)

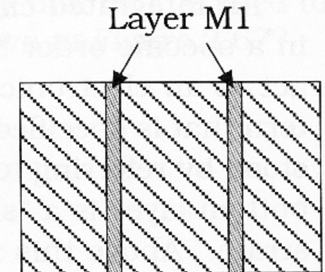
Integrated Circuit Layers

- Integrated circuits are a stack of patterned layers
  - **metals**, good conduction, used for interconnects
  - **insulators** (silicon dioxide), block conduction
  - **semiconductors** (silicon), conducts under certain conditions
- Stacked layers form 3-dimensional structures



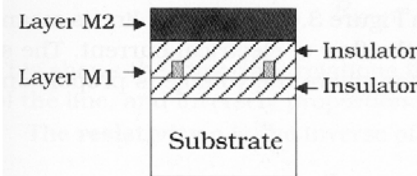


(a) Side view

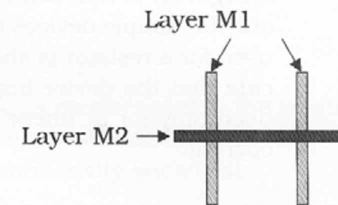


(b) Top view

- background assumed to be silicon covered by silicon dioxide



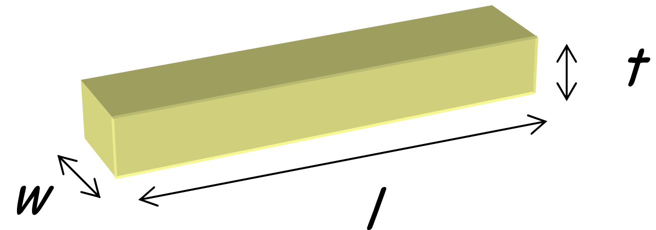
(a) Side view



(b) Top view

Interconnect Parasitics

- Parasitic = unwanted natural electrical elements
- Metal Resistance
  - metals have a linear resistance and obey Ohm's law
    - V = IR
  - generate parasitic interconnect resistance, R_{line}
    - $R_{line} = \frac{l}{\sigma A} = \frac{\rho l}{A}$
      - $A = wt$
      - ρ = resistivity, σ = conductivity

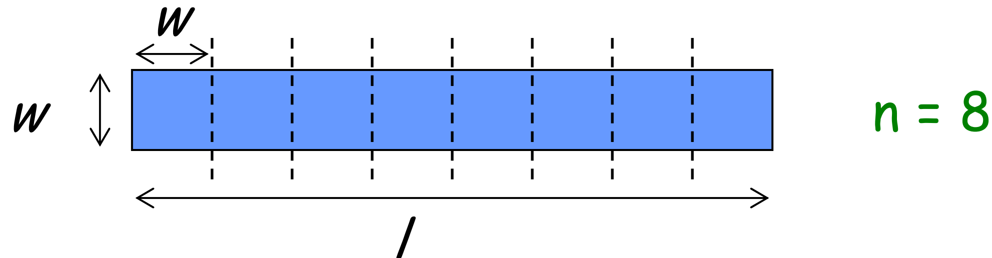


  - defined by **sheet resistance**
    - $R_s = \frac{1}{\sigma t} = \frac{\rho}{t}$, resistance per unit length [ohms, Ω]
    - $R_{line} = R_s \frac{l}{w}$, Rs determined by process, l & w by designer

Rline = Rs when $l = w$

Metal Resistance: Measuring 'squares'

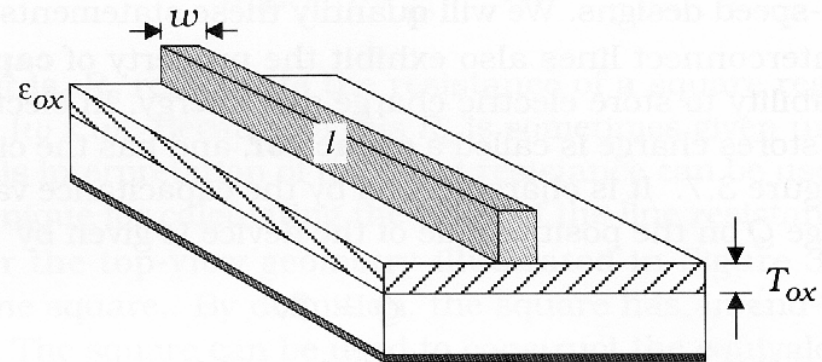
- From top view of layout, can determine how many '**squares**' of the layer are present
  - 'square' is a unit length equal to the width

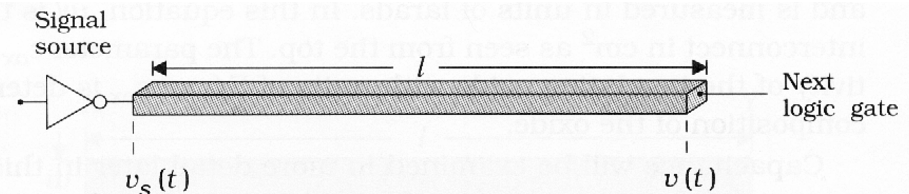


  - R_{line} = Rs n, where $n = \frac{l}{w}$ is the number of 'squares'
  - Get a unit of resistance, Rs, for each square, n.

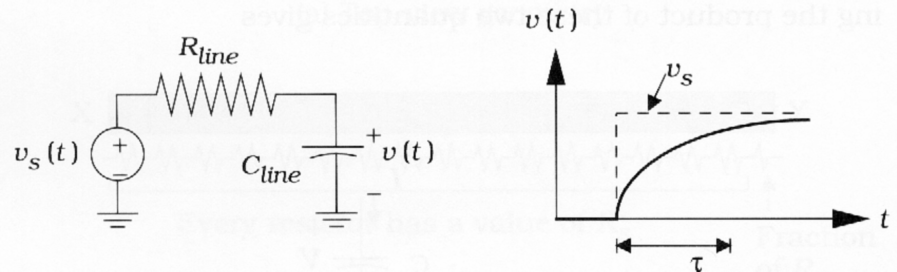
Parasitic Line Capacitances

- Capacitor Basics
  - $Q = CV$, C in units of Farads [F]
  - $I = C\, dV/dt$
- Parallel plate capacitance
  - $C_{line} = \dfrac{\varepsilon_{ox}\, w\, l}{t_{ox}}$ [F], w l = Area
  - ε_{ox} = permittivity of oxide
    - $\varepsilon_{ox} = 3.9\, \varepsilon_o$
    - $\varepsilon_o = 8.85 \times 10^{-14}$ [F/cm]
- RC time constant of an interconnect line
  - $\tau = R_{line}\, C_{line}$





(a) Physical structure

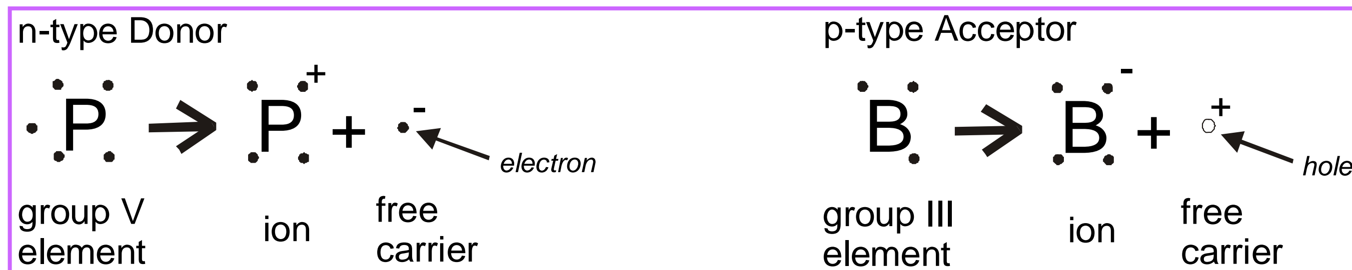


Electrical Properties of Silicon

- Silicon is a semiconductor… does it conduct or insulate?
  - doping = adding impurities (non-silicon) to Si: *will be covered later*
    - doping concentration and temperature determine resistivity
- Conduction/Resistance
  - generally, the Si we see in CMOS is doped
    - at room temp., doped silicon is a weak conductor = high resistance
- Capacitance
  - doped, room temp. Si is conductive
  - conduction → free charge carriers → no electric field
    → no capacitance (within bulk silicon)
  - exception: if free carries are removed (e.g., depletion layer of a diode) silicon becomes an insulator with capacitance

Conduction in Semiconductors -Review

- Intrinsic (undoped) Semiconductors
  - intrinsic carrier concentration ≡ n_i = 1.45x10^{10} cm^{-3}, at room temp.
  - n = p = n_i, in intrinsic (undoped) material
    - n ≡ number of electrons, p ≡ number of holes
  - mass-action law, $np = n_i^2$ applies to undoped and doped material
- Extrinsic (doped) Semiconductors
  - **dopants** added to modify material/electrical properties



•n-type (n+), add elements with extra an electron

- N_d ≡ conc. of donor atoms [cm^{-3}]
- $n_n = N_d$, n_n ≡ conc. of electrons in n-type material
- $p_n = n_i^2/N_d$, using mass-action law,
- p_n ≡ conc. of holes in n-type material
- always a lot more n than p in n-type material

•p-type = p+, add elements with an extra hole

- N_a ≡ concentration of acceptor atoms [cm^{-3}]
- $p_p = N_a$, p_p ≡ conc. of holes in p-type material
- $n_p = ni^2/N_a$, using mass-action law,
- n_p ≡ conc. of electrons in p-type material
- always a lot more p than n in p-type material

Conduction in Silicon Devices

- doping provides free charge carriers, alters conductivity
- conductivity in semic. w/ carrier densities n and p
  - $\sigma = q(\mu_n n + \mu_p p)$
    - q ≡ electron charge, $q = 1.6\text{x}10^{-19}$ [Coulombs]
    - μ ≡ mobility [cm²/V-sec], $\mu_n \cong 1360$, $\mu_p \cong 480$ (typical values in ***bulk*** Si)
- in n-type region, $n_n \gg p_n$
  - $\sigma \approx q\mu_n n_n$
- in p-type region, $p_p \gg n_p$
  - $\sigma \approx q\mu_p p_p$
- resistivity, $\rho = 1/\sigma$
- Can now calculate the resistance of an n+ or p+ region

$\mu_n > \mu_p$

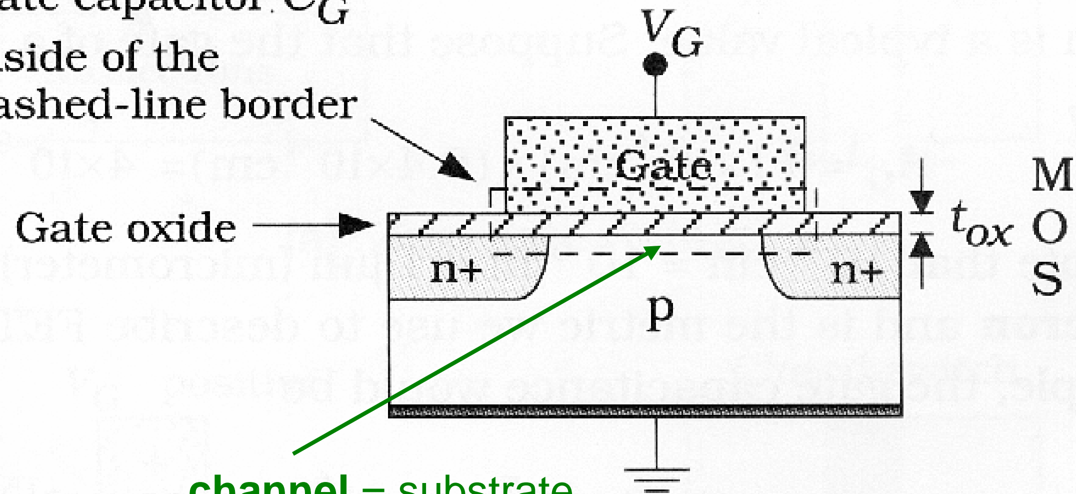
electrons more mobile than holes
conductivity of n+ > p+

Mobility often assumed constant

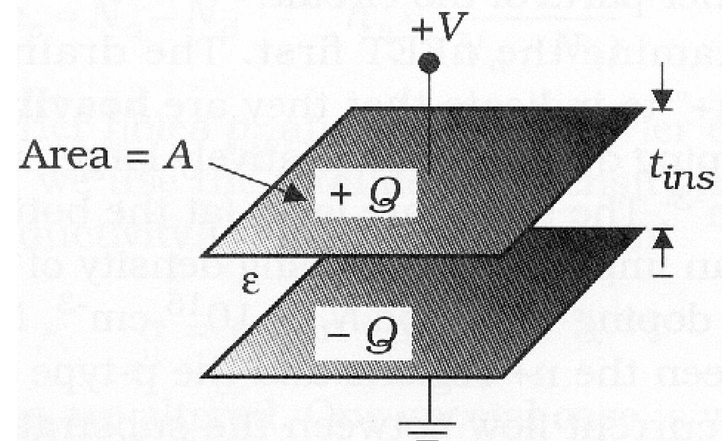
but is a function of Temperature and Doping Concentration

MOSFET Gate Operation

- Gate Capacitance
  - gate-substrate parallel plate capacitor
  - $C_G = \varepsilon_{ox} A / t_{ox}$ [F]
    - $\varepsilon_{ox} = 3.9\ \varepsilon_o$
    - $\varepsilon_o = 8.85 \times 10^{-14}$ [F/cm]
- Oxide Capacitance
  - $Cox = \varepsilon_{ox} / t_{ox}$ [F/cm^2]
  - $C_G = Cox\ A_G$ [F]
    - A_G=gate area = L•W [cm^2]
- Charge on Gate, +Q, induces charge -Q in substrate **channel**
  - channel charge allows conduction between source and drain



channel = substrate region under the gate, between S and D



Physical n/pMOS Devices

- nMOS and pMOS cross-section

Source Drain Gate Metal
n+ n+ p
highly doped n region
lightly doped p region

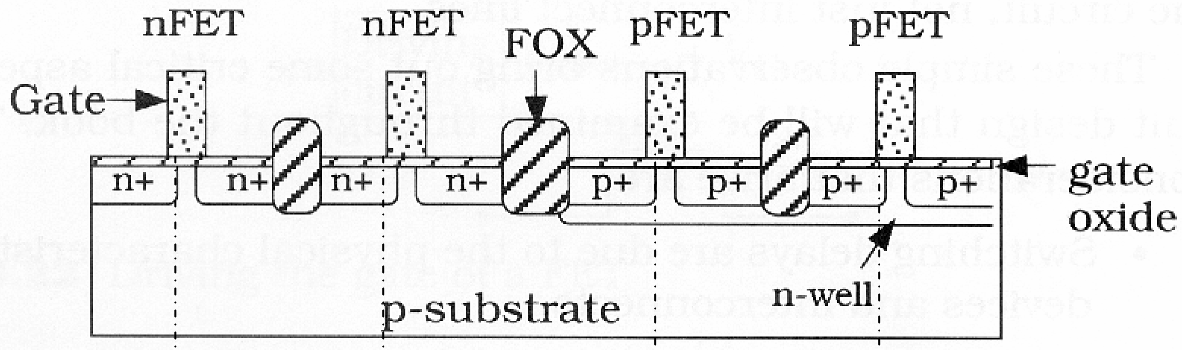
Drain Source Gate
p+ p+ n-well p
highly doped p region
lightly doped n region
lightly doped p region

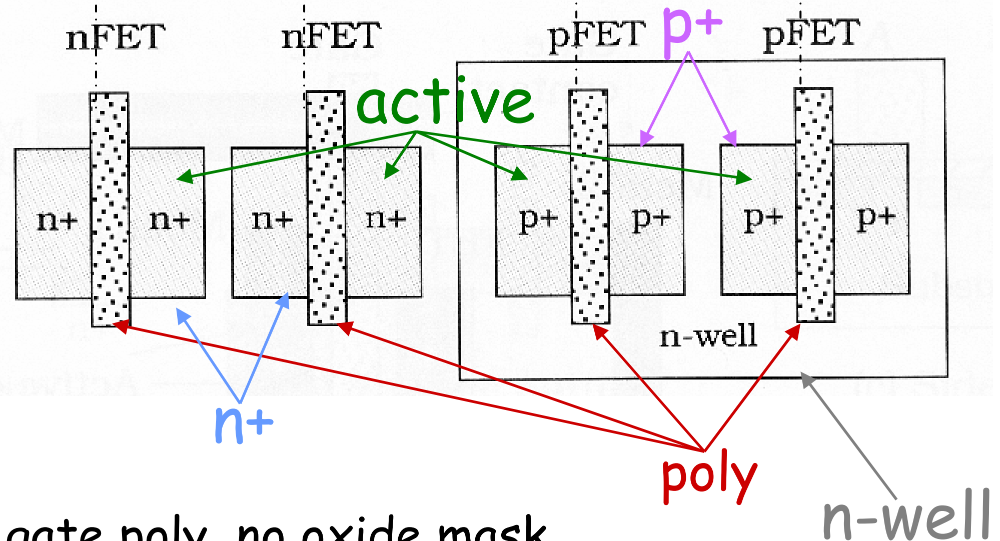
(a) nFET cross-section (b) pFET cross-section

- Layers
  - substrate, n-well, n+/p+ S/D, gate oxide, polysilicon gate, S/D contact, S/D metal
- Can you find all of the diodes (pn junctions)?
  - where? conduct in which direction? what purpose?

Lower CMOS Layers

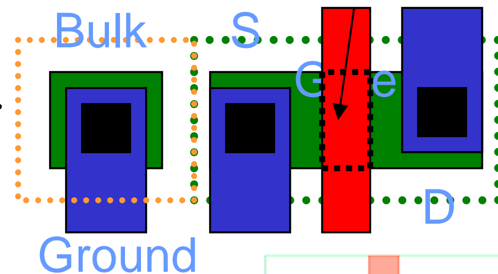
- Visible Features
  - p-substrate
  - n-well
  - n+ S/D regions
  - p+ S/D regions
  - gate oxide
  - polysilicon gate
- Mask Layers
  - n-well
  - active (S/D regions)
    - active = not FOX
  - n+ doping
  - p+ doping
  - poly patterning
    - gate oxide aligned to gate poly, no oxide mask

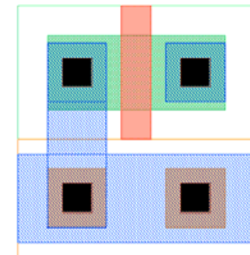




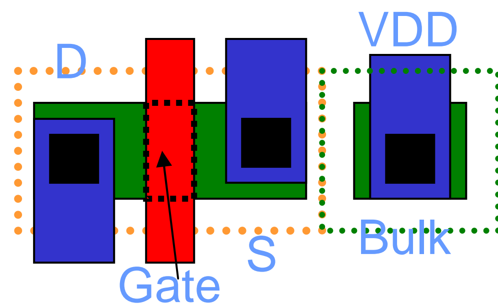
Physical Realization of a 4-Terminal MOSFETs

- nMOS Layout
  - gate is intersection of Active, Poly, and nSelect
  - S/D formed by Active with Contact to Metal1
  - bulk connection formed by p+ tap to substrate

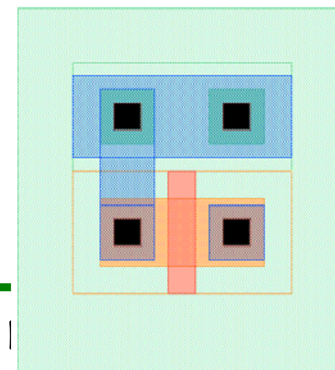




- pMOS Layout
  - gate is intersection of Active, Poly, and pSelect
  - S/D formed by Active with Contact to Metal1
  - bulk connection formed by n+ tap to nWell

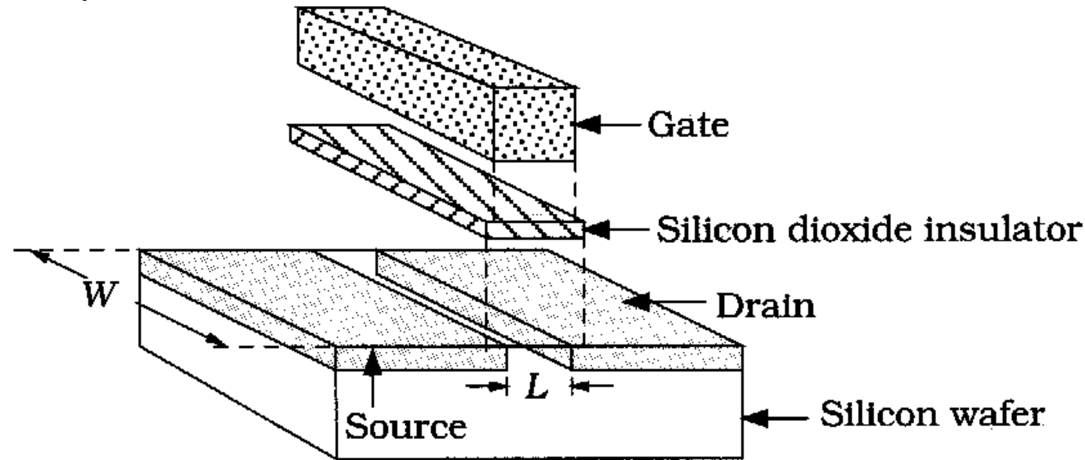


- Active layer
  - in lab we will use ***nactive*** and ***pactive***
    - nactive should always be covered by nselect
    - pactive should always be covered by pselect
  - nactive and pactive are the same mask layer (active)
    - different layout layers help differentiate nMOS/pMOS

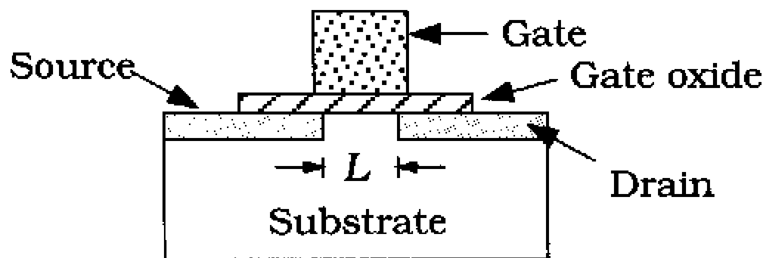


CMOS Device Dimensions

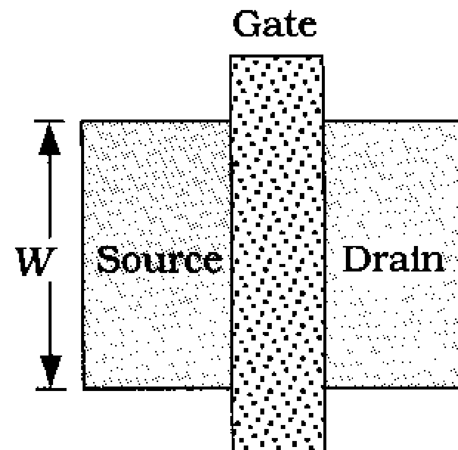
- Physical dimensions of a MOSFET
  - L = channel length
  - W = channel width



- Side and Top views



(a) Side view

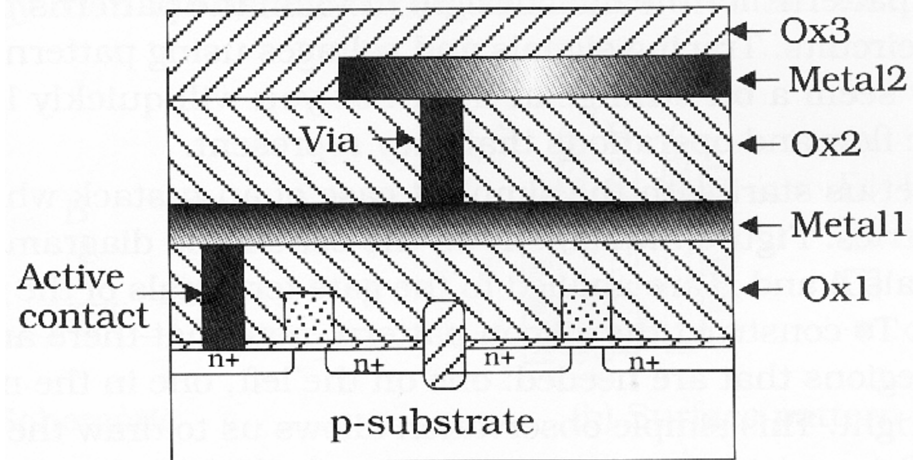


(b) Top view

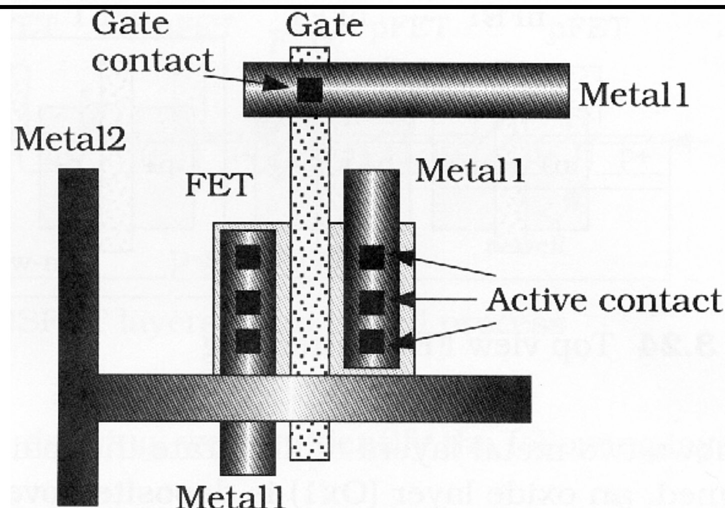
Upper CMOS Layers

- Cover lower layers with oxide insulator, Ox1
- Contacts through oxide, Ox1
  - metal1 contacts to poly and active
- Metal 1
- Insulator Ox2
- Via contacts
- Metal 2
- Repeat insulator/via/metal

only Metal 1 has direct contact to lower layers



- Full Device Illustration
  - active
  - poly gate
  - contacts (active & gate)
  - metal1
  - via
  - metal2



CMOS Cross Section View

- Cross section of a 2 metal, 1 poly CMOS process

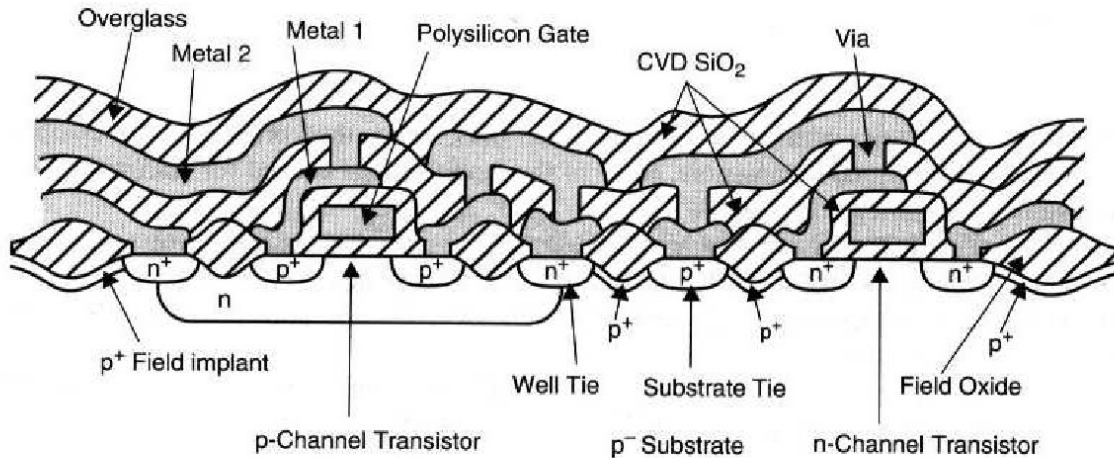
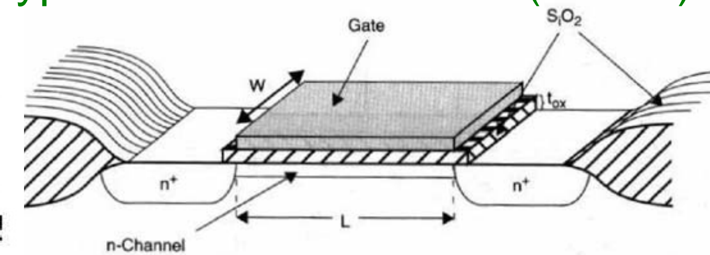
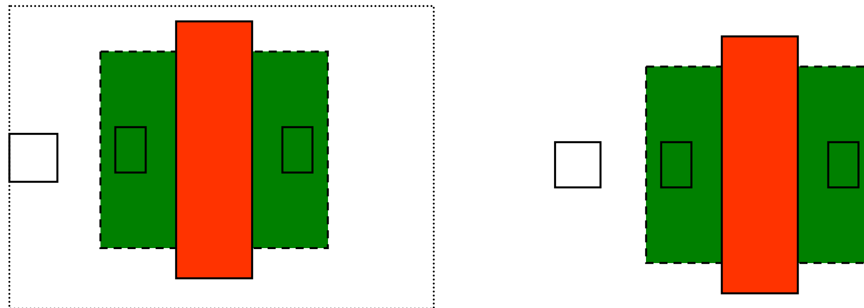


Figure 2.11 The final cross section of a CMOS microcircuit with two layers of metal.

Typical MOSFET Device (nMOS)

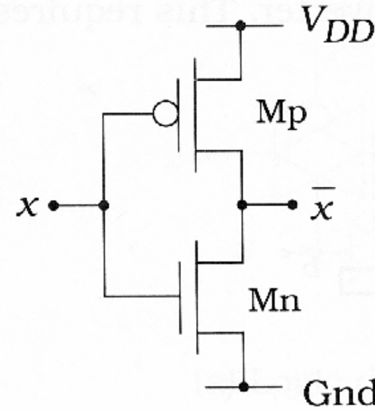


- Layout (top view) of the devices above (partial, simplified)



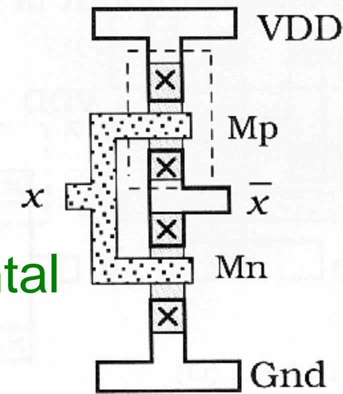
Inverter Layout

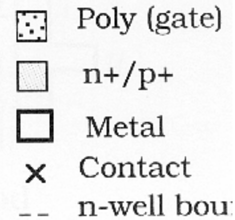
- Features
  - VDD & Ground 'rail'
    - using Metal1 layer
  - N-well region
    - for pMOS
  - Active layers
    - different n+ and p+
  - Contacts
    - n+/p+ to metal
    - poly to metal
- Alternate layout
  - advantage
    - simple poly routing
  - disadvantage
    - harder to make W large



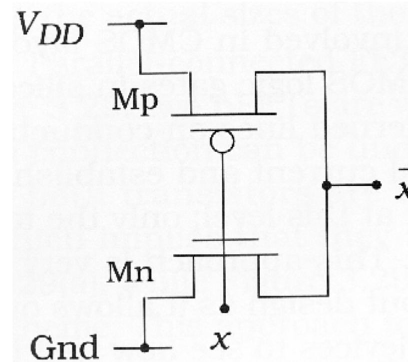
(a) Circuit

horizontal poly

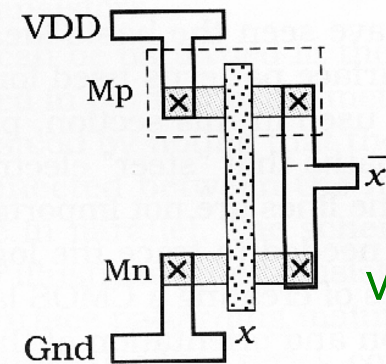




(b) Layer patterning



(a) Circuit

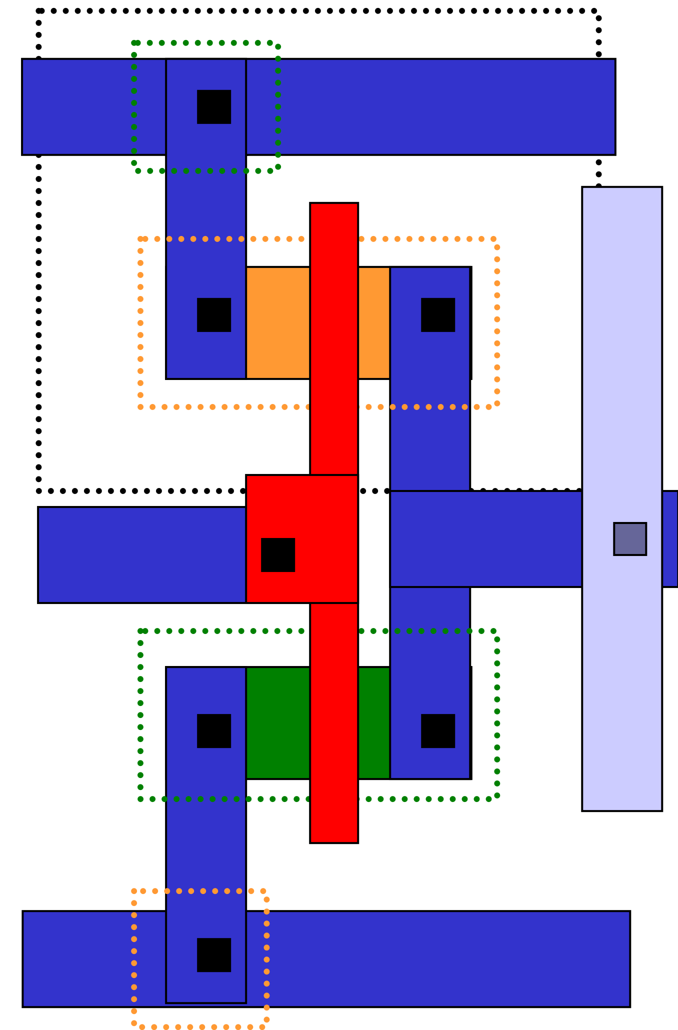


(b) Layer patt

vertical poly

CMOS Layout Layers

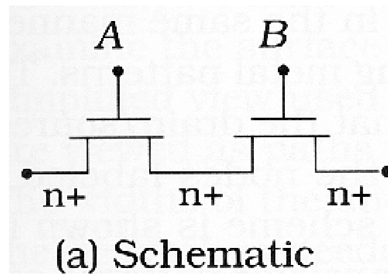
- Mask layers for 1 poly, 2 metal, n-well CMOS process
  - Background: p-substrate
  - nWell
  - Active (nactive and pactive)
  - Poly
  - pSelect
  - nSelect
  - Active **Contact**
  - Poly **Contact**
  - Metal1
  - Via
  - Metal2
  - Overglass



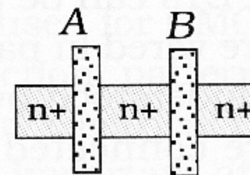
- See supplementary power point file for animated **CMOS process flow**
  - should be viewed as a slide show, not designed for printing

Series MOSFET Layout

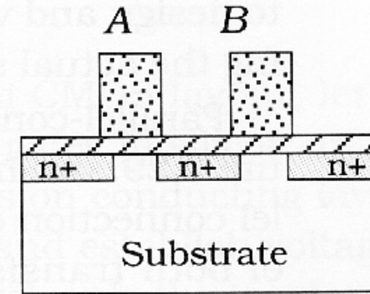
- Series txs
  - 2 txs share a S/D junction



(a) Schematic

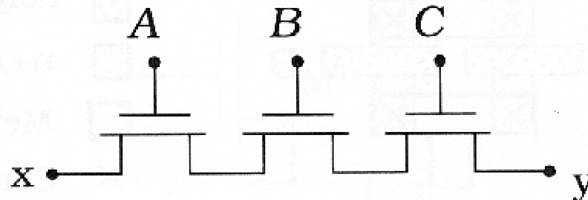


(b) Surface pattern



(c) Side view

- Multiple series transistors
  - draw poly gates side-by-side



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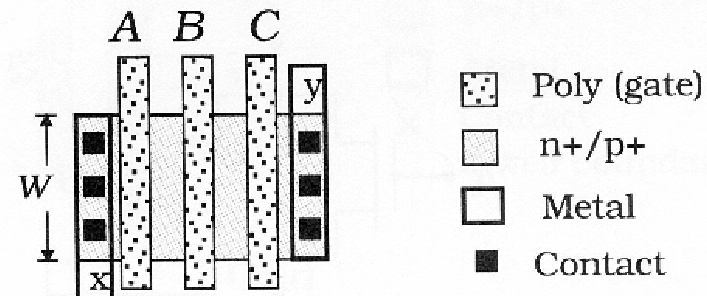
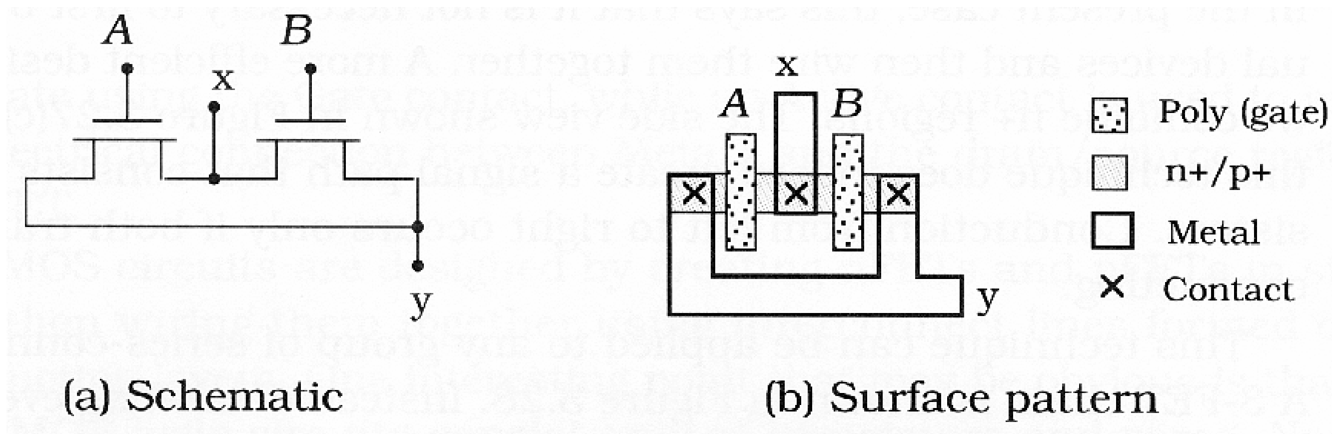


(b) Surface pattern

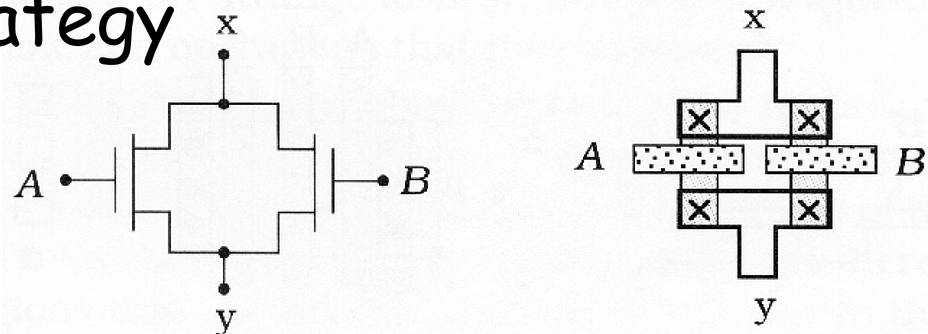
Parallel MOSFET Layout

- Parallel txs
  - one shared S/D junction with contact
  - short other S/D using interconnect layer (metal1)



(a) Schematic (b) Surface pattern

- Alternate layout strategy
  - horizontal gates



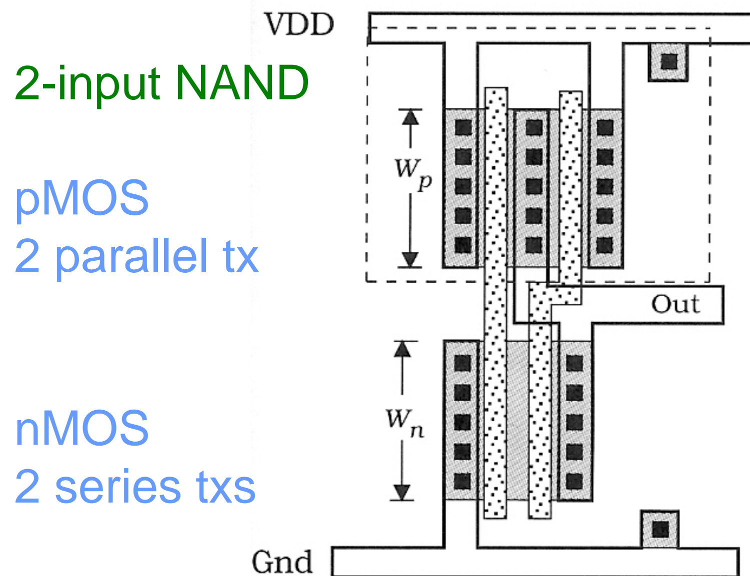
NAND/NOR Layouts

- One layout option with horizontal transistors (L runs horizontally)
  - ignore the size (W) for now

2-input NAND

pMOS
2 parallel tx

nMOS
2 series txs

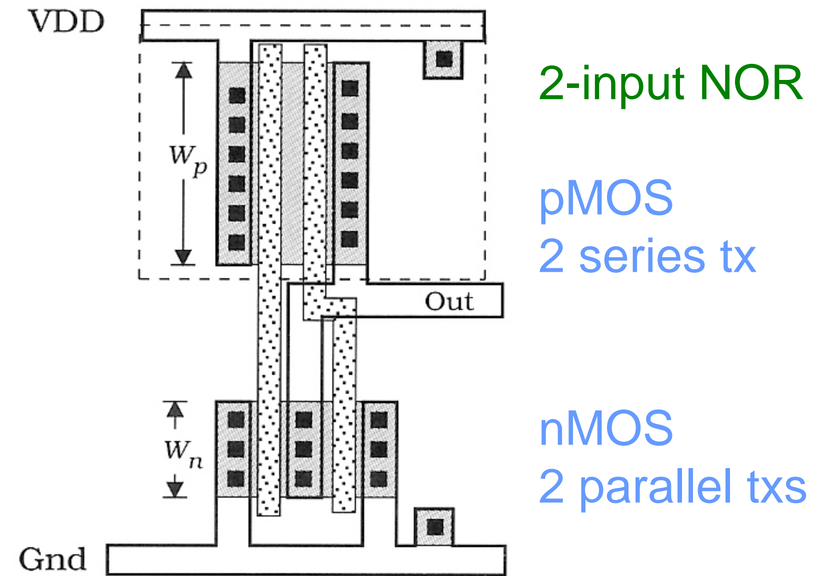


(a) NAND2

2-input NOR

pMOS
2 series tx

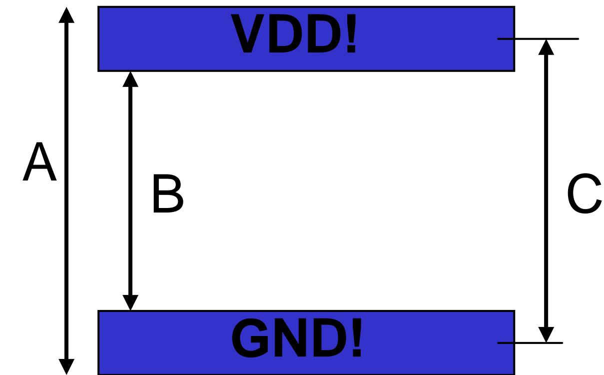
nMOS
2 parallel txs



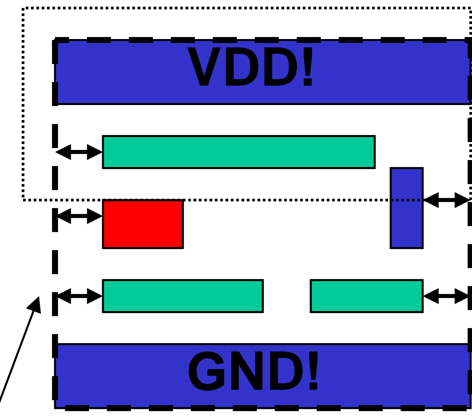
(b) NOR2

Layout Cell Definitions

- Cell Pitch = Height of standard cells
  measured between VDD & GND rails
  - A: 410 lab definition
    - top of VDD to bottom of GND
  - B: interior size, without power rails
  - C: textbook definition
    - middle of GND to middle of VDD



- Cell Boundary
  max extension of any layer (except nwell)
  - set boundary so that cells can be placed side-by-side without any rule violations
  - extend power rails 1.5λ (or 2λ to be safe) beyond any active/poly/metal layers
  - extend n-well to cell boundary (or beyond) to avoid breaks in n-well



cell boundary

Cell Layout Guidelines

- Internal Routing
  - use lowest routing layer possible, typically poly and metal1
  - keep all possible routing inside power rails
  - keep interconnects as short as possible
- Bulk (substrate/well) Contacts
  - must have many contacts to p-substrate and n-well
    - at least 1 for each connection to power/ground rails
  - consider how signals will be routed in/out of the cells
    - don't block access to I/O signals with substrate/well contacts
- S/D Area Minimization
  - minimize S/D junction areas to keep capacitance low
- I/O Pads
  - Placement: must be able to route I/O signals out of cell
  - Pad Layer: metal1 for smaller cells, metal2 acceptable in larger cells
- Cell Boundary
  - extend VDD and GND rail at least 1.5λ beyond internal features
  - extend n-well to cell boundary to avoid breaks in higher level cells

Layout CAD Tools

- Layout Editor
  - draw multi-vertices polygons which represent physical design layers
  - **Manhattan geometries**, only 90° angles
    - Manhattan routing: run each interconnect layer perpendicular to each other
- Design Rules Check (DRC)
  - checks rules for each layer (size, separation, overlap)
  - ***must pass DRC or will fail in fabrication***
- Parameter Extraction
  - create netlist of devices (tx, R, C) and connections
  - extract parasitic Rs and Cs, lump values at each line (R) / node (C)
- Layout Vs. Schematic (LVS)
  - compare layout to schematic
  - check devices, connections, power routing
    - can verify device sizes also
  - ensures layout matches schematic exactly
  - ***passing LVS is final step in layout***

Layout with Cadence Tools

- Layer Map

CMOS Features	CMOS Mask Layers	Cadence Layers
n-well	n-well	nwell
FOX	active	pactive, nactive
n+ S/D regions	n+ doping	nselect
p+ S/D regions	p+ doping	pselect
Gate	poly	poly
Active/Poly contact	Contact	cc
Metal 1	Metal 1	metal1
Via	VIA	via
Metal 2	Metal 2	metal2

- Inverter Example

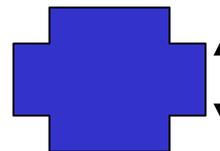
inv

in

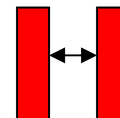
out

Design Rules: Intro

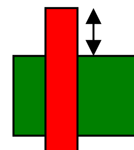
- Why have Design Rules
  - fabrication process has minimum/maximum feature sizes that can be produced for each layer
  - alignment between layers requires adequate separation (if layers unconnected) or overlap (if layers connected)
  - proper device operation requires adequate separation
- "Lambda" Design Rules
  - lambda, λ, = 1/2 minimum feature size, e.g., 0. 6μm process -> λ =0.3μm
  - can define design rules in terms of lambdas
    - allows for "scalable" design using same rules
- Basic Rules
  - minimum layer size/width

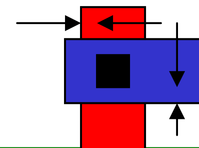


  - minimum layer separation



  - minimum layer overlap



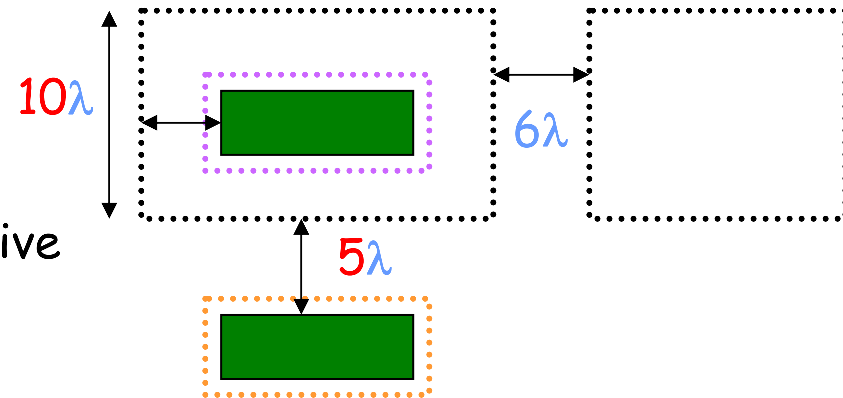


Design Rules: 1

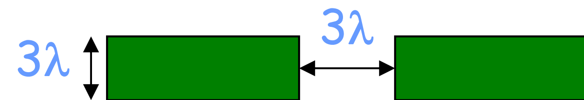
- n-well

MOSIS **SCMOS rules**; λ **=0.3μm** for AMI C5N

  - required everywhere pMOS is needed
  - rules
    - minimum width
    - minimum separation to self
    - minimum separation to nMOS Active
    - minimum overlap of pMOS Active

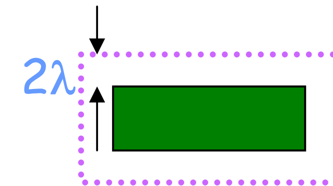


- Active
  - required everywhere a transistor is needed
  - any non-Active region is FOX
  - rules
    - minimum width
    - minimum separation to other Active

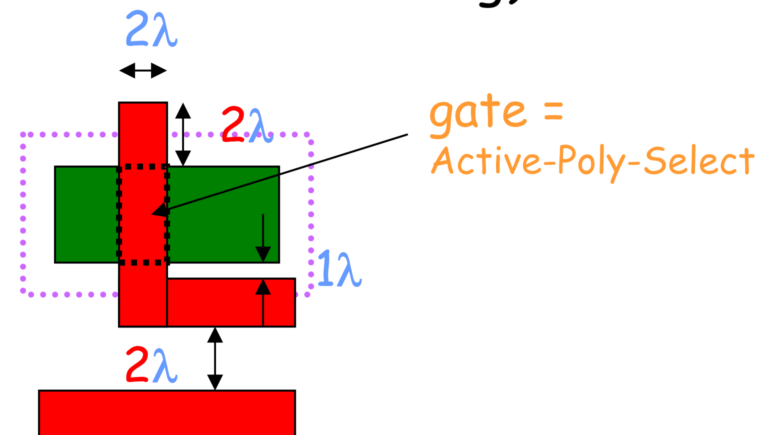


Design Rules: 2

- n/p Select
  - defines regions to be doped n+ and p+
  - tx S/D = Active AND Select NOT Poly
  - tx gate = Active AND Select AND Poly
  - rules
    - minimum overlap of Active
      - same for pMOS and nMOS
    - several more complex rules available



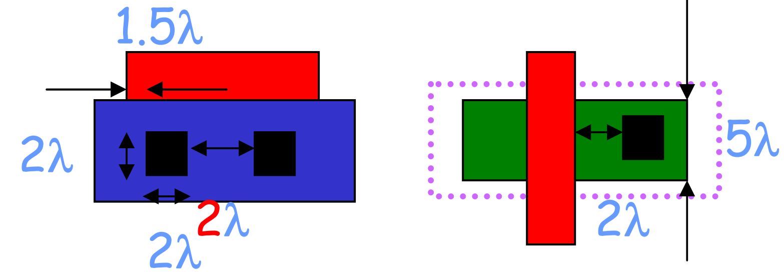
- Poly
  - high resistance conductor (can be used for short routing)
  - primarily used for tx gates
  - rules
    - minimum size
    - minimum space to self
    - minimum overlap of gate
    - minimum space to Active



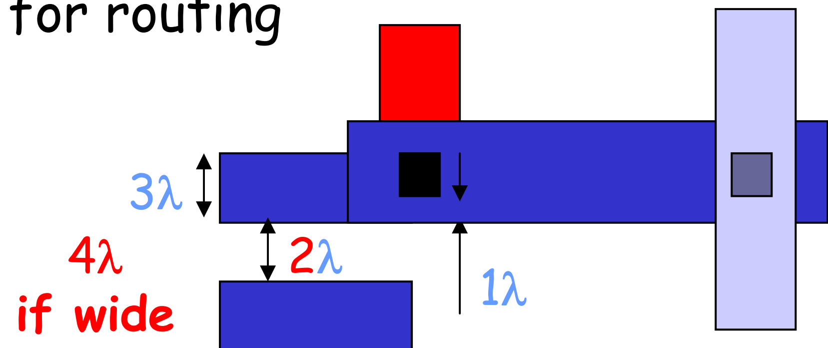
Design Rules: 3

- Contacts
  - Contacts to Metal1, from Active or Poly
    - use same layer and rules for both
  - must be SQUARE and MINIMUM SIZED
  - rules
    - exact size
    - minimum overlap by Active/Poly
    - minimum space to Contact
    - minimum space to gate

note: due to contact size and overlap rules, min. active size at contact will be 2+1.5+1.5=5λ



- Metal1
  - low resistance conductor used for routing
  - rules
    - minimum size
    - minimum space to self
    - minimum overlap of Contact

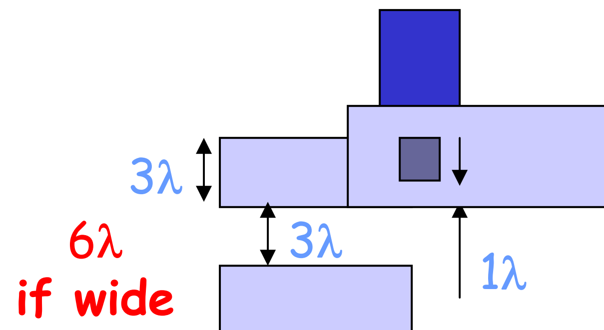


Design Rules: 4

- Vias
  - Connects Metal1 to Metal2
  - must be SQUARE and MINIMUM SIZED
  - rules
    - exact size 2λ
    - space to self 3λ
    - minimum overlap by Metal1/Metal2 1λ
    - minimum space to Contact 2λ
    - minimum space to Poly/Active edge 2λ

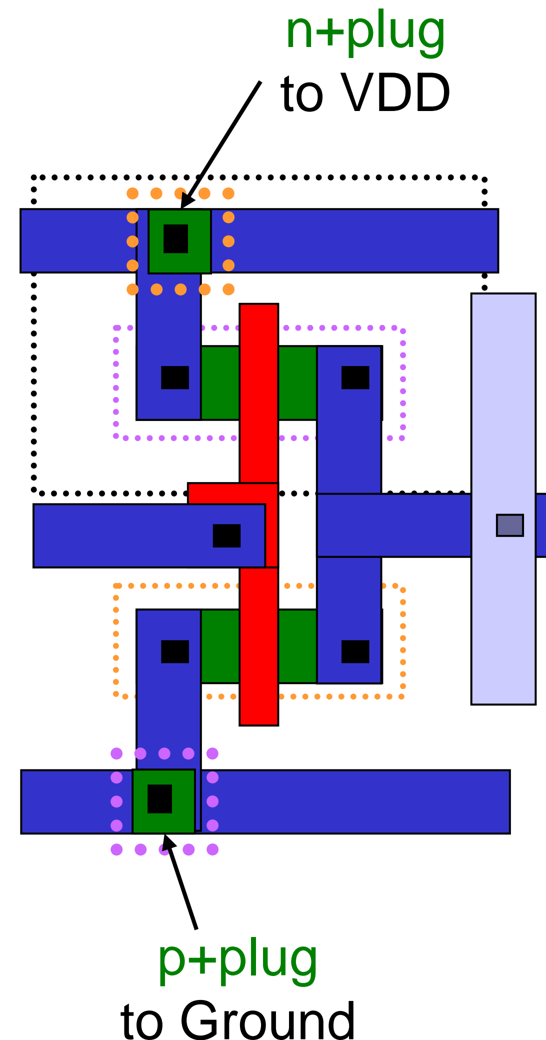
see MOSIS site for illustrations

- Metal2
  - low resistance conductor used for routing
  - rules
    - minimum size
    - minimum space to self
    - minimum overlap of Via



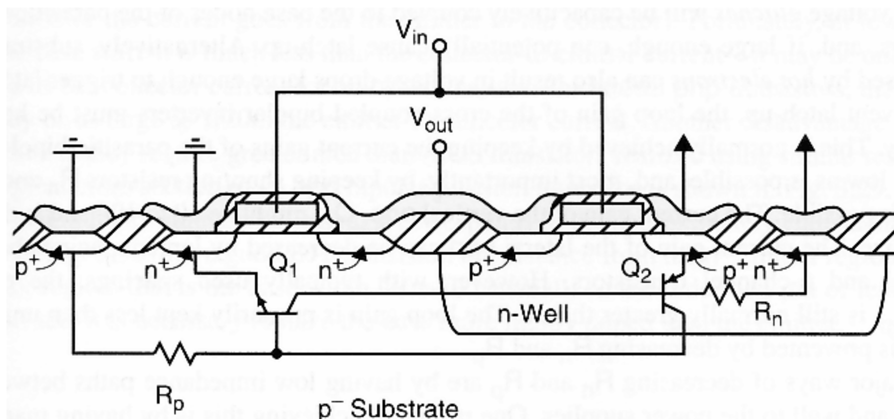
Substrate/well Contacts

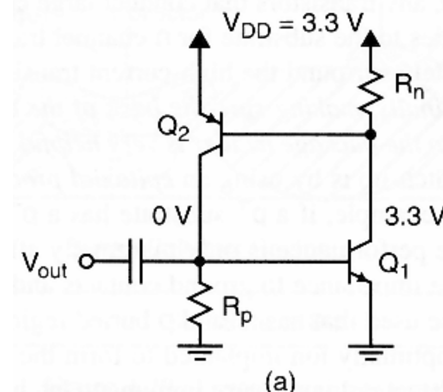
- Substrate and nWells must be connected to the power supply within each cell
  - use many connections to reduce resistance
  - generally place
    - ~ 1 substrate contact per nMOS tx
    - ~ 1 nWell contact per pMOS tx
  - this connection is called a tap, or plug
  - often done on top of VDD/Ground rails
  - need p+ plug to Ground at substrate
  - need n+ plug to VDD in nWell

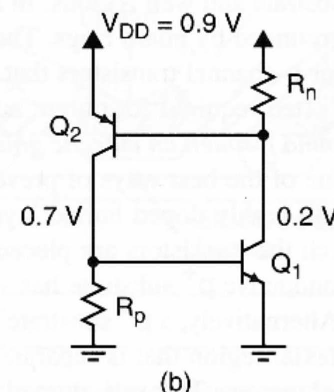


Latch-Up

- Latch-up is a very real, very important factor in circuit design that must be accounted for
- Due to (relatively) large current in substrate or n-well
  - create voltage drops across the resistive substrate/well
    - most common during large power/ground current spikes
  - turns on parasitic BJT devices, effectively shorting power & ground
    - often results in device failure with fused-open wire bonds or interconnects
  - hot carrier effects can also result in latch-up
    - latch-up very important for short channel devices
- Avoid latch-up by
  - including as many substrate/well contacts as possible
    - rule of thumb: one "plug" each time a tx connects to the power rail
  - limiting the maximum supply current on the chip

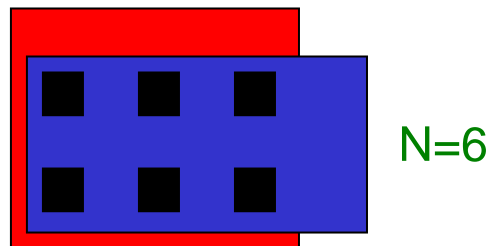




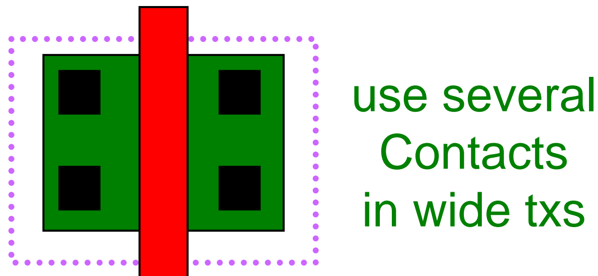


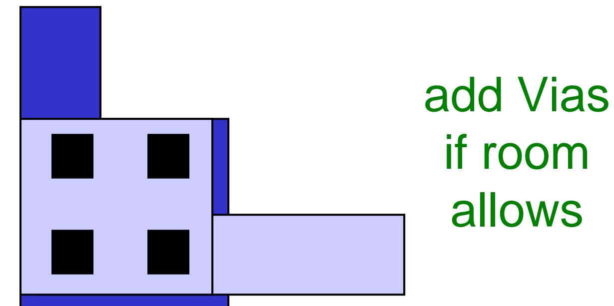
Multiple Contacts

- Each contact has a characteristic resistance, Rc
- Contact resistances are much higher than the resistance of most interconnect layers
- Multiple contacts can be used to reduce resistance
  - $R_{c,eff} = R_c / N$, N=number of contacts



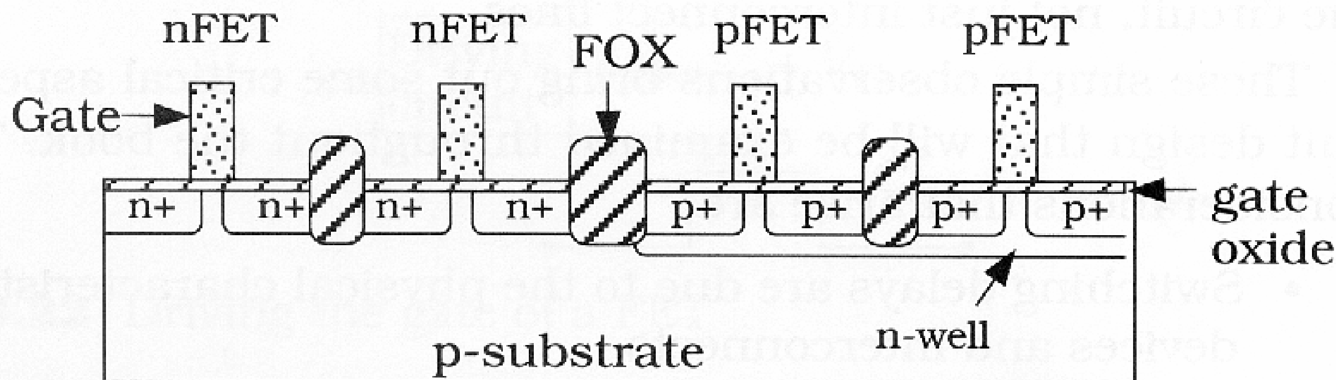
- Generally use as many contacts as space allows





CMOS Fabrication Process

- What is a "process"
  - sequence of step used to form circuits on a wafer
  - use additive (deposition) and subtractive (etching) steps
- n-well process
  - starts with p-type wafer (doped with acceptors)
    - can form nMOS directly on p-substrate
  - add an n-well to provide a place for pMOS
- Isolation between devices
  - thick insulator called Field Oxide, FOX



Overview of CMOS Fabrication

Topics:
- Wafer Growth
- Photolithography
- Doping
  - Diffusion
  - Implantation
- Oxidation
- Deposition
  - Dielectric
  - Polysilicon
  - Metals
- Etching
  - Chemical
  - Chemical-Mechanical
  - Mechanical
- Epitaxial Growth

Fig. 1-3 The fabrication process sequence of integrated circuits.

Wafer Growth

Methods - (1) Czochralski (CZ) (2) Horizontal Bridgman (3) Float Zone

•we will discuss only method #1 as it is the dominant production for Si

Seed
Melt
Noncontaminating liner
Graphite crucible
Growing crystal

(a) Seed being lowered down to melt

(b) Seed dipped in melt; freezing on seed just beginning

(c) Partially grown crystal

(a) As-grown crystal

(b) Grind crystal to remove undulations and saw to remove portions not in resistivity range

(c) Saw into slices (with orienting flats ground before sawing)

(d) Round edges of slice by grinding

(e) Lap and polish slice

•Create large ingots of semiconductor material by heating, twisting, and pulling. (~ 1-2 meters long by 100-300mm diameter)

•Entire ingot aligned to the same crystal lattice orientation (single-crystal).

•Remove all impurities → all one element.

•Slice ingot into very thin (~400-750µm) discs called wafers.

•Some wafer are uniformly doped with specific impurities (e.g. Boron for p-type wafer with $N_A = 10^{14}$ cm^{-3})

Photolithography

- Transfer desired pattern to an *optical mask* that is clear except where a pattern/shape is desired
- Cover the entire wafer surface with ***photoresist*** (PR) ~1μm thick
- (a-b) Expose the wafer to light through the optical mask
  - takes ~ 1-5 seconds exposure
- (c) Use chemical processing to remove PR only where it has been exposed to light
  - the pattern is now transferred from the optical mask to wafer surface

Resist
Wafer
Resist
Oxide
Wafer

spin on resist

Light source
Condenser lens
Mask
Projection lens
Image
Resist
Oxide
Wafer

illustration of ***projection printing***
other techniques:
contact and proximity printing

expose to light

Develop resist. Wafer — Developed resist showing pattern
Etch oxide. Wafer — Oxide etched to match resist pattern
Strip resist. Wafer — Resist removed

process wafer

Photolithography

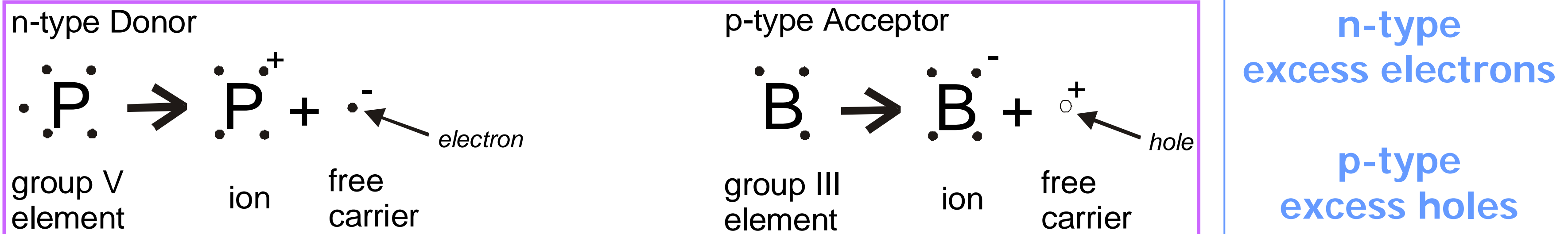
- (c) Subsequent process steps (e.g. oxidation, diffusion, deposition, etching) are performed. Fig. below shows etching of polysilicon
  - only areas without PR will be affected; PR blocks/masks remaining areas
- (d) After all necessary processing through PR pattern, remove all PR using a chemical process

photolithography and an example of etching polysilicon

Photomask
UV Light
Photomask
Photoresist
Polysilicon
(a)
(b)
Polysilicon
Photoresist
Etch
Photoresist
Polysilicon
(c)
Remove photoresist
Polysilicon
(d)

Doping: Diffusion

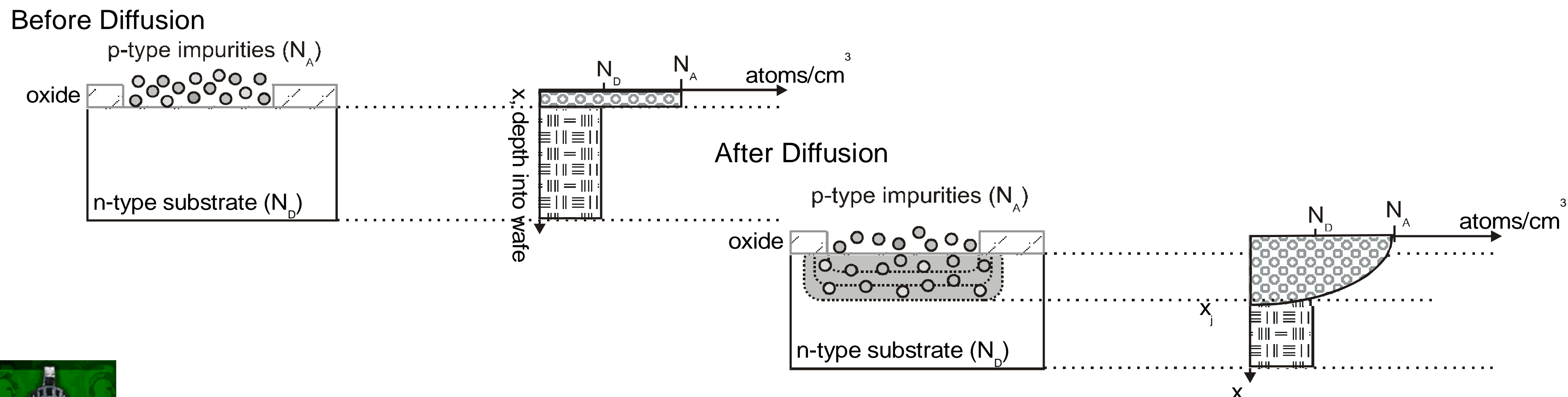
- *Doping*: addition of ***impurities*** (Phosphorus, Boron) to Si to change electrical properties by adding holes/electrons to the substrate
- *Diffusion*: movement of something from area of high concentration to area of low concentration



n-type
excess electrons

p-type
excess holes

- Masking layer (e.g. PR) used to block the wafer surface except where the dopants are desired



Diffusion

- Wafer placed in *high-temperature* furnace (~1000°C) with source of the impurity atom
  - high temperature speeds diffusion process
- Impurities uniformly spread into the exposed wafer surface at a shallow depth (0.5 - 5μm)
  - takes ~0.5 – 10 hours
  - concentration can be reliably controlled (~10^{12}-10^{19} cm^{-3})
- Profile different for (a) constant source and (b) finite source of impurities

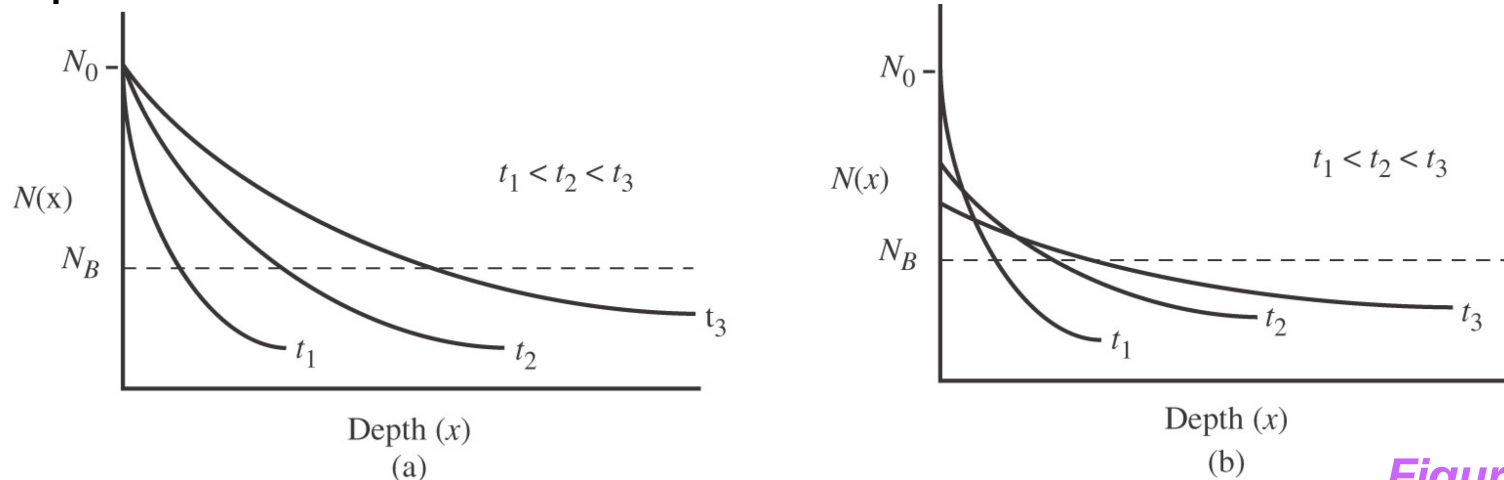


Figure 2.1-2

Doping: Ion Implantation

- Implantation functionally similar to diffusion
  - atoms are "shot" into the wafer surface
  - short (~10min.) high temperature (~800°C) *annealing* step fits the implanted atoms into the substrate crystal lattice

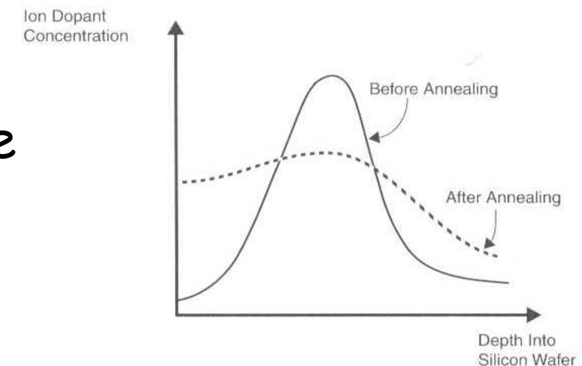
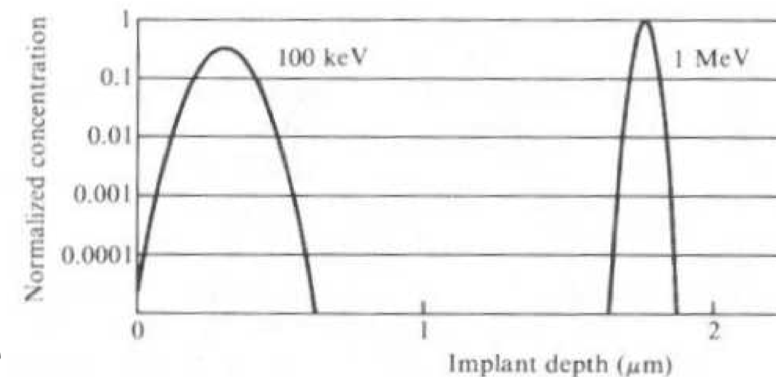


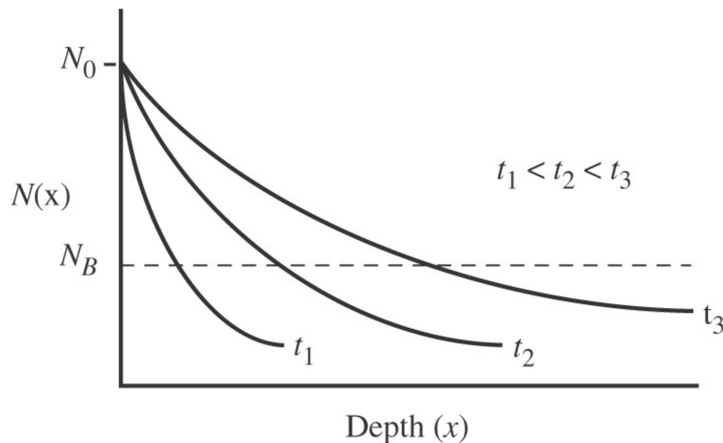
Figure 2.4 Dopant profiles after ion implantation both before and after annealing.

- Implantation vs. Diffusion - advantages
  - more uniform across the wafer than diffusion
  - allows for very precise control of where impurities will be
  - peak concentrations can be beneath the wafer surface
  - it does not require a long period of time at high temperature (which can be harmful).

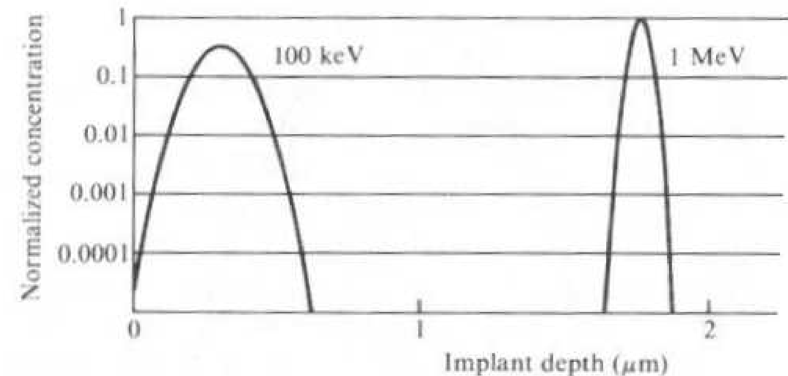


Doping: Ion Implantation

- Implantation vs. Diffusion -disadvantages
  - implanted junction must remain near wafer surface (~ 0.1 - 2μm)
  - cannot go as deep as a diffused junction.
- Impurity concentration profile (concentration vs. depth) is different for diffusion and implantation, but both are well known and predictable.



Diffusion



Implantation

Oxidation

- Insulating dielectric layers
  - key element in semiconductor fabrication
  - isolate conductive layers on the surface of the wafer.
- Si has a good *native oxide,*
  - Silicon oxidizes (combines with Oxygen) to form a dielectric oxide called silicon dioxide, SiO_2.
  - One of the most important reasons for the success of Silicon
- SiO_2
  - a good insulating layer
  - can be created by exposing Si to an O_2 environment
  - has similar material properties (e.g. thermal expansion coefficient, lattice size, etc.) of the native material (Si)
    - can be grown without creating significant stresses

Oxidation

- At elevated temperatures (~1000°C) the oxide grows quickly
  - native oxides grown at elevated temperatures are referred to as *thermal oxides*
  - thermal oxide grown in Si can be masked by PR
  - Si thermal oxide consumes 44% of its depth in Si

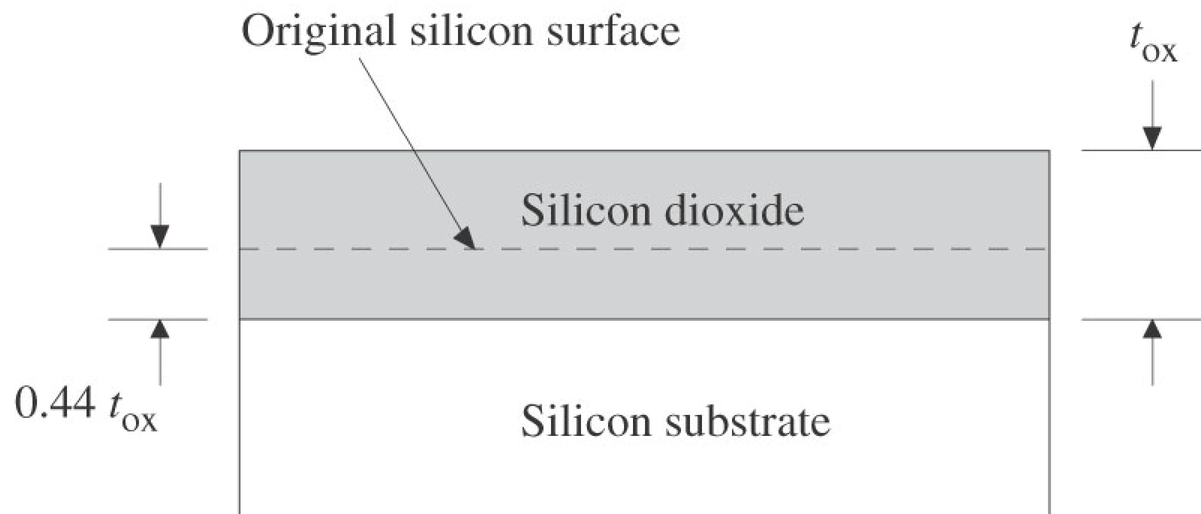


Figure 2.1-1

Deposition

Deposition: addition of materials to the top of wafer surface

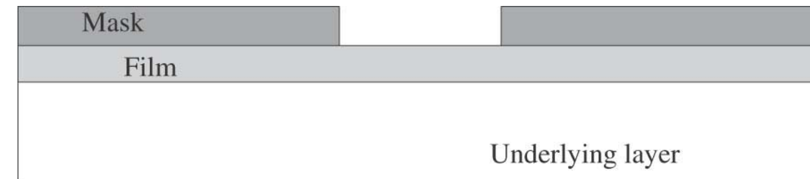
Dielectrics:
- Offer a variety of dielectric materials including SiO_2 and SiN.
- Can be deposited on top of all other materials used in semiconductor fabrication.
- Can be deposited in thick layers (~1-2 μm).

Polysilicon:
- Granular Si with similar material properties to single-crystal Si and SiO_2.
- Used to form MOS gates, resistors, capacitors, and memory cells.
- Native thermal oxide, SiO_2, can be grown on top of polysilicon.
- Can withstand subsequent high temperature steps (unlike metal)
- Can be doped to set resistance (low for interconnects, high for resistors)

Metals:
- Form low resistance interconnections.
- Can not withstand high temperature process steps.
- Many metal interconnect layers can be used, insulated by deposited dielectrics.

Etching

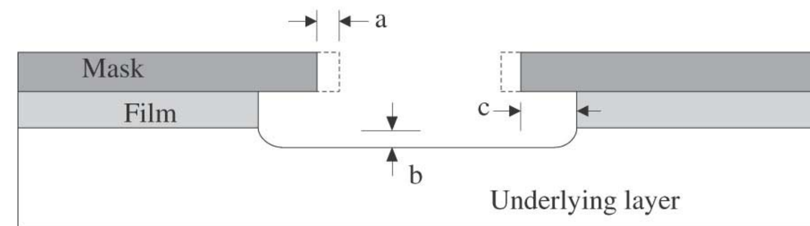
Etching: removal of materials from the wafer surface



(a)

Chemical Etching:

- Selective etching of desired material.
- Can be masked by PR or oxide.
- Isotropic etch will undercut masking layer



(b)

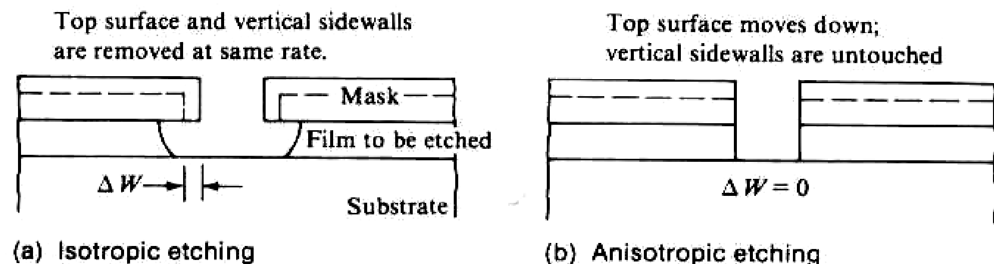
Figure 2.1-3

Chemical-Mechanical (Reactive Ion Etching):

- Mechanical etching process with some chemical selectivity.
- Can be masked by PR or oxide.
- Anisotropic etch → no undercut.

Mechanical (Ion Milling):

- No material selectivity
  → must be blocked by thick mask
- Anisotropic etch → no undercut



(a) Isotropic etching (b) Anisotropic etching

Epitaxial Growth

Epitaxial growth: process of creating single-crystal silicon from a thick layer of deposited silicon (polysilicon)

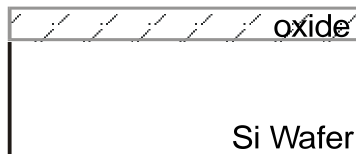
Process is somewhat complex and involves the use of a "seed crystal" that allows an annealing process to align the crystals of the deposited material

- Create single-crystal material from deposited (non-single-crystal) material
- Epitaxial layer has constant doping profile
  - important for buried layers in bipolar transistors
- Epi doping can be higher or lower and of same or opposite type than substrate doping
- Epi layer can be very thick (~1-20 μm).
- Epi layer formed by annealing a deposited layer from a "seed crystal"

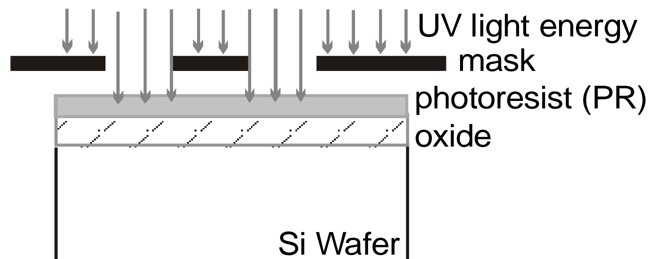
Example Photolithography Process

Patterning an oxide layer for diffusion of impurities (forming a pn junction).

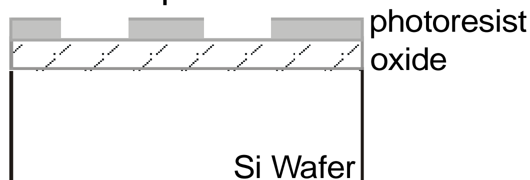
1) Example: patterning oxide layer



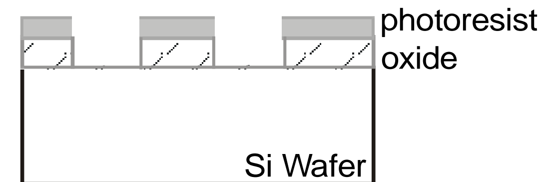
2) Expose PR to light energy though optical mask



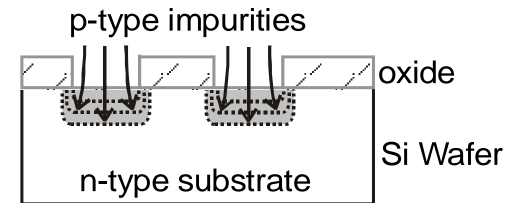
3) Remove exposed PR



4) Etch through mask created by PR



5) Remove PR and diffuse through oxide mask

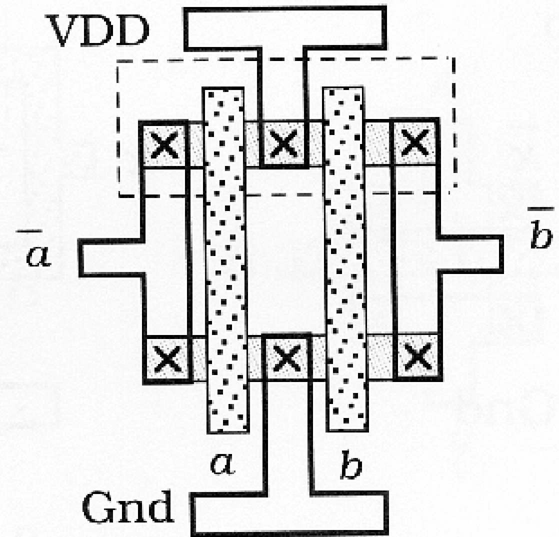


CMOS Fabrication Sequence

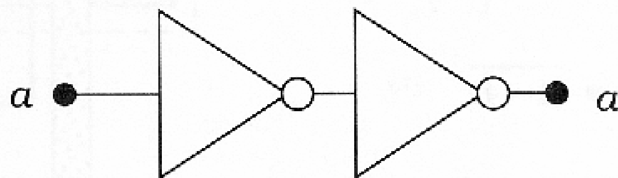
- view LOCOS slide show

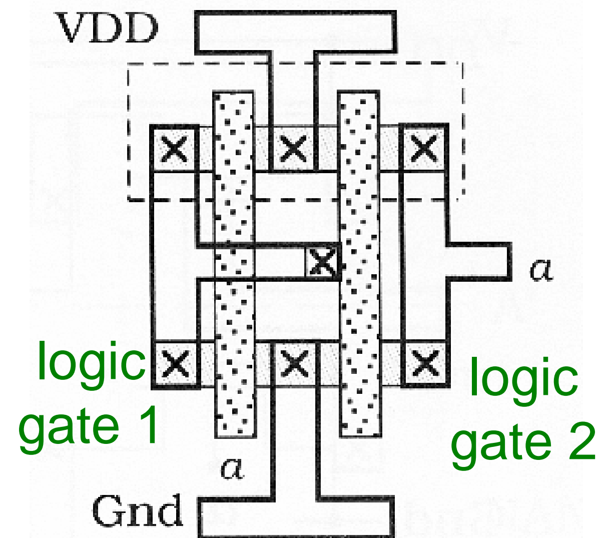
Multi Functional Cells

- Sharing power supply rail connections
  - independent gate inputs and outputs
  - shared power supply nodes
  - logic function?



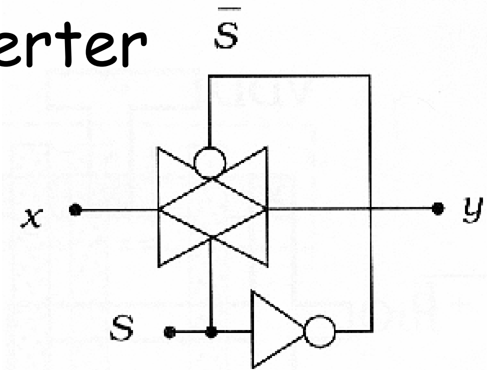
- Cascaded Gates
  - output of gate 1 = input of gate 2
    - g1 output metal connected (via contact) to g2 gate poly
  - shared power supply node
  - function?
    - non-inverting buffer

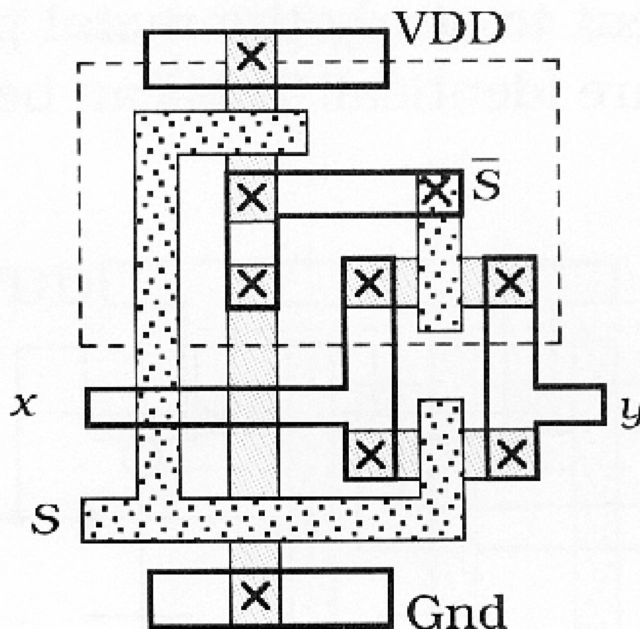




Complex Intra-Cell Routing

- Transmission gate with built-in select inverter
  - one TG gate driven by s at inverter input
  - one TG gate driven by s' at inverter output
  - complicates poly routing inside the cell
    - figures uses n+ to route signal under metal 1
      - not great choice due to higher S/D junction capacitance

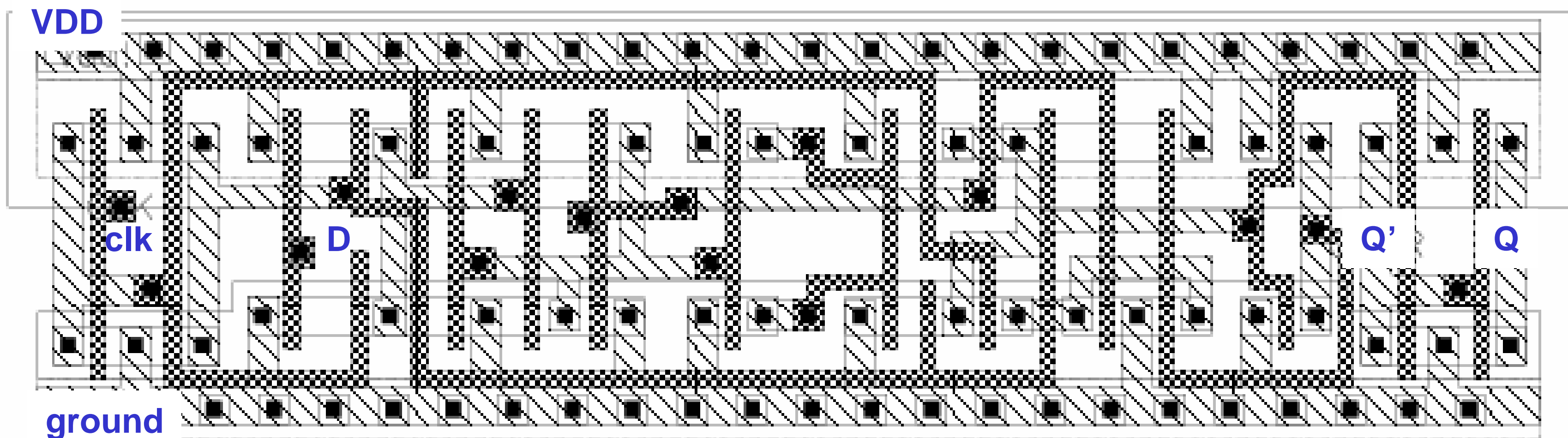




- Routing rules
  - poly can cross all layers except
    - poly (can't cross itself)
    - active (n+/p+), this forms a transistor
  - metal can cross all layers except
    - metal (can't cross itself)

Example: Layout of Complex Cell

- D-type Flip Flop with Reset
  - covered in Lab 7



- Features
  - same pitch as ECE410 inv, nand, nor, xor cells
  - complex intra-cell poly routing
    - passing under, above and between transistors
  - most I/O ports accessible via M1 or poly (M2 required for D)

Mapping Schematics to Layout

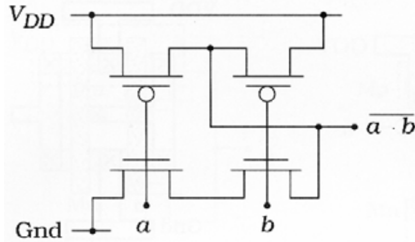
- Layout organization: how to optimize layout connections
  - trial and error
    - works OK for simple gates but can require a lot of iterations
  - Stick Diagrams
    - simple method to draw layout options and see what is best before committing to "real" layouts
- Mapping techniques: how to arrange txs in layout
  - trial and error
    - works OK for simple gates
  - Euler Graph (pronounced "oiler")
    - graphical method to determine transistor arrangement in layout
- Best approach: combine some Euler Graph methods and Stick Diagrams

Stick Diagram
method for sketching layouts

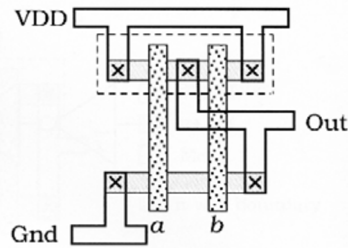
- Motivation
  - often hard to predict best way to make connections within a cell
  - Stick Diagram is a simple sketch of the layout that can easily be changed/modified/redrawn with minimal effort
- Stick Diagram
  - shows only active, poly, metal, **contact**, and n-well layers
  - each layer is color coded (typically use colored pencils or pens)
  - active, poly, metal traces are drawn with lines (not rectangles)
  - contacts are marked with an X
    - typically only need to show contacts between metal and active
  - n-well are indicated by a rectangle around pMOS transistors
    - typically using dashed lines
- Show routing between tx's, to VDD, Ground and Output

Stick Diagram NAND & NOR

- Simplified NAND Layout

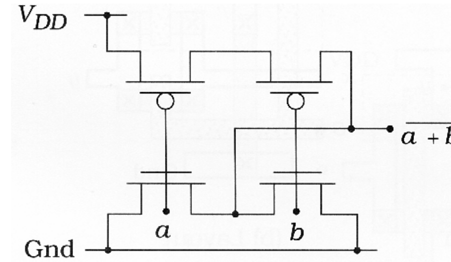


(a) Circuit

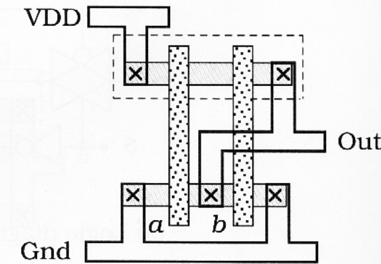


(b) Layer design

- Simplified NOR Layout



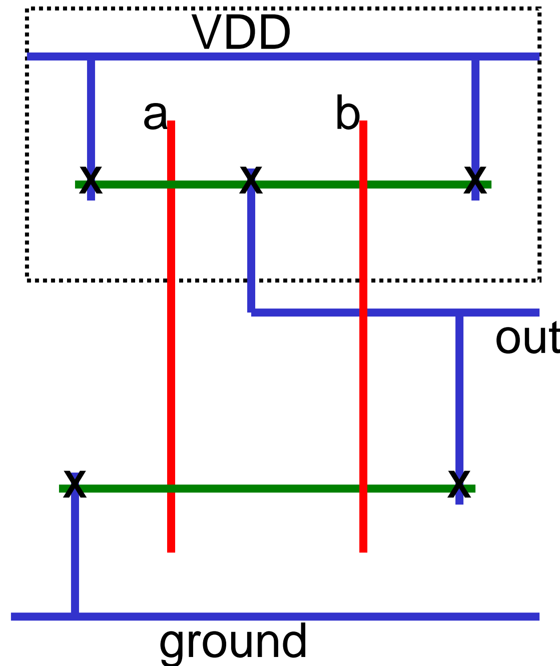
(a) Circuit

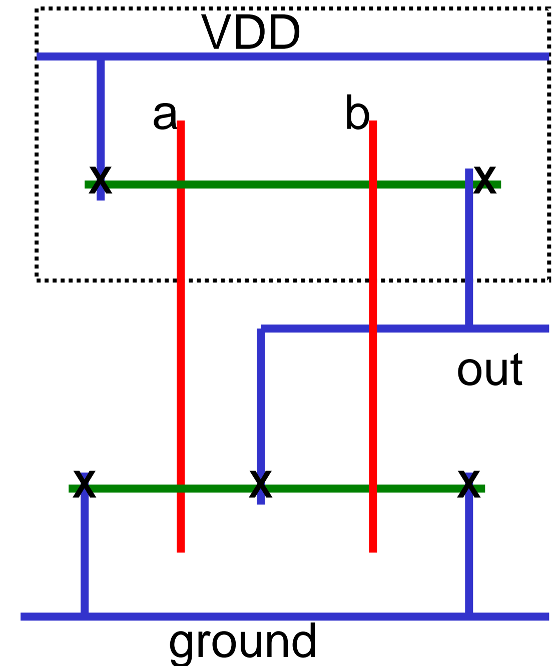


(b) Layer design

Stick Diagram

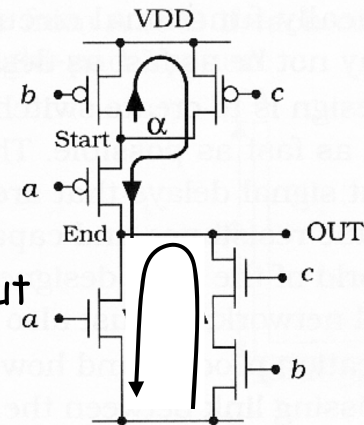
- Metal supply rails
  - blue
- n and p Active
  - green
- Poly gates
  - red
- Metal connections
  - supply, outputs
- Contacts
  - black X
- N-Well (optional)
  - dashed rectangle





Euler "Path"

- Euler "Path"
  - simplified layout methodology for multi-input circuits; based on Euler Graphs
    - see textbook for full Euler Graph method; unnecessarily confusing for most students
  - used to determine what order (left to right) to layout transistors
  - identifies if all transistors will fit onto a single (non-broken) active strip
- Method
  - try to draw a loop through all transistors
    - separate loop for nMOS and pMOS
    - starting point can be anywhere; may need to try different points to achieve goals
- Rules
  - can only trace through each transistor once
    - otherwise layout won't match schematic
  - can only re-cross any point/node once
    - otherwise multiple ***active*** strips will be required to complete layout
  - must trace through nMOS in the same order as pMOS

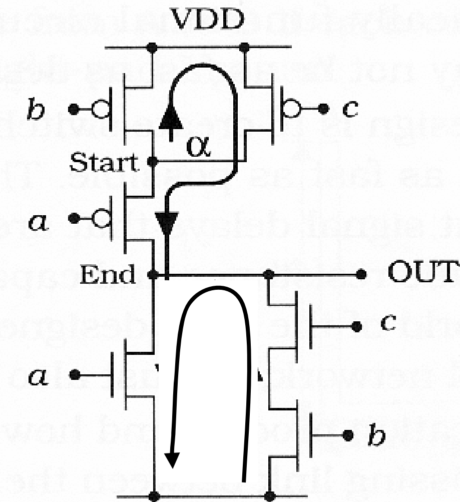


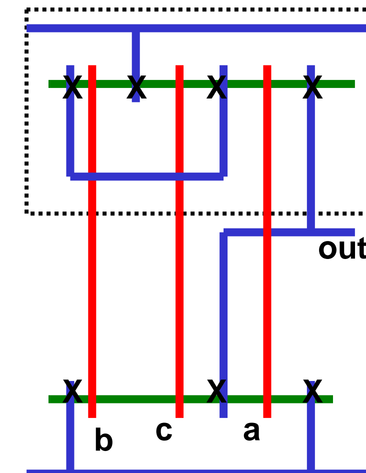
may have to rearrange txs in schematic (without changing function) to achieve rules

Euler Path Example

Example: OUT = a + bc

- PMOS Loop
  - start pMOS at node *α*, through 'b' to ***VDD***, through 'c' to *α*, through 'a' to OUT
  - check loop follows rules
- NMOS Loop
  - trace through same tx order as pMOS
  - start nMOS at ground, through 'b' and to 'c' *OUT* then through 'a' to *OUT* again
- Form stick diagram with polys in order b, c, a determined by Euler Path



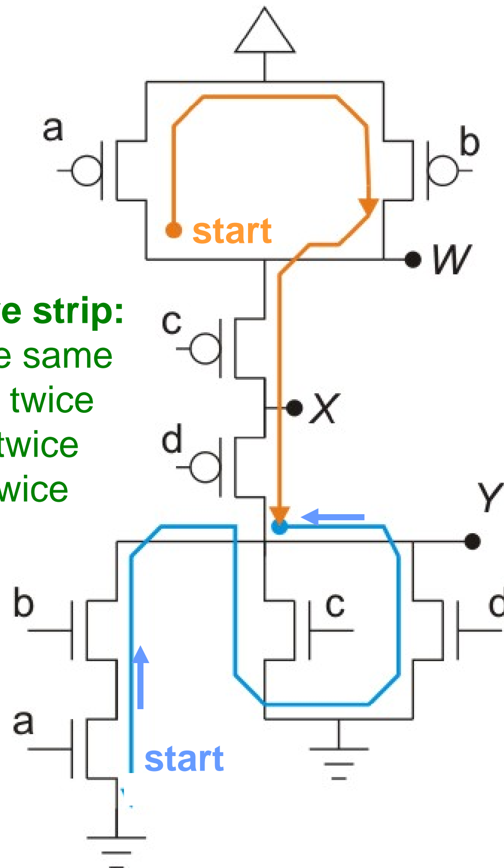


- Alternative Loops
  - start pMOS loop at OUT, through a, then b, then c.
  - to follow pMOS loop order, start at OUT, through a to ground then b, then c

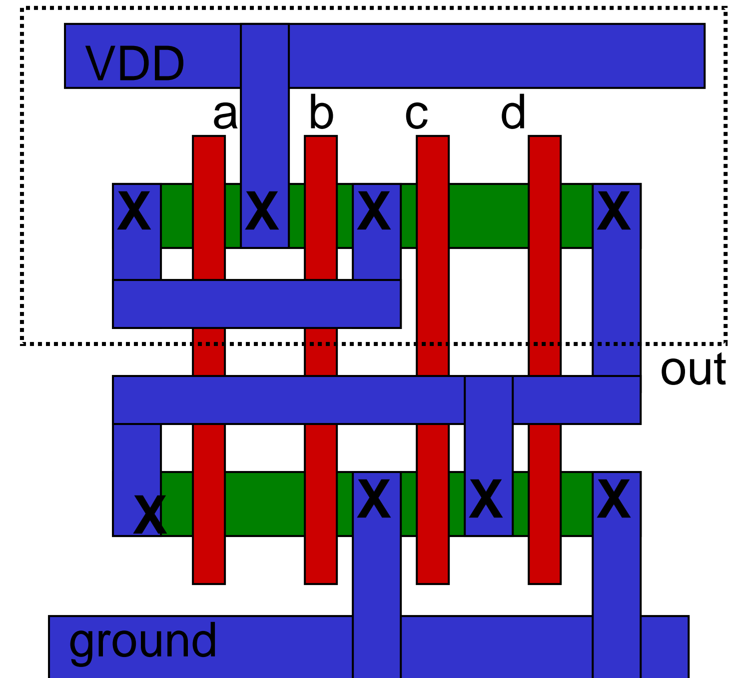
Example

- Circuit with pMOS and nMOS paths

Rule for single active strip:
loop can not cross the same point/node more than twice
- pMOS through W twice
- nMOS through Y twice



- Stick Diagram

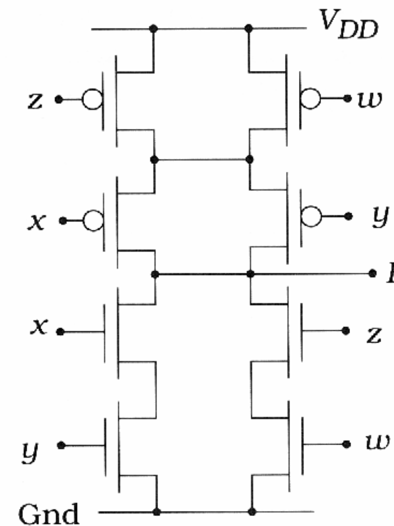


- Shows layout can be constructed with a single p/n active trace.
- Order of txs (poly traces) is a, b, c, d, on both p- and n-side

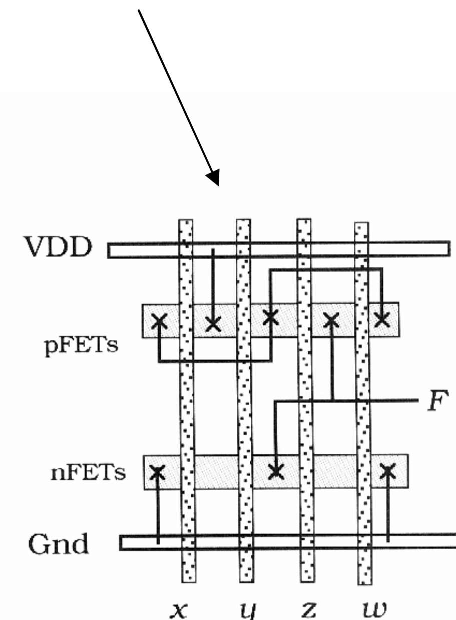
Structured Layout

- General Approach
  - power rails
  - horizontal Active
  - vertical Poly (inputs from top/bottom)
  - Metal1 connects nodes as needed in schematic
- Structured Layout
  - AOI circuit figure
  - useful for many logic functions
  - see examples in textbook
- Disadvantages
  - not optimized for speed
    - large S/D regions = higher capacitance
    - interconnect paths could be shorter
  - not optimized for area/size

good example of a "regular" cell layout useful for general logic functions



(a) Circuit

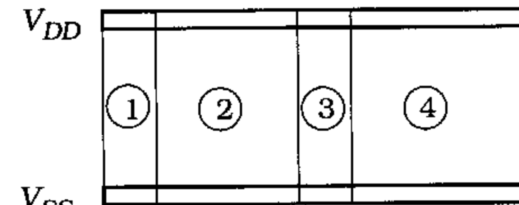


(b) Layout wiring

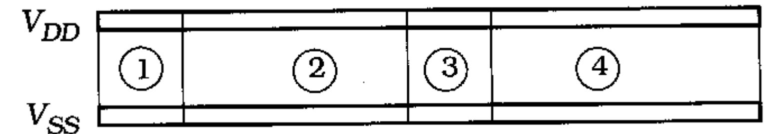
notice, need room inside cell (between VDD and Ground) to route internal connections

Transistor Orientation

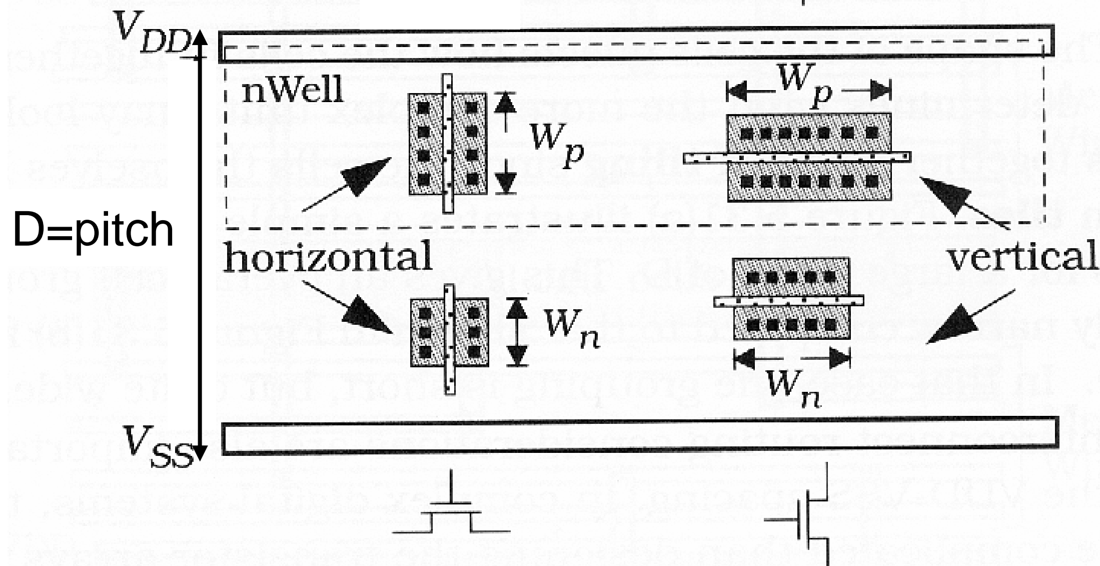
- Horizontal Tx (W run *vertically*)
  - can increase tx W with fixed pitch
  - cells short & wide
- Vertical Tx (W runs *horizontally*)
  - pitch sets max tx W
  - cells taller & narrow



(a) Larger D

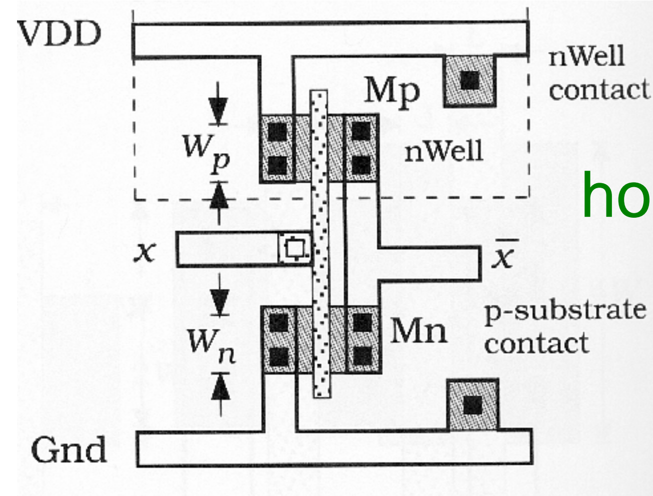


(b) Smaller D

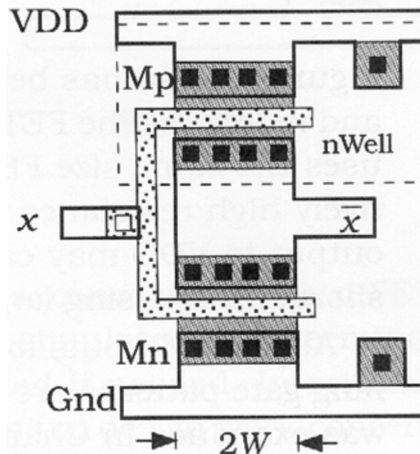


Inverter Layout Options

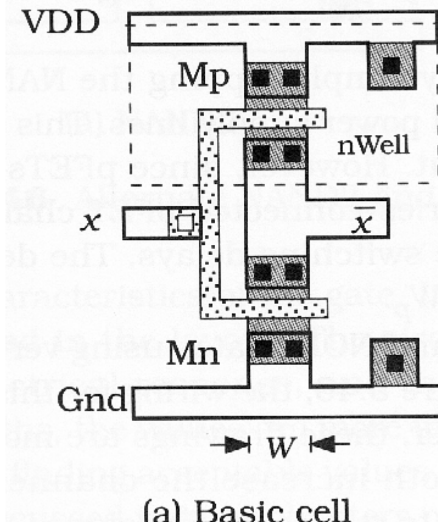
- Layout with Horizontal Tx
  - pitch sets max tx size
- Layout with Vertical Tx
  - allows tx size scaling without changing pitch
- Vertical Tx with 2x scaling



horizontal



(b) 2X cell

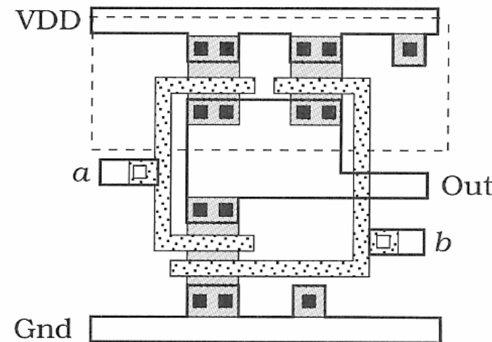


(a) Basic cell

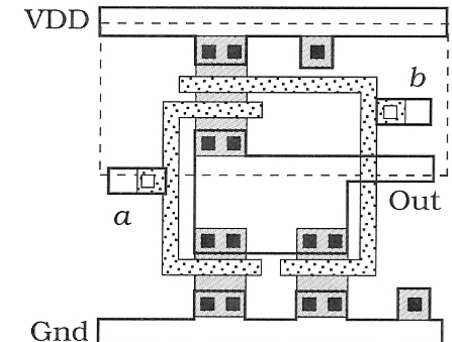
vertical

NAND/NOR Layout Alternatives

- vertical transistors
  - for smaller pitch (height) and wider cell

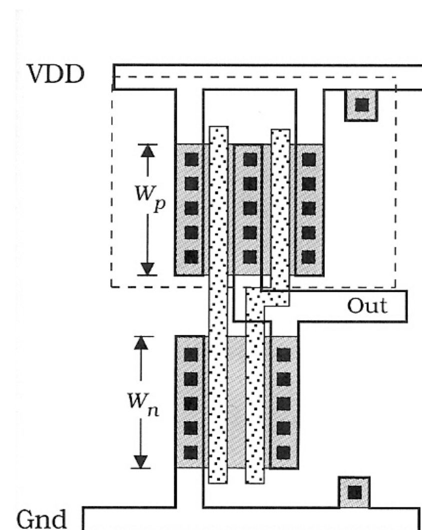


(a) NAND2 gate

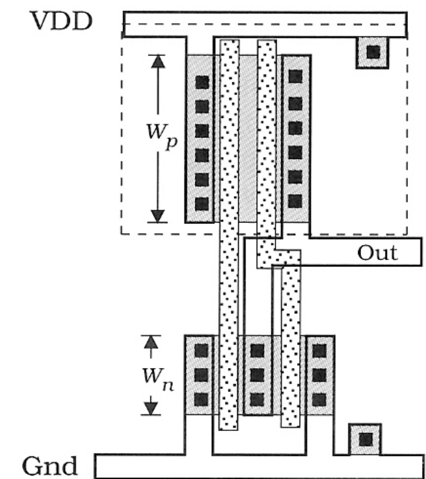


(b) NOR2 gate

- large horizontal transistors
  - for larger pitch (height) and narrower cell



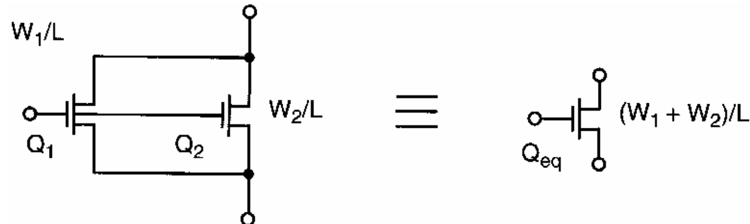
(a) NAND2



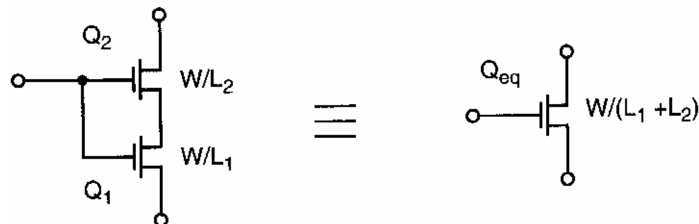
(b) NOR2

Building Large Transistors

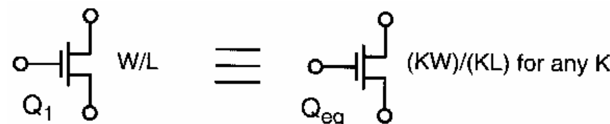
- Larger (up to 100xL) width (W) transistors sometimes needed
  - more common on analog than digital, but might need in buffers
  - NOTE: effective width (W) of parallel transistors add



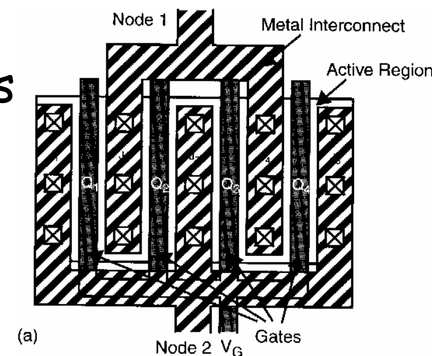
  - create wide tx using parallel (interdigitated) transistors
    - 4x wide transistor between node A (red) and B (blue)
- Series Transistors
  - increases effective L

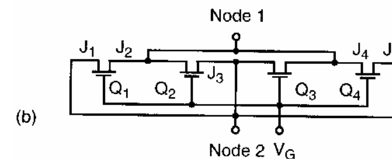


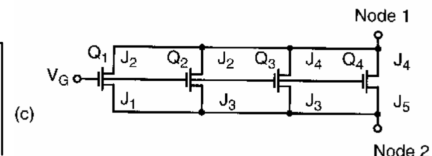
- Scale both W and L
  - no effective change in W/L
  - increases gate capacitance



Layout of Large W Txs

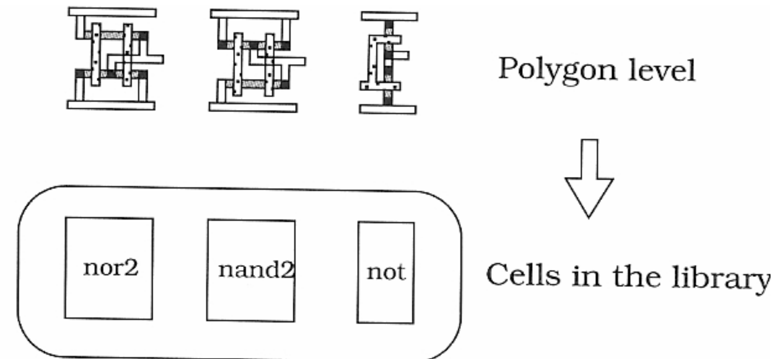




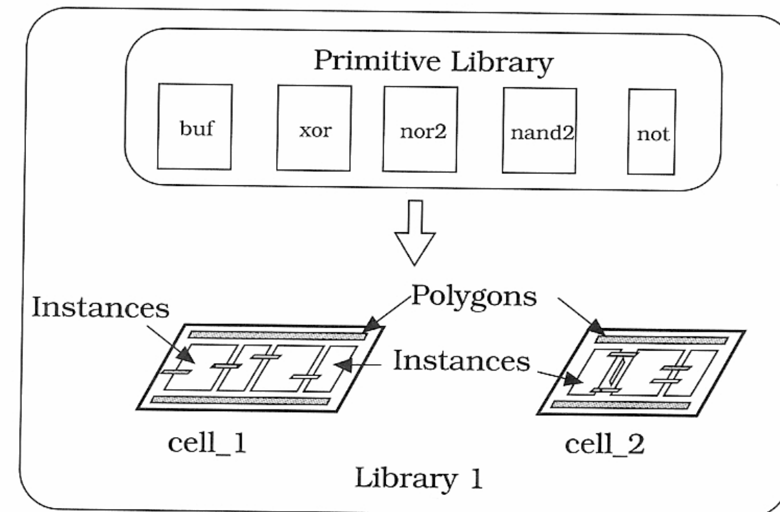


The Cell Concept

- Each physical design file is called a "cell"
- "Primitive" cells, polygon-level
  - create "cell library" of basic functions

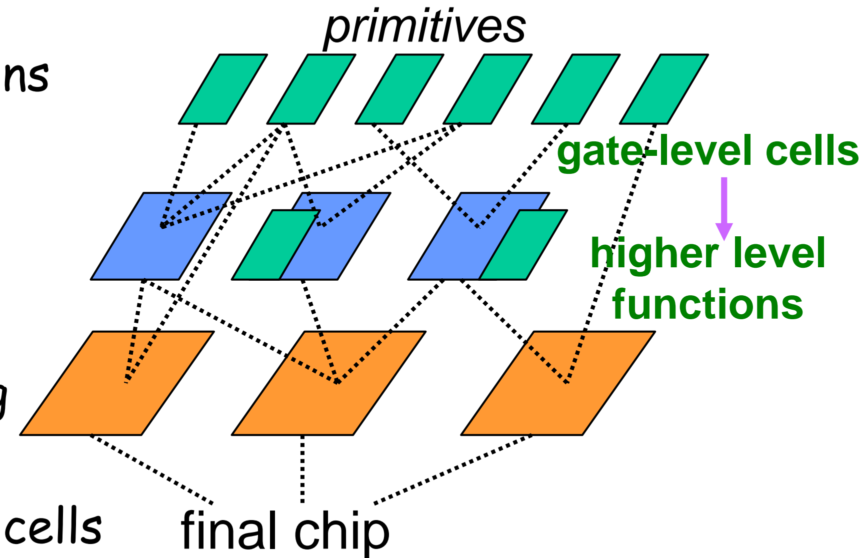


- Expanding library with more complex cells
  - primitive library cells added as to higher level cells to create more complex logic functions
  - the instantiated (added) cell is called an "instance"



Hierarchical Design

- Start with *Primitives*
  - basic transistor-level gates/functions
    - optimize performance and layout
  - layout with polygons
- Build larger cells from primitives
  - layout with instances of primitives
  - polygons for transistors and routing
- Build even larger cells
  - layout with instances of lower level cells
  - polygons only for signal routing
- Repeat for necessary levels of hierarchy until Final Chip

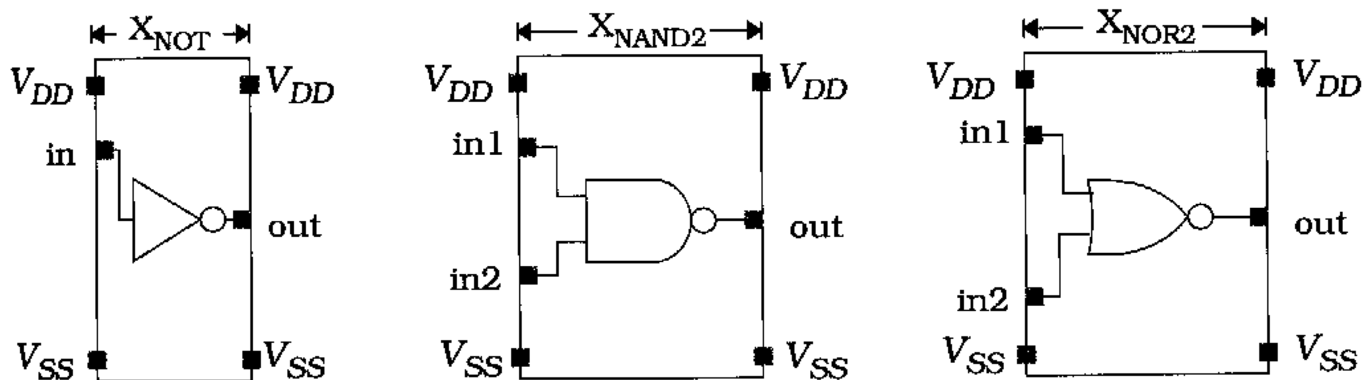


- Advantages of Hierarchical Design
  - allow layout optimization within each cell
  - eases layout effort at higher level
    - higher level layout deal with interconnects rather than tx layout

Primitives must be done using **custom** techniques, but higher level layout can use automated (***place-and-route***) CAD tools.

Cell View and Cell Ports

- Cell View
  - see only I/O ports (including power), typically in Metal1
  - can't see internal layer polygons of the primitive



Cell-level view of INV, NAND, and NOR primitives

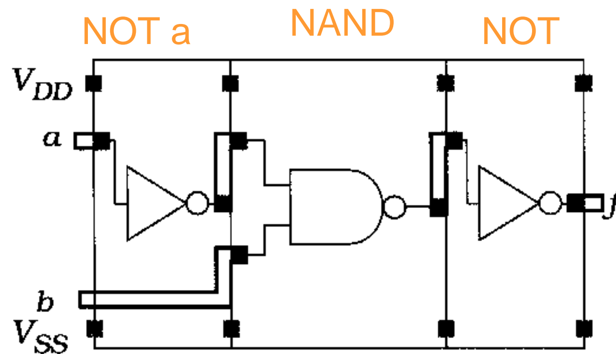
- Ports
  - all signals that connect to higher level cells
  - physical locations of the layout cell, typically in Metal1 or Metal2
- Metal1 vs Metal2 ports
  - best to keep ports in Metal1 for primitives
  - always try to use only the lowest level metals you can

Hierarchical Design Concepts

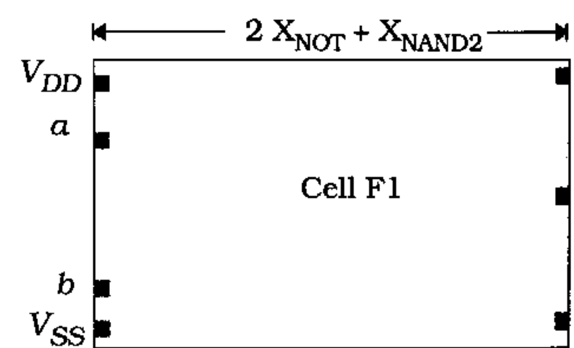
- Building Functions from Primitives
  - instantiate one or more lower-level cells to from higher-level function
  - Example: $f = a\,\overline{b}$

new cell has **ports** a, b, f (output), VDD, Gnd

NOT a NAND NOT



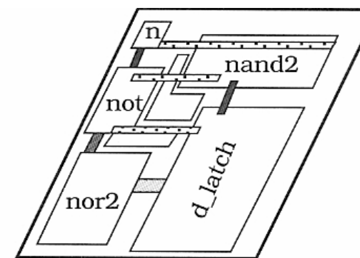
(a) Primitive cells



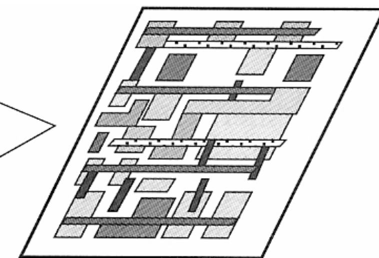
(b) New complex cell

- Final Chip
  - flatten all cells to create one level of polygons
  - allows masks to be made for each layout layer
  - removes hierarchy

IMPORTANT:
Don't flatten your cells! There are other ways to peak (see) lower level cells instantiated within a higher level cell.



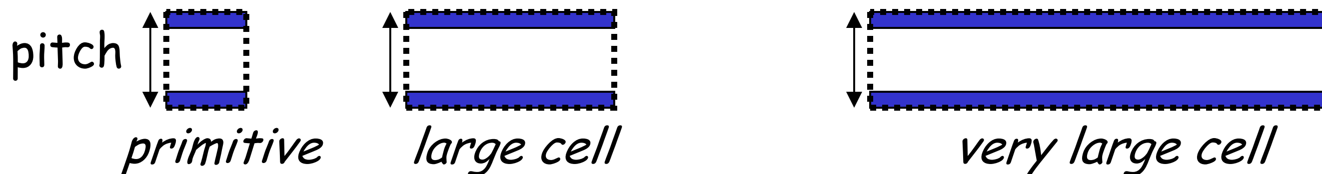
Cells and polygons



Polygons

Layout of Large Cells

- All cells should be formed within the standard cell pitch
  - pitch (cell height) set by primitives
  - non-standard cells complicate higher level layout
  - how do you layout 20+ transistors?
- Wide Cells
  - general rule: make cell as wide as necessary to maintain pitch



- Double Pitch Cells
  - non-standard approach, only for full custom designs
  - form cell with height 2 x pitch
  - internal power pass-through