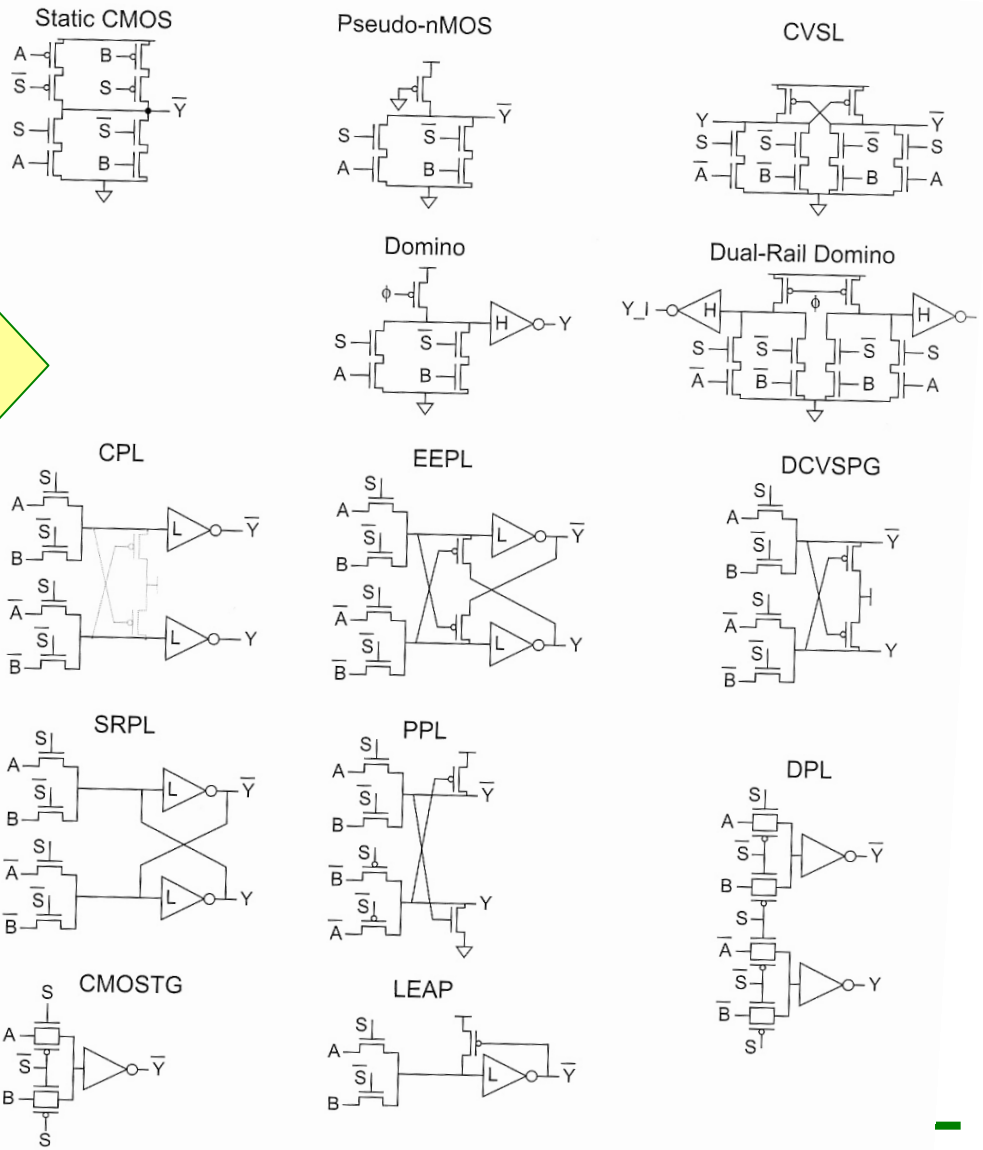
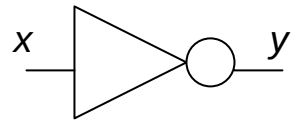
CMOS Logic Families

- Many "families" of logic exist beyond Static CMOS
- Comparison of logic families for a 2-input multiplexer
- Briefly overview
  - pseudo-nMOS
  - differential (CVSL)
  - dynamic/domino
  - complementary pass-gate



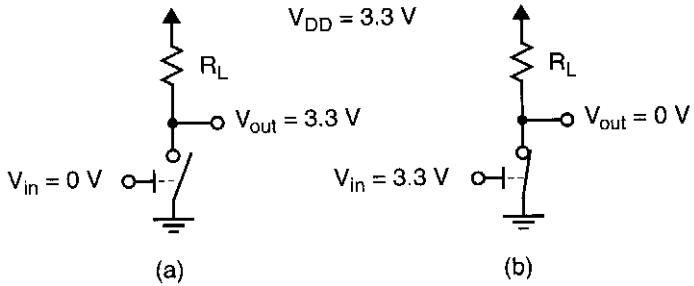
nMOS Inverter

- Logic Inverter
- nMOS Inverter
  - assume a resistive load to VDD
  - nMOS switches pull output low based on inputs



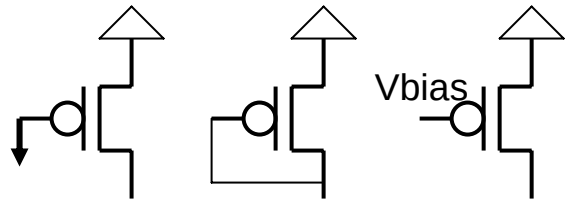
x	$y = \overline{x}$
0	1
1	0

nMOS Inverter



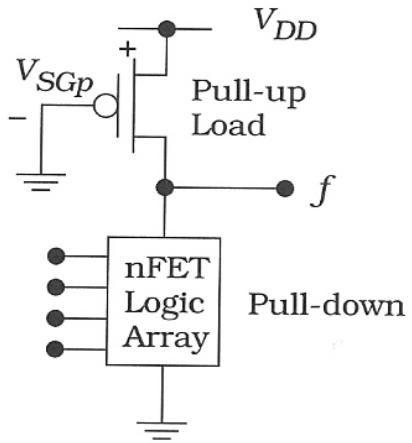
(a) nMOS is **off**,
(b) nMOS is **on**

- Active loads
  - use pMOS transistor in place of resistor
  - resistance varies with Gate connection
    - Ground → always on
    - Drain=Output → turns off when Vout > VDD-Vtp
      - $V_{SG} = V_{SD}$ so <u>always in saturation</u>
    - Vbias → can turn Vbias for needed switching characteristics

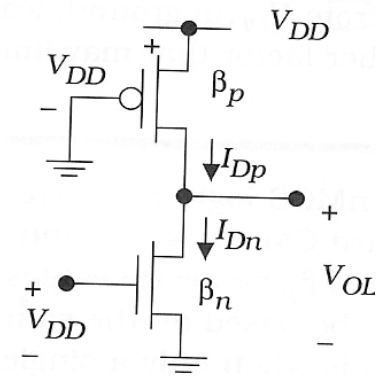


Pseudo-nMOS

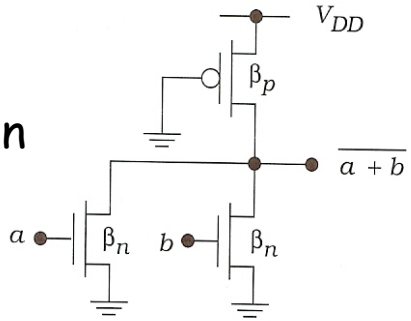
- full nMOS logic array
- replace pMOS array with single pull up transistor
- Ratioed Logic
  - requires proper tx size ratios
- Advantages
  - less load capacitance on input signals
    - faster switching
  - fewer transistors
    - higher circuit density
- Disadvantage
  - pull up is always on
    - significant static power dissipation
  - $V_{OL} > 0$

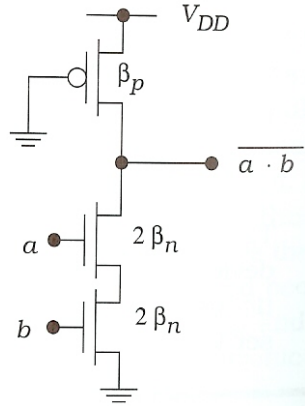


generic pseudo-nMOS logic gate



pseudo-nMOS inverter





pseudo-nMOS NAND and NOR

Pseudo nMOS DC Operation

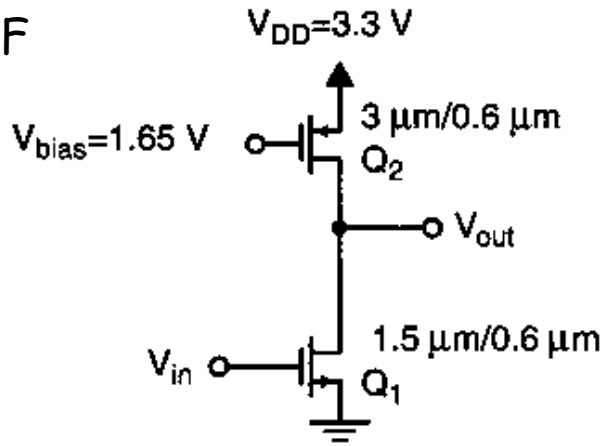
- Output High Voltage, V_{OH} (Maximum output)
  - occurs when input is low (Vin = 0V), nMOS is OFF
  - pMOS has very small V_{SD} → triode operation

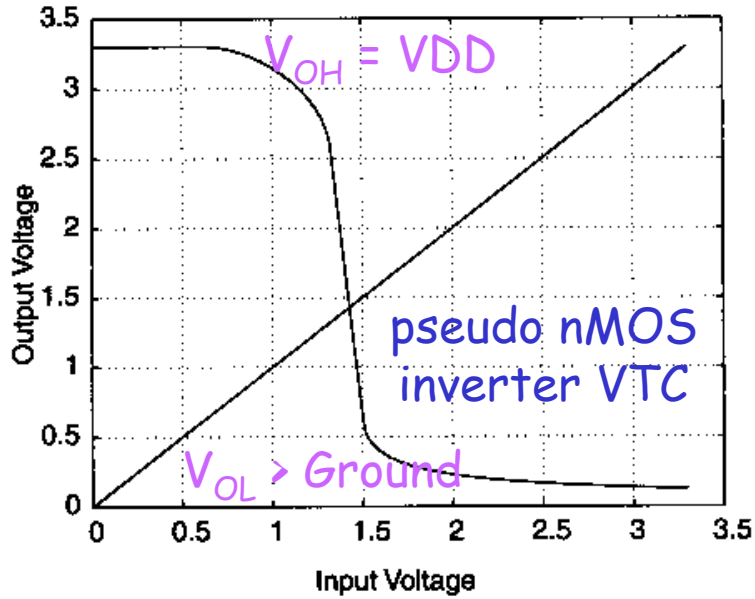
$$I_{D2} \cong \mu_p C_{ox} \left(\frac{W}{L}\right)_2 V_{eff\text{-}2} V_{SD\text{-}2}$$

  - pMOS pulls Vout to VDD
  - V_{OH} = VDD
- Output Low Voltage, V_{OL} (Minimum output)
  - occurs when input is high (Vin = VDD)
  - both nMOS and pMOS are ON
    - nMOS is "on stronger"; pulls Vout low
  - as Vout goes low, nMOS enters triode
    - continues to sink current from pMOS load

$$V_{OL} = I_{D\text{-}2} r_{ds\text{-}1} = \frac{1}{2}\frac{\mu_p (V_{DD}/2 + V_{tp})^2}{\mu_n (V_{DD} - V_{tn})} \frac{(W/L)_2}{(W/L)_1}$$

  - V_{OL} > 0 V (active load always pulling)
- Logic Swing (max output swing)
  - $V_L = V_{OH} - V_{OL} < VDD$

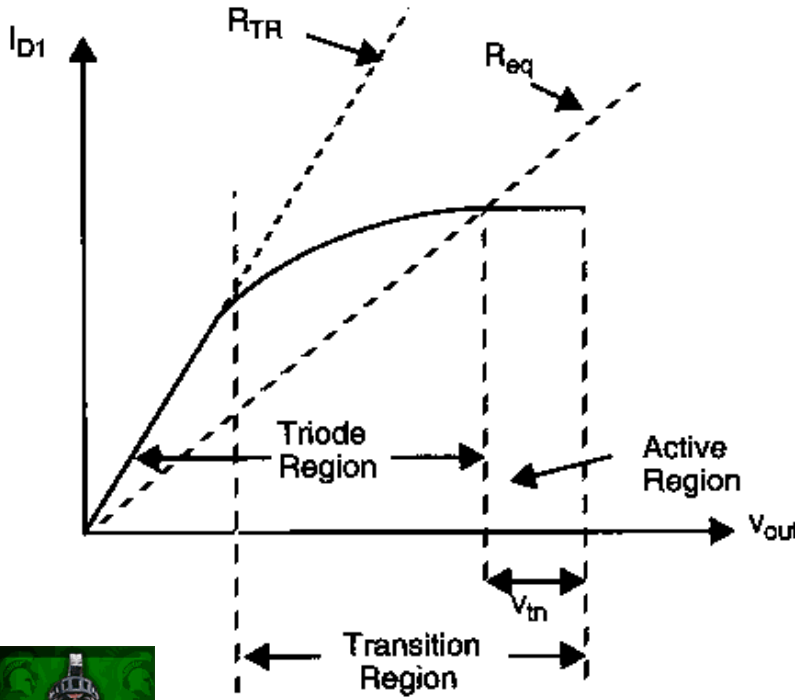


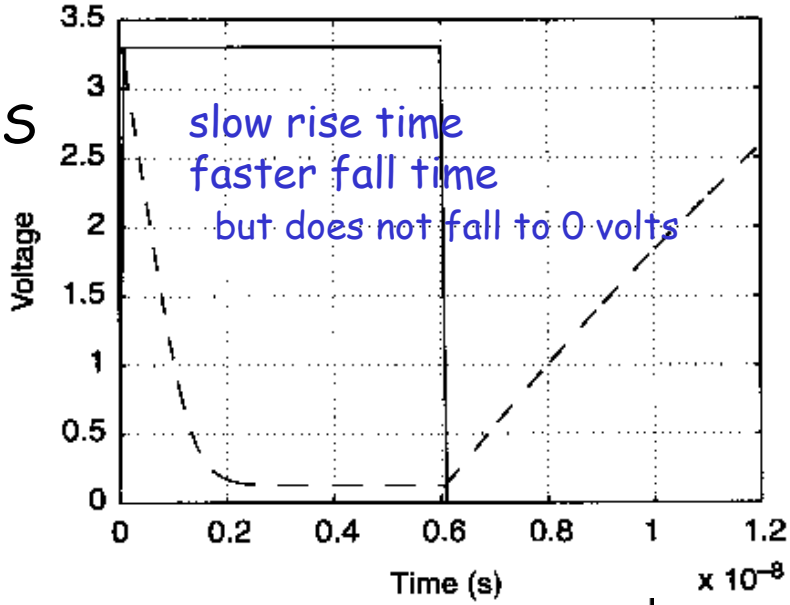


Pseudo nMOS Transient Analysis

- Rise and Fall Times
  - harder to analyze for pseudo nMOS
  - due to "always on" active load

$$t_{+70\%} = \frac{C_L}{I_{D-2}}\Delta V_{out} = \frac{2C_L 2.3}{\mu_p C_{ox}(W/L)_2[(V_{DD}/2) + V_{tp}]^2}$$





$$I_{D-1} = \frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right)_1 (V_{DD} - V_{tn})^2$$

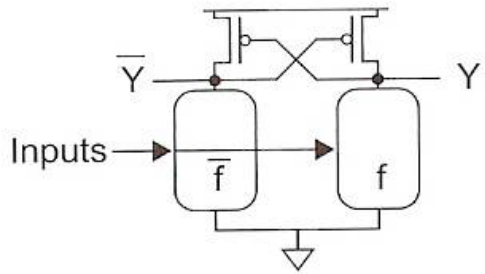
$$R_{TR} = \frac{1}{\mu_n C_{ox}(W/L)_1(V_{DD} - V_{tn})}$$

$$R_{eq} = \frac{V_{DD} - V_{tn}}{\frac{\mu_n C_{ox}}{2}(W/L)_1(V_{DD} - V_{tn})^2} = \frac{2}{\mu_n C_{ox}(W/L)_1(V_{DD} - V_{tn})}$$

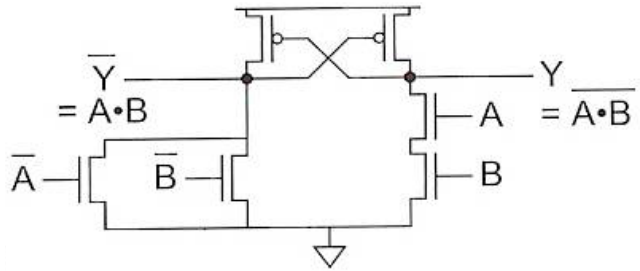
$$R_{eq} = \frac{2.5}{\mu_n C_{ox}(W/L)_1(V_{DD} - V_{tn})}$$

Differential Logic

- Cascode Voltage Switch Logic (CVSL)
  - aka, Differential Logic
- Performance advantage of ratioed circuits without the extra power
- Requires complementary inputs
  - produces complementary outputs
- Operation
  - two nMOS arrays
    - one for f, one for $\overline{f}$
  - cross-coupled load pMOS
  - one path is always active
    - since either f or $\overline{f}$ is always true
  - other path is turned off
    - no static power



generic differential logic gate

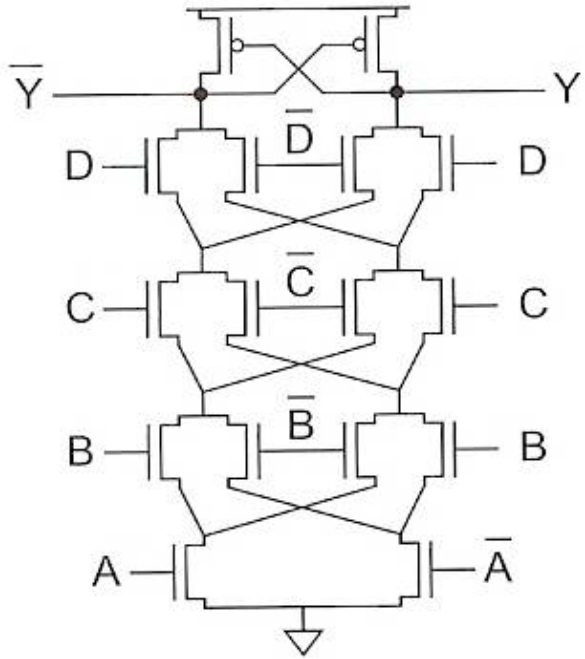


differential AND/NAND gate

(logic arrays turns off one load)

Differential Logic

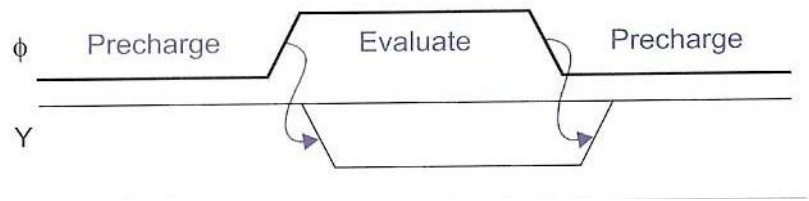
- Advantages of CVSL
  - low load capacitance on inputs
  - no static power consumption
  - automatic complementary functions
- Disadvantages
  - requires complementary inputs
  - more transistors
    - for single function
- Very useful in some circuit blocks where complementary signals are generally needed
  - interesting implementation in adders



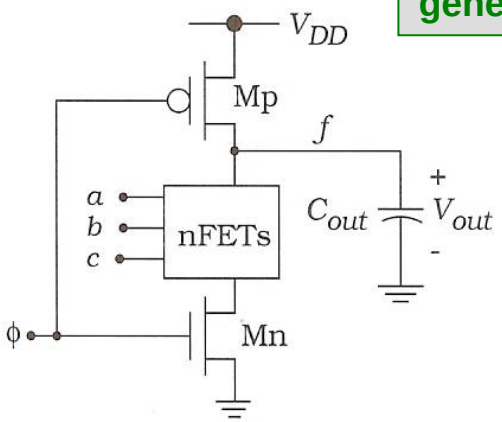
differential 4-input XOR/XNOR

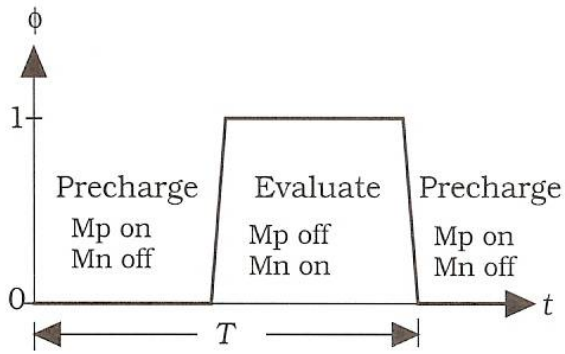
Dynamic Logic

- Advantages of ratioed logic without power consumption of pseudo-nMOS or excess tx of differential
- Dynamic operation: output not always valid
- Precharge stage
  - clock-gated pull-up precharges output high
  - logic array disabled
- Evaluation stage
  - precharge pull-up disabled
  - logic array enabled & if true, discharges output



generic dynamic logic gate





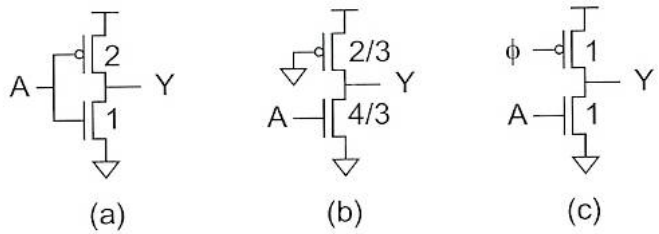
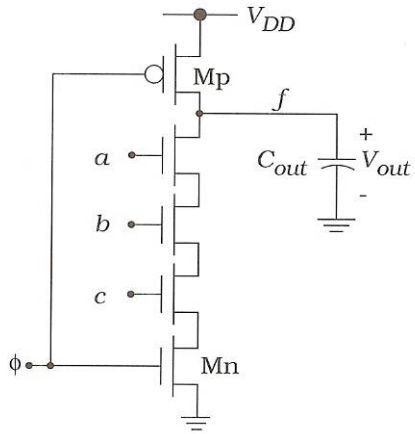


FIG 6.21 Comparison of (a) static CMOS, (b) pseudo-nMOS, and (c) dynamic inverters

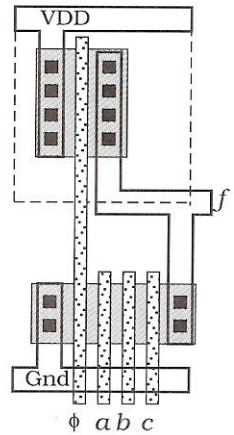
Dynamic Logic

- Example: Footed dynamic NAND3

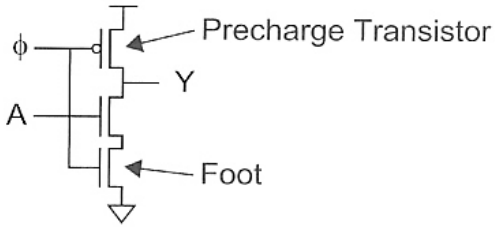
- Footed vs. Unfooted
  - foot tx ensures nMOS array disabled during precharge

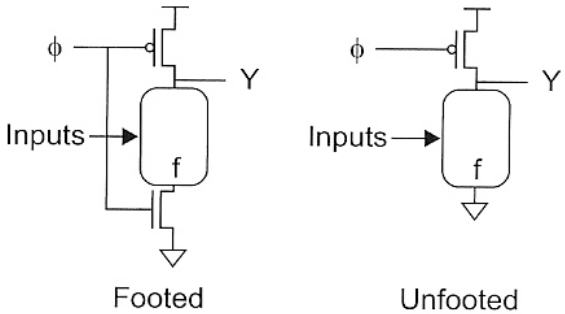


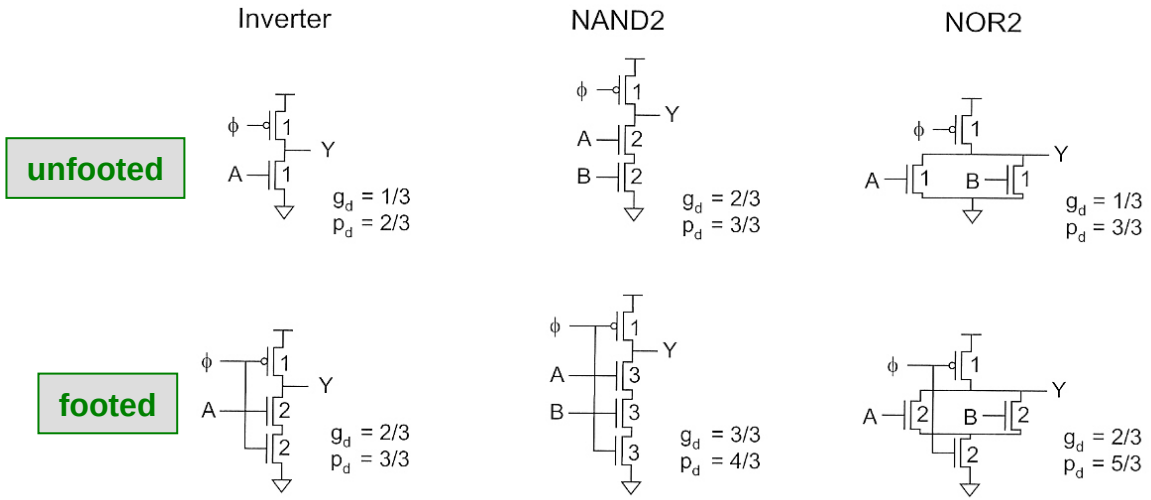
(a) Circuit



(b) Layout

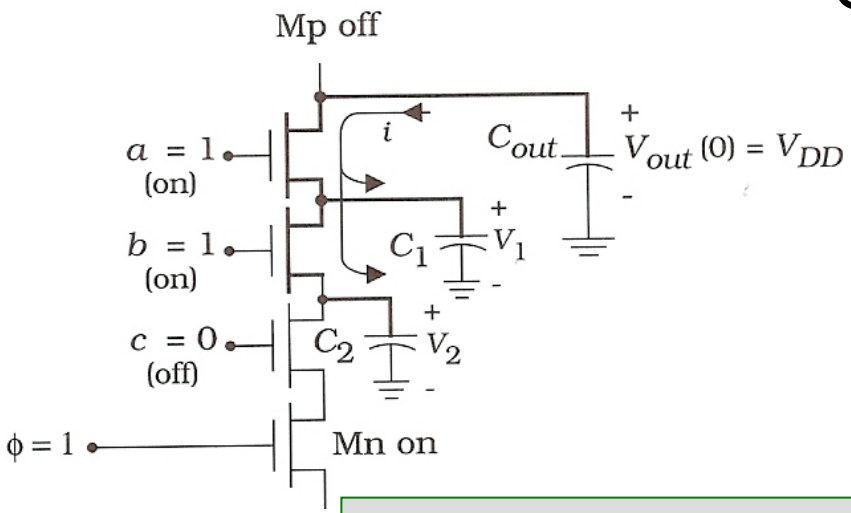






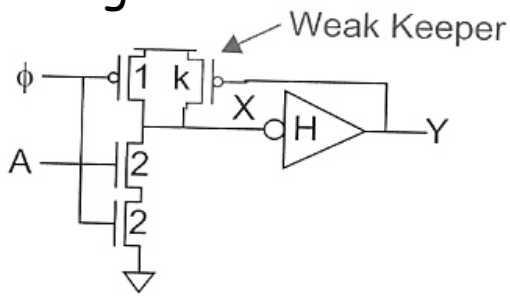
Charge Redistribution in Dynamic Logic

- Major potential problem
  - during evaluation, precharge charge is distributed over parasitic capacitances within the nMOS array
    - causes output to decrease (same charge over larger C → less V)
  - if the function is not true, output should be HIGH but could be much less than VDD



charge distribution over nMOS parasitics during *evaluation*

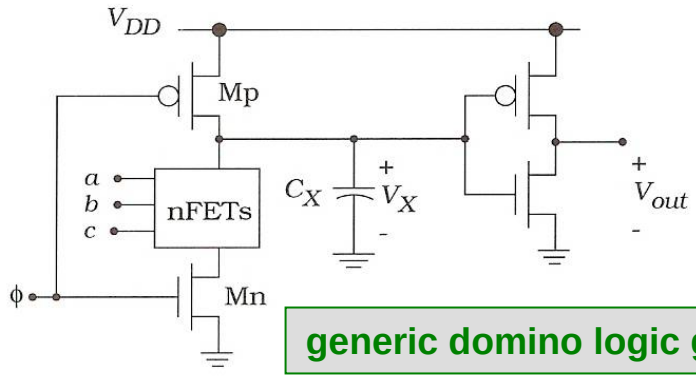
- One possible solution
  - "keeper" transistor
    - injects charge during evaluation if output should be HIGH
    - keeps output at VDD
  - keeper controlled by output_bar
    - on when output is high



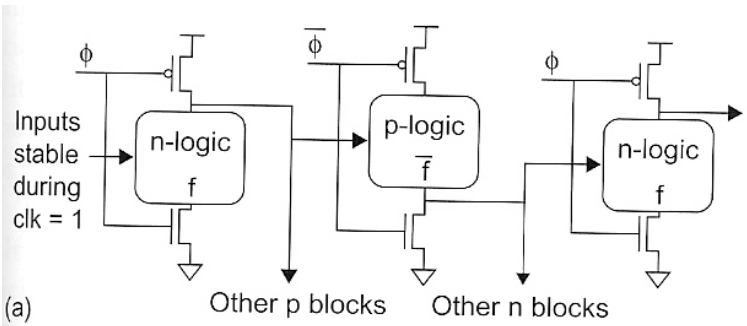
Domino Logic

- Dynamic logic can only *drive* an output LOW
  - output HIGH is precharged only with limited drive
- Domino logic adds and inverter buffer at output

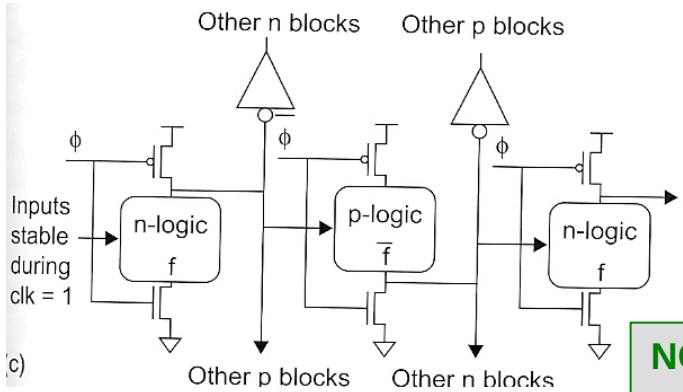
- Cascading domino logic
  - must alter precharge/eval cycles
  - clock each stage on opposite clock phase



generic domino logic gate

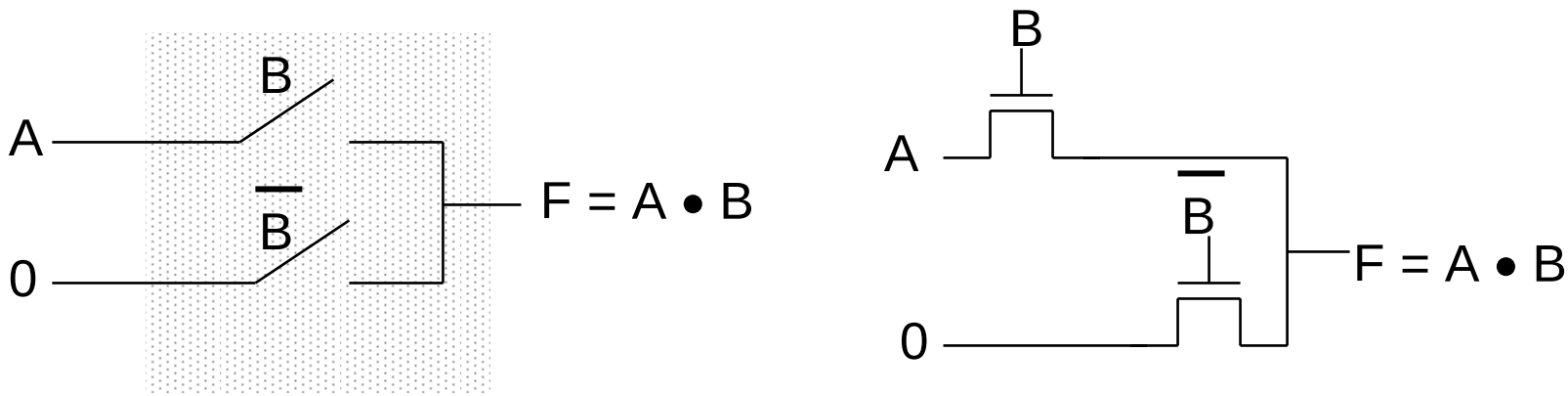


NP dynamic logic



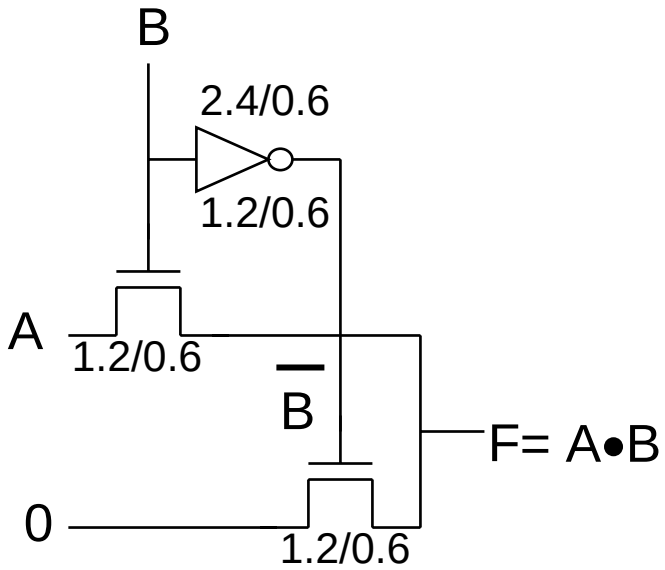
NO RAce (NORA) domino logic

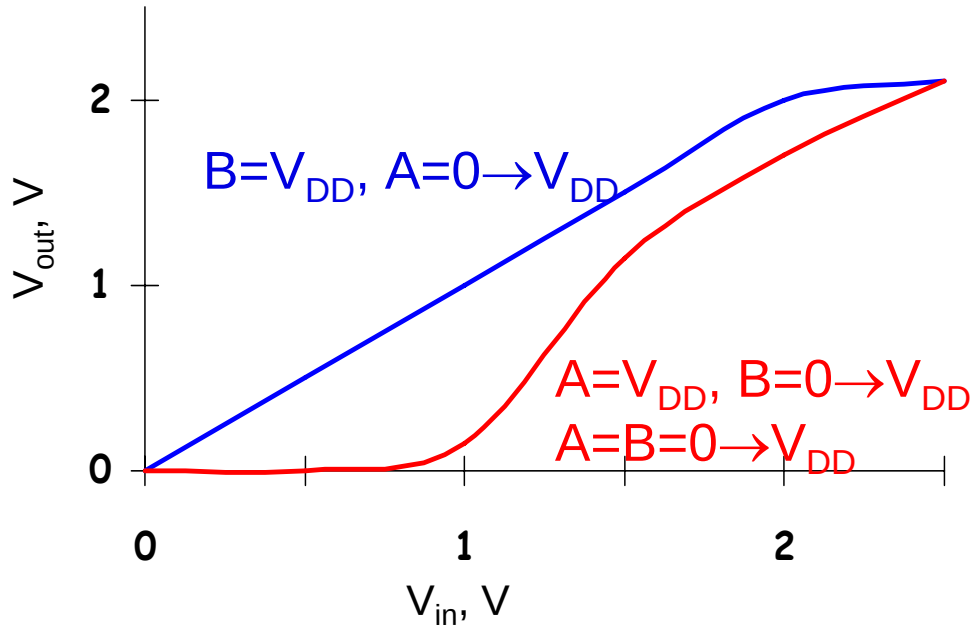
Pass Transistor (PT) Logic



- Gate is static – a low-impedance path exists to both supply rails under all circumstances
- N transistors instead of 2N
- No static power consumption
- Ratioless
- Bidirectional (versus undirectional)

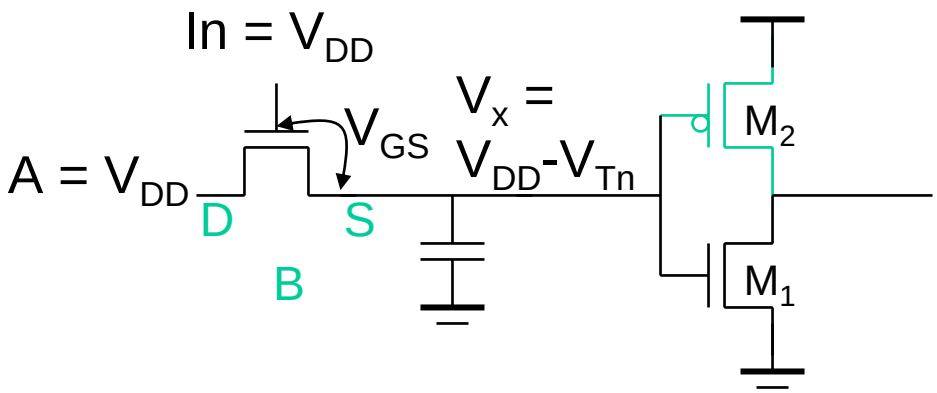
VTC of PT AND Gate





- Pure PT logic is not regenerative - the signal gradually degrades after passing through a number of PTs (can fix with static CMOS inverter insertion)

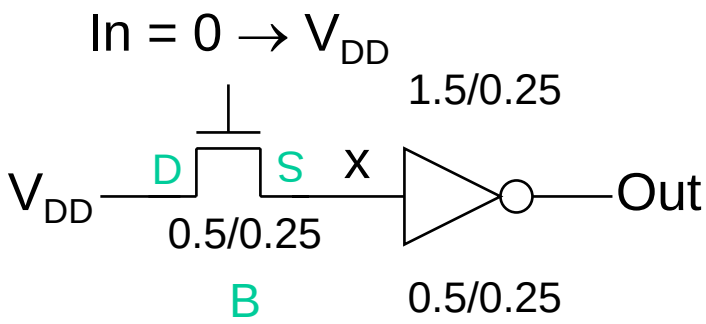
nMOS Only PT Driving an Inverter

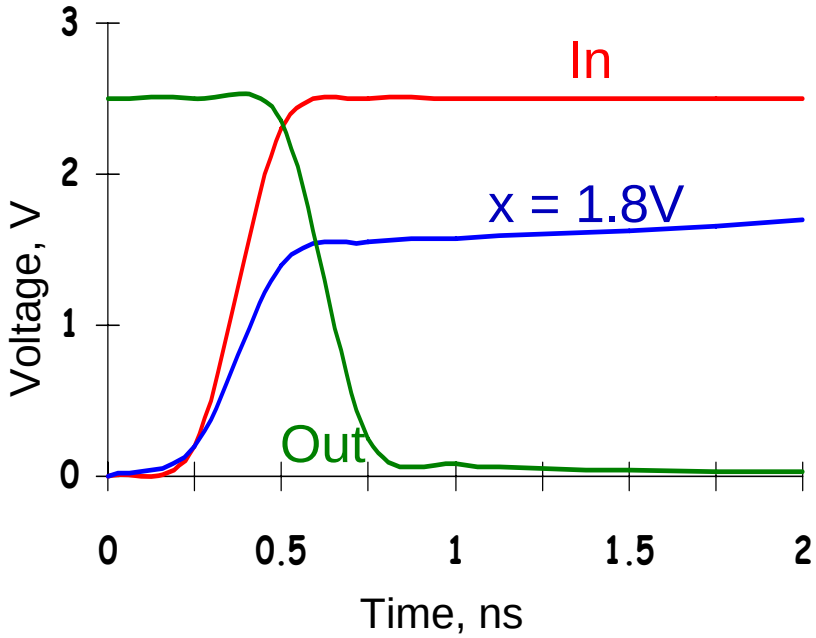


- V_x does not pull up to V_{DD}, but V_{DD} – V_{Tn}

- Threshold voltage drop causes static power consumption (M_2 may be weakly conducting forming a path from V_{DD} to GND)
- Notice V_{Tn} increases of pass transistor due to body effect (V_{SB})

Voltage Swing of PT Driving an Inverter

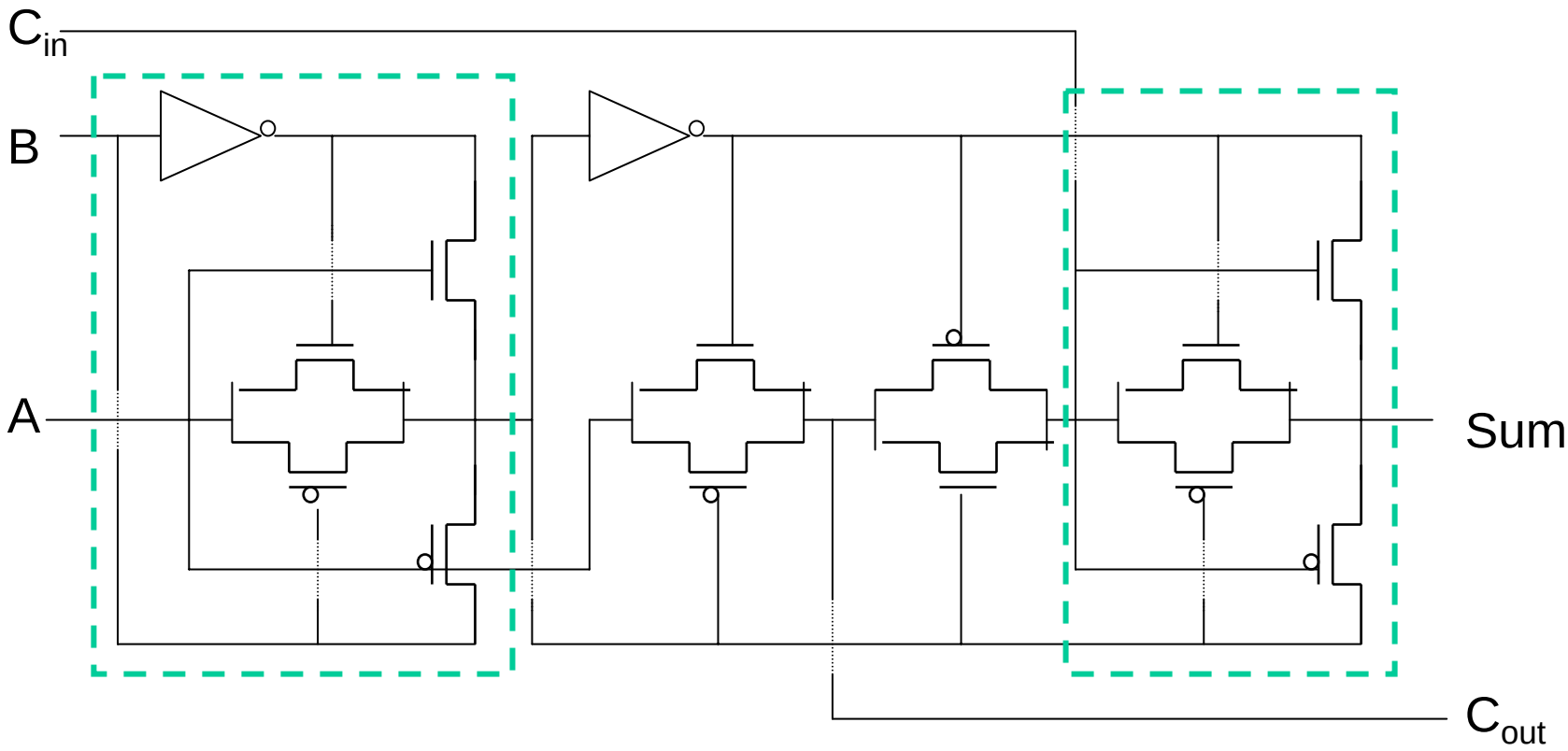




- Body effect – large V_{SB} at x - when pulling high (B is tied to GND and S charged up close to V_{DD})
- So the voltage drop is even worse

$$V_x = V_{DD} - (V_{Tn0} + \gamma(\sqrt{(|2\phi_f| + V_x)} - \sqrt{|2\phi_f|}))$$

TG Full Adder



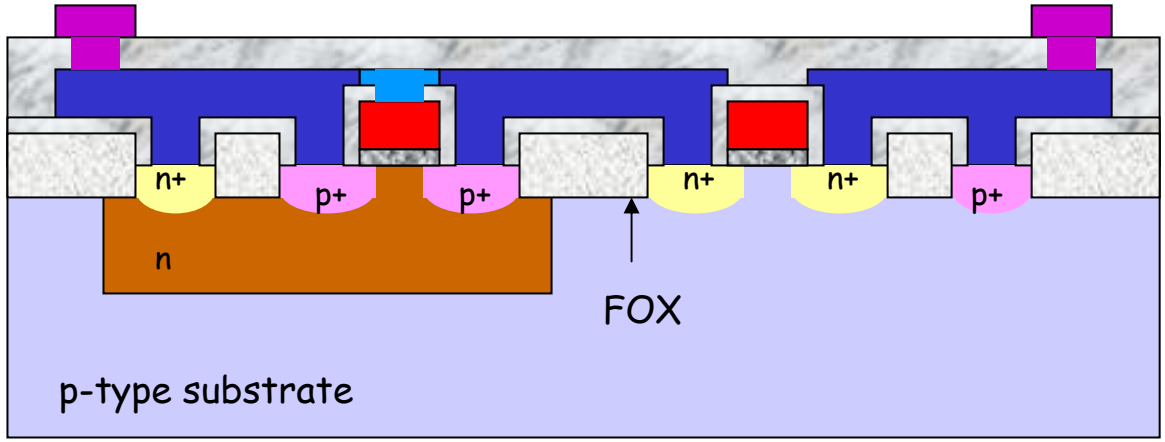
16 Transistors; full swing – transmission gates

Basic CMOS Isolation Structures

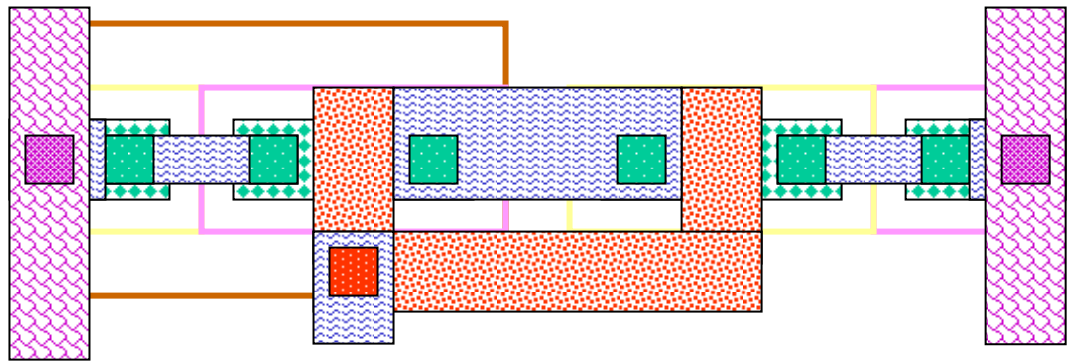
- LOCOS –Local Oxidation of Silicon
- STI –Shallow Trench Isolation
- LDD –Lightly-Doped Drain
  - Used to reduce the lateral electric field in the channel
- SOI –Silicon on Insulator
- BiCMOS -Bipolar and CMOS on same chip

LOCOS

- Isolation between transistor
  - Field Oxide (FOX)
- FOX formed by
  - masking active regions
  - thermal oxidation of non-masked areas
- Self-aligned gate
  - S/D formed after poly gate
  - S/D automatically aligned to gate



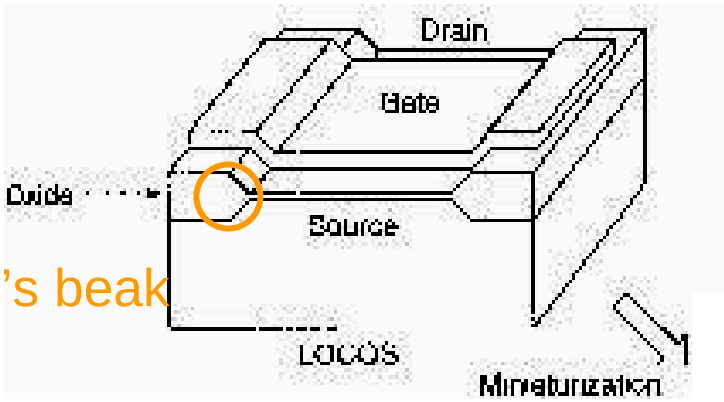
Cross section view

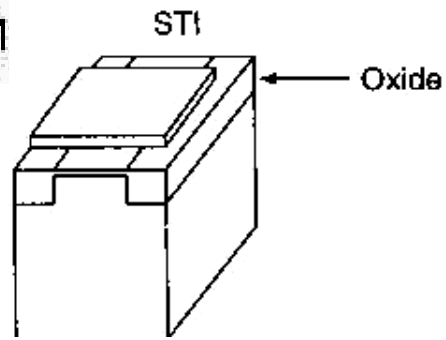


Layout view

Problems with LOCOS

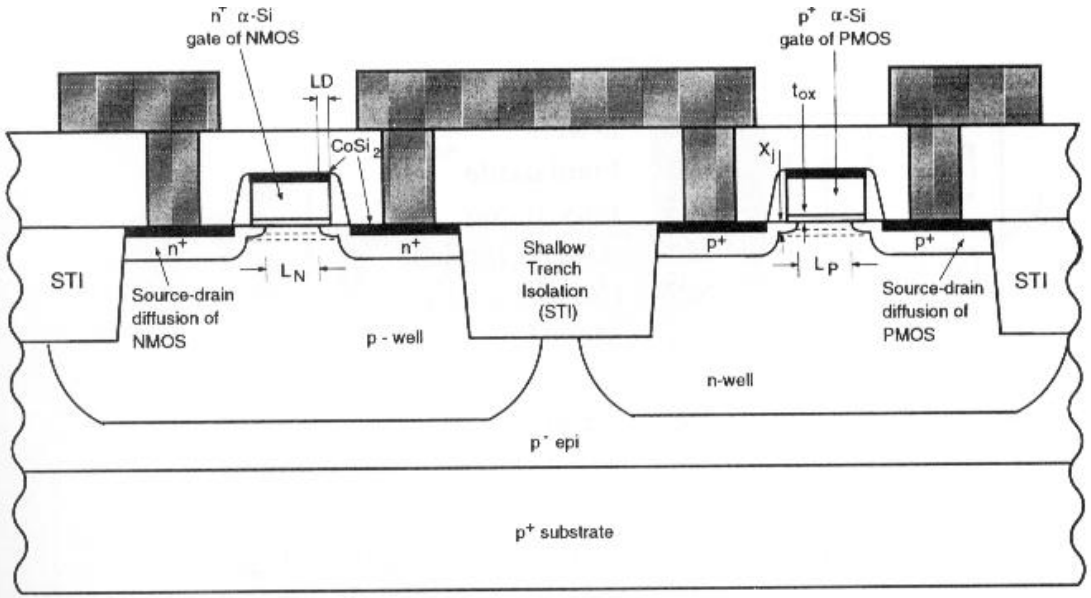
- Device "packing" density limited by "bird's beak effect of FOX isolation layer.
  - effects the width (W) of the transistor
- Can improve density with Shallow Trench Isolation (STI)

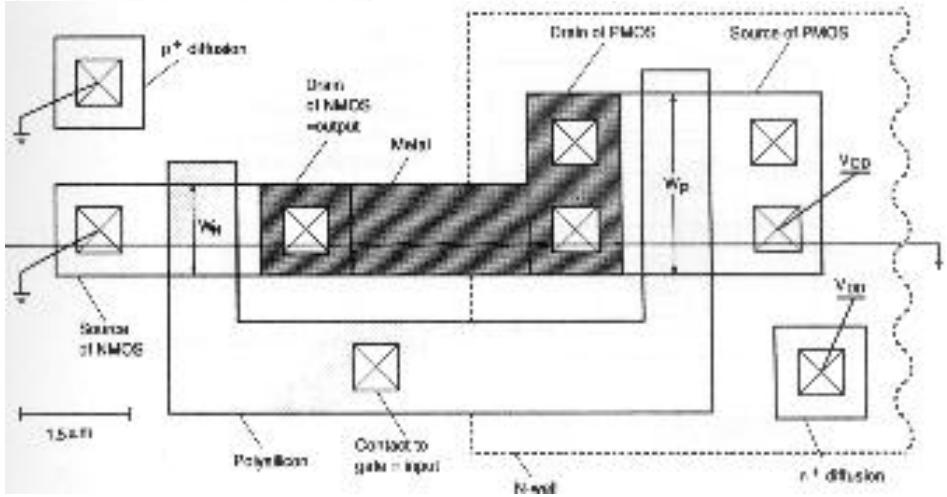




Shallow Trench Isolation (STI)

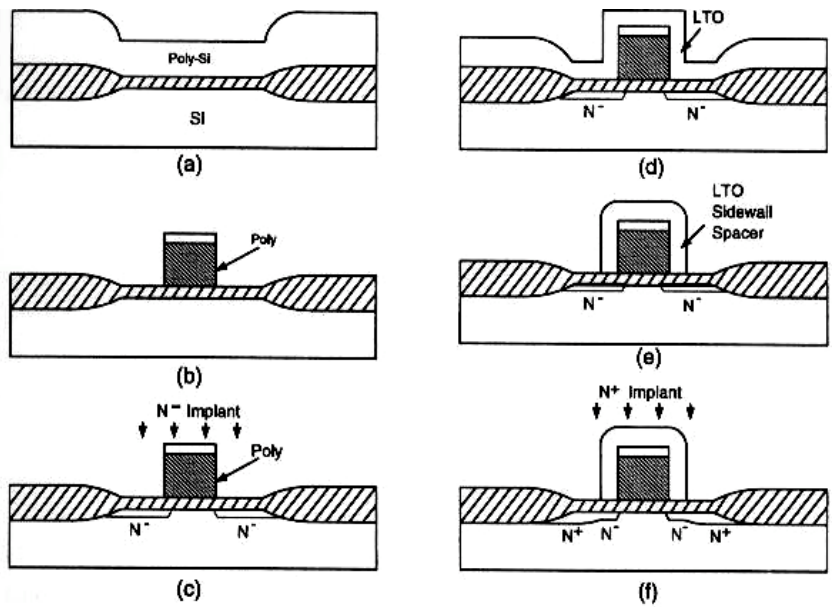
- Form Gate and S/D first
- Then isolate devices by
  - etching trench (~0.4um) in substrate between devices
  - filling trench with deposited oxide
- Eliminates the area lost to bird's beak effect of LOCOS
- Well doping and channel implants done later in process via high energy ion implantation





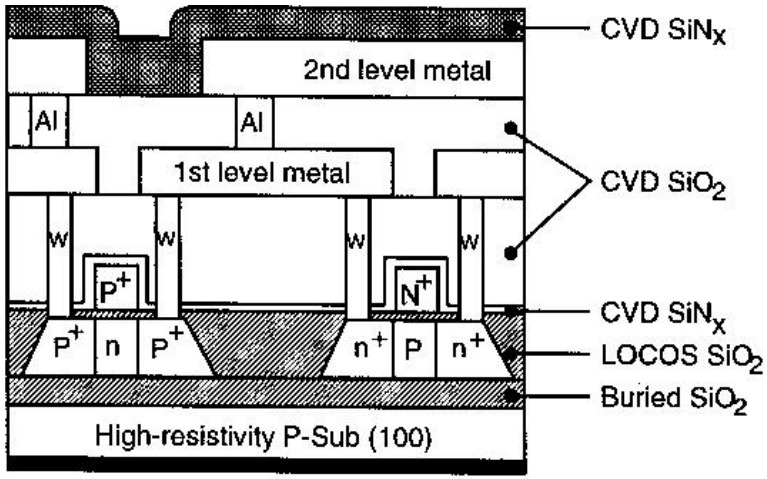
Lightly-Doped Drain (LDD)

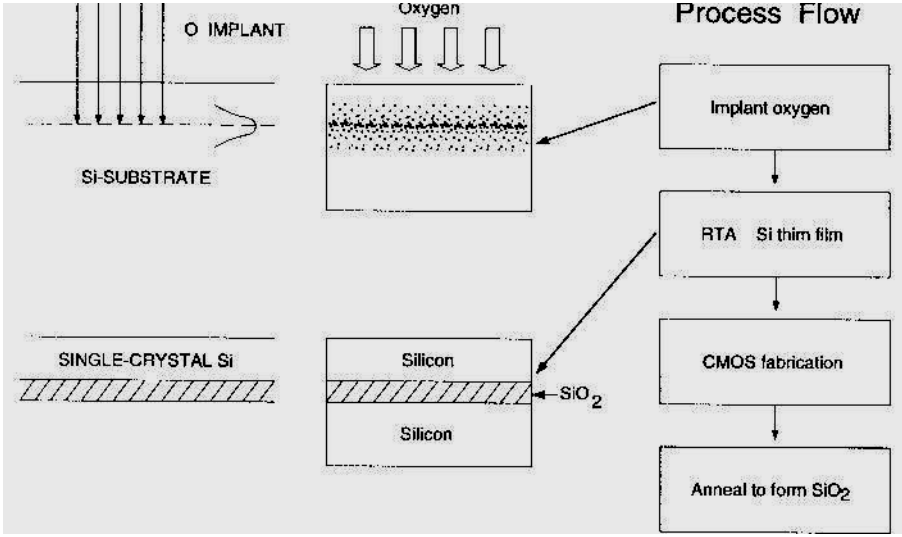
- Create lightly doped regions in S/D near the channel
- Necessary for submicron fabrication
  - reduces the electric field across the channel
  - reduces the velocity of electrons in the channel
    (hot carrier effect)
  - reduces performance, but allows higher density
- Can be used with any isolation process



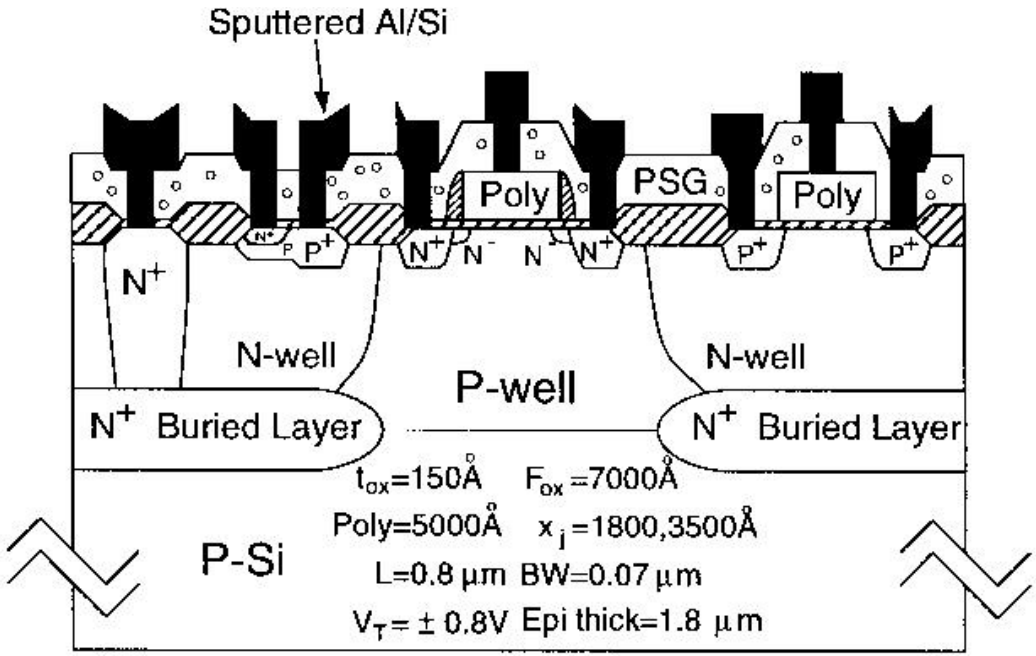
Silicon On Insulator (SOI)

- Buried SiO_2 layer beneath surface of active single-crystal Si substrate
- More expensive, but excellent isolation
  - no leakage current to substrate
  - no latchup
  - high transconductance
  - good subthreshold performance
  - reduced short channel effects
  - radiation immunity





BiCMOS



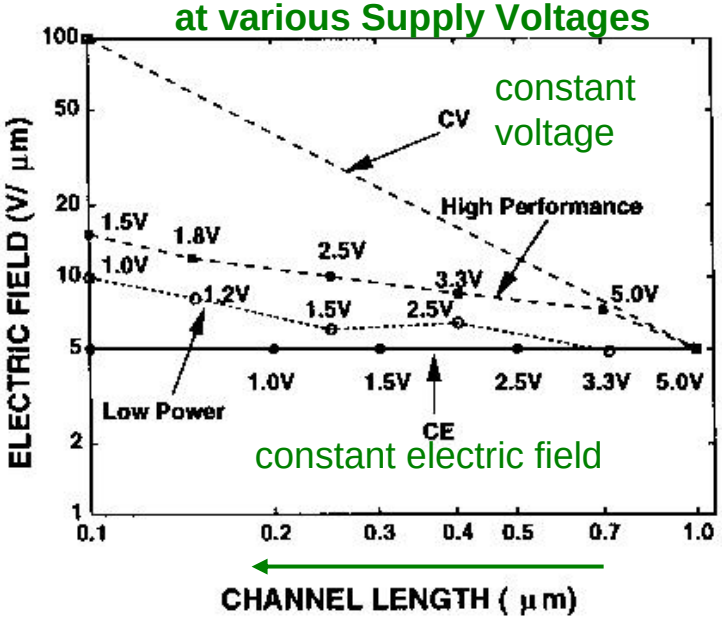
- Advantage
  - both Bipolar and CMOS transistor
- Disadvantage
  - Increased process complexity
  - Reduced density (just no way to make small BJTs)

Scaling Options

- Constant Voltage (CV)
  - voltage remains constant as feature size is reduced
  - causes electric field in channel to increase
    - decreases performance
  - but, device will fail if electric field gets too large

- Constant Electric Field (CE)
  - scale down voltage with feature size
  - keeps electric field constant
    - maintain good performance
  - but, limit to how low voltage can go

Electric Field in channel vs. Channel Length at various Supply Voltages

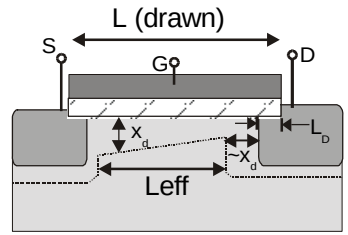


Low Voltage Issues

- Reasons modern/future circuits have lower voltage
  - lower voltage = lower dynamic power: $P_{dyn} = \alpha C_L V_{DD}^2 f_{CLK}$
  - lower voltage required for smaller feature size
    - feature sizes reduced to improve performance/speed
    - smaller features = shorter distances across the channel
      - ➔ stronger electric fields in channel
        - ➔ poorer performance or device failure
        - » unless voltage is reduced also
- Side effects of reducing voltage
  - reduces current (speed) and increases noise problems
  - as supply voltage decreases, must also reduce threshold voltage
    - otherwise, circuits will not switch correctly
  - reduced threshold voltage = increased subthreshold current
    - ➔ increased leakage currents
      - ➔ increased static power consumption

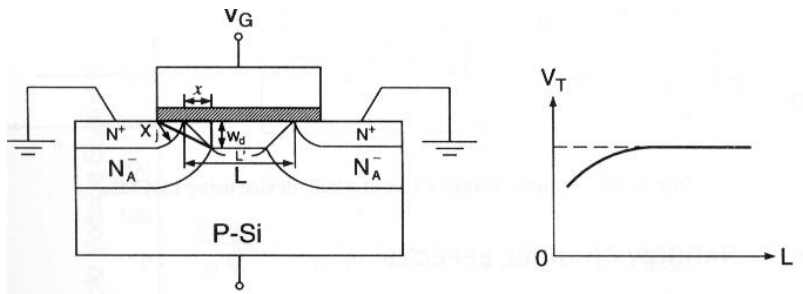
Short Channels

- Effective channel length
  - must account for depletion region spreading into the channel
  - more important as channel length gets shorter



$$Leff = L(drawn) - 2L_D - X_d \qquad X_d = \sqrt{\left(\frac{2\varepsilon_s(V_D - (V_G - V_t))}{qN_A}\right)}$$

- For short channels, roughly measured by L < 1μm
  - Source-Substrate and Drain-Substrate junction depletion layer extend noticeably into the channel
  - will reduce the about of bulk charge, Q_B, in the channel
  - thus reduce the threshold voltage as channel length decreases
  - called the ***short channel effect***
  - need a new way to calculate Q_B
    - some bulk charge lost to depletion layers



(from Kuo and Lou, p. 43)

Short Channel Effects

- Short channel lengths introduce effects which must be considered
  - in selecting process technologies for a given application
  - in design of circuits
- Short Channel Effects
  - mobility degradation
  - threshold voltage degradation
  - velocity saturation
  - hot carrier effects
- Other effects made worse by short channels
  - leakage currents
  - latch-up
  - subthreshold operation

Velocity Saturation

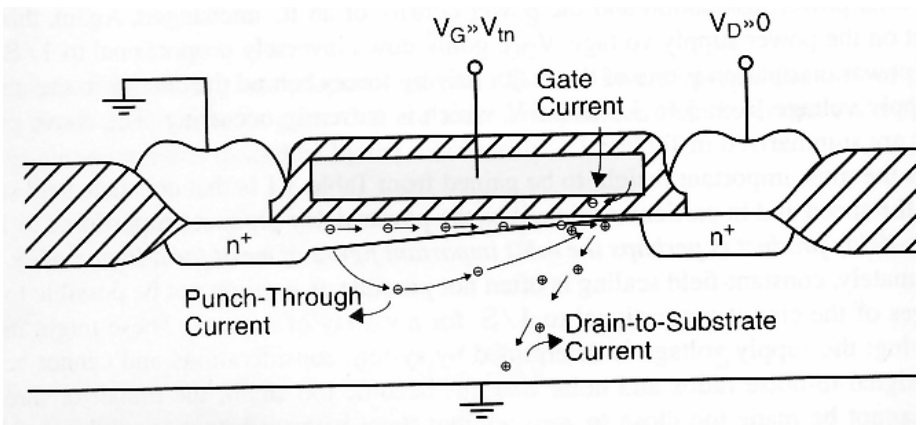
- Charge Velocity
  - $v_n = \mu E$, μ is mobility and E is electric field
  - valid for small E, as assumed in previous I-V equations
- Velocity Saturation
  - if E > Ec (critical field level), velocity will reach a maximum
  - v_{sat} = saturation velocity, velocity at E > Ec
- Short Channel Devices
  - lateral field near drain is very high → charge can experience velocity saturation
  - even at V_{DS} voltages before pinchoff occurs
  - here

$$I_D = \frac{\mu_n C_{OX}}{2}\frac{W}{L}\left[2(V_{GS} - V_t)V'_{DSAT} - V'^2_{DSAT}\right]$$

    - where V'_{DSAT} is the drain-source voltage which generates the critical electric field, Ec
    - valid when $V'_{DSAT} < V_{GS}-V_t$ (when velocity saturation occurs before channel pinchoff)
- Velocity Overshoot
  - with very short channels, carriers can travel faster than saturation velocity
  - occurs in deep submicron devices with channel lengths less than 0.1μm
  - the velocity saturation equation above becomes inaccurate for very small channel lengths and more detailed models are required.

Hot Carrier Effects

- High E-field in channel will accelerate charge carriers
- Accelerated carriers can start colliding with the substrate atoms
  - generates electron-hole pairs during the collision
  - these will be accelerated, collide with substrate atoms and form even more electron-hole pairs: called impact ionization
- Impact ionization can lead to
  - avalanche breakdown within the device
  - large substrate currents
  - degradation of the oxide
    - high energy electrons collide with gate oxide and become imbedded
    - causes a shift in threshold voltage
    - considered catastrophic effect
      - leads to unstable performance



Hot Carrier Effects II

- Supply voltages dropping slower than channel length
  - as a result electric fields in channel continue to increase.
- Hot carrier effect must be considered for submicron devices
  - may potentially be a limiting factor in how far devices can be scaled down
    - unless we can reduce electric fields in channel
- To reduce hot carrier effects, increase channel length

- pMOS devices may be better overall for deep submicron circuits
  - hole mobility is closer to electron mobility under high electric fields which occur in submicron devices
  - hot carrier effects are worse in nMOS devices than pMOS

Leakage Currents

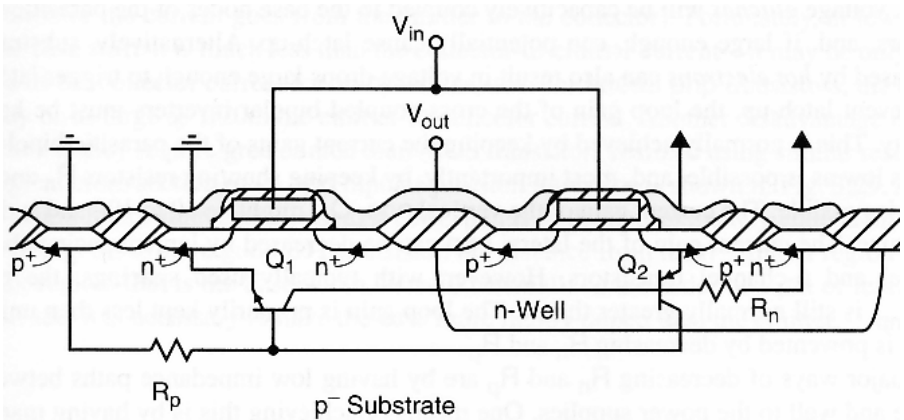
- All p-n junctions in the MOSFET structure will have a reverse bias leakage current
- Leakage Current, I_{lk}

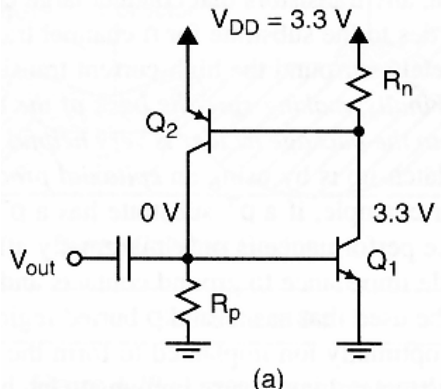
$$I_{lk} = \frac{qA_j n_i}{2\tau_0} x_d$$

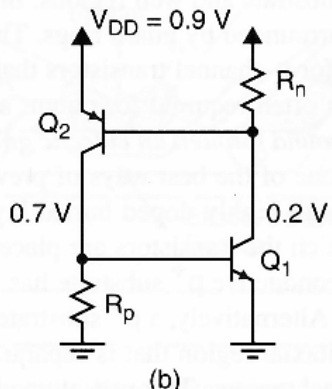
  - where
    - A_j is the junction area
    - n_i is the intrinsic carrier concentration
    - τ_0 is the effective minority carrier lifetime
    - x_d is the depletion layer thickness, $x_d = f(V_R)$
- Undesired effects of leakage currents
  - add to unwanted static power consumption
  - limit the charge storage time of dynamic circuits
- Factors in leakage
  - n_i is a strong function of temperature (doubles every 11°C)
    - significant in high power density circuit that generate heat

Latch-Up

- Latch-up is a very real, very important factor in circuit design that must be accounted for
- Due to (relatively) large current in substrate or n-well
  - create voltage drops across the resistive substrate/well
    - most common during large power/ground current spikes
  - turns on parasitic BJT devices, effectively shorting power & ground
    - often results in device failure with fused-open wire bonds or interconnects
  - hot carrier effects can also result in latch-up
    - latch-up very important for short channel devices
- Avoid latch-up by
  - including as many substrate/well contacts as possible
  - limiting the maximum supply current on the chip



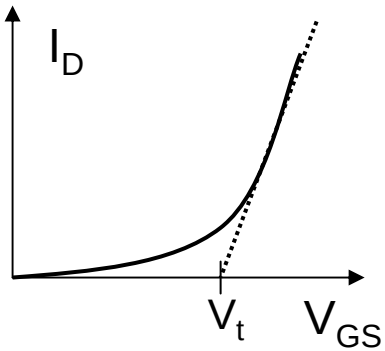




Subthreshold Operation

- Weak inversion, when $V_G > 0$ but $< V_t$
  - some channel change and the drain current is small but not zero.
  - referred to as the *subthreshold region*
- Subthreshold operation
  - the drain current is an exponential function of the gate voltage
  - the current increase sharply with V_{GS} until the device turns on

$$I_D = I_{D0} \frac{W}{L} e^{(qV_{GS} / \ nkT)}$$



  - where
    - I_{D0} is a process dependant constant, typically ~20nA
    - n is a process dependant constant, typically n=1.5
    - kT/q = 26mV at room temperature
- Channel Length
  - subthreshold currents are much larger in short channel devices
    - due to high e-fields at the drain reducing effective channel length
    - effect can be reduced my using lightly-doped drain regions under the gate

Subthreshold Operation

- Analog Circuits
  - subthreshold operation is exploited for low power operation in low frequency applications
- Digital Circuits
  - subthreshold current serves as undesired leakage current
  - want to quickly transition in/out of subthreshold
- How can we decrease subthreshold currents and speed transition?
  - thinner gate oxide = faster transition
    - same as current technology trend
  - lighter substrate doping = faster transition
    - opposite of current technology trend
      - higher doping needed for better short channel performance
  - faster transition = less subthreshold leakage current = lower power
  - process must be chosen to match the speed, power, and performance spec's for each circuit
    - what is best for DRAM is not best for microprocessors, etc.

$$I_D = I_{D0}\frac{W}{L}e^{(qV_{GS}/\ nkT)}$$