# Етапи на Проектиране - Типове Симулация

RTL is an acronym for register transfer level. This implies that your Verilog code describes how data is transformed as it is passed from register to register. The transforming of the data is performed by the combinational logic that exists between the registers.

# 

# Симулация



# 

| Модел module counter #(parameter N = 8) (  input clock,  input reset,  output logic [N-1:0] cnt  );  always\_ff @(posedge clock, posedge reset)  if (reset)          cnt <= 0;  else      cnt <= cnt+1;  endmodule | Тест (testbench) module counter\_test\_v1;  localparam size = 2;  logic clock;  logic reset;  logic [size-1:0] cnt;  // Instantiate the Unit Under Test (UUT)  counter #(.N(size)) uut (.\*);  initial begin  clock = 0;  forever #50 clock = ~clock;  end  initial begin  reset = 1;  #100 reset = 0;  #600;  $finish;  end  initial begin  $display("clock reset cnt(bin) cnt(dec) ");          $monitor(" %b %b %b %d",reset, clock, cnt, cnt);          $dumpfile("dump.vcd");      end  endmodule |
| --- | --- |

# Симулация - Xilinx Vivado

<https://www.xilinx.com/support/download.html>

**Команди за симулация**

call C:\Xilinx\Vivado\2019.1\settings64.bat

call xvlog -sv -nolog counter.sv;

if ERRORLEVEL 1 (

exit

)

call xelab -R -s run\_1 -nolog -debug all work.counter\_test\_v2

rem call xsim run\_1 -gui

**Пример**

**C:\Xilinx\Vivado\2019.1\settings64.bat**

**xvlog --sv counter.sv**

INFO: [VRFC 10-2263] Analyzing SystemVerilog file "C:/usr/verilog/2018/sim/counter.sv" into library work

INFO: [VRFC 10-311] analyzing module counter

INFO: [VRFC 10-311] analyzing module counter\_test\_v1

INFO: [VRFC 10-311] analyzing module counter\_test\_v2

**xelab -R -s run\_1 --debug all work.counter\_test\_v1**

Multi-threading is on. Using 2 slave threads.

Starting static elaboration

Completed static elaboration

Starting simulation data flow analysis

Completed simulation data flow analysis

Time Resolution for simulation is 1ps

Compiling module work.counter(N=2)

Compiling module work.counter\_test\_v1

Built simulation snapshot run\_1

\*\*\*\*\*\* xsim v2019.1 (64-bit)

\*\*\*\* SW Build 2258646 on Thu Jun 14 20:03:12 MDT 2018

\*\*\*\* IP Build 2256618 on Thu Jun 14 22:10:49 MDT 2018

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source xsim.dir/run\_1/xsim\_script.tcl

# xsim {run\_1} -autoloadwcfg -runall

Vivado Simulator 2019.1

Time resolution is 1 ps

run -all

clock reset cnt(bin) cnt(dec)

1 0 00 0

1 1 00 0

0 0 00 0

0 1 01 1

0 0 01 1

0 1 10 2

0 0 10 2

0 1 11 3

0 0 11 3

0 1 00 0

0 0 00 0

0 1 01 1

0 0 01 1

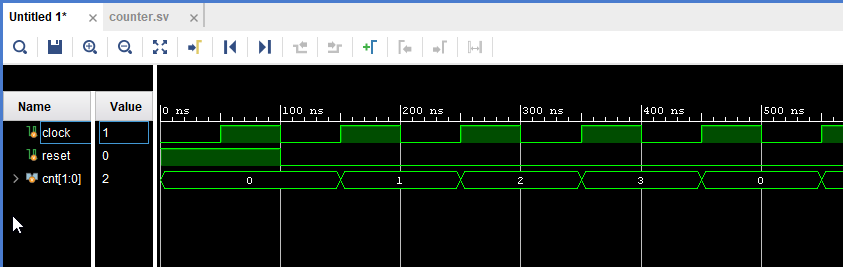
0 1 10 2

$finish called at time : 700 ns : File "C:/usr/verilog/2018/sim/counter.sv" Line 40

exit

INFO: [Common 17-206] Exiting xsim at Thu Oct 11 09:58:18 2018...

**xsim run\_1 -gui**



EDAPlayground

<https://www.edaplayground.com/>

