TOPSwitch®-GX Flyback Design Methodology

Application Note AN-32

Designing an off-line power supply involves many aspects of electrical engineering: analog and digital circuits, bipolar and MOS power device characteristics, magnetics, thermal considerations, safety requirements, control loop stability, etc. This represents an enormous challenge involving complex trade-offs with a large number of design variables. As a result, new off-line power supply development has always been tedious and time consuming even for the experts in the field. This application note introduces a simple, yet highly efficient methodology for the design of *TOPSwitch-GX* family based off-line power supplies. For *TOPSwitch-GX* Flyback designs, Power Integrations recommends the use of *PI Expert* which implements this design methodology and also includes a knowledge base and optimization feature for making key design choices, further reducing design time.

Introduction

The design of a switching power supply, by nature, is an iterative process with many variables requiring adjustment to optimize the design. The design method described in this document consists of two major sections: A design flow chart and a step-by-step design procedure. The flow chart shows the design sequence at a conceptual level for *TOPSwitch-GX* flyback power supply design. The step-by-step procedure gives details within each step of the design flow chart, including empirical design guidelines and look-up tables. All key equations and guidelines are provided wherever possible to assist the readers in better understanding and/or further optimization.

Basic Circuit Configuration

Because of the high level integration of *TOPSwitch-GX*, many power supply design issues are resolved in the chip. Far fewer issues are left to be addressed externally, resulting in one common circuit configuration for all applications. Different output power levels may require different values for some circuit components, but the circuit configuration stays unchanged. *TOPSwitch-GX* is a feature-rich product family. Advanced features like under-voltage, overvoltage, external I_{LIMIT}, line feed forward, and remote ON/OFF are easily implemented with a minimal number of external components, but do involve additional design considerations. Please refer to the *TOPSwitch-GX* data sheet for details. Other application

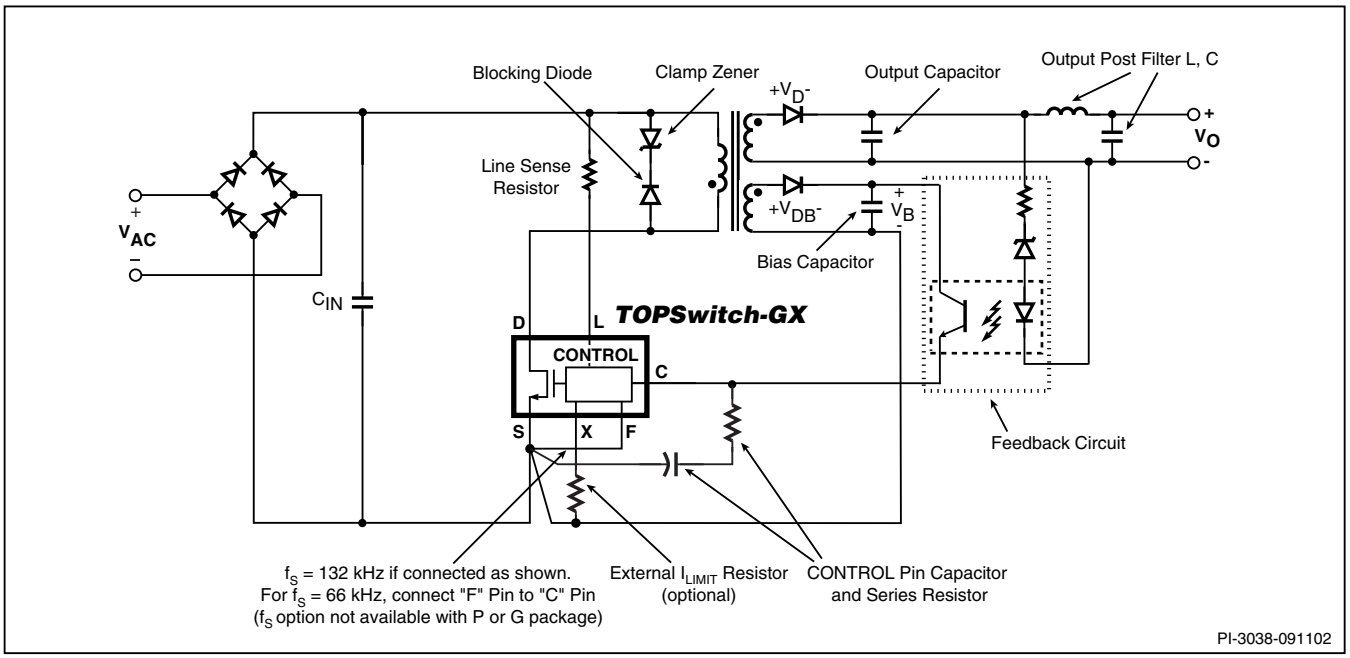

Figure 1. Typical TOPSwitch-GX Flyback Power Supply.

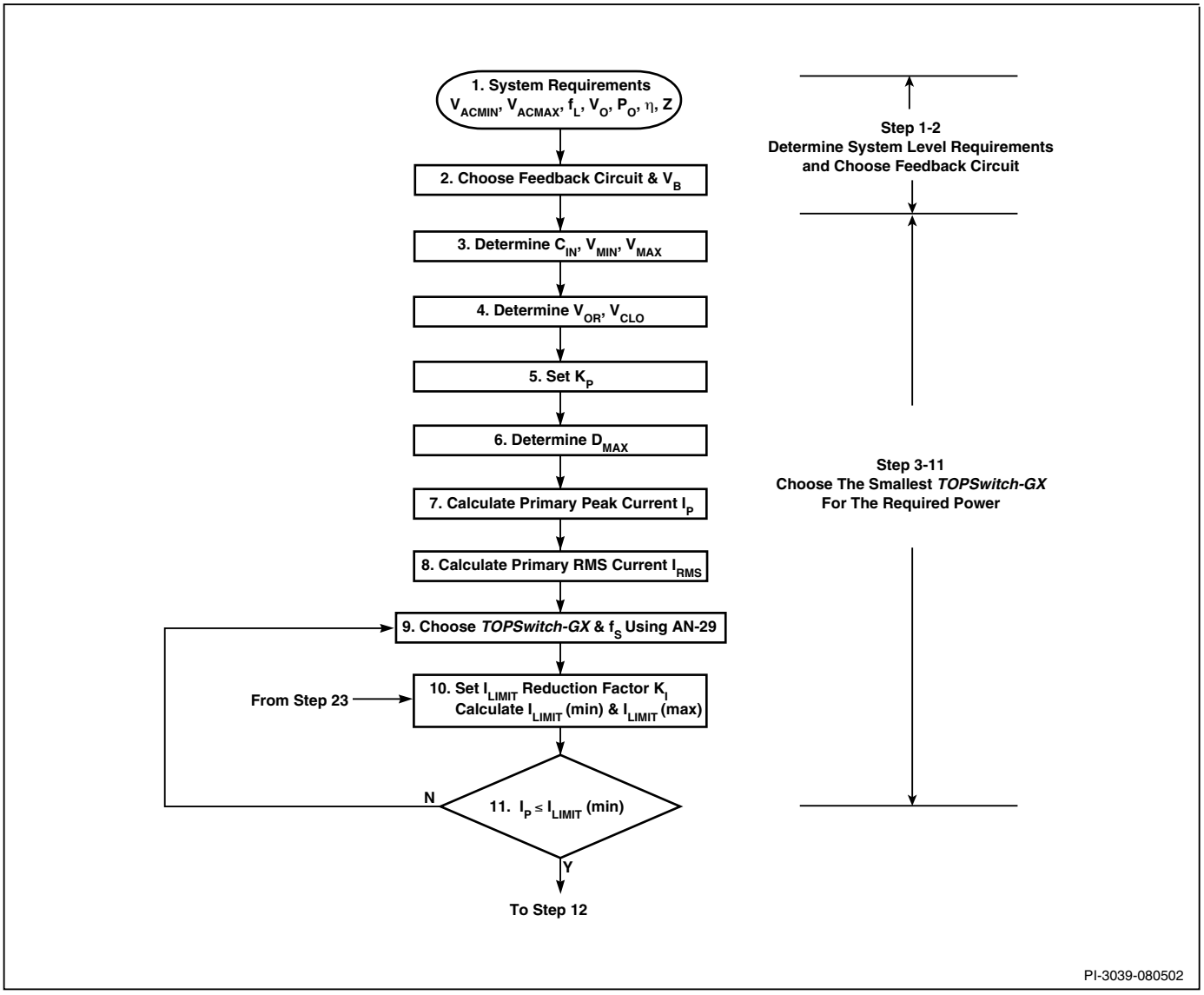

Figure 2A. TOPSwitch-GX Design Flow Chart. Step 1 to 11.

specific issues such as constant current, constant power outputs, etc. are beyond the scope of this application note. However, such requirements may be satisfied by adding additional circuitry to the basic converter configuration. The only part of the circuit configuration that may change from application to application is the feedback circuitry. Depending on the power supply output specifications, one of the four feedback circuits, shown in Figures 3, 4, 5 and 6, will be chosen for the application.

The basic circuit configuration used in *TOPSwitch-GX* flyback power supplies is shown in Figure 1, which also serves as the reference circuit for component identifications used in the description throughout this application note.

Design Flow

Figures 2A, 2B and 2C present a design flow chart showing the complete design procedure in 37 steps. With the basic circuit configuration shown in Figure 1 as its foundation, the logic behind this design approach can be summarized as follows:

1. Determine system requirements and decide on feedback circuit accordingly.
2. Choose the smallest *TOPSwitch-GX* capable of the required output power.
3. Design the smallest transformer for the *TOPSwitch-GX* chosen.
4. Select all other components in Figure 1 to complete the design.

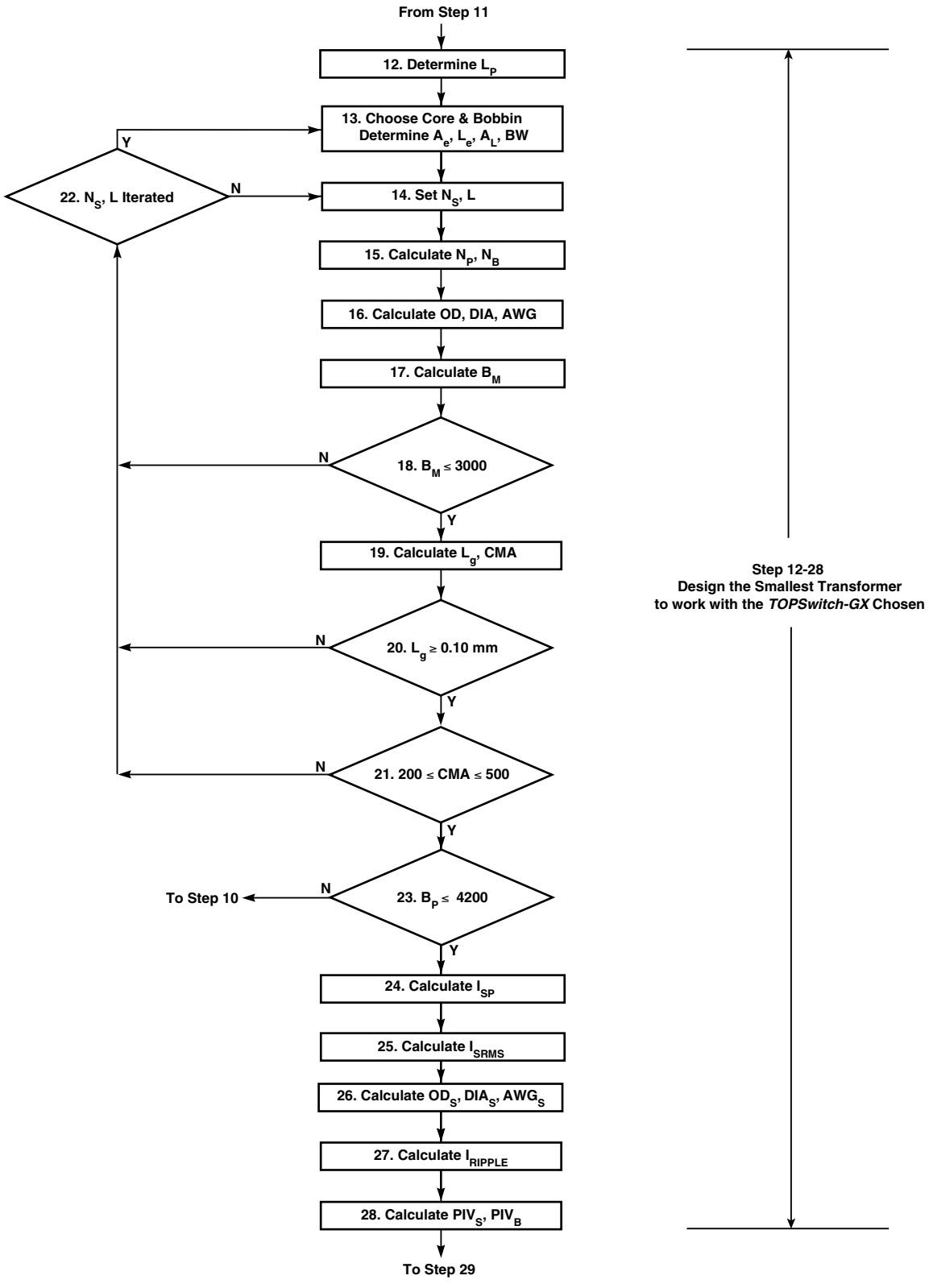

Figure 2B. TOPSwitch-GX Design Flow Chart. Step 12 to 28.

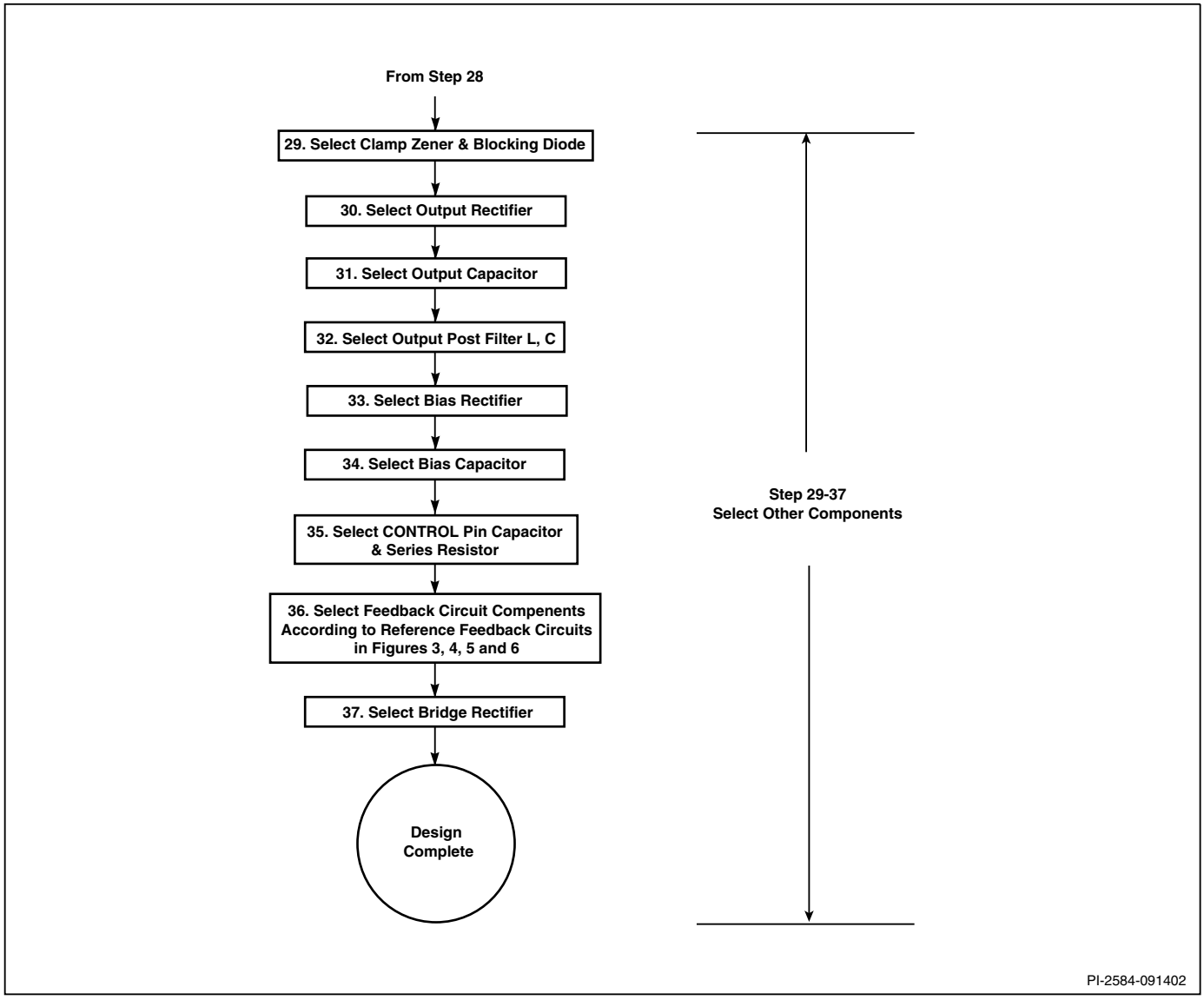

Figure 2C. TOPSwitch-GX Design Flow Chart. Step 29 to 37.

The overriding objective of this procedure is “design for cost effectiveness.” Using smaller components usually leads to a less expensive power supply. However, for applications with stringent size or weight limitations, the designer may need to strike a compromise between cost and specific design requirements in order to achieve the optimum cost effectiveness for the end product.

Step-by-Step Design Procedure

This design procedure uses the *PI Expert* design software (available from Power Integrations), which contains all the important equations required for a *TOPSwitch-GX* flyback power supply design, and automates most calculations. Designers are, therefore, relieved from the tedious calculations involved in the complicated and highly iterative design process. Look-up tables and empirical design guidelines are provided in this procedure where appropriate to facilitate the design task.

Step 1. Determine system requirements: V_{ACMAX}, V_{ACMIN}, f_L, V_O, P_O, η, Z

- Minimum AC input voltage, V_{ACMIN}: in volts.
- Maximum AC input voltage, V_{ACMAX}: in volts.
- Recommended AC input ranges:

Input (VAC)	V_{ACMIN} (VAC)	V_{ACMAX} (VAC)
Universal	85	265
230 or 115 with doubler	195	265

Table 1.

- Line frequency, f_L: 50 Hz or 60 Hz.
- Output voltage, V_O: in Volts.
- Output power: P_O: in Watts.
- Power supply efficiency, η: 0.8 if no better reference data available. (Refer to AN-29)
- Loss allocation factor, Z: If Z = 1, all losses are on the secondary side. If Z = 0, all losses are on the primary side. Set Z = 0.5 if no better reference data is available.

Step 2. Choose feedback circuit and bias voltage V_B based on output requirements

Feedback Circuit	V_B (V)	Circuit Tolerance	Load* Reg.	Line Reg.	Total Reg.
Pri./Basic	5.8	±10%	±5%	±1.5%	±16.5%
Pri./Enhan.	27.8	±5%	±2.5%	±1.5%	±9%
Opto/Zener	12	±5%	±1%	±0.5%	±6.5%
Opto/TL431	12	±1%	±0.2%	±0.2%	±1.4%

**Over 10% to 100% Load Range.*
Table 2.

- Use primary feedback for lowest cost (for low power applications only).
- Use Opto/Zener for low cost, good output accuracy.
- Use Opto/TL431 for best output accuracy.
- Set bias voltage V_B according to Table 2.
- Choose optocoupler from Table 3.

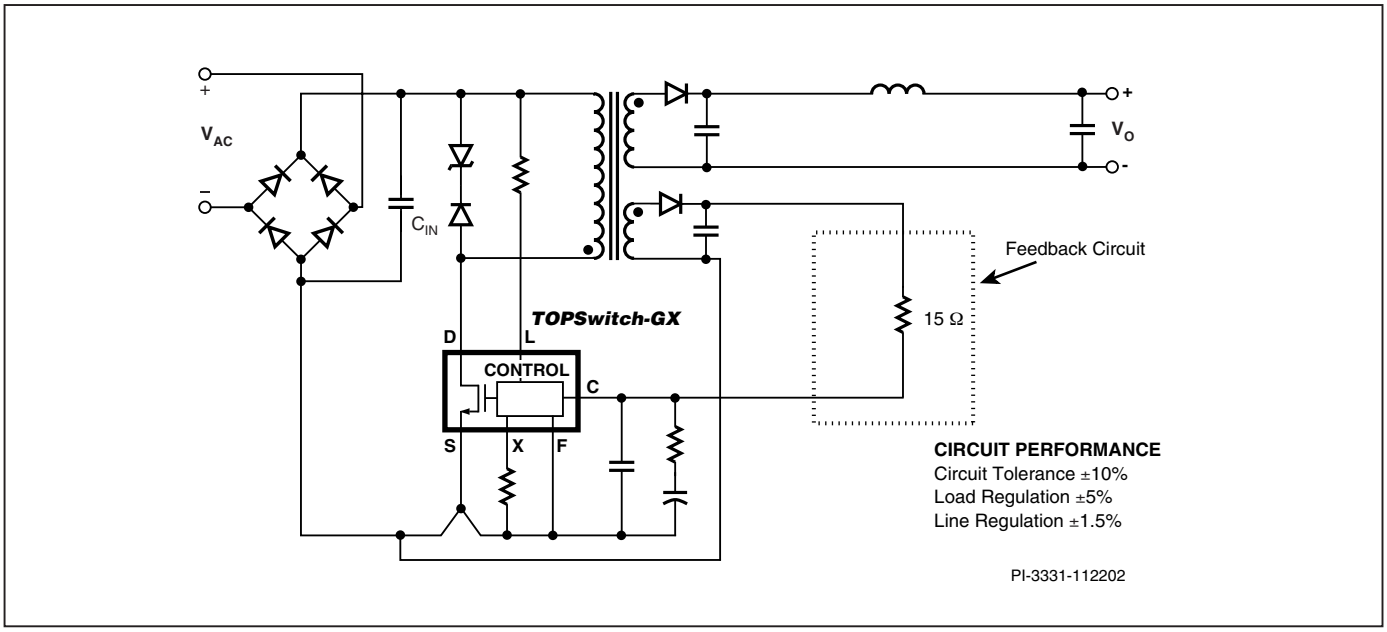

Figure 3. Primary/Basic Feedback Circuit.

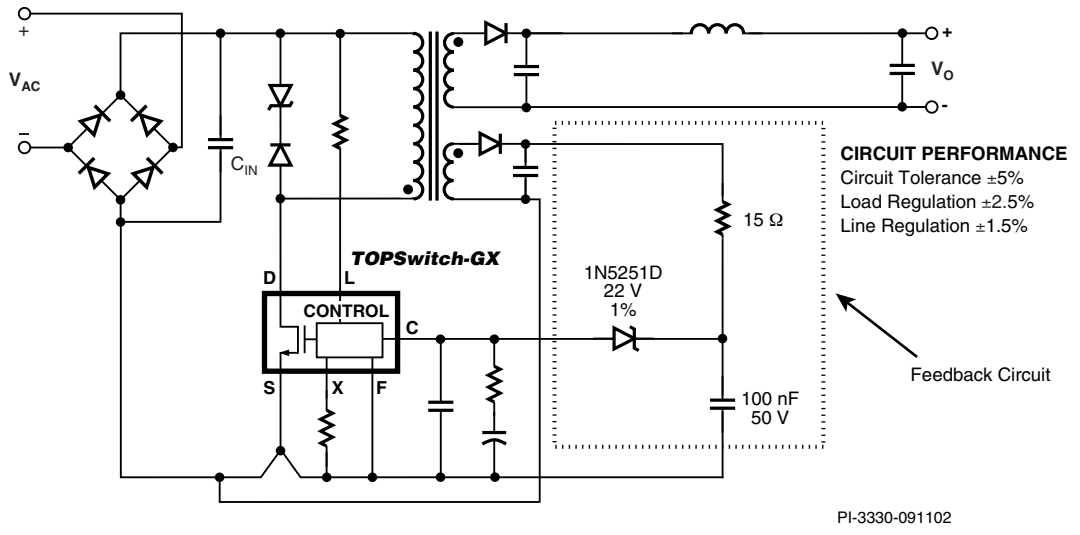

Figure 4. Primary/Enhanced Feedback Circuit.

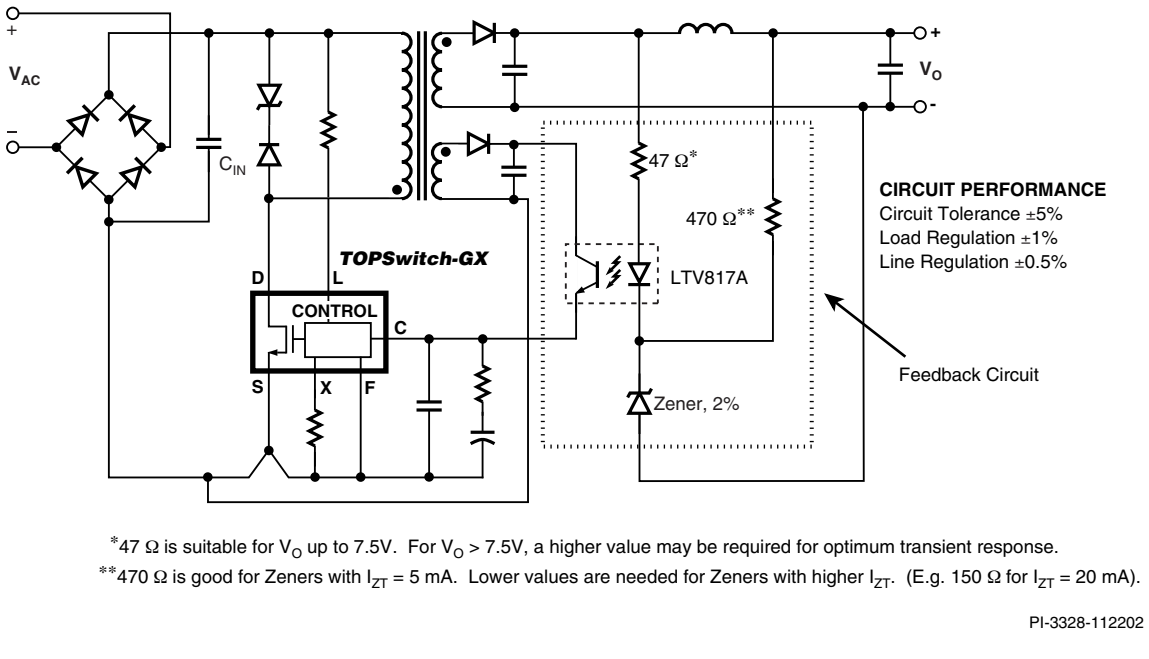

Figure 5. Opto/Zener Feedback Circuit.

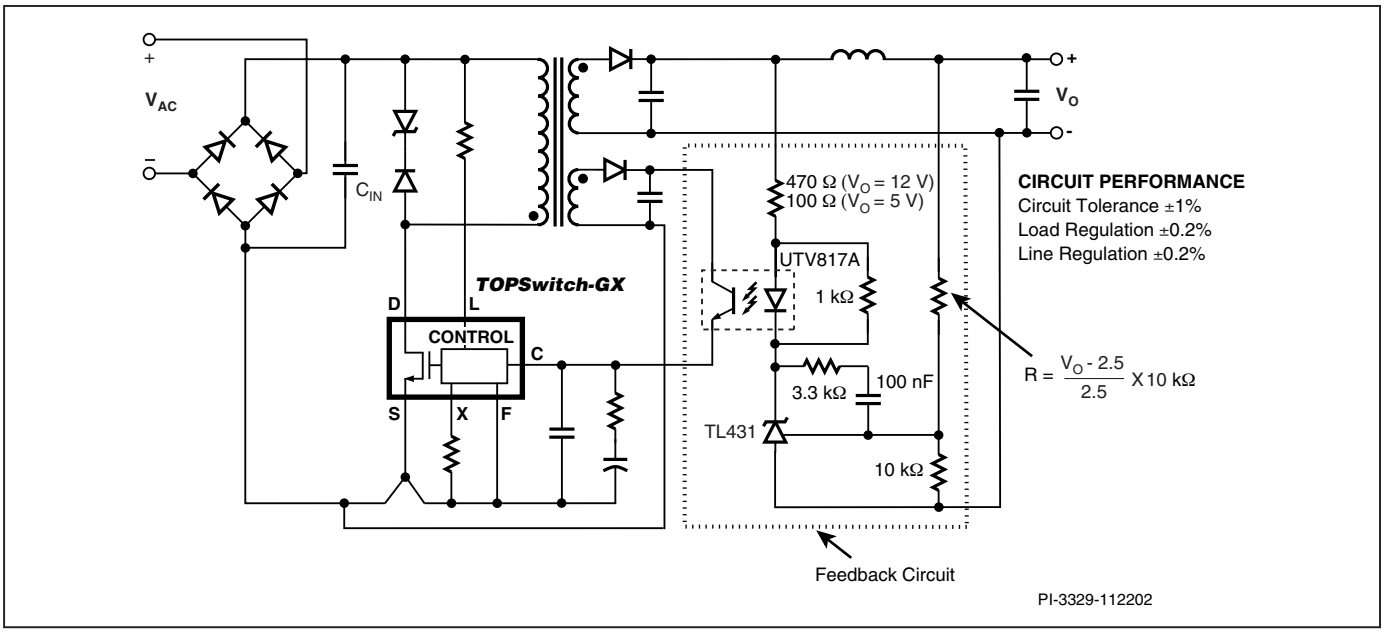

Figure 6. Opto/TL431 Feedback Circuit.

P/N	CTR(%)	BVCEO	Manufacturer
4 Pin DIP			
PC123Y6	80-160	70 V	Sharp
PC817X1	80-160	70 V	Sharp
SFH615A-2	63-125	70 V	Vishay, Isocom
SFH617A-2	63-125	70 V	Vishay, Isocom
SFH618A-2	63-125	55 V	Vishay, Isocom
ISP817A	80-160	35 V	Vishay, Isocom
LTV817A	80-160	35 V	Liteon
LTV816A	80-160	80 V	Liteon
LTV123A	80-160	70 V	Liteon
K1010A	60-160	60 V	Cosmo
6 Pin DIP			
LTV702FB	63-125	70 V	Liteon
LTV703FB	63-125	70 V	Liteon
LTV713FA	80-160	35 V	Liteon
K2010	60-160	60 V	Cosmo
PC702V2NSZX	63-125	70 V	Sharp
PC703V2NSZX	63-125	70 V	Sharp
PC713V1NSZX	80-160	35 V	Sharp
PC714V1NSZX	80-160	35 V	Sharp
MOC8102	73-117	30 V	Vishay, Isocom
MOC8103	108-173	30 V	Vishay, Isocom
MOC8105	63-133	30 V	Vishay, Isocom
CNY17F-2	63-125	70 V	Vishay, Isocom, Liteon

Table 3. Optocoupler

Step 3. Determine minimum and maximum DC input voltages V_{MIN}, V_{MAX} and input storage capacitance C_{IN} based on AC input voltage and P_O (Figure 7)

• Choose input storage capacitor, C_{IN} per Table 4.

Input (VAC)	C_{IN} (µF/Watt of P_O)	V_{MIN} (V)
Universal	2 ~ 3	≥ 90
230 or 115 with doubler	1	≥ 240

Table 4

• Set bridge rectifier conduction time, t_C = 3 ms.
• Derive minimum DC input voltage V_{MIN}

$$V_{MIN} = \sqrt{(2 \times V_{ACMIN}^2) - \frac{2 \times P_O \times \left(\frac{1}{2 \times f_L} - t_C\right)}{\eta \times C_{IN}}}$$

where units are volts, watts, Hz, seconds and farads

• Calculate maximum DC input voltage V_{MAX}:

$$V_{MAX} = \sqrt{2} \times V_{ACMAX}$$

Step 4. Determine reflected output voltage V_{OR} and clamp Zener voltage V_{CLO} (Figure 8)

- Set reflected output voltage, V_{OR} = 100 V for multiple output, 120 V for single output. These values optimize cross-regulation and efficiency. To obtain the maximum output power from a given *TOPSwitch-GX* device, set V_{OR} = 135 V.
- RCD (Resistor/Capacitor/Diode) clamp may be used with *TOPSwitch-GX* when and only when current limit is set externally with current limit reduction as a function of line voltage. Compared to Zener clamps, designs using RCD clamps usually have lower efficiency at light load. In addition, great care must be taken in RCD clamp design. Because of its inherent variation in clamp voltage across load range, if not designed properly, an RCD clamp may fail to protect *TOPSwitch-GX*, especially under startup or output overload conditions.

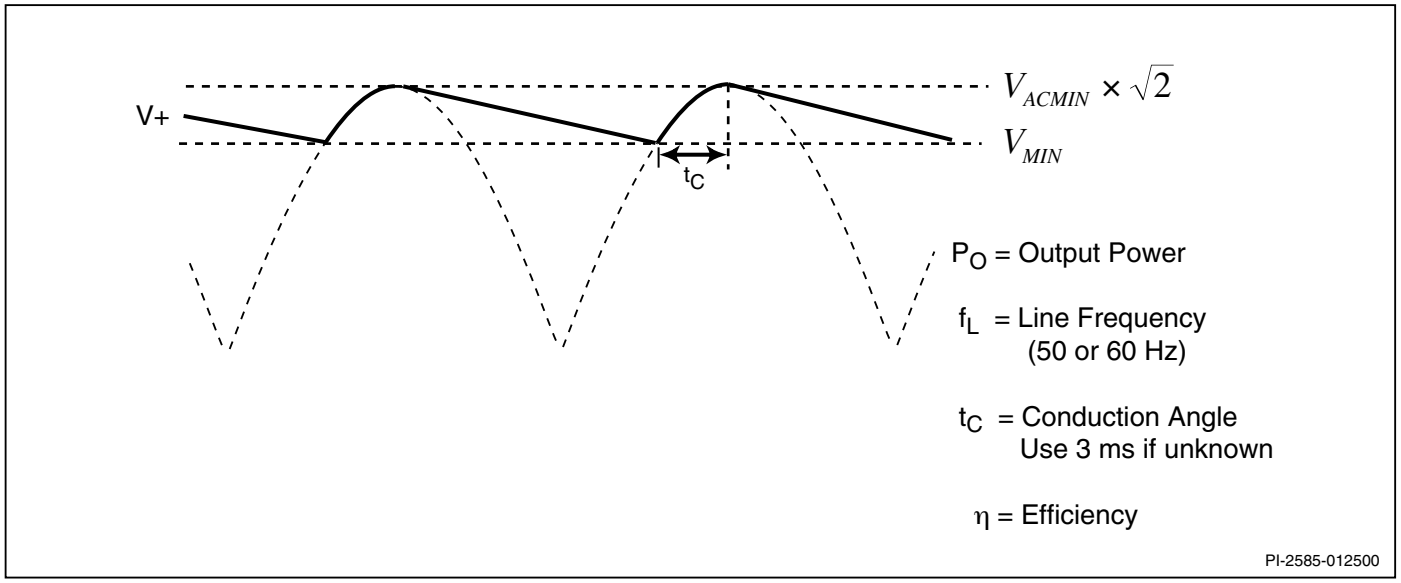

Figure 7. Input Voltage Waveform.

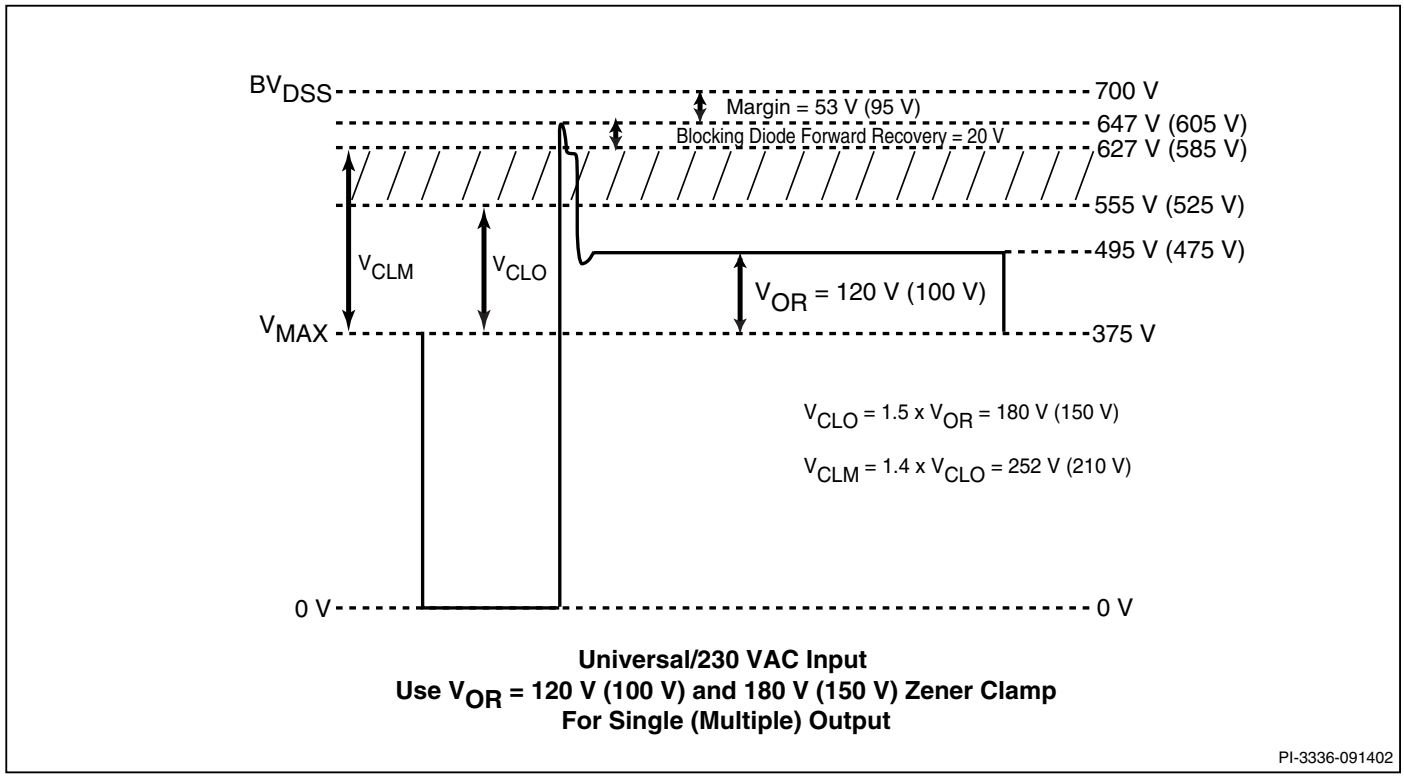

Figure 8. Reflected Voltage V_{OR} and Clamp Zener Voltage V_{CLO}.

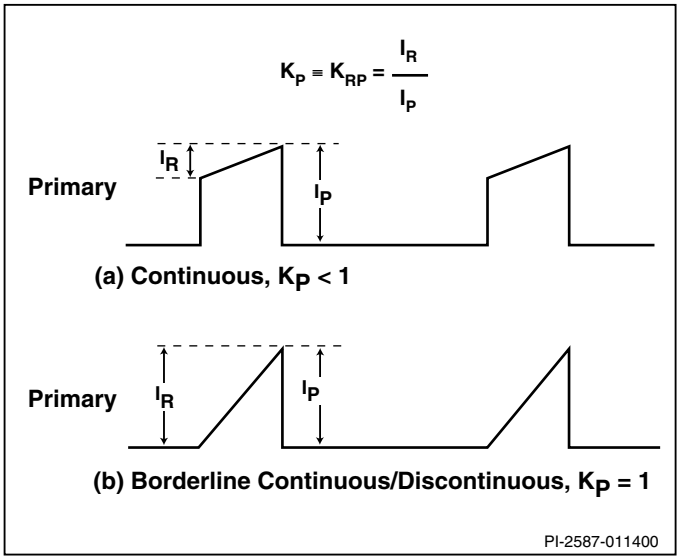

Figure 9. Continuous Mode Current Waveform, $K_P \leq 1$.

Step 5. Set current waveform parameter K_P for desired mode of operation and current waveform: $K_P \equiv K_{RP}$ for $K_P \leq 1.0$ and $K_P \equiv K_{DP}$ for $K_P \geq 1.0$ (Figures 9 and 10)

- For $K_P \leq 1.0$, $K_P \equiv K_{RP}$, continuous mode (see Figure 9)

$$K_P \equiv K_{RP} = \frac{I_R}{I_P}$$ where I_R is primary ripple current and I_P is primary peak current.

- For $K_P \geq 1.0$, $K_P \equiv K_{DP}$, discontinuous mode (see Figure 10)

$$K_P \equiv K_{DP} = \frac{V_{OR} \times (1 - D_{MAX})}{(V_{MIN} - V_{DS}) \times D_{MAX}}$$

- For continuous mode design, set
  K_P = 0.4 for universal input
  0.6 for 230 VAC or 115 VAC with doubler.
- For discontinuous mode design, set K_P = 1.0.
- K_P must be kept within the range specified in Table 5.

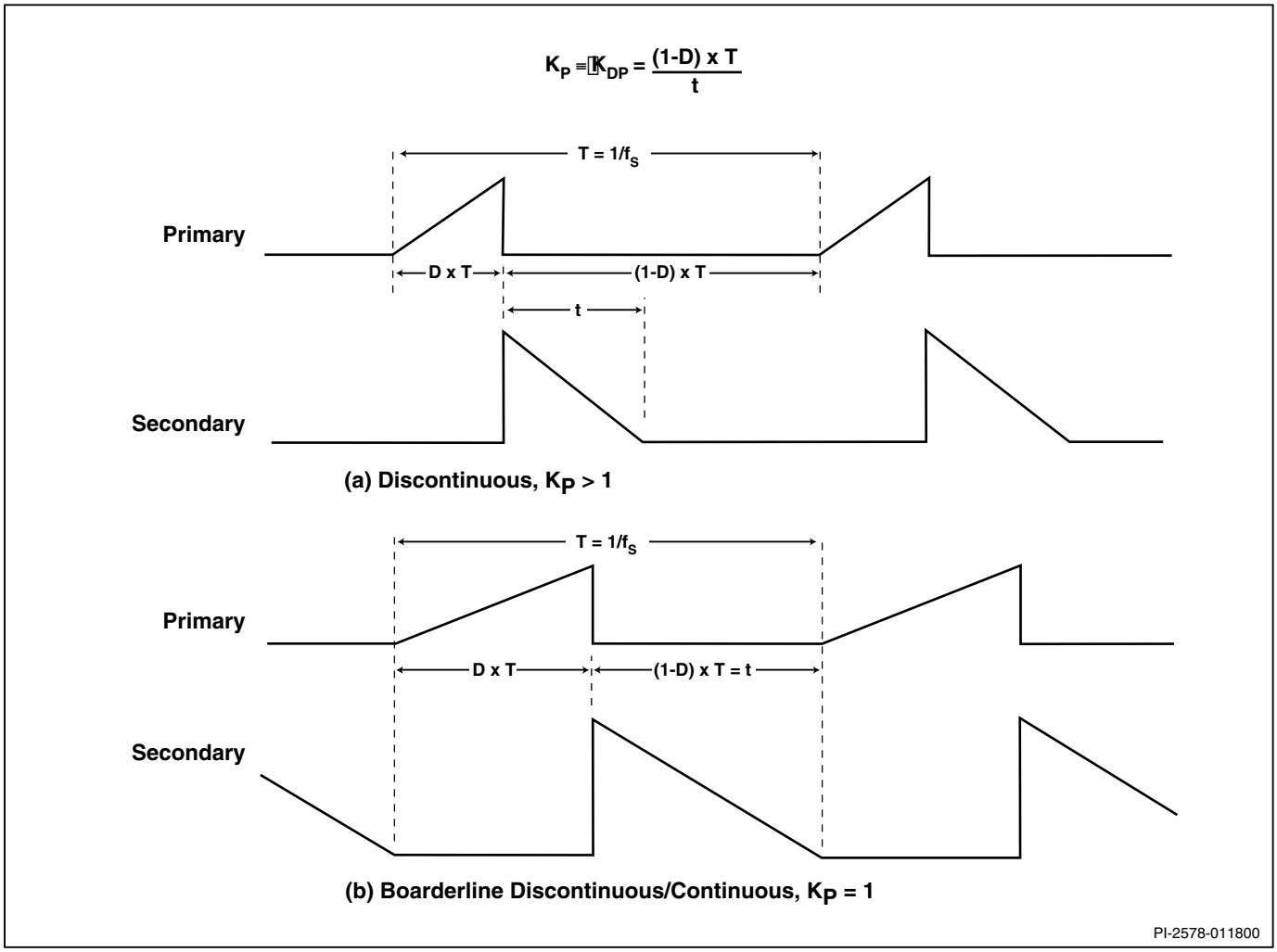

Figure 10. Discontinuous Mode Current Waveform, $K_P \geq 1$.

Input (VAC)	K_P	
	Continuous Mode	Discontinuous Mode
Universal	0.4~1.0	≥1.0
230	0.6~1.0	≥1.0

Table 5

Step 6. Determine D_{MAX} based on V_{MIN} and V_{OR}

- Continuous mode

$$D_{MAX} = \frac{V_{OR}}{(V_{MIN} - V_{DS}) + V_{OR}}$$

- Discontinuous mode

$$D_{MAX} = \frac{V_{OR}}{K_P \times (V_{MIN} - V_{DS}) + V_{OR}}$$

- Set *TOPSwitch-GX* Drain to Source voltage, V_{DS} = 10 V.

Step 7. Calculate primary peak current I_P

- Continuous mode ($K_P \le 1.0$)

$$I_P = \frac{I_{AVG}}{\left(1 - \frac{K_P}{2}\right) \times D_{MAX}}$$

- Discontinuous mode ($K_P \ge 1.0$)

$$I_P = \frac{2 \times I_{AVG}}{D_{MAX}}$$

- Input average current $I_{AVG} = \frac{P_O}{\eta \times V_{MIN}}$

Step 8. Calculate primary RMS current I_{RMS}

- Continuous mode

$$I_{RMS} = I_P \times \sqrt{D_{MAX} \times \left(\frac{K_P^2}{3} - K_P + 1\right)}$$

- Discontinuous mode

$$I_{RMS} = \sqrt{D_{MAX} \times \frac{I_P^2}{3}}$$

Step 9. Choose *TOPSwitch-GX* based on AC input voltage, V_O, P_O and η using AN-29 selection curves

- Choose the smallest *TOPSwitch-GX* using *TOPSwitch-GX* Selection Curves in AN-29.
- Identify appropriate selection curves according to AC input voltage and output voltage, V_O.
- Continuous mode: Use selection curves as is.
- Discontinuous mode: Use selection curves with the output power derated by 33%. This effectively makes a 10 W discontinuous design equivalent to a 15 W continuous design in *TOPSwitch-GX* selection.
- Switching Frequency f_S: For DIP and SMP packages, set f_S = 132 kHz. For TO-220 package, choose between 66 kHz and 132 kHz.

Step 10. Set I_{LIMIT} reduction factor K_I for External I_{LIMIT}

- $K_I = \frac{external\ I_{LIMIT}}{default\ I_{LIMIT}}$ where $0.3 \le K_I \le 1.0$
- K_I is set by the value of the resistor connected between M pin and SOURCE pin (Refer to *TOPSwitch-GX* data sheet).
- For applications demanding very high efficiency, a *TOPSwitch-GX* bigger than necessary may be used by lowering I_{LIMIT} externally to take advantage of the lower $R_{DS(ON)}$.
- If no special requirement, set K_I = 1.0.
- Calculate I_{LIMIT}(min) and I_{LIMIT}(max)

$$I_{LIMIT}(\min) = default\ I_{LIMIT}(\min) \times K_I$$

$$I_{LIMIT}(\max) = default\ I_{LIMIT}(\max) \times K_I$$

Step 11. Validate *TOPSwitch-GX* selection by checking I_P against I_{LIMIT}(min)

- For K_I = 1.0, check $I_P \le 0.96 \times I_{LIMIT}(\min)$.
- For $K_I < 1.0$, check $I_P \le 0.94 \times I_{LIMIT}(\min)$.
- Choose larger *TOPSwitch-GX* if necessary.

Step 12. Calculate primary inductance L_P

- Continuous mode

$$L_P = \frac{10^6 \times P_O}{I_P^2 \times K_P \times \left(1 - \frac{K_P}{2}\right) \times f_S(\min)} \times \frac{Z \times (1 - \eta) + \eta}{\eta}$$

where units are μH, watts, amps and Hz

- Discontinuous mode.

$$L_P = \frac{10^6 \times P_O}{I_P^2 \times \frac{1}{2} \times f_S(\min)} \times \frac{Z \times (1 - \eta) + \eta}{\eta}$$

where units are μH, watts, amps and Hz

• Z is loss allocation factor and η is efficiency from Step 1.

Step 13. Choose core and bobbin based on f_S and P_O using Table 6 and determine A_e, L_e, A_L and BW from core and bobbin catalog

• Core effective cross-sectional area, A_e: in cm^2.
• Core effective path length, L_e: in cm.
• Core ungapped effective inductance, A_L: in $nH/turn^2$.
• Bobbin width, BW: in mm.
• Choose core and bobbin based on f_S, P_O and construction type.

Output Power	66 kHz		132 kHz	
	Triple Insulated Wire	Margin Wound	Triple Insulated Wire	Margin Wound
0-10 W	EF12.6 EE13 EF16 EE16 EE19 EI22 EI22/19/6	EI22 EE19 EI22/19/6 EEL16 EF20 EI25 EEL19	EF12.6 EE13 EF16 EE16	EI22 EE19 E122/19/6 EEL16
10 W-20 W	EF20	EI28 EEL22 EF25	EE19 EI22 EI22/19/6 EF20	EF20 EI25 EEL19
20 W-30 W	EF25	EI30 EPC30 EEL25		E128
30 W-50 W	EI28 EI30 E30/15/7 EER28	E30/15/7 EER28 ETD29 EI35 EI33/29/13-Z EER28L	EF25	EEL22 EF25 EI30 EPC30
50 W-70 W	ETD29 EI35 EF32	EF32 ETD34	EI28	EEL25 E30/15/7 EER28
70 W-100 W	ETD34 E36/18/11 EI40	EI40 E36/18/11 EER35	EI30 E30/15/7 EER28 ETD29	ETD29 EI35 EI33/29/13-Z EER28L EF32
100 W-150 W	ETD39 EER40	ETD39 EER40 E42/21/15	EI35 EF32 ETD34	ETD34 EI40 E36/18/11 EER35
>150W	E42/21/15 E42/21/20 E55/28/21	E42/21/20 E55/28/21	E36/18/11 EI40 ETD39 EER40 E42/21/15 E42/21/20 E55/28/21	ETD39 EER40 E42/21/15 E42/21/20 E55/28/21

Table 6. Transformer Core.

Step 14. Set value for number of primary layers L and number of secondary turns N_S (may need iteration)

• Starting with L = 2 (Keep 1.0 ≤ L ≤ 2.0 throughout iteration).
• Starting with N_S = 0.6 turn/volt.
• Both L and N_S may need iteration.

Step 15. Calculate number of primary turns N_P and number of bias turns N_B

• Diode forward voltages: 0.7 V for ultra-fast P/N diode and 0.5 V for Schottky diode.
• Set output rectifier forward voltage, V_D.
• Set bias rectifier forward voltage, V_{DB}.
• Calculate number of primary turns.

$$N_P = N_S \times \frac{V_{OR}}{V_O + V_D}$$

• Calculate number of bias turns N_B.

$$N_B = N_S \times \frac{V_B + V_{DB}}{V_O + V_D}$$

Step 16. Determine primary winding wire parameters OD, DIA, AWG

• Primary wire outside diameter in mm.

$$OD = \frac{L \times (BW - 2 \times M)}{N_P}$$

where L is number of primary layers,
BW is bobbin width in mm,
M is safety margin in mm.

• Determine primary wire bare conductor diameter DIA and primary wire gauge AWG.

Step 17 to Step 22. Check B_M, CMA and L_g. Iterate if necessary by changing L, N_S or core/bobbin until within specified range

• Set safety margin, M. Use 3 mm (118 mils) for margin wound and zero for triple insulated secondary.
• Maximum flux density: 3000 ≥ B_M ≥ 2000, in gauss or 0.3 ≥ B_M ≥ 0.2, in tesla.

$$B_M = \frac{100 \times I_P \times L_P}{N_P \times A_e}$$

where units are gauss, amps, μH and cm^2

• Gap length in mm: $L_g \geq 0.1$

$$L_g = 40 \times \pi \times A_e \times \left(\frac{N_P^2}{1000 \times L_P} - \frac{1}{A_L} \right)$$

where L_g in mm, A_e in cm^2, A_L in nH/turn^2 and L_P in µH

• Primary winding current capacity in circular mils per amp: $500 \geq CMA \geq 200$

$$CMA = \frac{1.27 \times DIA^2 \times \frac{\pi}{4}}{I_{RMS}} \times \left(\frac{1000}{25.4} \right)^2$$

where DIA is the bare conductor diameter in mm

• Iterate by changing L, N_S, core/bobbin according to Table 7.

		B_M	L_g	CMA
L	↑	-	-	↑
N_S	↑	↓	↑	↓
core size	↑	↓	↑	↑

Table 7.

Step 23. Check $B_P \leq 4200$. If necessary, reduce current limit by lowering I_{LIMIT} reduction factor K_I

• $$B_P = \frac{I_{LIMIT}(\max)}{I_P} \times B_M$$

• Check $B_P \leq 4200$ gauss (0.42 tesla) to avoid transformer saturation at startup and output over load.
• Decrease K_I, if necessary, until $B_P \leq 4200$.

Step 24. Calculate secondary peak current I_{SP}

• $$I_{SP} = I_P \times \frac{N_P}{N_S}$$

Step 25. Calculate secondary RMS current I_{SRMS}

• Continuous mode

$$I_{SRMS} = I_{SP} \times \sqrt{(1 - D_{MAX}) \times \left(\frac{K_P^2}{3} - K_P + 1 \right)}$$

• Discontinuous mode

$$I_{SRMS} = I_{SP} \times \sqrt{\frac{1 - D_{MAX}}{3 \times K_P}}$$

Step 26. Determine secondary winding wire parameters OD_S, DIA_S, AWG_S

• Secondary wire outside diameter in mm

$$OD_S = \frac{BW - (2 \times M)}{N_S}$$

• Secondary wire bare conductor diameter in mm

$$DIA_S = \sqrt{\frac{4 \times CMA_S \times I_{SRMS}}{1.27 \times \pi}} \times \frac{25.4}{1000}$$

where CMA_S is secondary winding current capacity in circular mils per amp. Minimum wire diameter is calculated by using a CMA_S of 200.

• Determine secondary winding wire gauge AWG_S based on DIA_S. If the bare conductor diameter of the wire is larger than that of the 27 AWG for 132 kHz or 25 AWG for 66 kHz, a parallel winding using multiple strands of thinner wire should be used to minimize skin effect.

Step 27. Determine output capacitor ripple current I_{RIPPLE}

• Output capacitor ripple current

$$I_{RIPPLE} = \sqrt{I_{SRMS}^2 - I_O^2}$$

where I_O is the output DC current

Step 28. Determine maximum peak inverse voltages PIV_S, PIV_B for secondary and bias windings

• Secondary winding maximum peak inverse voltage.

$$PIV_S = V_O + (V_{MAX} \times \frac{N_S}{N_P})$$

• Bias winding maximum peak inverse voltage.

$$PIV_B = V_B + (V_{MAX} \times \frac{N_B}{N_P})$$

Step 29. Select clamp Zener and blocking diode per Table 8 for primary clamping based on V_{OR} and the type of output

PS Output	V_{OR}	Blocking Diode	Clamp Zener
Multiple Output	100 V	BYV26C MUR160 UF4005	P6KE150
Single Output	120 V	BYV26C MUR160 UF4005	P6KE180

Table 8.

Step 30. Select output rectifier per Table 9

- $V_R \geq 1.25 \times PIV_S$; where PIV_S is from Step 28 and V_R is the rated reverse voltage of the rectifier diode.
- $I_D \geq 3 \times I_O$; where I_D is the diode rated DC current and $I_O = P_O / V_O$.

Rec. Diode	V_R(V)	I_D(A)	Package	Manufacturer
Schottky				
1N5819	40	1	Axial	General Semi
SB140	40	1	Axial	General Semi
SB160	60	1	Axial	General Semi
MBR160	60	1	Axial	IR
11DQ06	60	1.1	Axial	IR
1N5822	40	3	Axial	General Semi
SB340	40	3	Axial	General Semi
MBR340	40	3	Axial	IR
SB360	60	3	Axial	General Semi
MBR360	60	3	Axial	IR
SB540	40	5	Axial	General Semi
SB560	60	5	Axial	General Semi
MBR745	45	7.5	TO-220	General Semi IR
MBR760	60	7.5	TO-220	General Semi
MBR1045	45	10	TO-220	General Semi IR
MBR1060	60	10	TO-220	General Semi
MBR10100	100	10	TO-220	General Semi
MBR1645	45	16	TO-220	General Semi IR
MBR1660	60	16	TO-220	General Semi
MBR2045CT	45	20(2x10)	TO-220	General Semi IR
MBR2060CT	60	20(2x10)	TO-220	General Semi
MBR20100	100	20(2x10)	TO-220	General Semi IR
UFR				
UF4002	100	1	Axial	General Semi
UF4003	200	1	Axial	General Semi
MUR120	200	1	Axial	General Semi
EGP20D	200	2	Axial	General Semi
BYV27-200	200	2	Axial	General Semi Philips
UF5401	100	3	Axial	General Semi
UF5402	200	3	Axial	General Semi
EGP30D	200	3	Axial	General Semi
BYV28-200	200	3.5	Axial	General Semi Philips
MUR420	200	4	TO-220	General Semi
BYW29-200	200	8	TO-220	General Semi Philips
BYV32-200	200	18	TO-220	General Semi Philips

Table 9.

Step 31. Select output capacitor

- Ripple current specification at 105 °C, 100 kHz: Must be equal to or larger than $I_{RIPPLE,}$ where I_{RIPPLE} is from Step 27.
- ESR specification: Use low ESR, electrolytic capacitor. Output switching ripple voltage is $I_{SP} \times$ ESR , where I_{SP} is from Step 24.
- Examples:

Output	Output Capacitor
5 V to 24 V, 1 A	330 µF, 35 V, low ESR, electrolytic UnitedChemicon LXZ35VB331M10X16LL Rubycon 35YXG330M10x16 Panasonic EEUFC1V331
5 V to 24 V, 2 A	1000 µF, 35 V, low ESR, electrolytic United Chemicon LXZ35VB102M12X25LL Rubycon 35YXG1000M12.5x25 Panasonic EEUFC1V102

Step 32. Select output post filter L, C

- Inductor L: 2.2 µH to 4.7 µH. Use ferrite bead for low current (≤1A) output and standard off-the-shelf choke for higher current output. Increase choke current rating or wire size, if necessary, to avoid significant DC voltage drop.
- Capacitor C:100 µF to 330 µF, 35 V, electrolytic

  Examples for 100 µF, 35 V, electrolytic:

  United Chemicon KMG35VB101M6X11LL
  Rubycon 35YXA100M6.3x11
  Panasonic ECA1VHG101

Step 33. Select bias rectifier from Table 10

- $V_R \geq 1.25 \times PIV_B$; where PIV_B is from Step 28 and V_R is the rated reverse voltage of the rectifier diode.

Rectifier	V_R (V)	Manufacturer
BAV21	200	Philips
UF4003	200	General Semi
1N4148	75	Motorola

Table 10.

Step 34. Select bias capacitor

- Use 0.1 µF, 50 V, ceramic.

Step 35. Select CONTROL pin capacitor and series resistor

- CONTROL pin capacitor: 47 µF, 10 V, low cost electrolytic (Do not use low ESR capacitor).

- Series resistor: 6.8 Ω, 1/4 W (Not needed if $K_P \geq 1$, i.e. discontinuous mode).

Step 36. Select feedback circuit components according to applicable reference feedback circuits shown in Figures 3, 4, 5 and 6

- Applicable reference circuit: Identified in Step 2.

Step 37. Select input bridge rectifier

- $V_R \geq 1.25 \times \sqrt{2} \times V_{ACMAX}$; where V_{ACMAX} is from Step 1.
- $I_D \geq 2 \times I_{AVE}$; where I_D is the bridge rectifier rated current and I_{AVE} is average input current.

  Note: $I_{AVE} = \dfrac{P_{OUT}}{V_{MIN} \times \eta}$;

  where V_{MIN} is from Step 3 and η from Step 1.

Appendix A

Multiple Output Flyback Power Supply Design

The only difference between a multiple output flyback power supply and a single output flyback power supply of the same total output power is in the secondary side design. Instead of delivering all power to one output as in the single output case, a multiple output flyback distributes its output power among several outputs. Therefore, the design procedure for the primary side stays the same, while that for the secondary side demands further considerations.

Design with lumped output power

One simple way of doing multiple output flyback design is described in detail in AN-22, "Designing Multiple Output Flyback Power Supplies with *TOPSwitch*". The design method starts with a single output equivalent by lumping output power of all outputs to one main output. Secondary peak current I_{SP} and RMS current I_{SRMS} are derived. Output average current I_O corresponding to the lumped power is also calculated.

Assumption for simplification

The current waveforms in the individual output windings are determined by the impedance in each circuit, which is a function of leakage inductance, rectifier characteristics, capacitor value and most importantly, output load. Although this current waveform may not be exactly the same from output to output, it is reasonable to assume that, to the first order, all output currents have the same shape as for the single output equivalent of lumped power.

Output RMS current vs. average current

The output average current is always equal to the DC load current, while the RMS value is determined by current wave shape. Since the current wave shapes are assumed to be the same for all outputs, their ratio of RMS to average currents must also be identical. Therefore, with the output average current known, the RMS current for each output winding can be calculated as

$$I_{SRMS}(n) = I_O(n) \times \frac{I_{SRMS}}{I_O}$$

where $I_{SRMS}(n)$ and $I_O(n)$ are the secondary RMS current and output average current of the n^{th} output and I_{SRMS} and I_O are the secondary RMS current and output average current for the lumped single output equivalent design.

Customization of secondary designs for each output

The turns for each secondary winding are calculated based on the respective output voltage $V_O(n)$:

$$N_S(n) = N_S \times \frac{V_O(n) + V_D(n)}{V + V_D}$$

Output rectifier maximum inverse voltage is

$$PIV_S(n) = V_{MAX} \times \frac{N_S(n)}{N_P} + V_O(n)$$

With output RMS current $I_{SRMS}(n)$, secondary number of turns $N_S(n)$ and output rectifier maximum inverse voltage $PIV_S(n)$ known, the secondary side design for each output can now be carried out exactly the same way as for the single output design.

Secondary winding wire size

The *TOPSwitch-GX* design spreadsheet assumes a CMA of 200 when calculating secondary winding wire diameters. This gives the minimum wire sizes required for the RMS currents of each output using seperate windings. Designers may wish to use larger size wire for better thermal performance. Other considerations such as skin effect and bobbin coverage may suggest the use of a smaller wire by using multiple strands wound in parallel. In addition, practical considerations in transformer manufacturing may also dictate the wire size.

Revision	Notes	Date
A	1) Final release.	9/02
B	1) Minor revision.	12/02
C	1) Minor revision: Corrected V_{MAX} equation.	7/04

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Power Integrations Worldwide Sales Support Locations

WORLD HEADQUARTERS
5245 Hellyer Avenue
San Jose, CA 95138, USA.
Main: +1-408-414-9200
Customer Service:
Phone: +1-408-414-9665
Fax: +1-408-414-9765
e-mail: usasales@powerint.com

CHINA (SHANGHAI)
Rm 807, Pacheer
Commercial Centre
555 Nanjing West Road
Shanghai, 200041, China
Phone: +86-21-6215-5548
Fax: +86-21-6215-2468
e-mail: chinasales@powerint.com

CHINA (SHENZHEN)
Room 2206-2207, Block A,
Electronics Science & Technology Bldg.,
2070 Shennan Zhong Road,
Shenzhen, Guangdong,
China, 518031
Phone: +86-755-8379-3243
Fax: +86-755-8379-5828
e-mail: chinasales@powerint.com

GERMANY
Rueckertstrasse 3
D-80336, Muenchen, Germany
Phone: +49-89-5527-3910
Fax: +49-89-5527-3920
e-mail: eurosales@powerint.com

INDIA (TECHNICAL SUPPORT)
Innovatech
261/A, Ground Floor
7th Main, 17th Cross,
Sadashivanagar
Bangalore 560080
Phone: +91-80-5113-8020
Fax: +91-80-5113-8023
e-mail: indiasales@powerint.com

ITALY
Via Vittorio Veneto 12,
Bresso
Milano, 20091, Italy
Phone: +39-028-928-6001
Fax: +39-028-928-6009
e-mail: eurosales@powerint.com

JAPAN
Keihin-Tatemono 1st Bldg.
12-20 Shin-Yokohama
2-Chome,
Kohoku-ku, Yokohama-shi,
Kanagawa 222-0033, Japan
Phone: +81-45-471-1021
Fax: +81-45-471-3717
e-mail: japansales@powerint.com

KOREA
8th Floor, DongSung Bldg.
17-8 Yoido-dong,
Youngdeungpo-gu,
Seoul, 150-874, Korea
Phone: +82-2-782-2840
Fax: +82-2-782-4427
e-mail: koreasales@powerint.com

SINGAPORE
51 Newton Road
#15-08/10 Goldhill Plaza
Singapore, 308900
Phone: +65-6358-2160
Fax: +65-6358-2015
e-mail: singaporesales@powerint.com

TAIWAN
5F-1, No. 316, Nei Hu Rd., Sec. 1
Nei Hu Dist.
Taipei, Taiwan 114, R.O.C.
Phone: +886-2-2659-4570
Fax: +886-2-2659-4550
e-mail: taiwansales@powerint.com

UK (EUROPE & AFRICA HEADQUARTERS)
1st Floor, St. James's House
East Street
Farnham
Surrey
GU9 7TJ
United Kingdom
Phone: +44 (0) 1252-730-140
Fax: +44 (0) 1252-727-689
e-mail: eurosales@powerint.com

APPLICATIONS HOTLINE
World Wide +1-408-414-9660

APPLICATIONS FAX
World Wide +1-408-414-9760