HDMI Input Peripheral

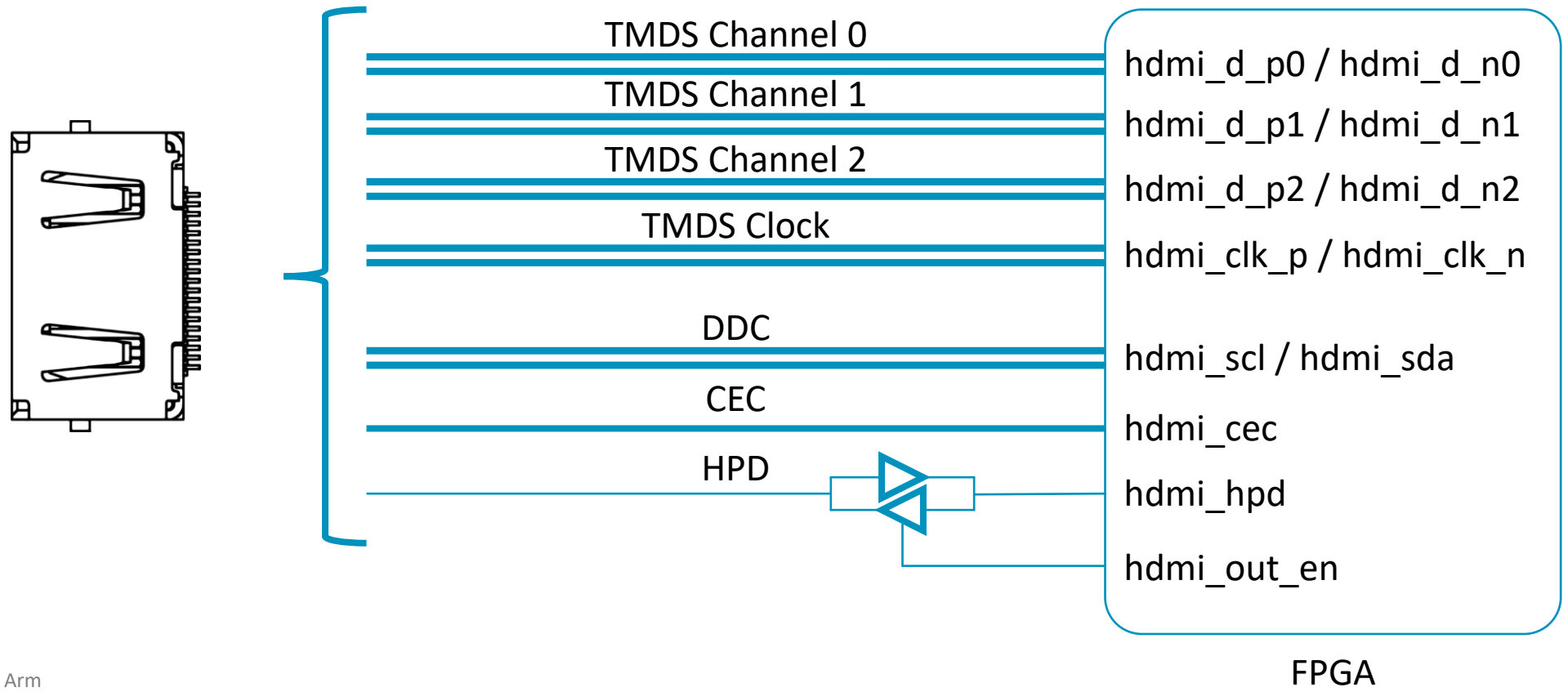
Learning Outcomes

At the end of this module, you will be able to:

- Identify the function of miscellaneous HDMI signals including DDC, CEC, and HPD.
- Outline the operation of an example implementation of an AXI4-Stream HDMI input peripheral.

HDMI Interface

- HDMI port on some development boards can be configured as either input or output, controlled by a HDMI_OUT_EN signal (for example).



HDMI Signals: Display Data Channel (DDC)

- Used by the HDMI source device to read the E-EDID data from the HDMI sink device.
  - Used to learn what audio/video formats it can take.
- Based on the I^2C bus specification.
  - Usually implemented by an I^2C EEPROM at address 0x50.
  - Implemented on FPGA in our Lab.

HDMI Signals: Consumer Electronics Control (CEC)

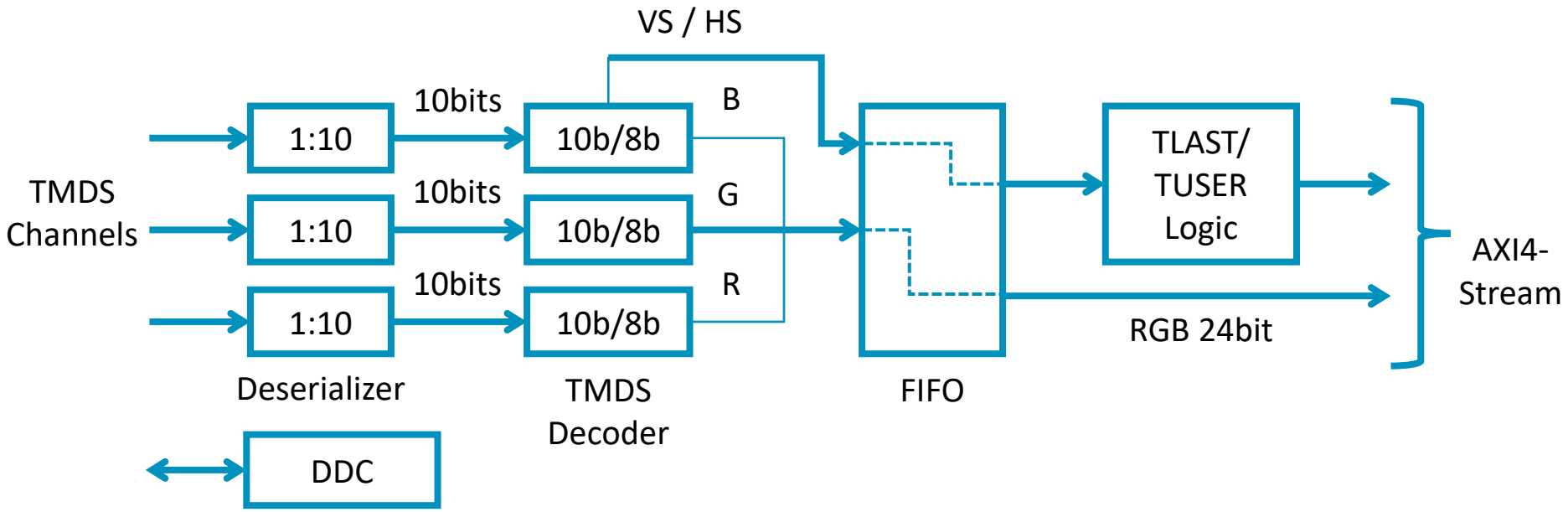
- Designed to allow the command and control of up-to 15 CEC-enabled devices connected through HDMI by using only one of their remote controls.
- One-wire bidirectional serial bus based on the CENELEC standard AV.link protocol.
- Implementation is optional.

HDMI Signals: Hot Plug Detect (HPD)

- Weak pulled-up to a positive voltage on sink devices.
- Pulled-down to ground on source devices.
- Allow sink devices to detect a plug action of sources

AXI4-Stream HDMI Input Peripheral

- Deserializing TMDS channels to 10-bit parallel data.
- 10b/8b decoding to 8-bit video data and VSYNC/HSYNC.
- Transmitting video data and VSYNC/HSYNC to AXI-Stream clock domain using a FIFO.
- Generating TLAST and TUSER of AXI-Stream interface.
- DDC implementation.



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TMDS Deserialization and Decoding in Xilinx FPGA

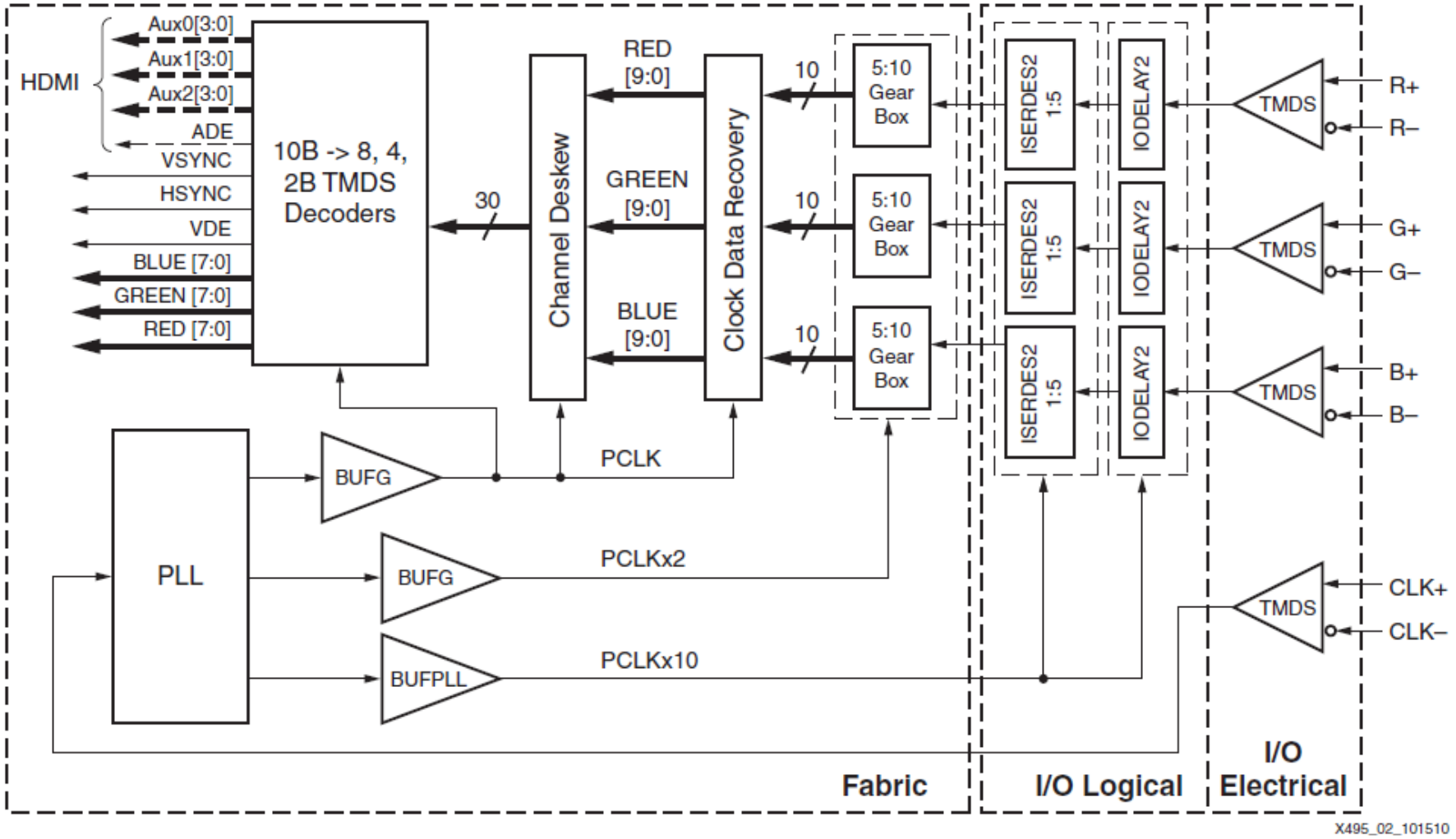
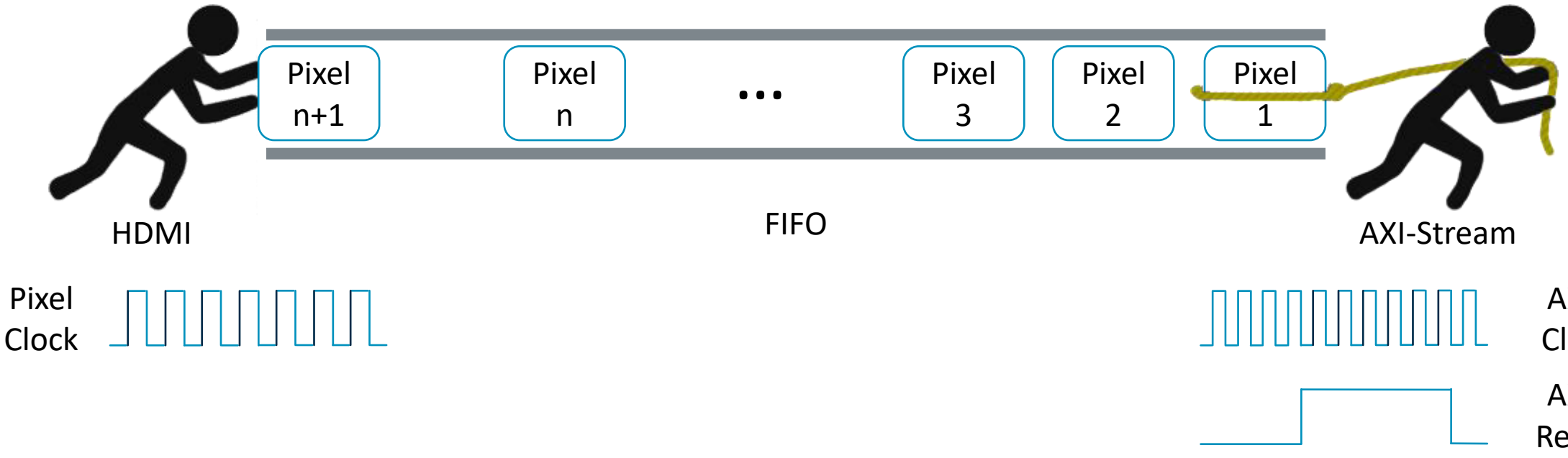


Figure source: Xilinx XAPP495 (v1.0), 2010

Utilization of FIFO

- Clock domain crossing from HDMI pixel clock to AXI-Stream clock.
- Buffering pixels when AXI-Stream is busy.



TVALID / TUSER / TLAST Logic

- TVALID is asserted when FIFO is not empty.
- TUSER is asserted when the first pixel of each frame.
  - Set when vertical blanking.
  - Reset when negative clock edge after the first pixel.
- TLAST is asserted at the last pixel of each line.
  - Use a counter to count pixels of each line.
  - Set TLAST at negative clock edge before the last pixel.