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HDMI overview

Learning Outcomes

At the end of this module, you will be able to:

- Explain what HDMI is and what it does in comparison with other video connection types.
- Identify the HDMI interfaces including the TDMS channels.
- Describe the properties of TDMS timing.

What is HDMI?

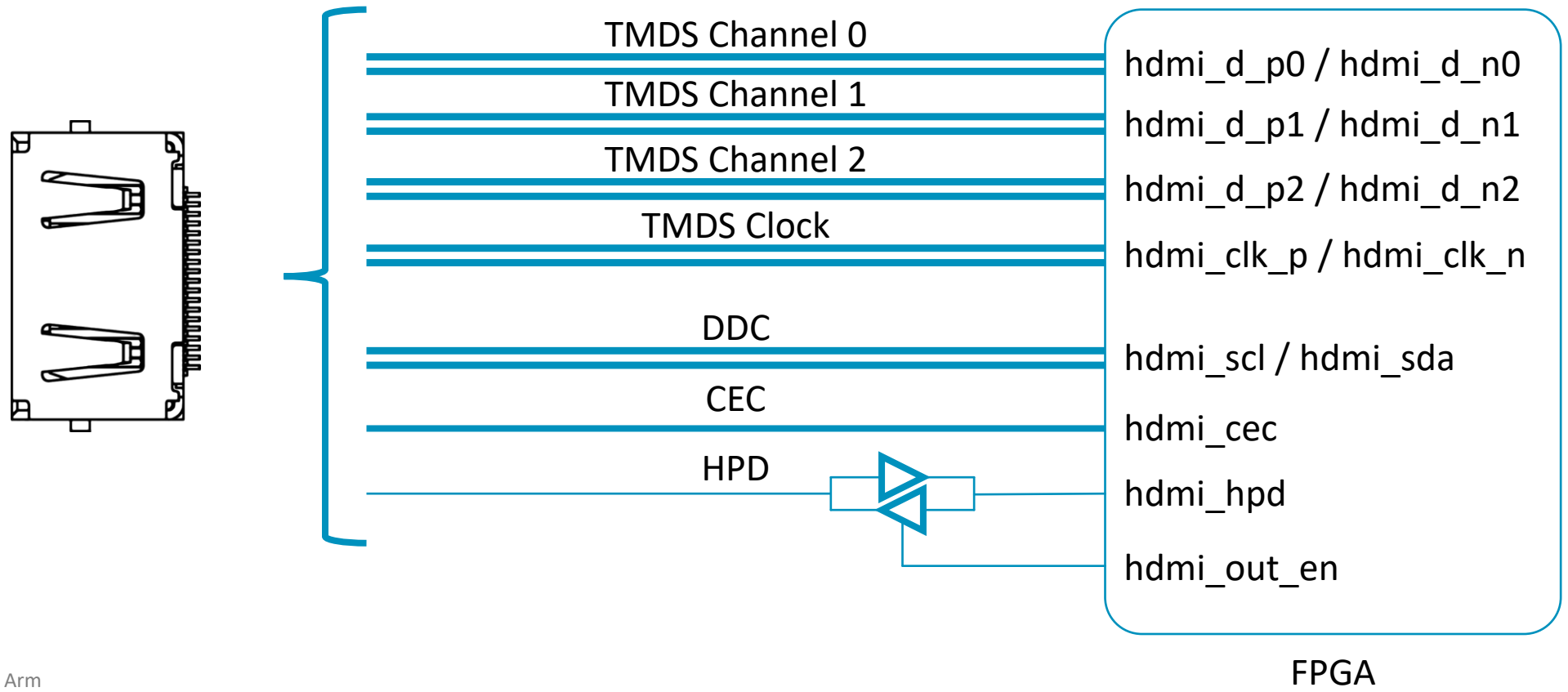
- HDMI (High-Definition Multimedia Interface)
  - Compact audio/video interface
  - Transfers uncompressed video data and compressed or uncompressed digital audio data.
  - A digital replacement for existing analog video standards.

Comparison among Video Connections

		Resolution	Signals
Composite Video		625 lines	Analog 1 + shield
VGA		2048×1536@60Hz (Device-dependent)	Analog 3 + VS/HS
DVI		1920×1200@60Hz (Single link) 2560×1600@60Hz (Dual link)	Digital 6 TMDS
HDMI		1920×1200@60Hz (v1.0) 4096×2160@60Hz (v2.0)	Digital 3 TMDS
DisplayPort		2560×1600@60Hz (v1.1) 7680×4320@60Hz (v1.3)	Digital 4 LVDS

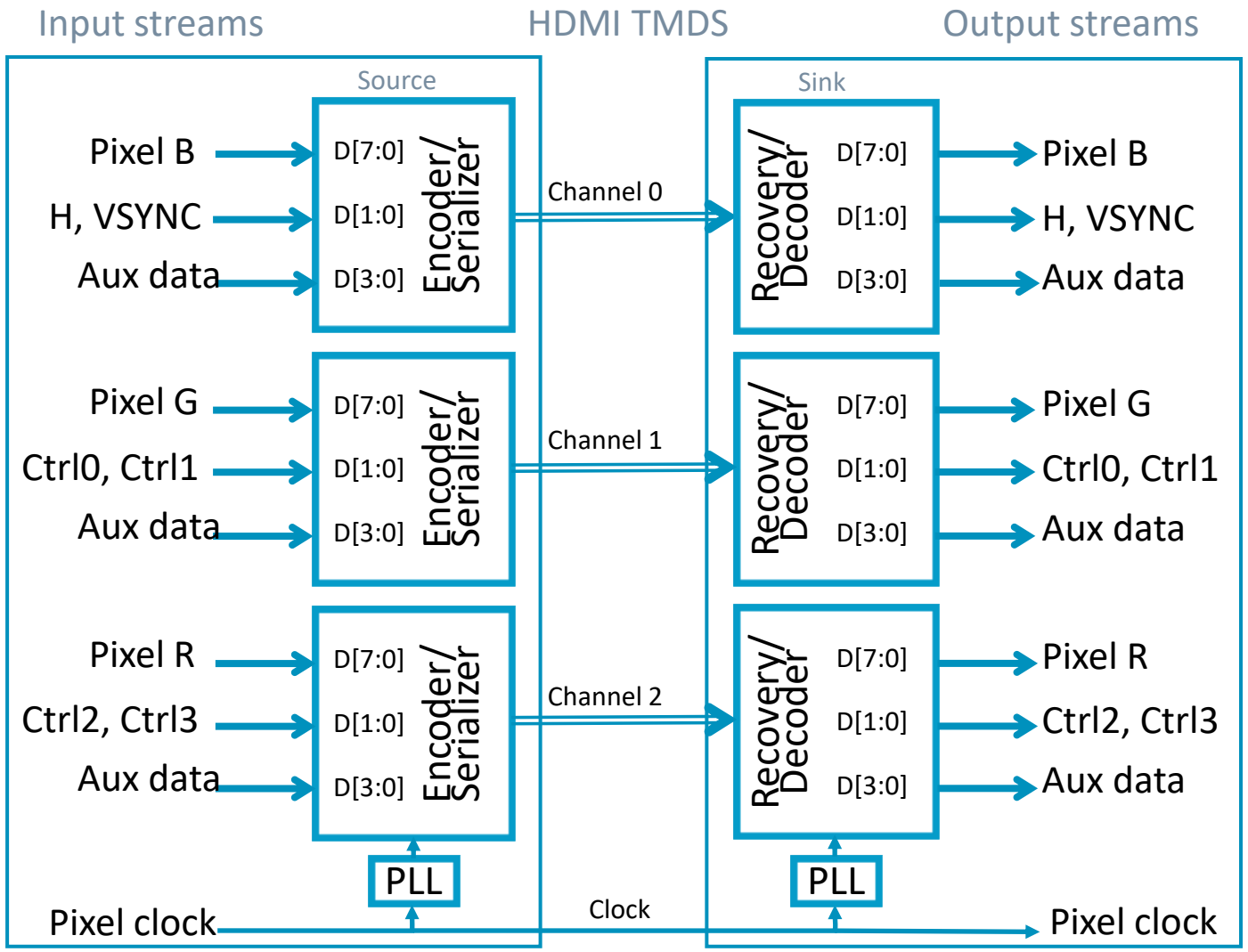
HDMI Interface

- HDMI port on some development boards can be configured as either input or output, controlled by a HDMI_OUT_EN signal (for example).



HDMI Signals: TMDS channels

- 3 pairs of TMDS and 1 Clock:
  - 3.3V level
  - 8b/10b encoding
  - 10 bits on PHY during I clock period
- Transmitting video data, control data, and audio data.



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HDMI Signals: TMDS Timing

- A video frame contains vertical blanking, horizontal blanking and active video.
- Blanking contains Control Period and Data Island Period (e.g. audio).
- A Control Period is required between any two periods that are not Control Periods.
- The Preamble, contained in each Control Period, indicates the type of the following data period.

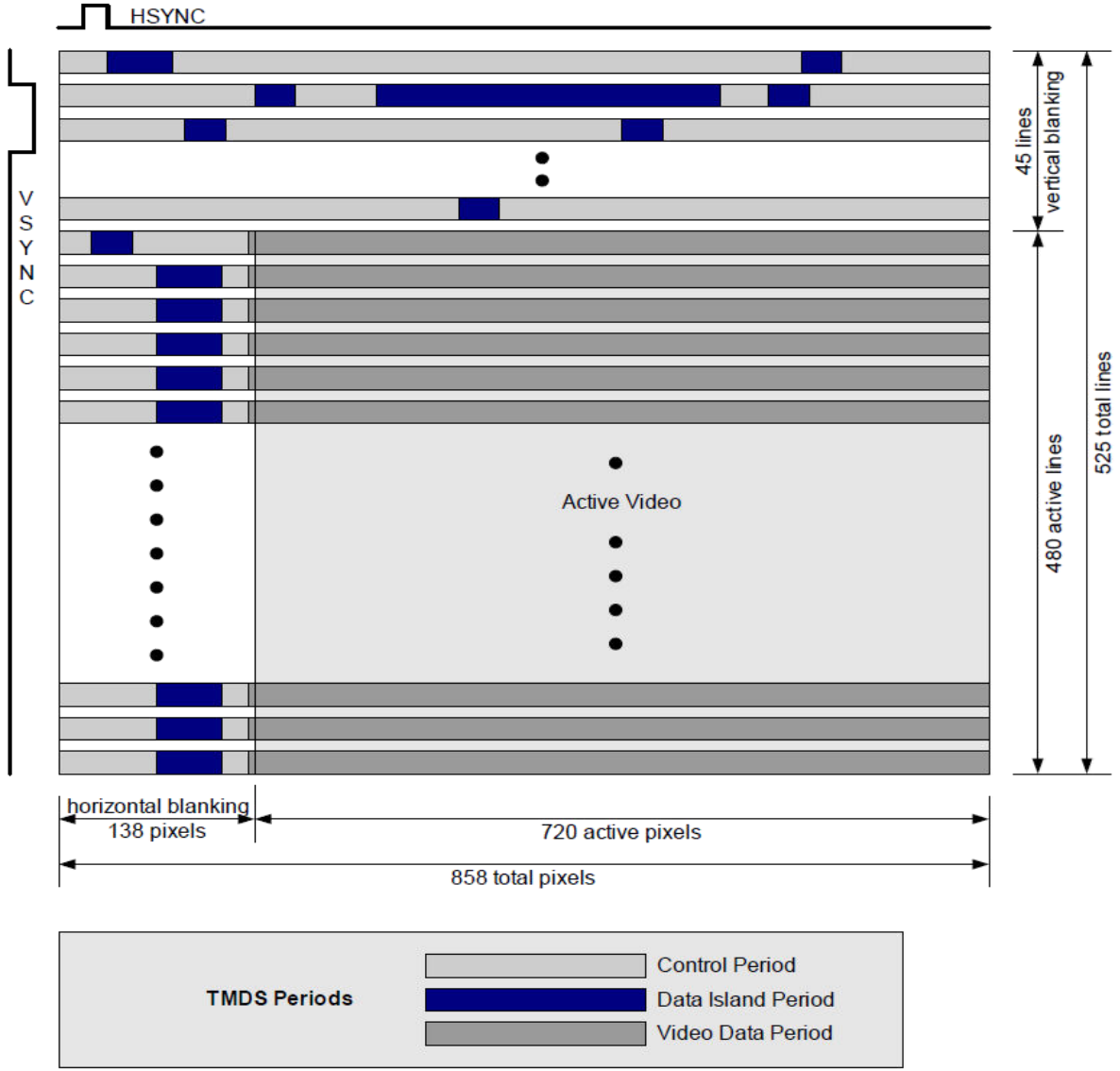


Figure source: High-Definition Multimedia Interface Specification Version 1.3a.

HDMI Signals: Display Data Channel (DDC)

- Used by the HDMI source device to read the E-EDID data from the HDMI sink device.
  - Used to learn what audio/video formats it can take.
- Based on the I^2C bus specification.
  - Usually implemented by an I^2C EEPROM at address 0x50.
  - Implemented on FPGA in our Lab.

HDMI Signals: Consumer Electronics Control (CEC)

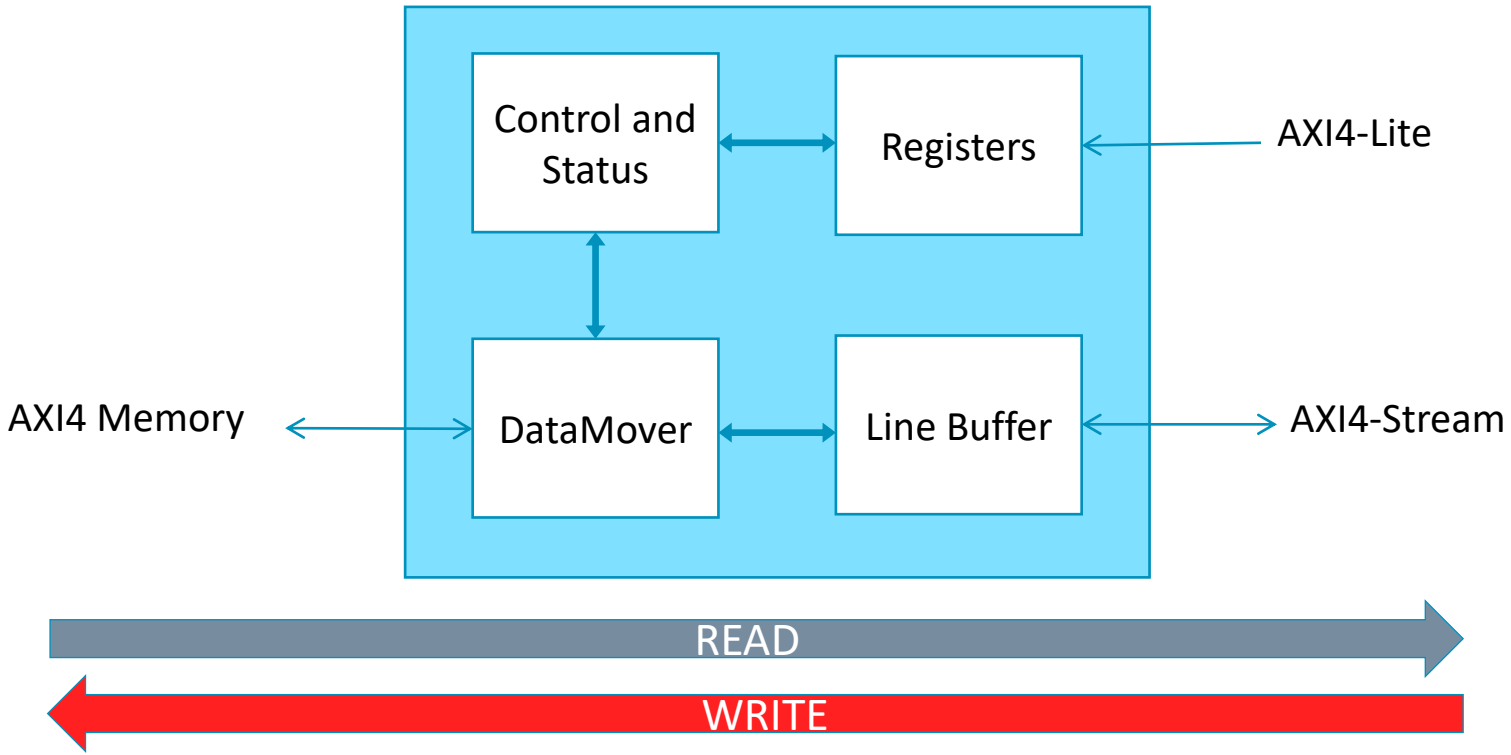
- Allows the command and control of up-to 15 CEC-enabled devices connected through HDMI by using only one of their remote controls.
- One-wire bidirectional serial bus
- Based on the CENELEC standard AV.link protocol.
- Implementation is optional (not used in our Lab).

HDMI Signals: Hot Plug Detect (HPD)

- Weak pulled-up to a positive voltage on sink devices.
- Pulled-down to ground on source devices.
- Allow sink devices to detect a plug action of sources.

Hardware Implementation

- In Xilinx AXI Video DMA IP core
  - TDATA is used as 24-bit RGB data.
  - TLAST is used to indicate the end of each line.
  - TUSER is used to indicate the start of each frame.



Useful Resources

- AMBA® 4 AXI4-Stream Protocol Specification. ARM, 2010.
- AXI Video Direct Memory Access v6.2. LogiCORE IP Product Guide. Vivado Design Suite. Xilinx, 2015.