Signal Processors Lecture Notes, Pt 4

Institute for Technical Informatics, DI Dr. Eugen Brenner

Signal Processors, 448.032

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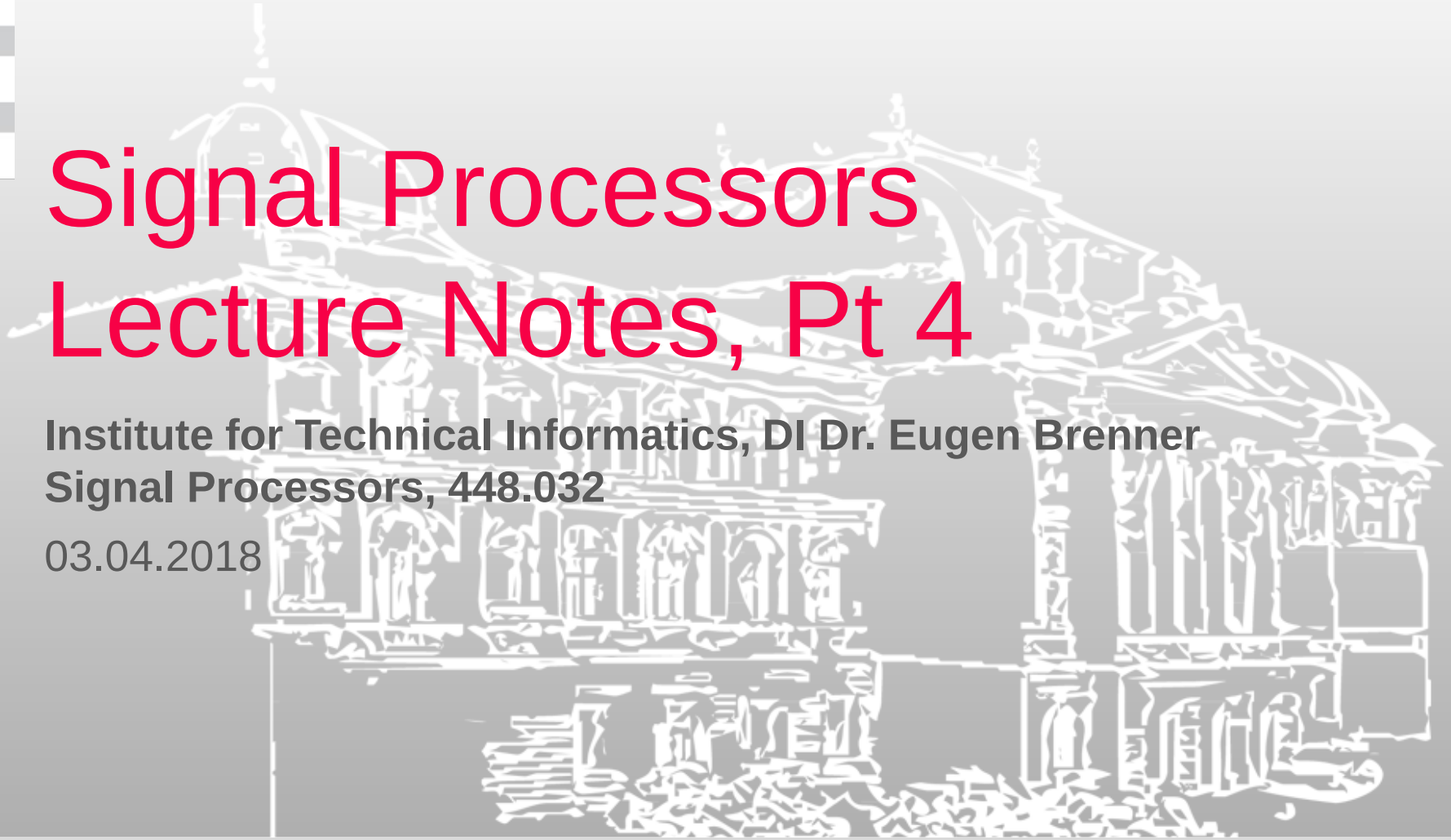


Chapter Overview

4. DSP Platforms & Performance Criteria
   - Performance Criteria
   - Texas Instruments DSPs
   - Alternative Platforms
   - Comparison
   - Conclusion

Performance Criteria

Performance Criteria

- Performance evaluation / comparison is difficult
  - Several possibilities
- Performance characteristics
  - Simple “parameters” for the classification of the processors
- Benchmarks
  - Performance evaluation of well-defined test programs such as Dhrystone, Whetstone, etc.
- Application
  - Performance of the overall system (application)

Characteristic – Architectures

- Fixed-point / floating point
  - Internal processing in the data path
- Clock rate
  - Clock rate of processor core, memory
- Data width
  - Internal data width of ALU and registers
- Instruction format
  - Format of assembler instructions
- Memory size
  - Internal or external memory, size of caches

Characteristic – Performance

- Computing performance
  - MIPS (million instructions per second)
    - Does not consider performance of individual instructions
  - MFLOPS (million floating-point operations per second)
    - Parallelism is considered (e.g., ADD & MULT)
  - MMACS (million multiply & accumulates per second)
    - Specific for DSPs
  - MOPS (million operations per second)
    - All functional units are considered (DMA, address generation, etc.)
- Communication
  - MBPS (million bits/bytes per second)
    - Broken down into busses / channels

Characteristics

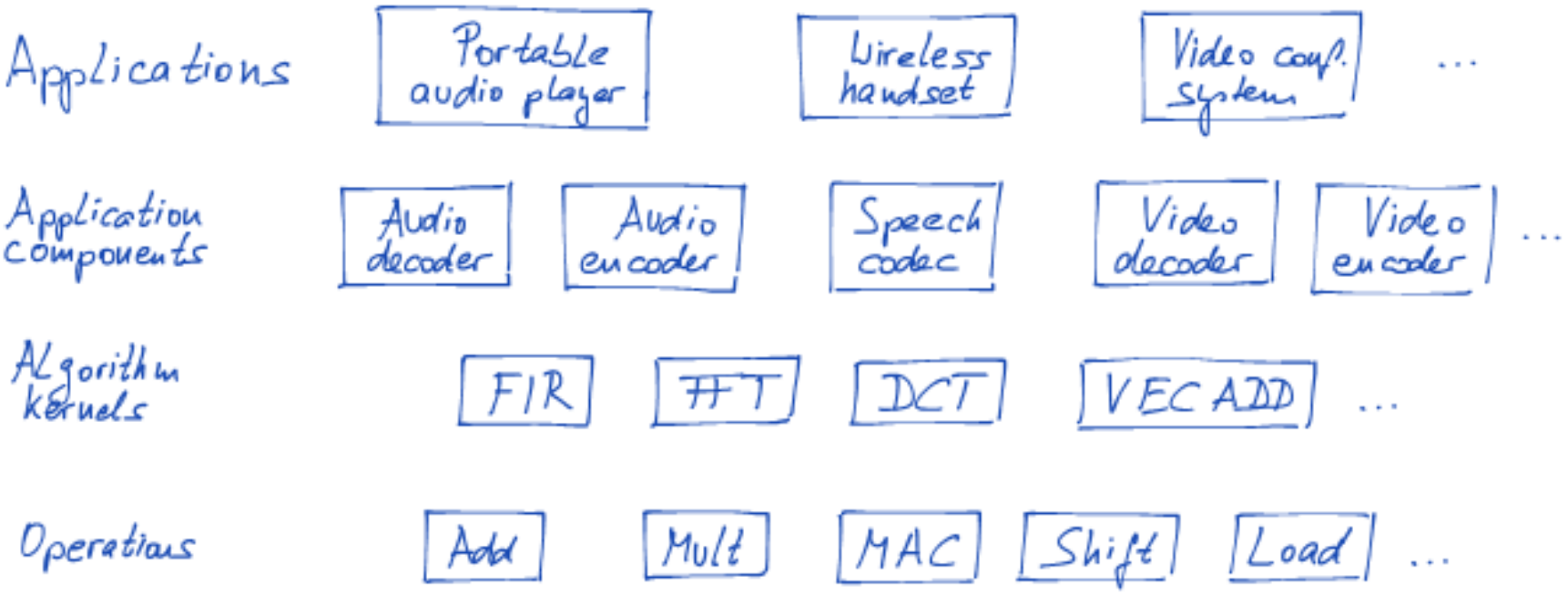
- Others
  - Size
    - Chip area, number of pins, packaging, etc.
  - Power consumption
    - Typical average values, peak consumption
  - Costs
    - Mainly sold in large units (e.g. 1000 pcs)
  - Normalized values
    - Cost / MIPS
    - Watt / MIPS
    - . . .

Are these characteristic values meaningful?

Example

- Example: C5510 and PXA255
  - 200 MHz C5510: 400 MMACS and 1,200 million bytes/sec
  - 400 MHz PXA255: 800 MMACS and 1,600 million bytes/sec
- These two processors have comparable signal processing speed!

Typical Application Decomposition



Algorithm Kernels

- The most computationally intensive portions of signal processing applications
  - e.g., FFT, FIR, IIR filters, encoder/decoder
- Application-relevant kernels are strong predictors for overall performance
- Results for common kernels are widely available
- Modest programming effort

BDTImark2000 & BDTIsimMark2000

- BDTIsimMark2000 – e.g., for licensable kernels
  - Relevance
  - Fairness and accuracy
  - Simplicity (single number)
  - Applicability
  - Independent Benchmark
- Derived metrics
  - BDTImark2000 / $
  - BDTImark2000 / mm^2
  - BDTImark2000 / mW
- BDTImemMark2000

BDTImark2000 Benchmark

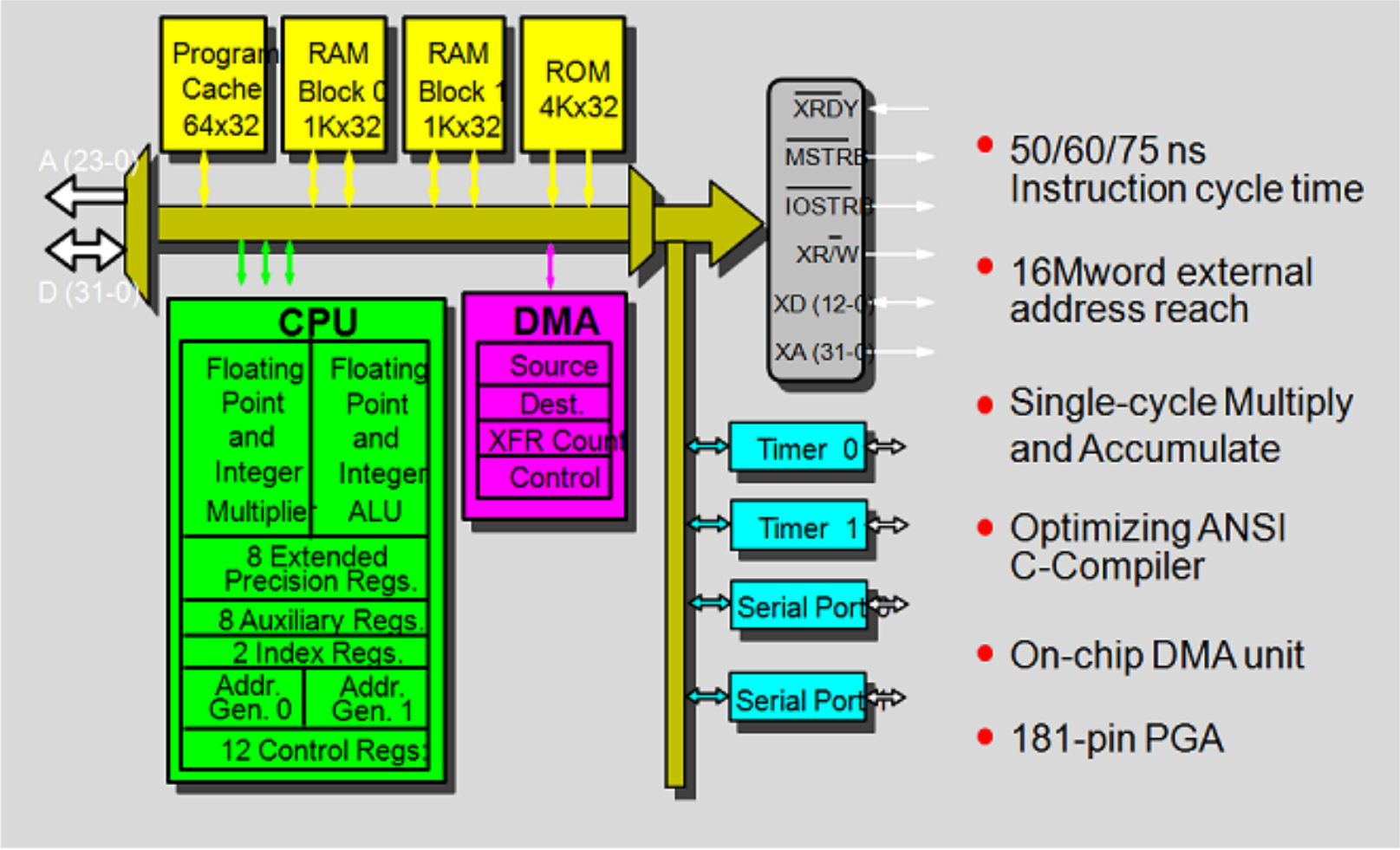
Function	Description	Example Application
Real Block FIR	Finite impulse response filter that operates on a block of real (not complex) data.	Speech processing, e.g., G.728 speech compression.
Single-Sample FIR	FIR filter that operates on a single sample of real data.	Speech processing, general filtering.
Complex Block FIR	FIR filter that operates on a block of complex data.	Modem channel equalization.
LMS Adaptive FIR	Least-mean-square adaptive filter; operates on a single sample of real data.	Channel equalization, servo control, linear predictive coding.
Two-Biquad IIR	Infinite impulse response filter that operates on a single sample of real data.	Audio processing, general filtering.
Vector Dot Product	Sum of the point-wise multiplication of two vectors.	Convolution, correlation, matrix multiplication, multi-dimensional signal processing.

BDTImark2000 Benchmark

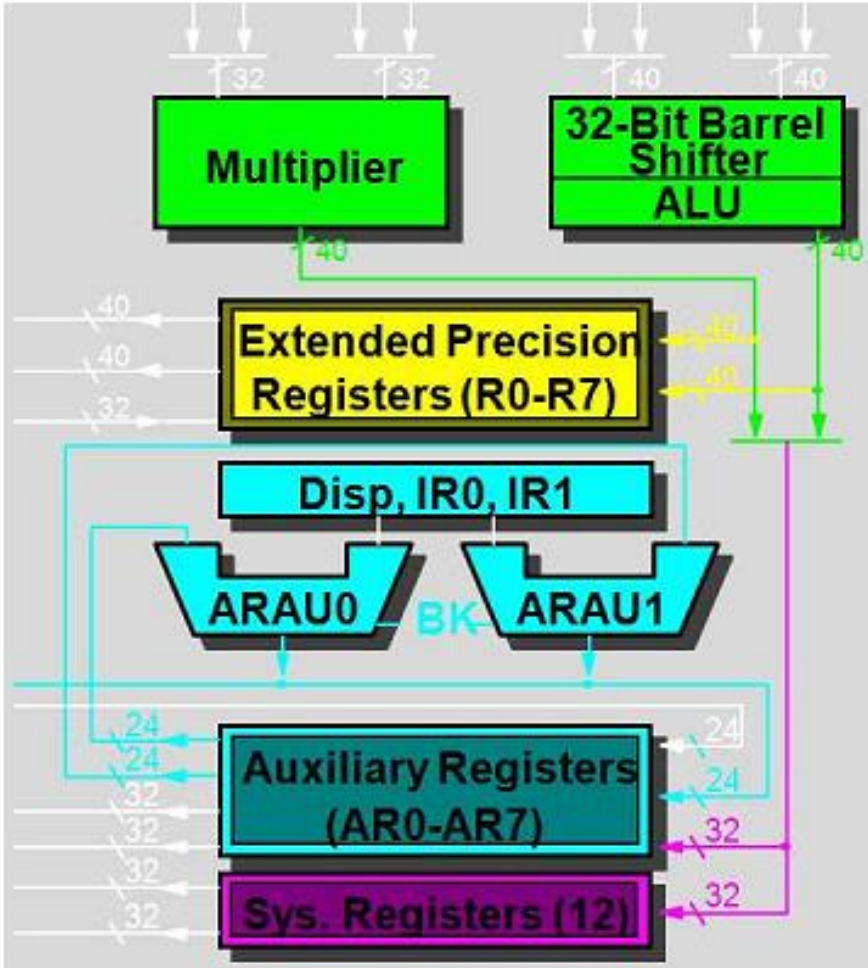
Function	Description	Example Application
Vector Add	Point-wise addition of two vectors, producing a third vector.	Graphics, combining audio signals or images, vector search.
Vector Maximum	Find the value and location of the maximum value in a vector.	Error control coding, algorithms using block floating-point.
Viterbi Decoder	Decodes a convolutionally encoded bit stream.	Wired and wireless communications, e.g., digital cellular phones.
Control	A contrived series of control (test, branch, push, pop) and bit manipulation operations.	Virtually all signal processing applications include some "control" code.
256-Point FFT	The Fast Fourier Transform converts a normal time-domain signal to the frequency domain.	Radar, sonar, MPEG audio compression, spectral analysis.
Bit Unpack	Unpacks words of varying length from a continuous bit stream.	Audio and speech decompression.

Texas Instruments DSPs

TMS320C30 Architecture

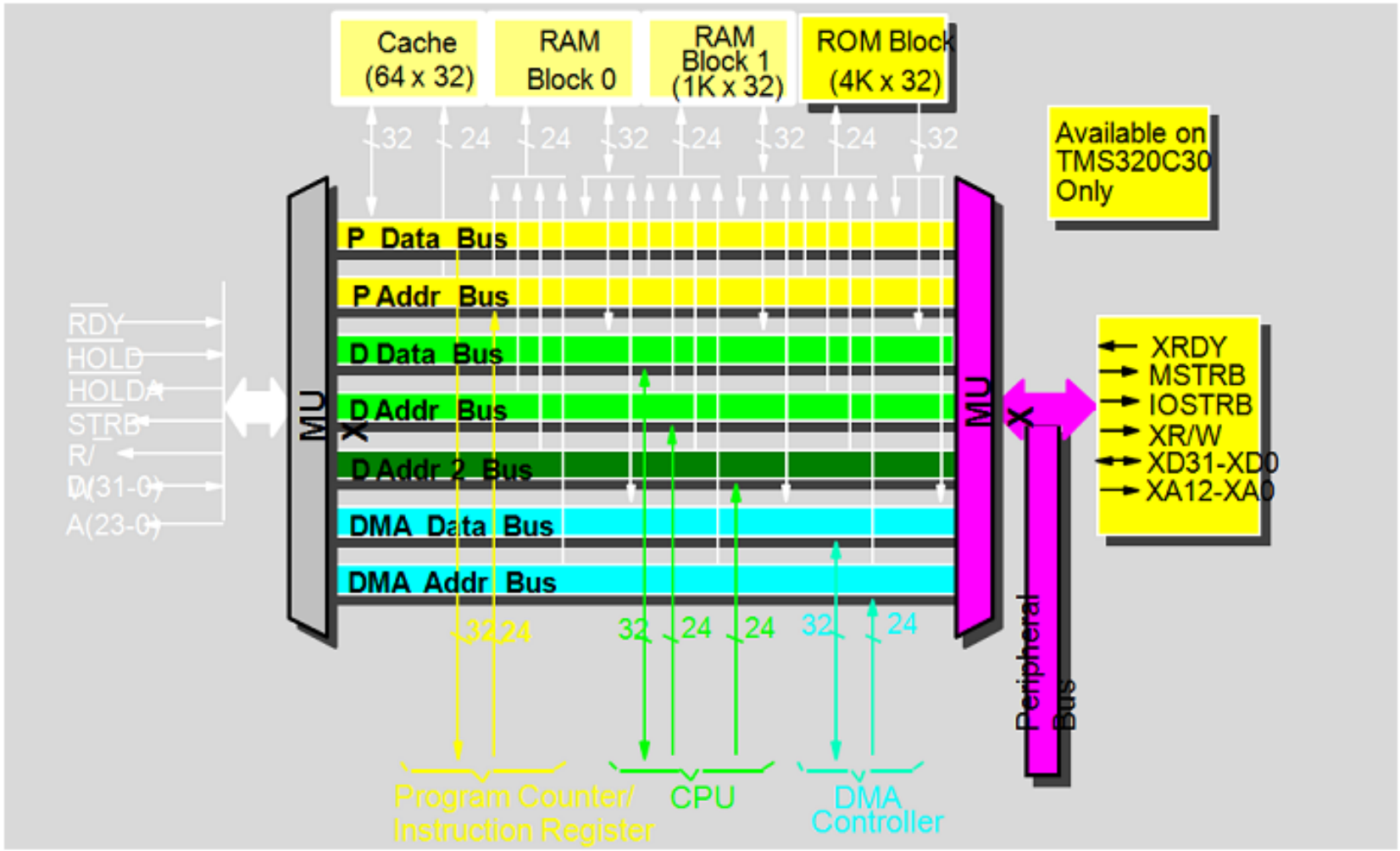


TMS320C30 CPU



- 60 Mflop CPU
- Register-based CPU
- Floating point/integer multiplier
- Floating point/integer ALU
- 32-bit Barrel Shifter
- 8 40-bit extended precision registers
- 2 address generators
- 2 index registers
- 8 indirect address registers

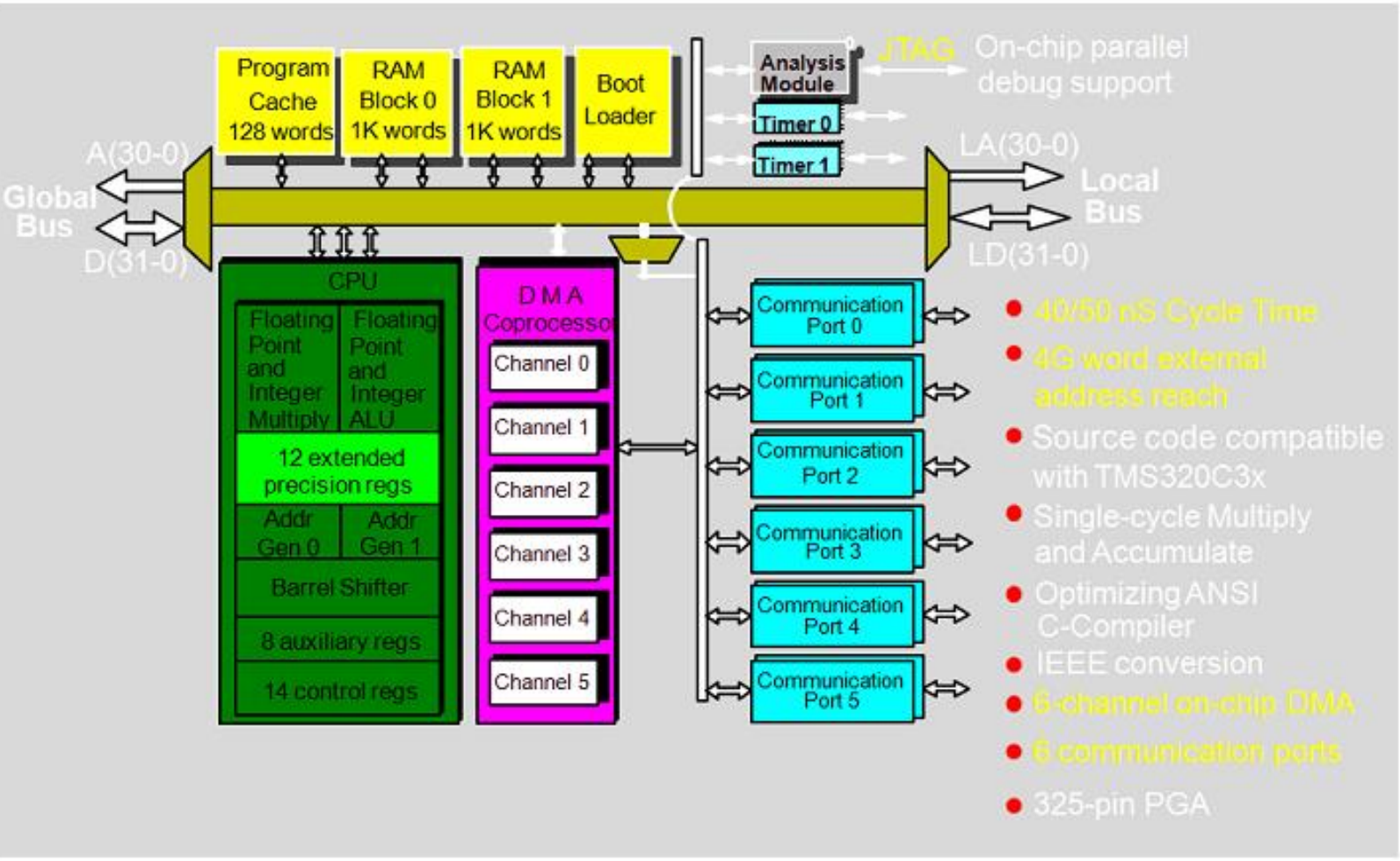
TMS320C30 Memory



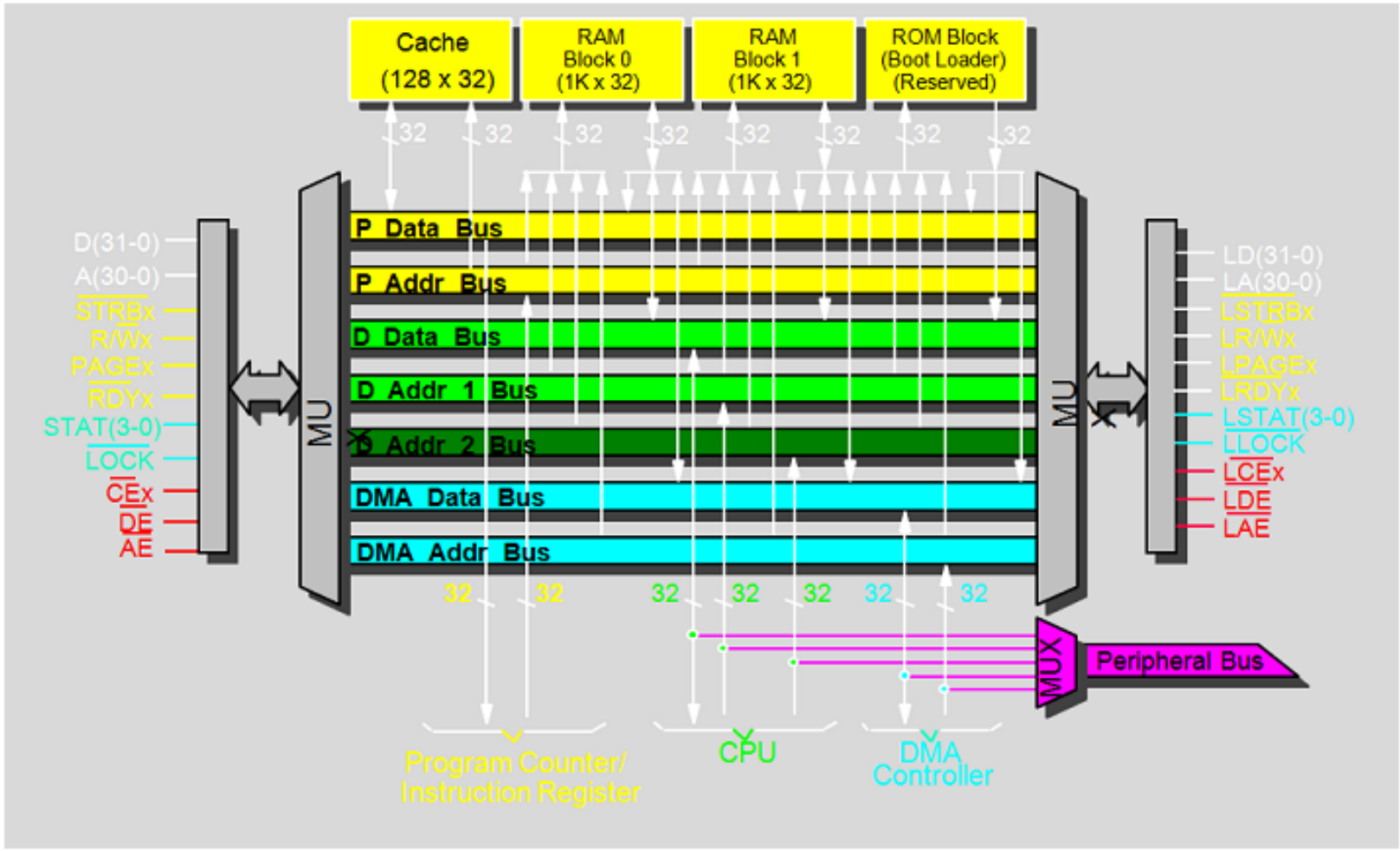
TMS320C30 Application Domains

- Neuronal nets
- DSP based graphics
  - Multiprocessor pipeline
  - Transformations
  - IBM PC host processor

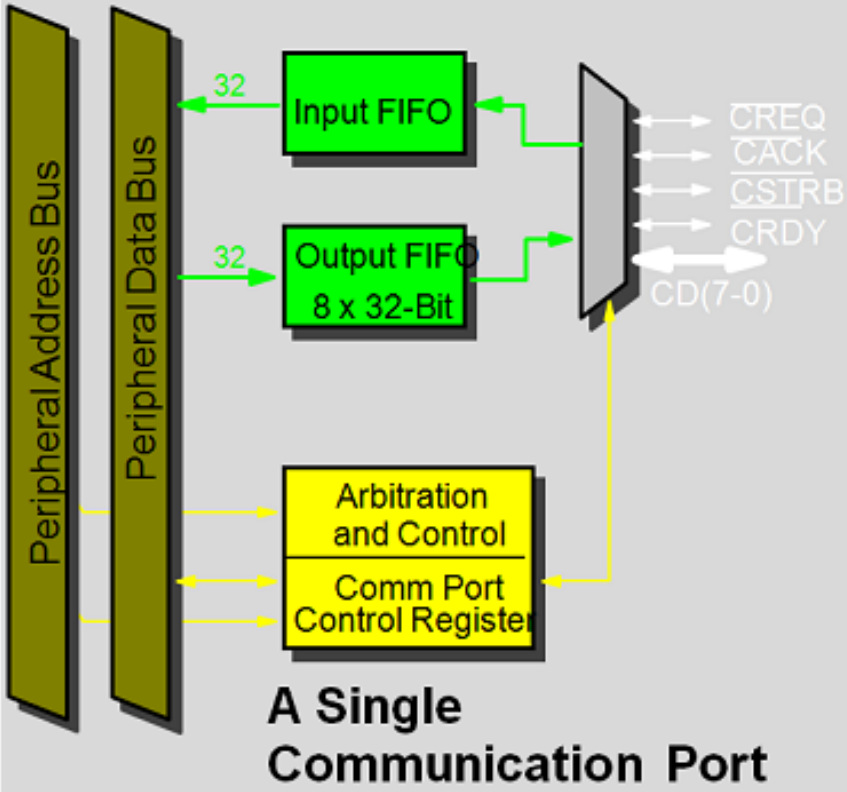
TMS320C40 Architecture



TMS320C40 Memory



TMS320C40 Communication Ports

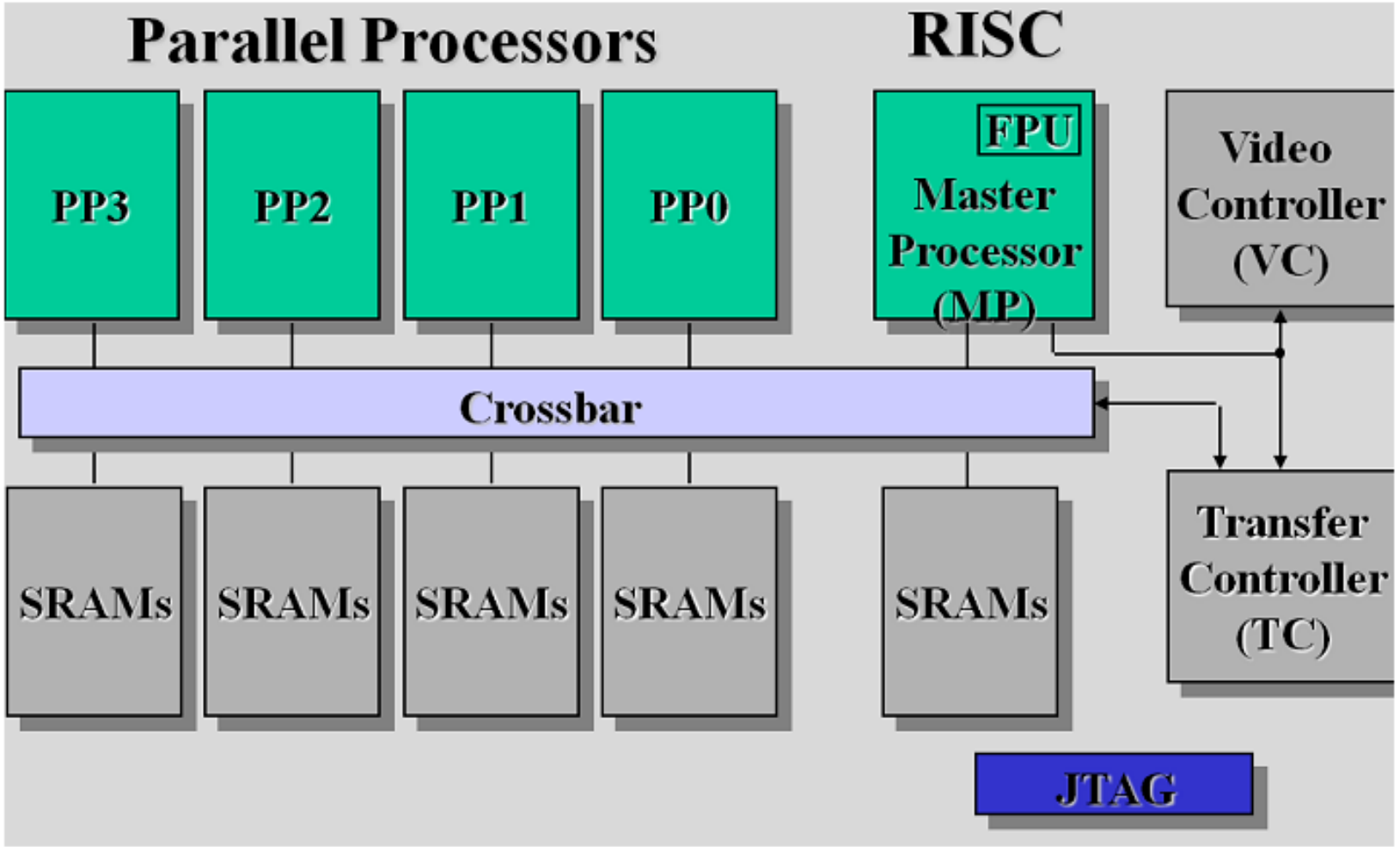


- 6 communication ports (4 on C44) for direct (glueless) asynchronous interprocessor communication and processor I/O
- 28 MBytes/sec bidirectional interface on each comm port for high speed and low cost parallel processor interface
- 8-word deep input FIFO and 8-word deep output FIFObuffer for bidirectional processor to processor communication and I/O
- Automatic arbitration and handshaking for direct processor to processor connection

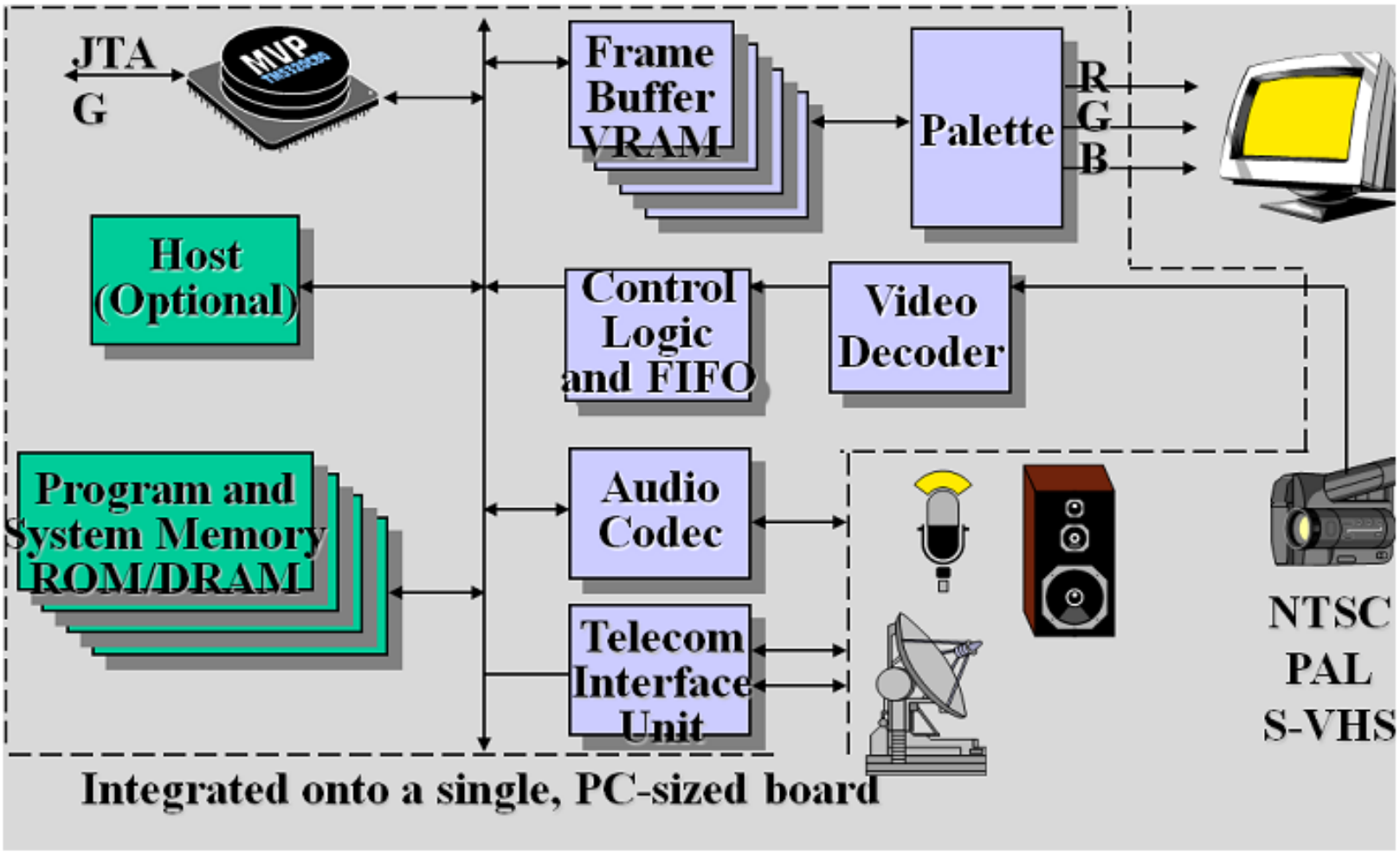
TMS320C40 Application Domains

- Real-time image processing
  - CCD camera
  - Wavelet
  - Multi-DSP
- Hardware Monitor: Multi-DSP power measurement
  - On-chip analysis unit
  - Boundary scan: JTAG
  - Kiviat-diagram

TMS320C80 Architecture



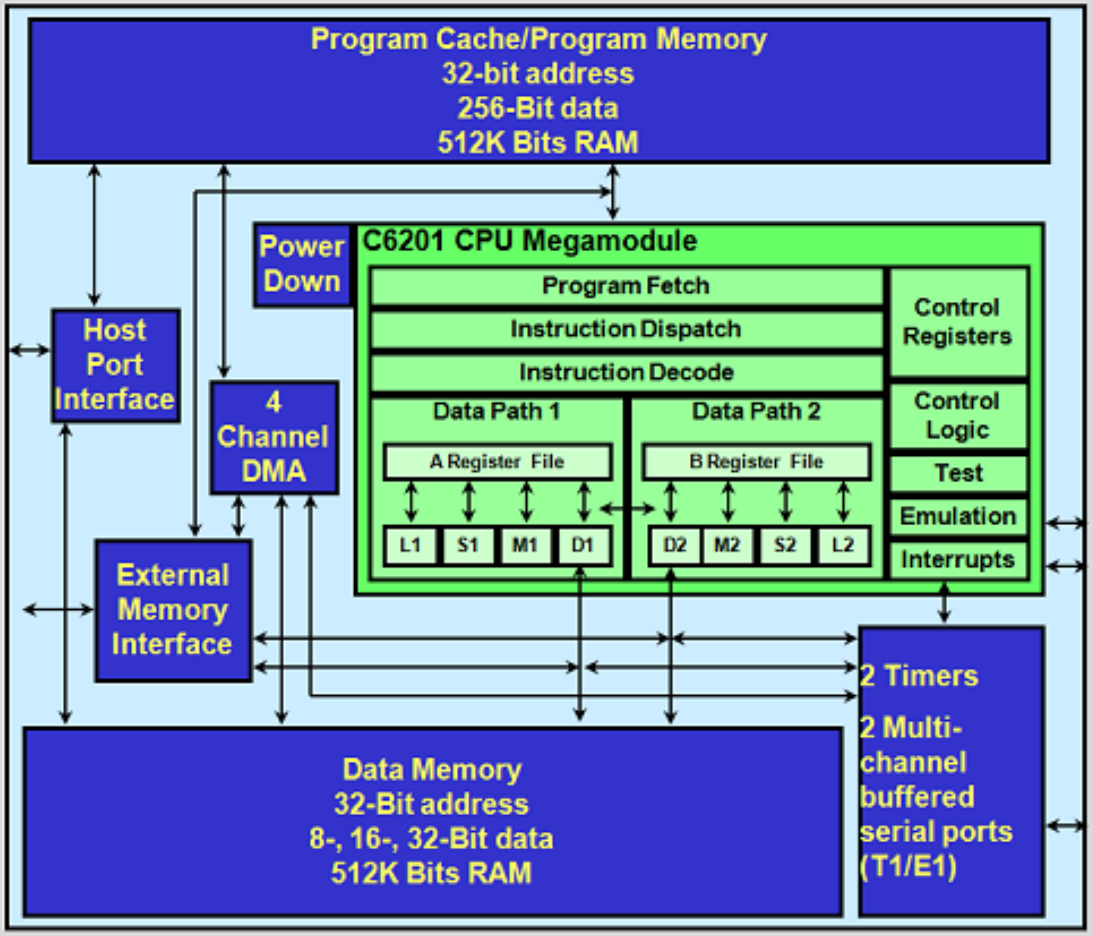
TMS320C80 Application Domains



TMS320C80 Application Domains

- Acoustic echo cancellation
  - Adaptive FIR filter
  - LMS algorithm
  - Speech recognition
- Frame buffer
  - Video controller
  - VRAM
  - Serial register transfer

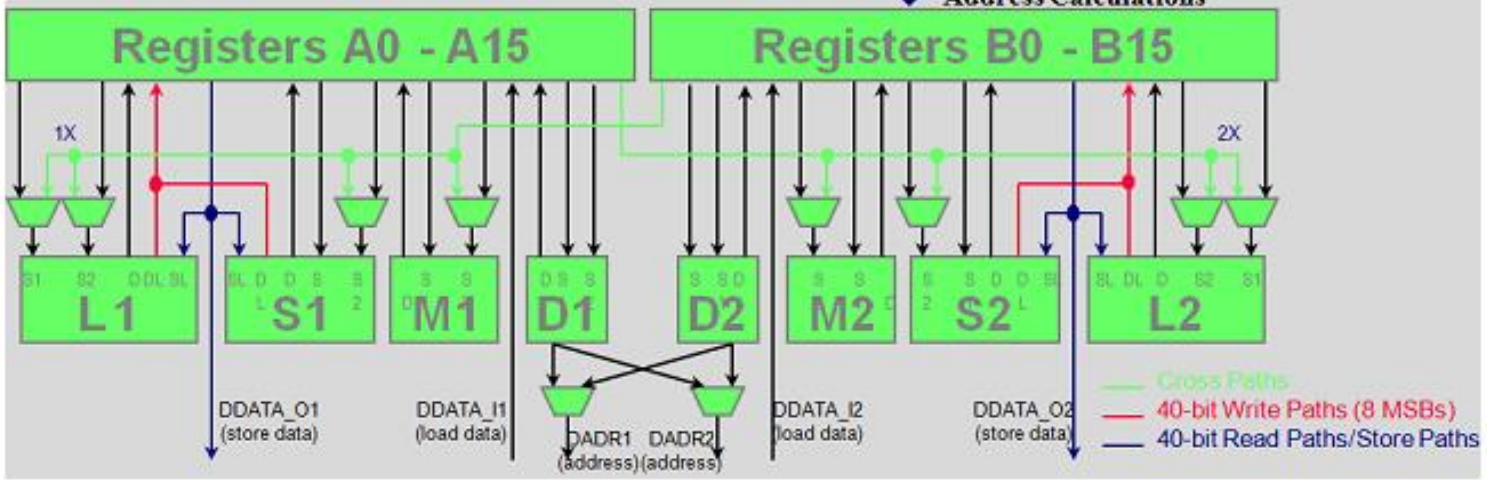
TMS320C6x Architecture



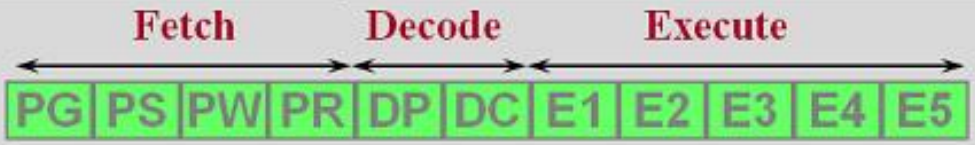
TMS320C6x Datapath

- 2 Data Paths
- 8 Functional Units
  - Orthogonal/Independent
  - 6 Arithmetic Units
  - 2 Multipliers
- Control
  - Independent
  - Up to 8 32-bit Instructions in parallel
- Registers
  - 2 Files
  - 32, 32-bit Registers Total
- Cross paths (1X, 2X)

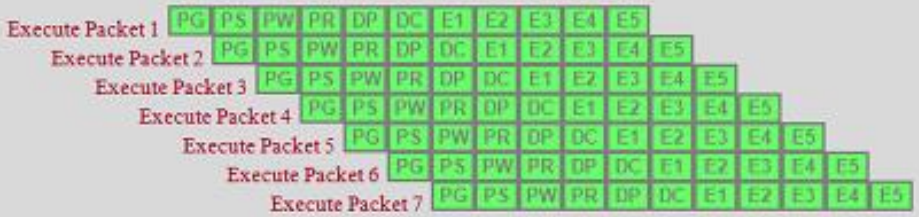
- L-Unit (L1, L2)
  - 40-bit Integer ALU
  - Comparisons
  - Bit Counting
  - Normalization
- S-Unit (S1, S2)
  - 32-bit ALU
  - 40-bit Shifter
  - Bitfield Operations
  - Branching
- M-Unit (M1, M2)
  - 16 x 16 -> 32
- D-Unit (D1, D2)
  - 32-bit Add/Subtract
  - Address Calculations



TMS320C6x Pipeline

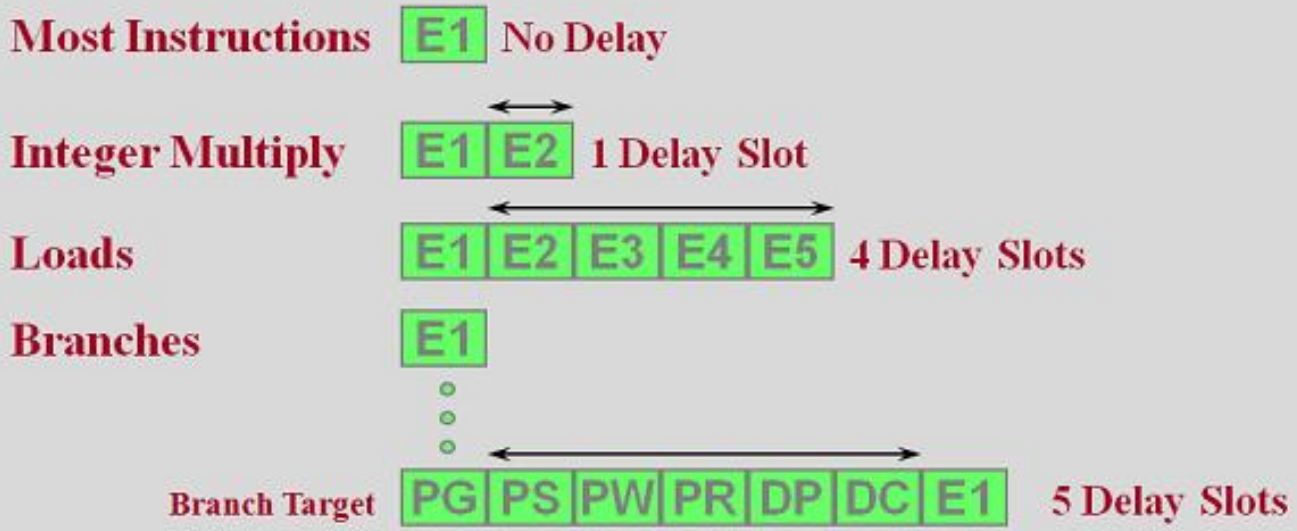


- Single-Cycle Throughput
- Operate in Lock Step
- Fetch
  - PG Program Address Generate
  - PS Program Address Send
  - PW Program Access Ready Wait
  - PR Program Fetch Packet Receive
- Decode
  - DP Instruction Dispatch
  - DC Instruction Decode
- Execute
  - E1 - E5 Execute 1 through Execute 5



TMS320C6x Pipeline

- Delay Slots: number of extra cycles until result is:
  - written to register file
  - available for use by a subsequent instructions
  - Multi-cycle NOP instruction can fill delay slots while minimizing codesize impact

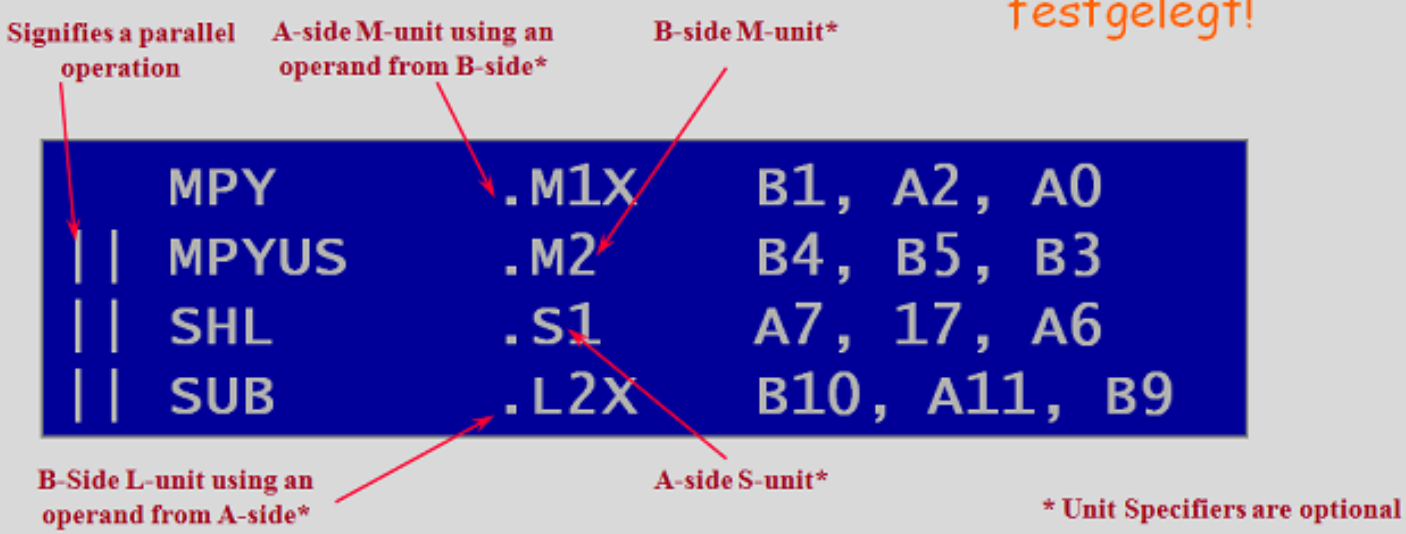


TMS320C6x VLIW

```
short B1, A2, B4, B5;
int A7, A6, B10, A11, B9;
A0 = B1 * A2;
B3 = (unsigned) B4 * (signed) B5;
A6 = A7 << 17;
B9 = B10 - A11;
```

8 Befehle parallel

zur Compile-Zeit festgelegt!



TMS320C6x Application Domains

- C621x/C671x EDMA performance
  - Latency
  - Throughput
  - Caching
- C64x Video Bg/Fg Detection
  - Intelligent video content analysis
  - Background/foreground segmentation
  - Performance

EDMA Latency

CPU Frequency (MHz)	EMIF Frequency (MHz)	Source Peripheral	Expected Transfer Latency		Actual Transfer Latency	
			nS	CPU cycles†	nS	CPU cycles†
225	100	EMIF (SBSRAM)	118.9	26.8	117	26.3
225	66	EMIF (SBSRAM)	134.3	30.2	124	27.9
225	100	EMIF (SDRAM)	138.9	31.3	134	30.2
225	66	EMIF (SDRAM)	164.6	37.0	160	36.0
150	100	EMIF (SBSRAM)	163.3	24.5	158	23.7
150	66	EMIF (SBSRAM)	178.8	26.8	164	24.6
150	100	EMIF (SDRAM)	183.3	27.5	181	27.2
150	66	EMIF (SDRAM)	209.1	31.4	205	30.8
Don't care	Don't care	L2 Memory	–	21	–	21
Don't care	Don't care	McBSP	–	25	–	25

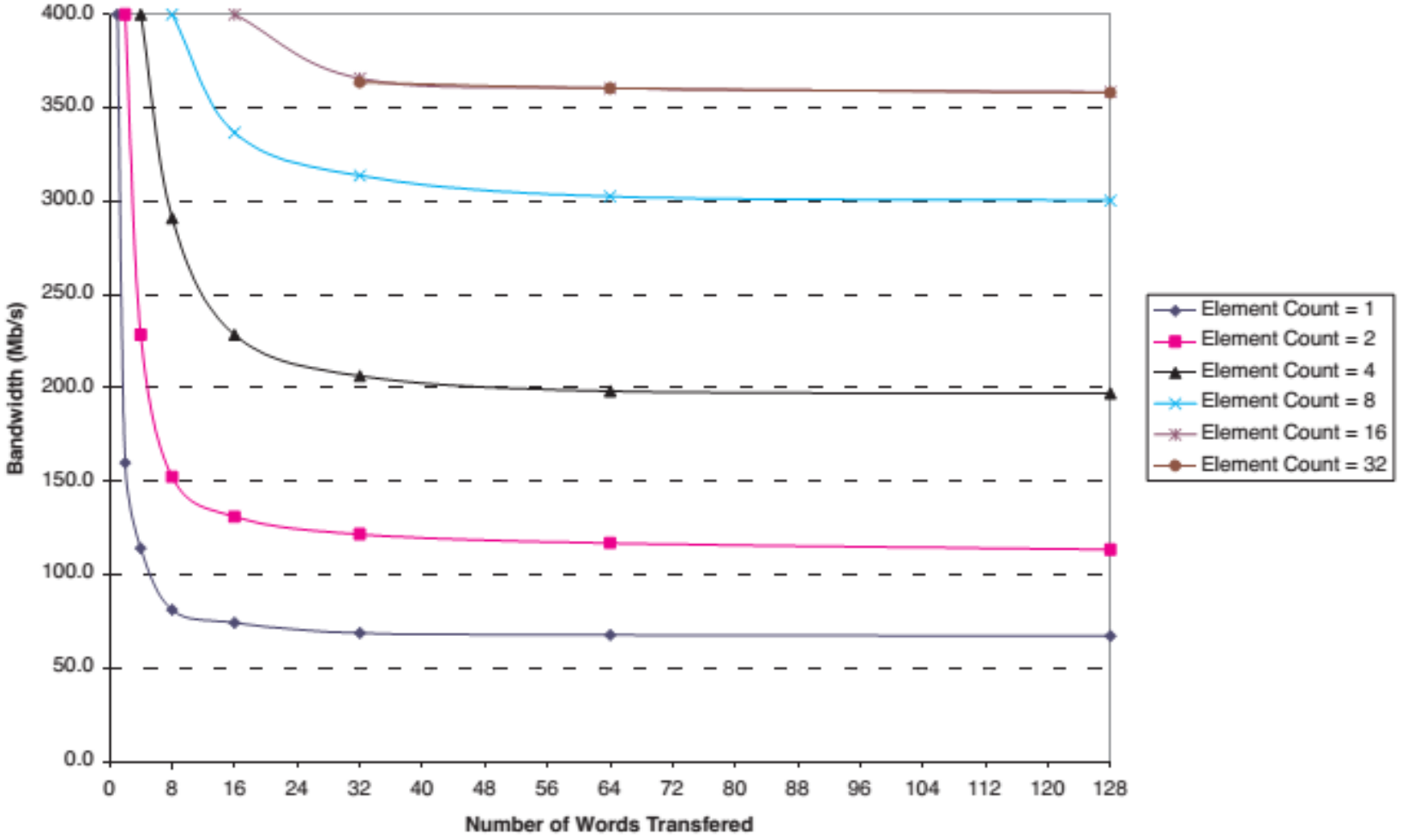
† Note that CPU cycle period is defined by the CPU frequency shown.

EDMA Throughput Efficiency

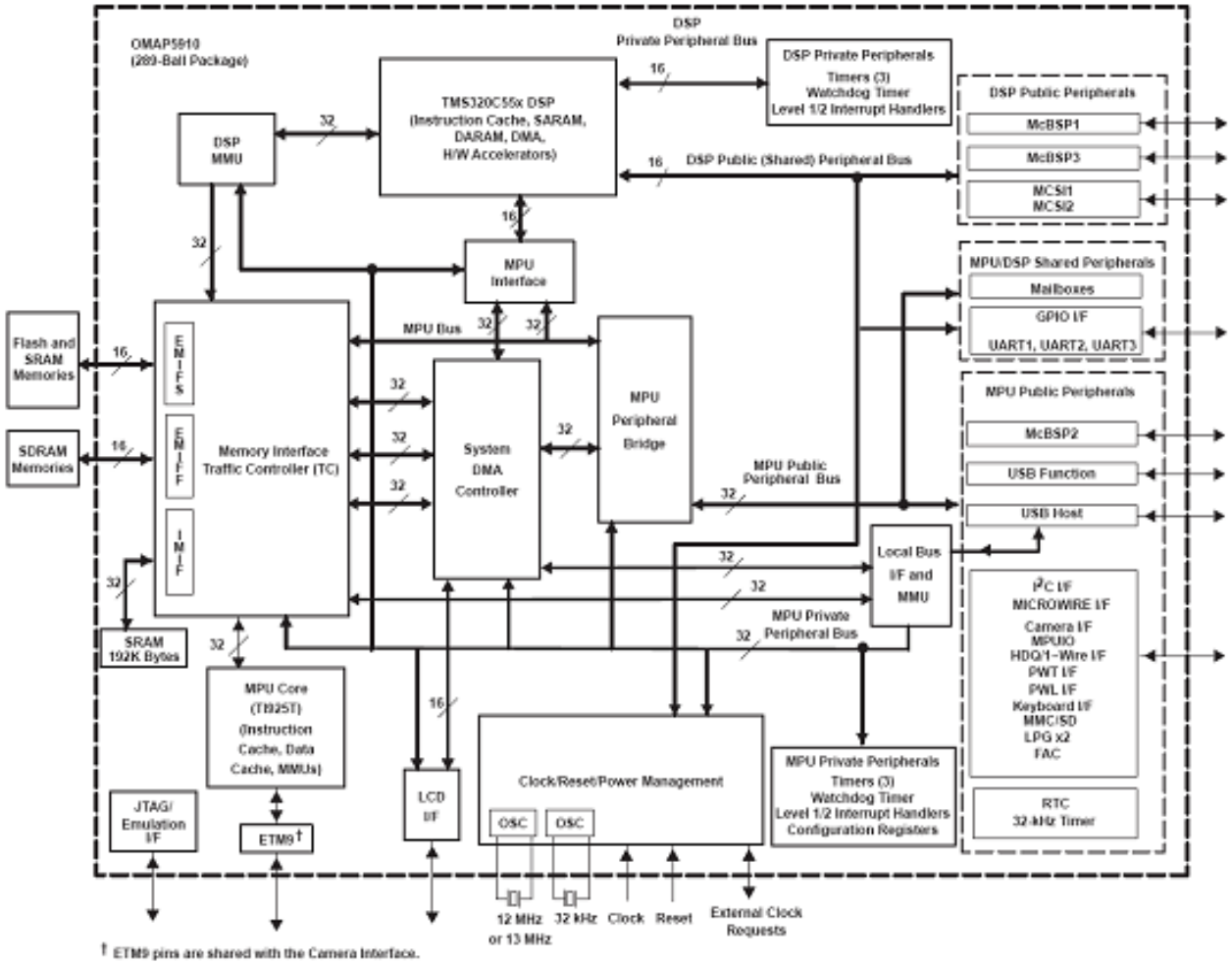
Element Size	Total Data (bytes)	Read Access		Write Access	
		Transfer Bandwidth (Mb/sec)	SBSRAM Bandwidth Utilization	Transfer Bandwidth (Mb/sec)	SBSRAM Bandwidth Utilization
32-bit	4†	400	100%	400.0	100.0%
32-bit	16	320	80%	307.7	76.9%
32-bit	128	376.5	94.1%	390.2	97.6%
16-bit	4	200	50.0%	50.0	12.5%
16-bit	16	64	16.0%	42.1	10.5%
16-bit	128	58	14.5%	40.3	10.1%
8-bit	4	40	10%	30.3	7.6%
8-bit	16	30.8	7.7%	22.0	5.5%
8-bit	128	28.8	7.2%	20.2	5.1%

† Note that a 4-byte (32 bit) transfer to a 64-bit SBSRAM cannot fully utilize bandwidth.

EDMA Bandwidth vs. Element Count



OMAP Architecture



OMAP 5910

- Dual-Core Processor
  - ARM9 + TMS320C55x
  - RISC Peripherals: USB, McBSP, Camera Interface, PWL, PWT, . . .
  - DSP Peripherals: MCSI, McBSP
  - Shared UART, GPIO, Mailbox-Register
- Multimedia Applications
  - Embedded system
  - Audio-, video-, image processing
  - Mobile communication

Alternative Platforms

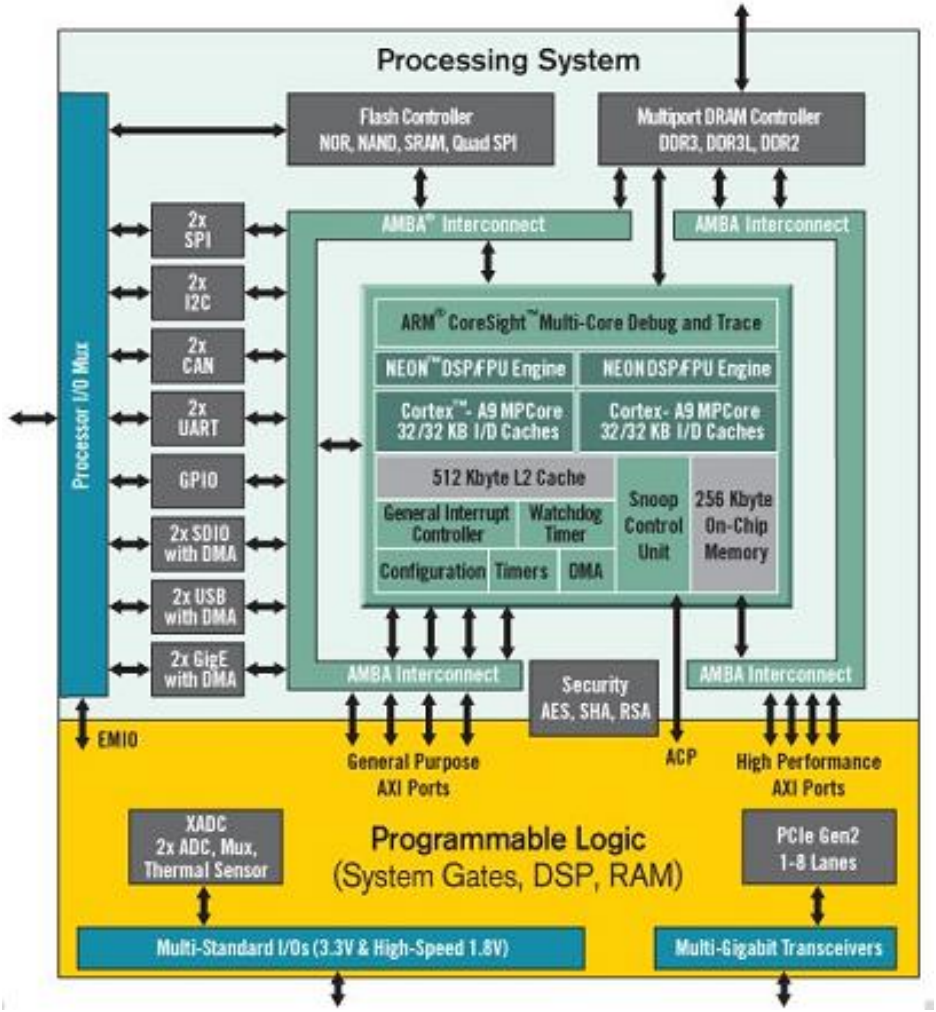
FPGA for DSPs

- Field Programmable Gate Array (FPGA)
  - Alternative to custom ICs, can be used to implement entire system on chip (SoC)
  - Main advantage: ability *to re-program the chip*
  - FPGA contains two-dimensional arrays of logic blocks and interconnections between the logic blocks
- FPGA has become a competitive alternative for high-performance DSPs (DSP co-processor or stand-alone DSP engine)
- Advantages of using FPGA in DSP application
  - System performance (hardware tailored to the actual needs)
  - Reduced component count
  - Design flexibility and adaptability

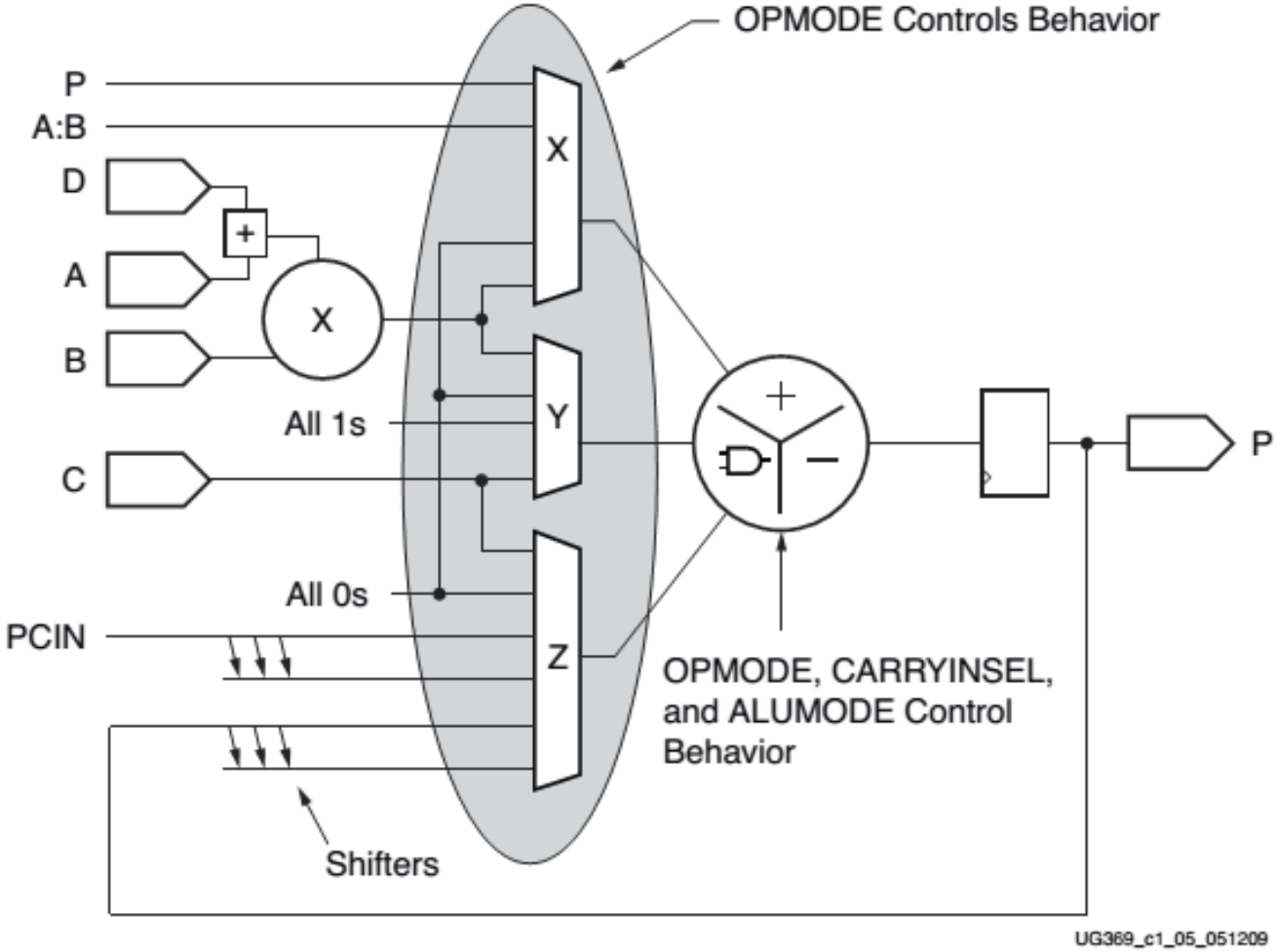
DSP Cores on FPGA

- Hard Cores
  - Dedicated part of the integrated circuit
- Soft Cores
  - DSP core as intellectual property (IP)
- Advantages
  - Increased design re-use
  - Integration of additional IP components into SoC
    - Ethernet MAC
    - UART
    - . . .

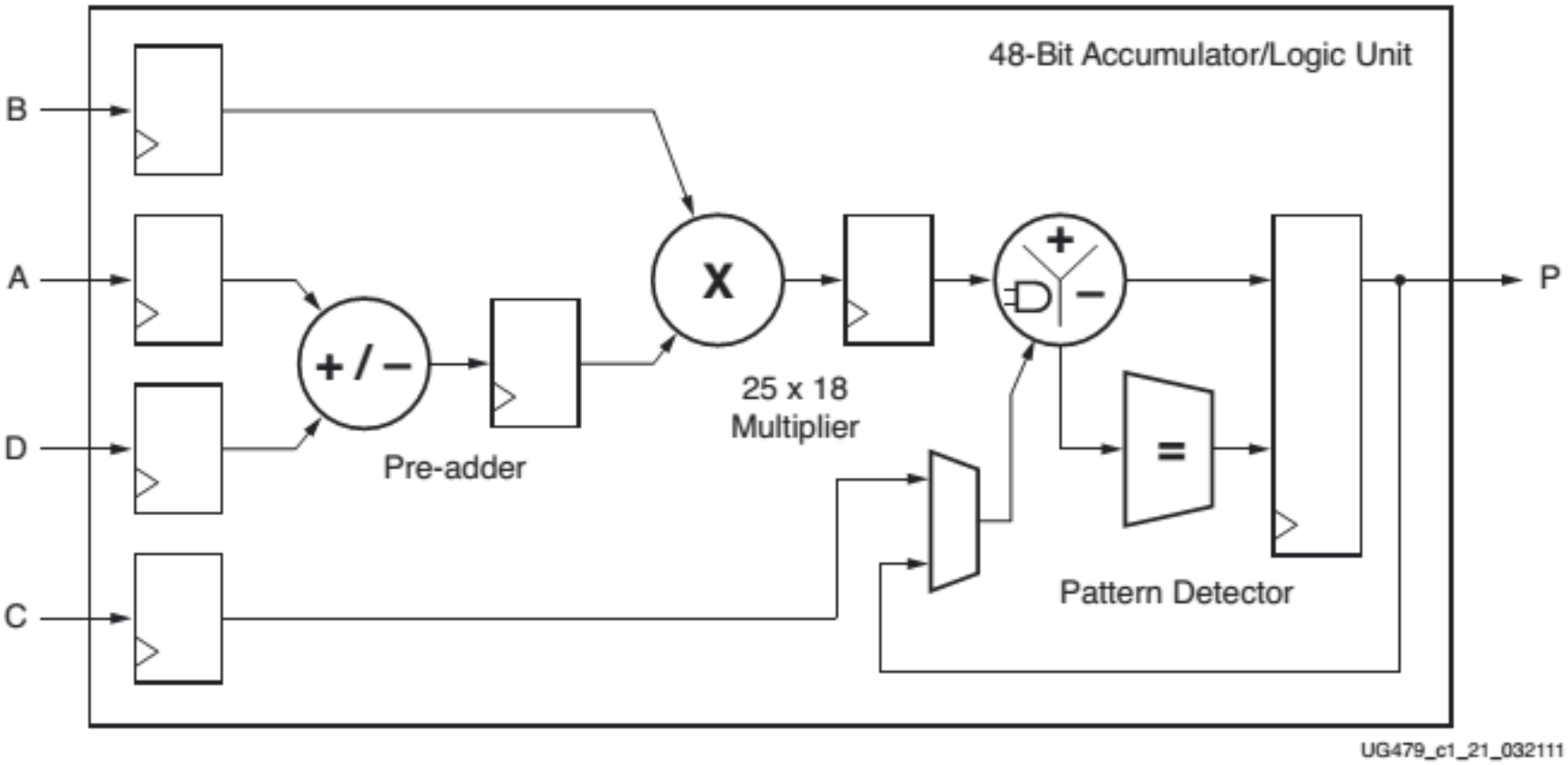
Example: Xilinx Zynq



Xilinx Zynq DSP Slice



Xilinx Zynq DSP Slice



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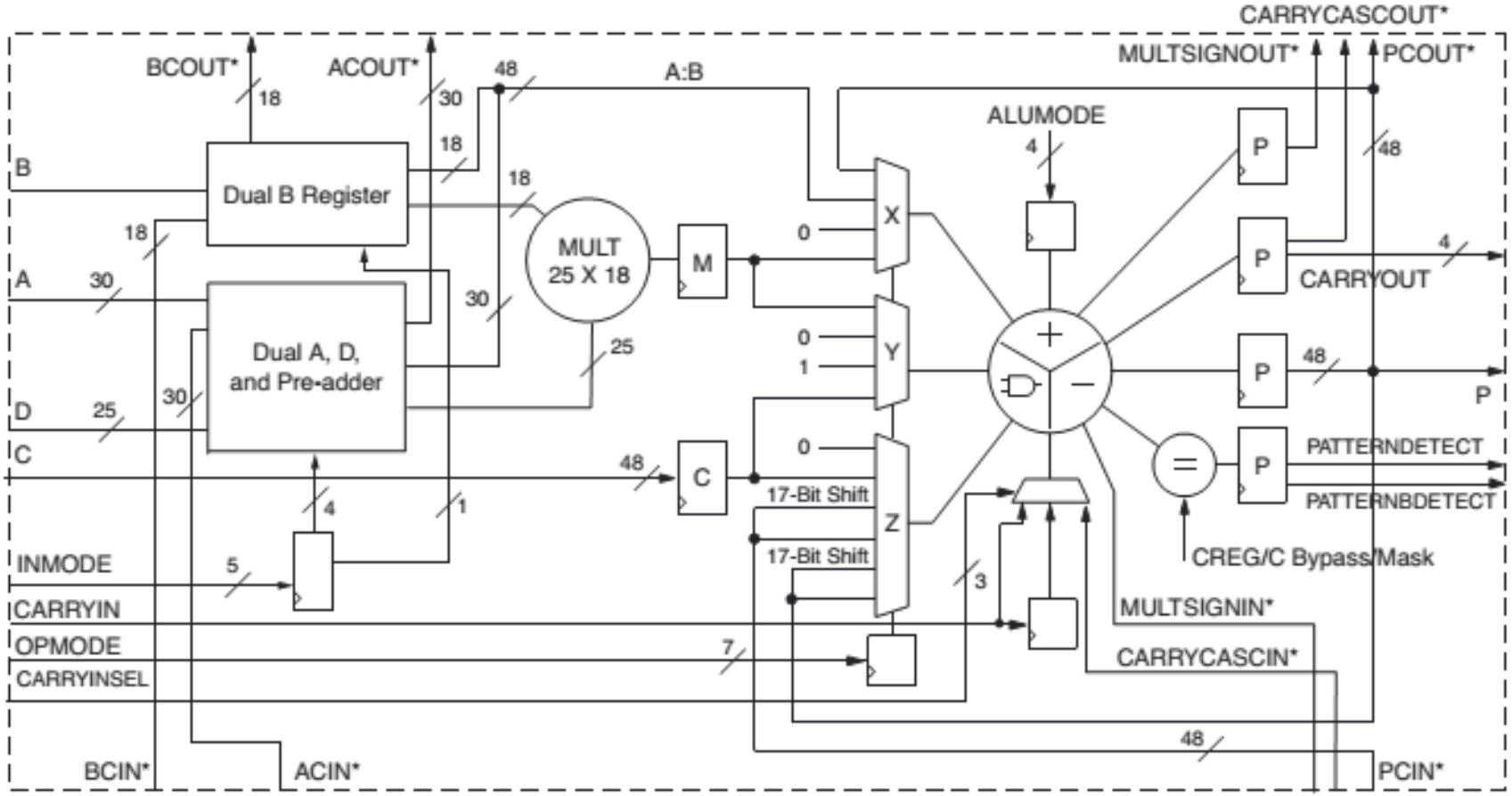

*These signals are dedicated routing paths internal to the DSP48E1 column. They are not accessible via fabric routing resources.

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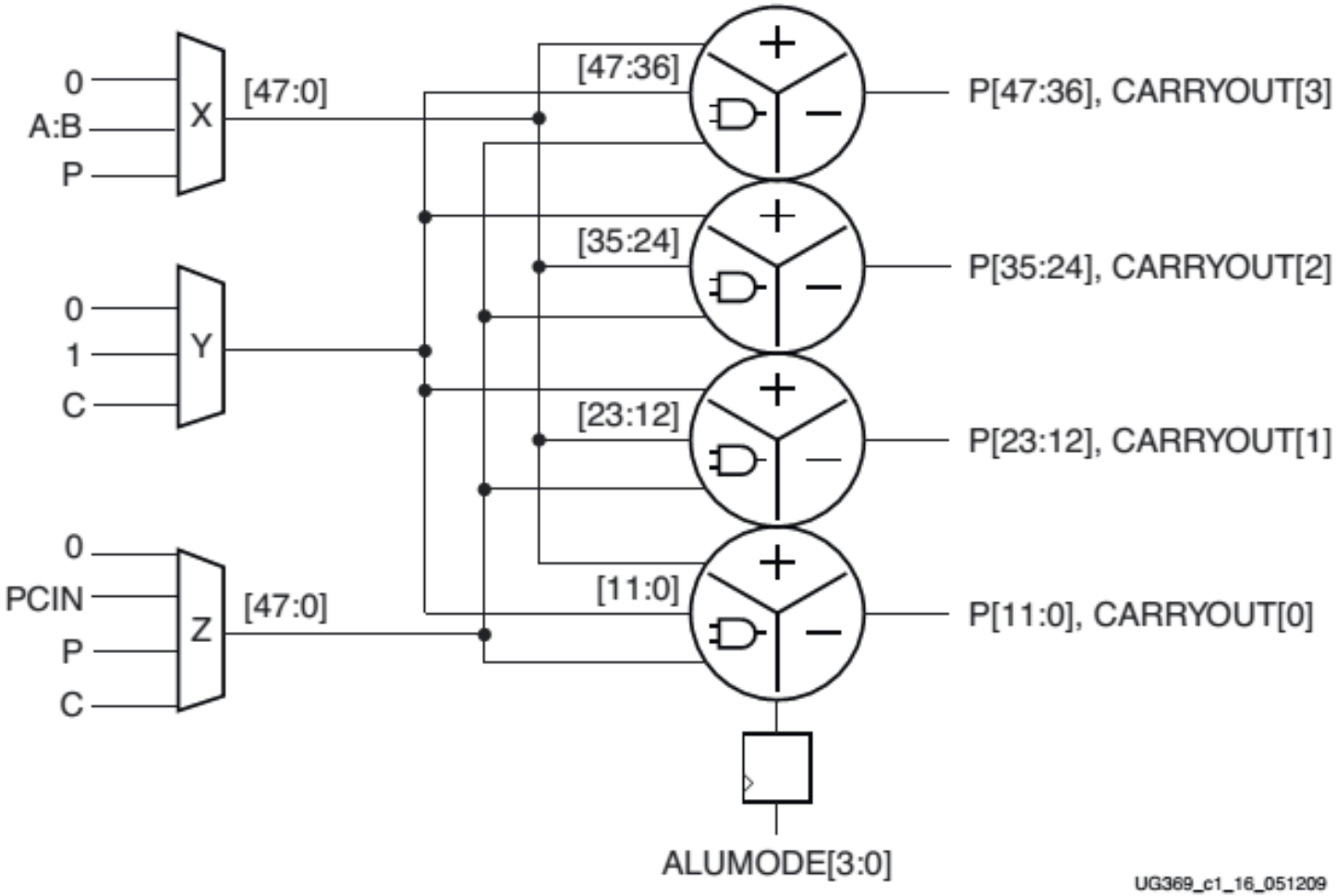
Xilinx Zynq DSP Slice



GPU for DSP

- Modern GPUs: multiple single-instruction multiple-data (SIMD) cores on a single chip
- Specialized in processing-intensive data-parallel computations (no specific flow-control required)
- Available for mobile devices (ES) to high-end graphics cards
  - E.g. Nvidia ION platform

Comparison

Freescale DSP5685x

- 16-bit fixed-point DSP 120 MHz
  - 16 x 16-bit multiplier
  - 2-stage pipeline
  - Harvard architecture
  - 4 36-bit register, 7 16-bit register
- “teledatacom” Applications
  - “low-end” mobile phones, PDA, Internet radio, . . .

Benchmarking DSP5685x vs. C6202

BDTIMark2000 @ DSP5685x

120 MHz * 1 Instruktion: 120 MIPS

```
MOVEU.W  X:DLYPTR,R0 ; load data address into r0 pointer
MOVEU.W  #COEFADDR,R3; load coefficient address into r3 pointer
REP      #NTAP       ; repeat the next instruction Ntap times
MAC      X0,Y1,B    X:(R0)+,Y1    X:(R3)+,X0
                     ; multiply and accumulate a sample and coef
```

BDTIMark2000 @ C6202

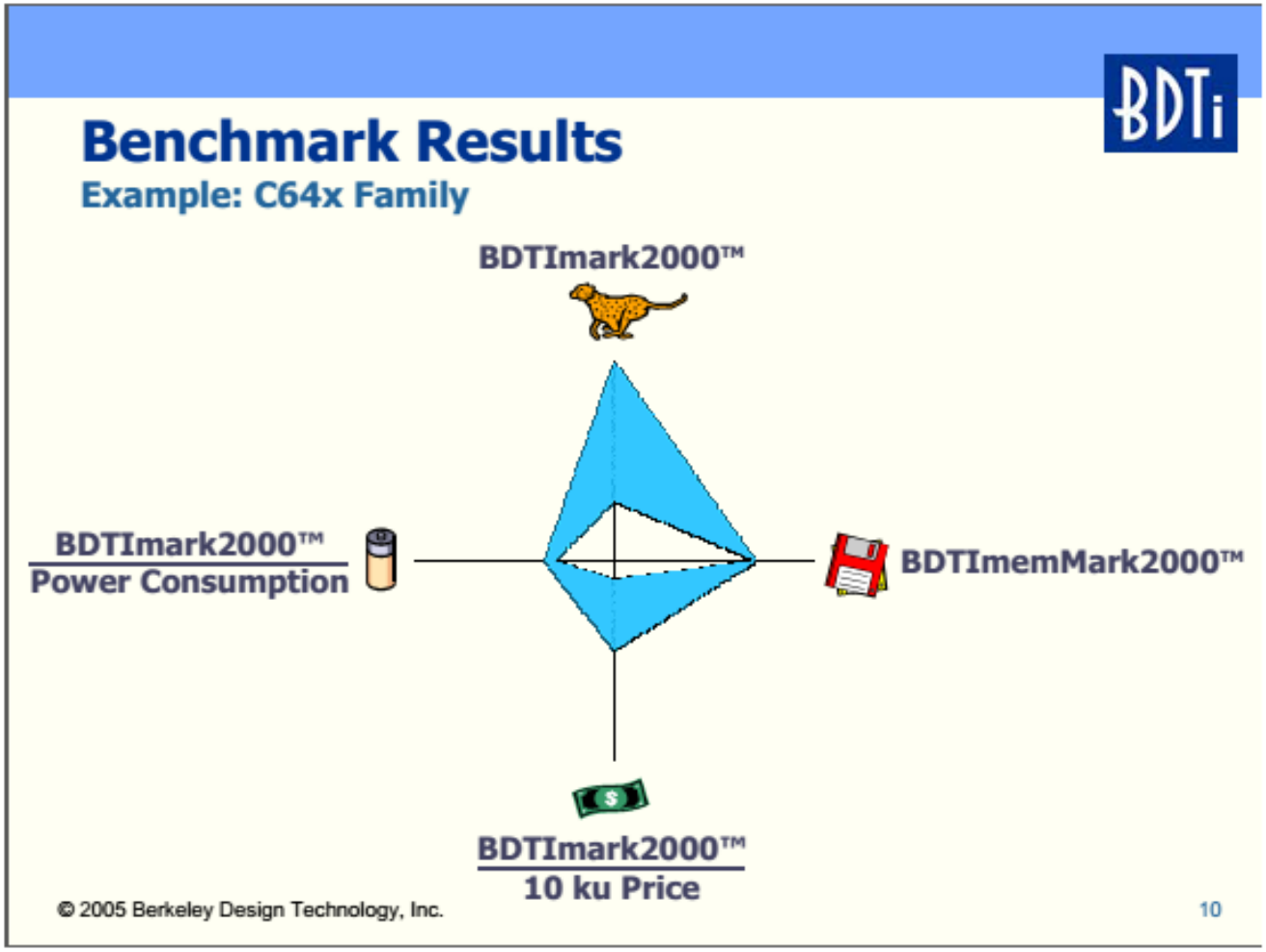
300 MHz * 8 Instruktionen: 2400 MIPS

```
loop:
         ADD.L1      A0,A3,A0   ; A0=A0+A3
||       ADD.L2      B1,B7,B1   ; B1=B1+B7
||       MPYHL.M1X   A2,B2,A3   ; A3=A2(hi)*B2(lo)
||       MPYLH.M2X   A2,B2,B7   ; B7=A2(lo)*B2(hi)
||       LDW.D2      *B4++,B2   ; load into B2
||       LDW.D1      *A7--,A2   ; load into A2
||       ADD.S2      -1,B0,B0   ; decrement counter
||       [B0]        B.S1 loop  ; branch if B0 nonzero
```

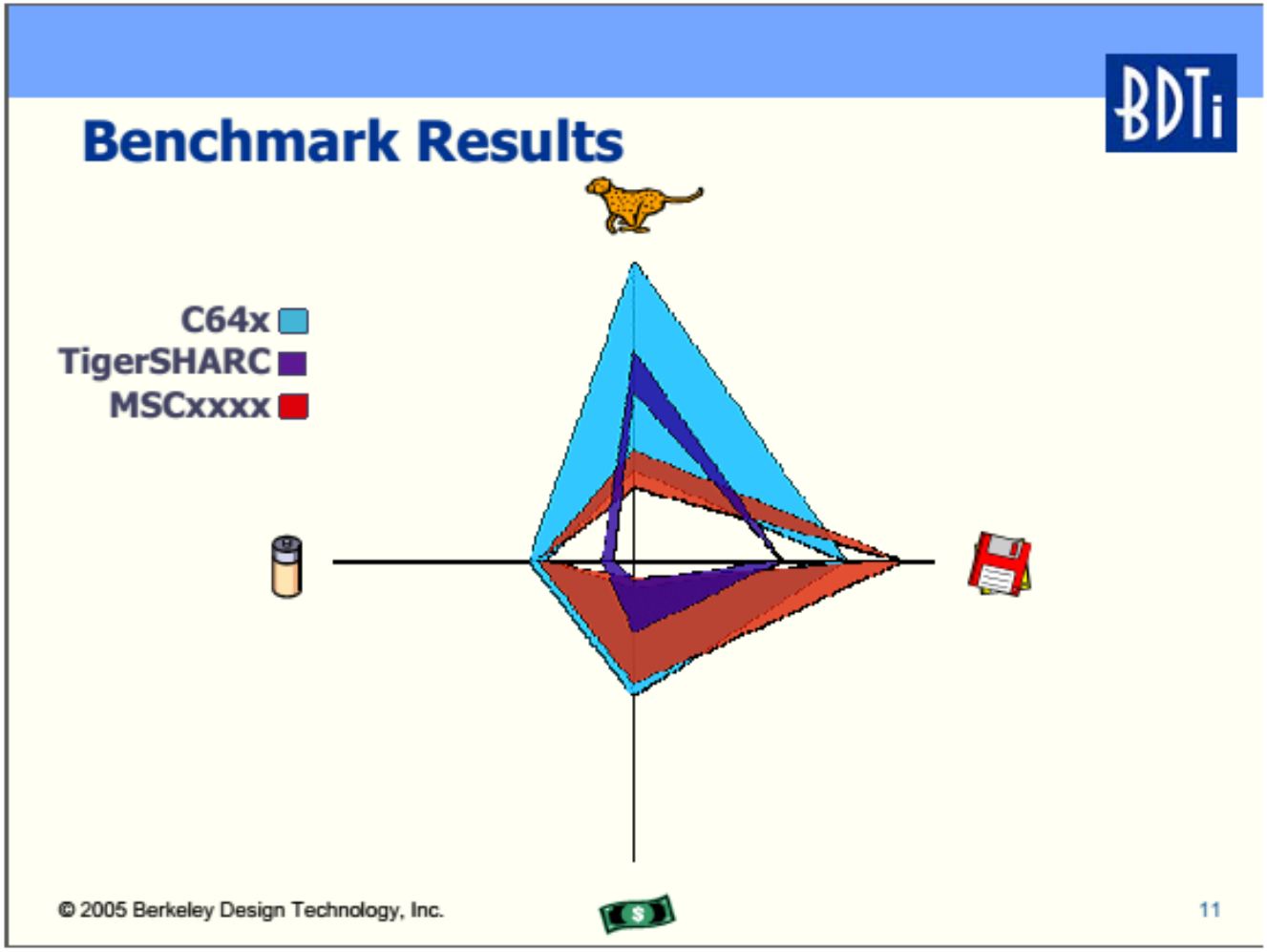
StarCore SC140

- 16-bit fixed-point VLIW DSP core
  - 4 16-bit data-paths
  - up to 6 instructions in parallel
  - 16 x 16-bit multiplier in each data-path
  - 2 data buses (32 bit addr, 64 bit data)
  - Instructions: 32 bit addr, 128 bit data
- Application domain(s): telecommunication
  - IP-Phones, wireless comm., modem, low-power applications, . . .

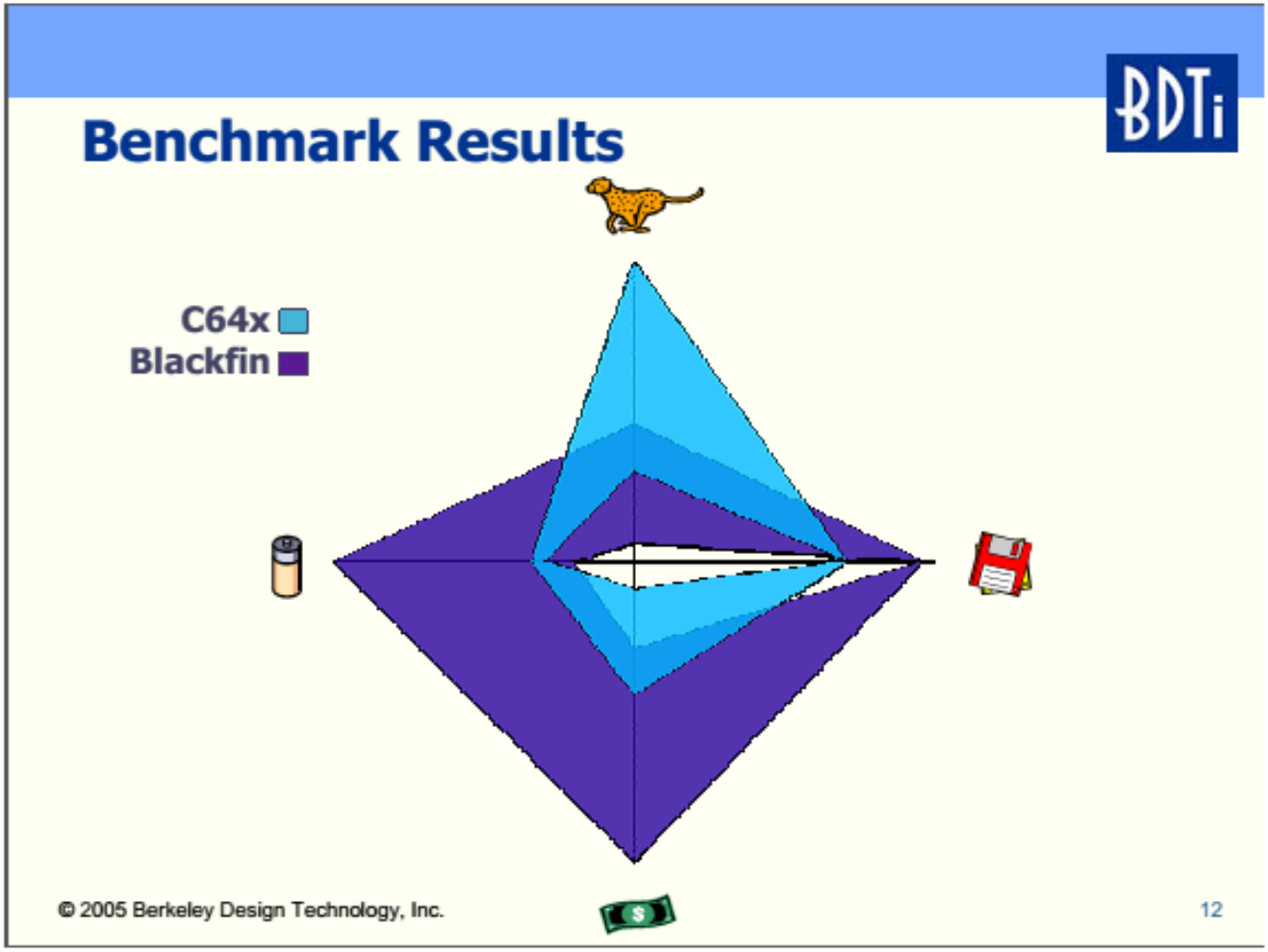
BDTI Benchmarks



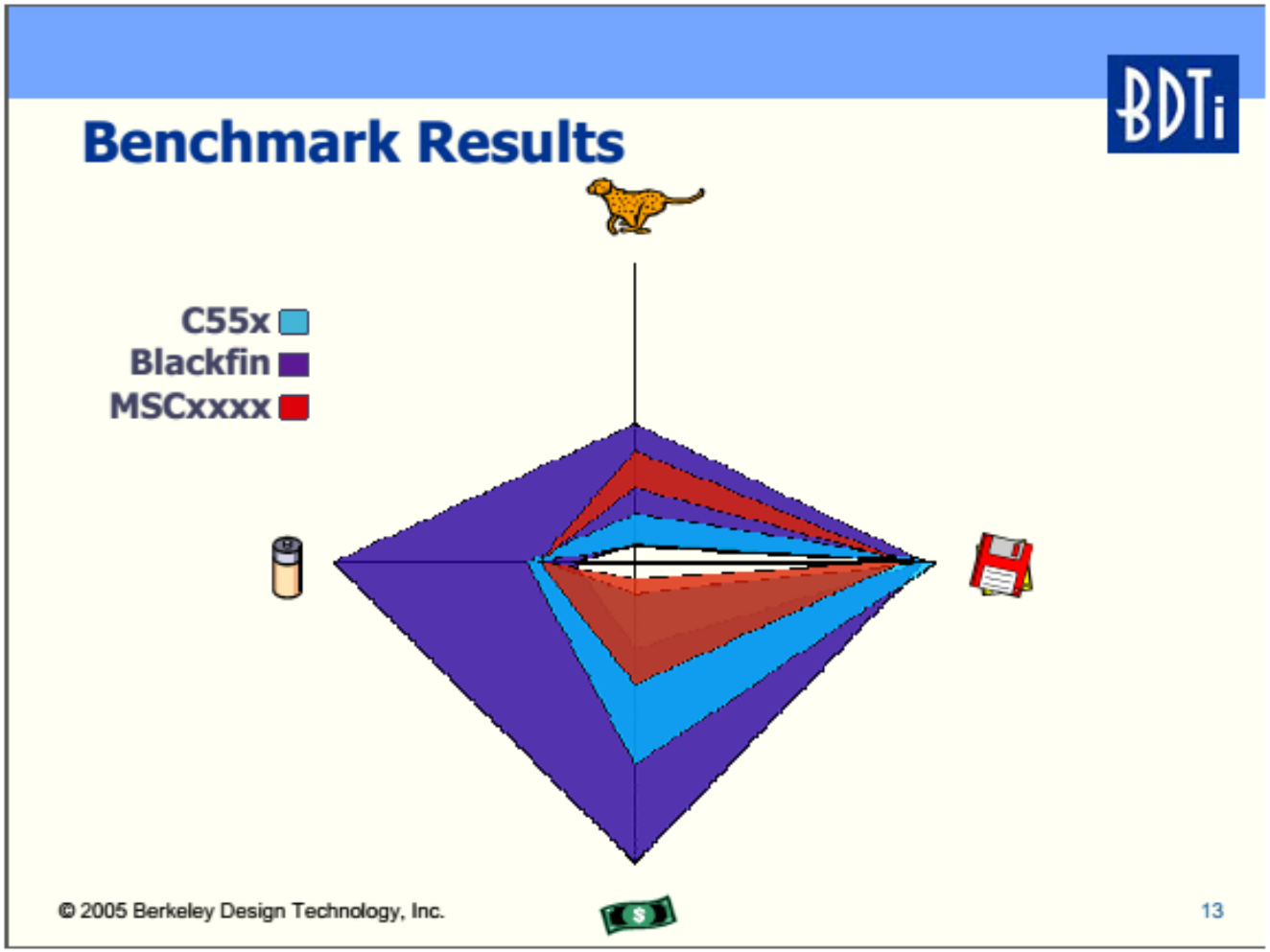
BDTI Benchmarks



BDTI Benchmarks



BDTI Benchmarks



Conclusion

Additional Literature

- “Choosing a DSP Processor”, Berkeley Design Technology, Inc.
- “Evaluating DSP Processor Performance”, Berkeley Design Technology, Inc.
- “Benchmarking Processors for DSP Applications”, Berkeley Design Technology, Inc.
- “Independent DSP Benchmarks: Methodologies and Results”, Berkeley Design Technology, Inc.
- “The BDTImark2000: A Summary Measure of Signal Processing Speed”, Berkeley Design Technology, Inc.