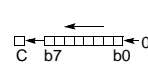
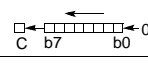
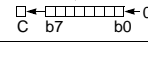
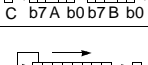

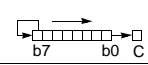
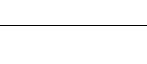


3.5 Instruction Set

Refer to **Table 3-2**, which shows all the M68HC11 instructions in all possible addressing modes. For each instruction, the table shows the operand construction, the number of machine code bytes, and execution time in CPU E-clock cycles.

Table 3-2 Instruction Set (Sheet 1 of 7)

Mnemonic	Operation	Description	Addressing Mode	Instruction			Condition Codes								
				Opcode	Operand	Cycles	S	X	H	I	N	Z	V	C	
ABA	Add Accumulators	$A + B \Rightarrow A$	INH	1B	—	2	—	—	Δ	—	Δ	Δ	Δ	Δ	
ABX	Add B to X	$IX + (00 : B) \Rightarrow IX$	INH	3A	—	3	—	—	—	—	—	—	—	—	
ABY	Add B to Y	$IY + (00 : B) \Rightarrow IY$	INH	18 3A	—	4	—	—	—	—	—	—	—	—	
ADCA (opr)	Add with Carry to A	$A + M + C \Rightarrow A$	A	IMM	89	ii	2	—	—	Δ	—	Δ	Δ	Δ	Δ
			A	DIR	99	dd	3								
			A	EXT	B9	hh ll	4								
			A	IND,X	A9	ff	4								
			A	IND,Y	A9	ff	5								
ADCB (opr)	Add with Carry to B	$B + M + C \Rightarrow B$	B	IMM	C9	ii	2	—	—	Δ	—	Δ	Δ	Δ	Δ
			B	DIR	D9	dd	3								
			B	EXT	F9	hh ll	4								
			B	IND,X	E9	ff	4								
			B	IND,Y	E9	ff	5								
ADDA (opr)	Add Memory to A	$A + M \Rightarrow A$	A	IMM	8B	ii	2	—	—	Δ	—	Δ	Δ	Δ	Δ
			A	DIR	9B	dd	3								
			A	EXT	BB	hh ll	4								
			A	IND,X	AB	ff	4								
			A	IND,Y	AB	ff	5								
ADDB (opr)	Add Memory to B	$B + M \Rightarrow B$	B	IMM	CB	ii	2	—	—	Δ	—	Δ	Δ	Δ	Δ
			B	DIR	DB	dd	3								
			B	EXT	FB	hh ll	4								
			B	IND,X	EB	ff	4								
			B	IND,Y	EB	ff	5								
ADDD (opr)	Add 16-Bit to D	$D + (M : M + 1) \Rightarrow D$		IMM	C3	jj kk	4	—	—	—	—	Δ	Δ	Δ	Δ
				DIR	D3	dd	5								
				EXT	F3	hh ll	6								
				IND,X	E3	ff	6								
				IND,Y	E3	ff	7								
ANDA (opr)	AND A with Memory	$A \cdot M \Rightarrow A$	A	IMM	84	ii	2	—	—	—	—	Δ	Δ	0	—
			A	DIR	94	dd	3								
			A	EXT	B4	hh ll	4								
			A	IND,X	A4	ff	4								
			A	IND,Y	A4	ff	5								
ANDB (opr)	AND B with Memory	$B \cdot M \Rightarrow B$	B	IMM	C4	ii	2	—	—	—	—	Δ	Δ	0	—
			B	DIR	D4	dd	3								
			B	EXT	F4	hh ll	4								
			B	IND,X	E4	ff	4								
			B	IND,Y	E4	ff	5								
ASL (opr)	Arithmetic Shift Left			EXT	78	hh ll	6	—	—	—	—	Δ	Δ	Δ	Δ
				IND,X	68	ff	6								
				IND,Y	68	ff	7								
ASLA	Arithmetic Shift Left A		A	INH	48	—	2	—	—	—	—	Δ	Δ	Δ	Δ
ASLB	Arithmetic Shift Left B		B	INH	58	—	2	—	—	—	—	Δ	Δ	Δ	Δ
ASLD	Arithmetic Shift Left D			INH	05	—	3	—	—	—	—	Δ	Δ	Δ	Δ
ASR	Arithmetic Shift Right			EXT	77	hh ll	6	—	—	—	—	Δ	Δ	Δ	Δ
				IND,X	67	ff	6								
				IND,Y	67	ff	7								
ASRA	Arithmetic Shift Right A		A	INH	47	—	2	—	—	—	—	Δ	Δ	Δ	Δ
ASRB	Arithmetic Shift Right B		B	INH	57	—	2	—	—	—	—	Δ	Δ	Δ	Δ
BCC (rel)	Branch if Carry Clear	? C = 0	REL	24	rr	3	—	—	—	—	—	—	—	—	

Freescale Semiconductor, Inc.

Table 3-2 Instruction Set (Sheet 2 of 7)

Mnemonic	Operation	Description	Addressing Mode	Instruction			Condition Codes								
				Opcode	Operand	Cycles	S	X	H	I	N	Z	V	C	
BCLR (opr) (msk)	Clear Bit(s)	$M \cdot (mm) \Rightarrow M$	DIR IND,X IND,Y	15	dd mm	6	—	—	—	—	Δ	Δ	0	—	
				18	1D	ff mm	7	—	—	—	—	—	—	—	
					1D	ff mm	8	—	—	—	—	—	—	—	—
BCS (rel)	Branch if Carry Set	$? C = 1$	REL	25	rr	3	—	—	—	—	—	—	—		
BEQ (rel)	Branch if = Zero	$? Z = 1$	REL	27	rr	3	—	—	—	—	—	—	—		
BGE (rel)	Branch if Δ Zero	$? N \oplus V = 0$	REL	2C	rr	3	—	—	—	—	—	—	—		
BGT (rel)	Branch if > Zero	$? Z + (N \oplus V) = 0$	REL	2E	rr	3	—	—	—	—	—	—	—		
BHI (rel)	Branch if Higher	$? C + Z = 0$	REL	22	rr	3	—	—	—	—	—	—	—		
BHS (rel)	Branch if Higher or Same	$? C = 0$	REL	24	rr	3	—	—	—	—	—	—	—		
BITA (opr)	Bit(s) Test A with Memory	$A \cdot M$	A A A A A	IMM	85	ii	2	—	—	—	—	Δ	Δ	0	—
				DIR	95	dd	3	—	—	—	—	—	—	—	
				EXT	B5	hh ll	4	—	—	—	—	—	—	—	
				IND,X	A5	ff	4	—	—	—	—	—	—	—	
				IND,Y	18	A5	ff	5	—	—	—	—	—	—	—
BITB (opr)	Bit(s) Test B with Memory	$B \cdot M$	B B B B B	IMM	C5	ii	2	—	—	—	—	Δ	Δ	0	—
				DIR	D5	dd	3	—	—	—	—	—	—	—	
				EXT	F5	hh ll	4	—	—	—	—	—	—	—	
				IND,X	E5	ff	4	—	—	—	—	—	—	—	
				IND,Y	18	E5	ff	5	—	—	—	—	—	—	—
BLE (rel)	Branch if Δ Zero	$? Z + (N \oplus V) = 1$	REL	2F	rr	3	—	—	—	—	—	—	—		
BLO (rel)	Branch if Lower	$? C = 1$	REL	25	rr	3	—	—	—	—	—	—	—		
BLS (rel)	Branch if Lower or Same	$? C + Z = 1$	REL	23	rr	3	—	—	—	—	—	—	—		
BLT (rel)	Branch if < Zero	$? N \oplus V = 1$	REL	2D	rr	3	—	—	—	—	—	—	—		
BMI (rel)	Branch if Minus	$? N = 1$	REL	2B	rr	3	—	—	—	—	—	—	—		
BNE (rel)	Branch if not = Zero	$? Z = 0$	REL	26	rr	3	—	—	—	—	—	—	—		
BPL (rel)	Branch if Plus	$? N = 0$	REL	2A	rr	3	—	—	—	—	—	—	—		
BRA (rel)	Branch Always	$? 1 = 1$	REL	20	rr	3	—	—	—	—	—	—	—		
BRCLR(opr) (msk) (rel)	Branch if Bit(s) Clear	$? M \cdot mm = 0$	DIR IND,X IND,Y	13	dd mm rr	6	—	—	—	—	—	—	—		
				18	1F	ff mm rr	7	—	—	—	—	—	—		
					1F	ff mm rr	8	—	—	—	—	—	—	—	
BRN (rel)	Branch Never	$? 1 = 0$	REL	21	rr	3	—	—	—	—	—	—	—		
BRSET(opr) (msk) (rel)	Branch if Bit(s) Set	$? (M) \cdot mm = 0$	DIR IND,X IND,Y	12	dd mm rr	6	—	—	—	—	—	—	—		
				18	1E	ff mm rr	7	—	—	—	—	—	—		
					1E	ff mm rr	8	—	—	—	—	—	—	—	
BSET (opr) (msk)	Set Bit(s)	$M + mm \Rightarrow M$	DIR IND,X IND,Y	14	dd mm	6	—	—	—	—	Δ	Δ	0	—	
				18	1C	ff mm	7	—	—	—	—	—	—		
					1C	ff mm	8	—	—	—	—	—	—	—	
BSR (rel)	Branch to Subroutine	See Figure 3–2	REL	8D	rr	6	—	—	—	—	—	—	—		
BVC (rel)	Branch if Overflow Clear	$? V = 0$	REL	28	rr	3	—	—	—	—	—	—	—		
BVS (rel)	Branch if Overflow Set	$? V = 1$	REL	29	rr	3	—	—	—	—	—	—	—		
CBA	Compare A to B	$A - B$	INH	11	—	2	—	—	—	—	Δ	Δ	Δ	Δ	
CLC	Clear Carry Bit	$0 \Rightarrow C$	INH	0C	—	2	—	—	—	—	—	—	—	0	
CLI	Clear Interrupt Mask	$0 \Rightarrow I$	INH	0E	—	2	—	—	—	0	—	—	—	—	
CLR (opr)	Clear Memory Byte	$0 \Rightarrow M$	EXT IND,X IND,Y	7F	hh ll	6	—	—	—	—	0	1	0	0	
				18	6F	ff	6	—	—	—	—	—	—	—	
					6F	ff	7	—	—	—	—	—	—	—	—

CENTRAL PROCESSING UNIT

Freescale Semiconductor, Inc.

Table 3-2 Instruction Set (Sheet 3 of 7)

Mnemonic	Operation	Description	Addressing Mode		Instruction			Condition Codes							
					Opcode	Operand	Cycles	S	X	H	I	N	Z	V	C
CLRA	Clear Accumulator A	$0 \Rightarrow A$	A	INH	4F	—	2	—	—	—	—	0	1	0	0
CLRB	Clear Accumulator B	$0 \Rightarrow B$	B	INH	5F	—	2	—	—	—	—	0	1	0	0
CLV	Clear Overflow Flag	$0 \Rightarrow V$		INH	0A	—	2	—	—	—	—	—	—	0	—
CMPA (opr)	Compare A to Memory	A – M	A	IMM	81	ii	2	—	—	—	—	Δ	Δ	Δ	Δ
				DIR	91	dd	3								
				EXT	B1	hh ll	4								
				IND,X	A1	ff	4								
				IND,Y	A1	ff	5								
CMPB (opr)	Compare B to Memory	B – M	B	IMM	C1	ii	2	—	—	—	—	Δ	Δ	Δ	Δ
				DIR	D1	dd	3								
				EXT	F1	hh ll	4								
				IND,X	E1	ff	4								
				IND,Y	B1	ff	5								
COM (opr)	Ones Complement Memory Byte	$\$FF - M \Rightarrow M$		EXT	73	hh ll	6	—	—	—	—	Δ	Δ	0	1
				IND,X	63	ff	6								
				IND,Y	18 63	ff	7								
COMA	Ones Complement A	$\$FF - A \Rightarrow A$	A	INH	43	—	2	—	—	—	—	Δ	Δ	0	1
COMB	Ones Complement B	$\$FF - B \Rightarrow B$	B	INH	53	—	2	—	—	—	—	Δ	Δ	0	1
CPD (opr)	Compare D to Memory 16-Bit	D – M : M + 1		IMM	1A 83	jj kk	5	—	—	—	—	Δ	Δ	Δ	Δ
				DIR	1A 93	dd	6								
				EXT	1A B3	hh ll	7								
				IND,X	1A A3	ff	7								
				IND,Y	CD A3	ff	7								
CPX (opr)	Compare X to Memory 16-Bit	IX – M : M + 1		IMM	8C	jj kk	4	—	—	—	—	Δ	Δ	Δ	Δ
				DIR	9C	dd	5								
				EXT	BC	hh ll	6								
				IND,X	AC	ff	6								
				IND,Y	CD AC	ff	7								
CPY (opr)	Compare Y to Memory 16-Bit	IY – M : M + 1		IMM	18 8C	jj kk	5	—	—	—	—	Δ	Δ	Δ	Δ
				DIR	18 9C	dd	6								
				EXT	18 BC	hh ll	7								
				IND,X	1A AC	ff	7								
				IND,Y	18 AC	ff	7								
DAA	Decimal Adjust A	Adjust Sum to BCD		INH	19	—	2	—	—	—	—	Δ	Δ	Δ	Δ
DEC (opr)	Decrement Memory Byte	M – 1 \Rightarrow M		EXT	7A	hh ll	6	—	—	—	—	Δ	Δ	Δ	—
				IND,X	6A	ff	6								
				IND,Y	18 6A	ff	7								
DECA	Decrement Accumulator A	A – 1 \Rightarrow A	A	INH	4A	—	2	—	—	—	—	Δ	Δ	Δ	—
DECB	Decrement Accumulator B	B – 1 \Rightarrow B	B	INH	5A	—	2	—	—	—	—	Δ	Δ	Δ	—
DES	Decrement Stack Pointer	SP – 1 \Rightarrow SP		INH	34	—	3	—	—	—	—	—	—	—	—
DEX	Decrement Index Register X	IX – 1 \Rightarrow IX		INH	09	—	3	—	—	—	—	—	Δ	—	—
DEY	Decrement Index Register Y	IY – 1 \Rightarrow IY		INH	18 09	—	4	—	—	—	—	—	Δ	—	—
EORA (opr)	Exclusive OR A with Memory	A \oplus M \Rightarrow A	A	IMM	88	ii	2	—	—	—	—	Δ	Δ	0	—
				DIR	98	dd	3								
				EXT	B8	hh ll	4								
				IND,X	A8	ff	4								
				IND,Y	18 A8	ff	5								
EORB (opr)	Exclusive OR B with Memory	B \oplus M \Rightarrow B	B	IMM	C8	ii	2	—	—	—	—	Δ	Δ	0	—
				DIR	D8	dd	3								
				EXT	F8	hh ll	4								
				IND,X	E8	ff	4								
				IND,Y	18 E8	ff	5								
FDIV	Fractional Divide 16 by 16	D / IX \Rightarrow IX; r \Rightarrow D		INH	03	—	41	—	—	—	—	—	Δ	Δ	Δ
IDIV	Integer Divide 16 by 16	D / IX \Rightarrow IX; r \Rightarrow D		INH	02	—	41	—	—	—	—	—	Δ	0	Δ

CENTRAL PROCESSING UNIT

Table 3-2 Instruction Set (Sheet 4 of 7)

Mnemonic	Operation	Description	Addressing Mode	Instruction			Condition Codes							
				Opcode	Operand	Cycles	S	X	H	I	N	Z	V	C
INC (opr)	Increment Memory Byte	$M + 1 \Rightarrow M$	EXT IND,X IND,Y	7C	hh ll	6	—	—	—	—	Δ	Δ	Δ	—
				6C	ff	6								
				18 6C	ff	7								
INCA	Increment Accumulator A	$A + 1 \Rightarrow A$	A INH	4C	—	2	—	—	—	—	Δ	Δ	Δ	—
INCB	Increment Accumulator B	$B + 1 \Rightarrow B$	B INH	5C	—	2	—	—	—	—	Δ	Δ	Δ	—
INS	Increment Stack Pointer	$SP + 1 \Rightarrow SP$	INH	31	—	3	—	—	—	—	—	—	—	—
INX	Increment Index Register X	$IX + 1 \Rightarrow IX$	INH	08	—	3	—	—	—	—	—	Δ	—	—
INY	Increment Index Register Y	$IY + 1 \Rightarrow IY$	INH	18 08	—	4	—	—	—	—	—	Δ	—	—
JMP (opr)	Jump	See Figure 3-2	EXT IND,X IND,Y	7E	hh ll	3	—	—	—	—	—	—	—	—
				6E	ff	3								
				18 6E	ff	4								
JSR (opr)	Jump to Subroutine	See Figure 3-2	DIR EXT IND,X IND,Y	9D	dd	5	—	—	—	—	—	—	—	—
				BD	hh ll	6								
				AD	ff	6								
				18 AD	ff	7								
LDAA (opr)	Load Accumulator A	$M \Rightarrow A$	A IMM A DIR A EXT A IND,X A IND,Y	86	ii	2	—	—	—	—	Δ	Δ	0	—
				96	dd	3								
				B6	hh ll	4								
				A6	ff	4								
				18 A6	ff	5								
LDAB (opr)	Load Accumulator B	$M \Rightarrow B$	B IMM B DIR B EXT B IND,X B IND,Y	C6	ii	2	—	—	—	—	Δ	Δ	0	—
				D6	dd	3								
				F6	hh ll	4								
				E6	ff	4								
				18 E6	ff	5								
LDD (opr)	Load Double Accumulator D	$M \Rightarrow A, M + 1 \Rightarrow B$	IMM DIR EXT IND,X IND,Y	CC	jj kk	3	—	—	—	—	Δ	Δ	0	—
				DC	dd	4								
				FC	hh ll	5								
				EC	ff	5								
				18 EC	ff	6								
LDS (opr)	Load Stack Pointer	$M : M + 1 \Rightarrow SP$	IMM DIR EXT IND,X IND,Y	8E	jj kk	3	—	—	—	—	Δ	Δ	0	—
				9E	dd	4								
				BE	hh ll	5								
				AE	ff	5								
				18 AE	ff	6								
LDX (opr)	Load Index Register X	$M : M + 1 \Rightarrow IX$	IMM DIR EXT IND,X IND,Y	CE	jj kk	3	—	—	—	—	Δ	Δ	0	—
				DE	dd	4								
				FE	hh ll	5								
				EE	ff	5								
				CD EE	ff	6								
LDY (opr)	Load Index Register Y	$M : M + 1 \Rightarrow IY$	IMM DIR EXT IND,X IND,Y	18 CE	jj kk	4	—	—	—	—	Δ	Δ	0	—
				18 DE	dd	5								
				18 FE	hh ll	6								
				1A EE	ff	6								
				18 EE	ff	6								
LSL (opr)	Logical Shift Left		EXT IND,X IND,Y	78	hh ll	6	—	—	—	—	Δ	Δ	Δ	Δ
				68	ff	6								
				18 68	ff	7								
LSLA	Logical Shift Left A		A INH	48	—	2	—	—	—	—	Δ	Δ	Δ	Δ
LSLB	Logical Shift Left B		B INH	58	—	2	—	—	—	—	Δ	Δ	Δ	Δ
LSLD	Logical Shift Left Double		INH	05	—	3	—	—	—	—	Δ	Δ	Δ	Δ
LSR (opr)	Logical Shift Right		EXT IND,X IND,Y	74	hh ll	6	—	—	—	—	0	Δ	Δ	Δ
				64	ff	6								
				18 64	ff	7								
LSRA	Logical Shift Right A		A INH	44	—	2	—	—	—	—	0	Δ	Δ	Δ

Freescale Semiconductor, Inc.

Table 3-2 Instruction Set (Sheet 5 of 7)

Mnemonic	Operation	Description	Addressing Mode	Instruction			Condition Codes								
				Opcode	Operand	Cycles	S	X	H	I	N	Z	V	C	
LSRB	Logical Shift Right B		B	INH	54	—	2	—	—	—	—	0	Δ	Δ	Δ
LSRD	Logical Shift Right Double			INH	04	—	3	—	—	—	—	0	Δ	Δ	Δ
MUL	Multiply 8 by 8	$A * B \Rightarrow D$		INH	3D	—	10	—	—	—	—	—	—	—	Δ
NEG (opr)	Two's Complement Memory Byte	$0 - M \Rightarrow M$		EXT IND,X IND,Y	70 60 60	hh ll ff ff	6 6 7	—	—	—	—	Δ	Δ	Δ	Δ
NEGA	Two's Complement A	$0 - A \Rightarrow A$	A	INH	40	—	2	—	—	—	—	Δ	Δ	Δ	Δ
NEGB	Two's Complement B	$0 - B \Rightarrow B$	B	INH	50	—	2	—	—	—	—	Δ	Δ	Δ	Δ
NOP	No operation	No Operation		INH	01	—	2	—	—	—	—	—	—	—	—
ORAA (opr)	OR Accumulator A (Inclusive)	$A + M \Rightarrow A$	A	IMM DIR EXT IND,X IND,Y	8A 9A BA AA AA	ii dd hh ll ff ff	2 3 4 4 5	—	—	—	—	Δ	Δ	0	—
ORAB (opr)	OR Accumulator B (Inclusive)	$B + M \Rightarrow B$	B	IMM DIR EXT IND,X IND,Y	CA DA FA EA EA	ii dd hh ll ff ff	2 3 4 4 5	—	—	—	—	Δ	Δ	0	—
PSHA	Push A onto Stack	$A \Rightarrow \text{Stk}, \text{SP} = \text{SP} - 1$	A	INH	36	—	3	—	—	—	—	—	—	—	—
PSHB	Push B onto Stack	$B \Rightarrow \text{Stk}, \text{SP} = \text{SP} - 1$	B	INH	37	—	3	—	—	—	—	—	—	—	—
PSHX	Push X onto Stack (Lo First)	$\text{IX} \Rightarrow \text{Stk}, \text{SP} = \text{SP} - 2$		INH	3C	—	4	—	—	—	—	—	—	—	—
PSHY	Push Y onto Stack (Lo First)	$\text{IY} \Rightarrow \text{Stk}, \text{SP} = \text{SP} - 2$		INH	18 3C	—	5	—	—	—	—	—	—	—	—
PULA	Pull A from Stack	$\text{SP} = \text{SP} + 1, A \Leftarrow \text{Stk}$	A	INH	32	—	4	—	—	—	—	—	—	—	—
PULB	Pull B from Stack	$\text{SP} = \text{SP} + 1, B \Leftarrow \text{Stk}$	B	INH	33	—	4	—	—	—	—	—	—	—	—
PULX	Pull X From Stack (Hi First)	$\text{SP} = \text{SP} + 2, \text{IX} \Leftarrow \text{Stk}$		INH	38	—	5	—	—	—	—	—	—	—	—
PULY	Pull Y from Stack (Hi First)	$\text{SP} = \text{SP} + 2, \text{IY} \Leftarrow \text{Stk}$		INH	18 38	—	6	—	—	—	—	—	—	—	—
ROL (opr)	Rotate Left			EXT IND,X IND,Y	79 69 69	hh ll ff ff	6 6 7	—	—	—	—	Δ	Δ	Δ	Δ
ROLA	Rotate Left A		A	INH	49	—	2	—	—	—	—	Δ	Δ	Δ	Δ
ROLB	Rotate Left B		B	INH	59	—	2	—	—	—	—	Δ	Δ	Δ	Δ
ROR (opr)	Rotate Right			EXT IND,X IND,Y	76 66 66	hh ll ff ff	6 6 7	—	—	—	—	Δ	Δ	Δ	Δ
RORA	Rotate Right A		A	INH	46	—	2	—	—	—	—	Δ	Δ	Δ	Δ
RORB	Rotate Right B		B	INH	56	—	2	—	—	—	—	Δ	Δ	Δ	Δ
RTI	Return from Interrupt	See Figure 3-2		INH	3B	—	12	Δ	↓	Δ	Δ	Δ	Δ	Δ	Δ
RTS	Return from Subroutine	See Figure 3-2		INH	39	—	5	—	—	—	—	—	—	—	—
SBA	Subtract B from A	$A - B \Rightarrow A$		INH	10	—	2	—	—	—	—	Δ	Δ	Δ	Δ

Freescale Semiconductor, Inc.

Freescale Semiconductor, Inc.

Table 3-2 Instruction Set (Sheet 6 of 7)

Mnemonic	Operation	Description	Addressing Mode	Instruction			Condition Codes							
				Opcode	Operand	Cycles	S	X	H	I	N	Z	V	C
SBCA (opr)	Subtract with Carry from A	$A - M - C \Rightarrow A$	A IMM	82	ii	2	—	—	—	—	Δ	Δ	Δ	Δ
			A DIR	92	dd	3								
			A EXT	B2	hh ll	4								
			A IND,X	A2	ff	4								
			A IND,Y	A2	ff	5								
SBCB (opr)	Subtract with Carry from B	$B - M - C \Rightarrow B$	B IMM	C2	ii	2	—	—	—	—	Δ	Δ	Δ	Δ
			B DIR	D2	dd	3								
			B EXT	F2	hh ll	4								
			B IND,X	E2	ff	4								
			B IND,Y	E2	ff	5								
SEC	Set Carry	$1 \Rightarrow C$	INH	0D	—	2	—	—	—	—	—	—	—	1
SEI	Set Interrupt Mask	$1 \Rightarrow I$	INH	0F	—	2	—	—	—	1	—	—	—	—
SEV	Set Overflow Flag	$1 \Rightarrow V$	INH	0B	—	2	—	—	—	—	—	—	1	—
STAA (opr)	Store Accumulator A	$A \Rightarrow M$	A DIR	97	dd	3	—	—	—	—	Δ	Δ	0	—
			A EXT	B7	hh ll	4								
			A IND,X	A7	ff	4								
			A IND,Y	A7	ff	5								
STAB (opr)	Store Accumulator B	$B \Rightarrow M$	B DIR	D7	dd	3	—	—	—	—	Δ	Δ	0	—
			B EXT	F7	hh ll	4								
			B IND,X	E7	ff	4								
			B IND,Y	E7	ff	5								
STD (opr)	Store Accumulator D	$A \Rightarrow M, B \Rightarrow M + 1$	DIR	DD	dd	4	—	—	—	—	Δ	Δ	0	—
			EXT	FD	hh ll	5								
			IND,X	ED	ff	5								
			IND,Y	ED	ff	6								
STOP	Stop Internal Clocks	—	INH	CF	—	2	—	—	—	—	—	—	—	
STS (opr)	Store Stack Pointer	$SP \Rightarrow M : M + 1$	DIR	9F	dd	4	—	—	—	—	Δ	Δ	0	—
			EXT	BF	hh ll	5								
			IND,X	AF	ff	5								
			IND,Y	AF	ff	6								
STX (opr)	Store Index Register X	$IX \Rightarrow M : M + 1$	DIR	DF	dd	4	—	—	—	—	Δ	Δ	0	—
			EXT	FF	hh ll	5								
			IND,X	EF	ff	5								
			IND,Y	EF	ff	6								
STY (opr)	Store Index Register Y	$IY \Rightarrow M : M + 1$	DIR	18	DF	5	—	—	—	—	Δ	Δ	0	—
			EXT	18	FF	6								
			IND,X	1A	EF	6								
			IND,Y	18	EF	6								
SUBA (opr)	Subtract Memory from A	$A - M \Rightarrow A$	A IMM	80	ii	2	—	—	—	—	Δ	Δ	Δ	Δ
			A DIR	90	dd	3								
			A EXT	B0	hh ll	4								
			A IND,X	A0	ff	4								
			A IND,Y	A0	ff	5								
SUBB (opr)	Subtract Memory from B	$B - M \Rightarrow B$	A IMM	C0	ii	2	—	—	—	—	Δ	Δ	Δ	Δ
			A DIR	D0	dd	3								
			A EXT	F0	hh ll	4								
			A IND,X	E0	ff	4								
			A IND,Y	E0	ff	5								
SUBD (opr)	Subtract Memory from D	$D - M : M + 1 \Rightarrow D$	IMM	83	jj kk	4	—	—	—	—	Δ	Δ	Δ	Δ
			DIR	93	dd	5								
			EXT	B3	hh ll	6								
			IND,X	A3	ff	6								
			IND,Y	A3	ff	7								
SWI	Software Interrupt	See Figure 3-2	INH	3F	—	14	—	—	—	1	—	—	—	—
TAB	Transfer A to B	$A \Rightarrow B$	INH	16	—	2	—	—	—	—	Δ	Δ	0	—
TAP	Transfer A to CC Register	$A \Rightarrow CCR$	INH	06	—	2	Δ	\downarrow	Δ	Δ	Δ	Δ	Δ	Δ
TBA	Transfer B to A	$B \Rightarrow A$	INH	17	—	2	—	—	—	—	Δ	Δ	0	—
TEST	TEST (Only in Test Modes)	Address Bus Counts	INH	00	—	*	—	—	—	—	—	—	—	—
TPA	Transfer CC Register to A	$CCR \Rightarrow A$	INH	07	—	2	—	—	—	—	—	—	—	—
TST (opr)	Test for Zero or Minus	$M - 0$	EXT	7D	hh ll	6	—	—	—	—	Δ	Δ	0	0
			IND,X	6D	ff	6								
			IND,Y	6D	ff	7								
TSTA	Test A for Zero or Minus	$A - 0$	A INH	4D	—	2	—	—	—	—	Δ	Δ	0	0
TSTB	Test B for Zero or Minus	$B - 0$	B INH	5D	—	2	—	—	—	—	Δ	Δ	0	0

CENTRAL PROCESSING UNIT

Freescale Semiconductor, Inc.

Table 3-2 Instruction Set (Sheet 7 of 7)

Mnemonic	Operation	Description	Addressing Mode	Instruction			Condition Codes							
				Opcode	Operand	Cycles	S	X	H	I	N	Z	V	C
TSX	Transfer Stack Pointer to X	SP + 1 ⇒ IX	INH	30	—	3	—	—	—	—	—	—	—	—
TSY	Transfer Stack Pointer to Y	SP + 1 ⇒ IY	INH	18 30	—	4	—	—	—	—	—	—	—	—
TXS	Transfer X to Stack Pointer	IX - 1 ⇒ SP	INH	35	—	3	—	—	—	—	—	—	—	—
TYS	Transfer Y to Stack Pointer	IY - 1 ⇒ SP	INH	18 35	—	4	—	—	—	—	—	—	—	—
WAI	Wait for Interrupt	Stack Regs & WAIT	INH	3E	—	**	—	—	—	—	—	—	—	—
XGDX	Exchange D with X	IX ⇒ D, D ⇒ IX	INH	8F	—	3	—	—	—	—	—	—	—	—
XGDY	Exchange D with Y	IY ⇒ D, D ⇒ IY	INH	18 8F	—	4	—	—	—	—	—	—	—	—