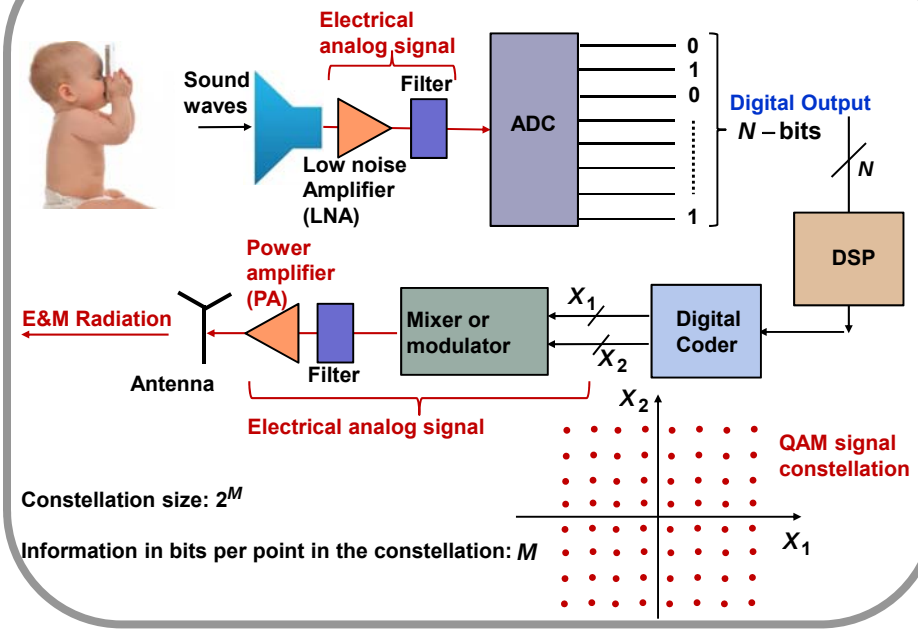
Lecture 22

FET Circuit Design Techniques for RF Applications and Wireless Communications

In this lecture you will learn:

- Circuits for wireless communications
- Signal multipliers and mixers
- Single-balanced and double-balanced mixers
- CMOS RF Oscillators
- Analog to digital converters
- Digital to analog converters

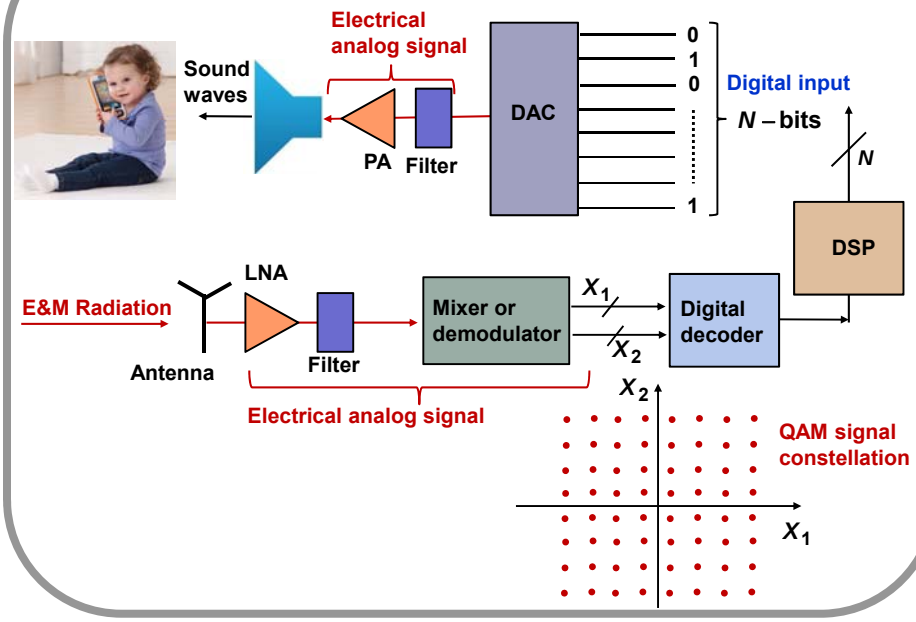
Signal Transmission in Wireless Communications



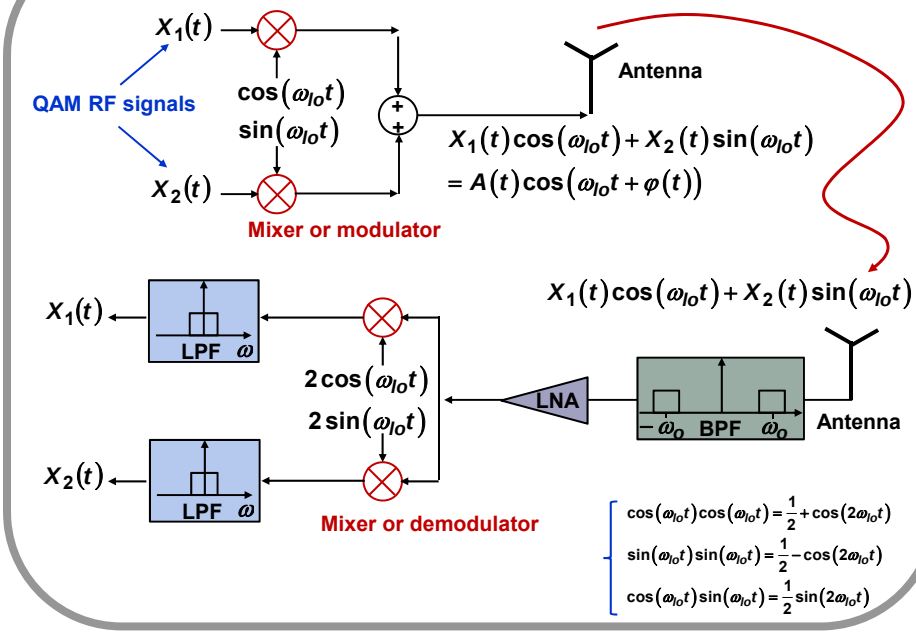
Constellation size: 2^M

Information in bits per point in the constellation: M

Signal Reception in Wireless Communications



RF Mixer or Modulator/Demodulator



Signal Mixers

$\omega_{lo} >> \omega_{rf}$

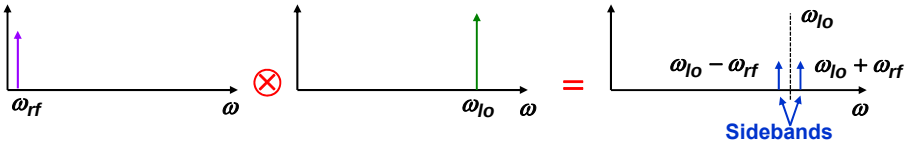
Mixer Function:

$$X_1(t) = v_{rf}\cos(\omega_{rf}t)$$

$$v_{lo}\cos(\omega_{lo}t)$$

$$Av_{rf}v_{lo}\cos(\omega_{rf}t)\cos(\omega_{lo}t)$$

$$= \frac{A}{2}v_{rf}v_{lo}\left[\cos\left((\omega_{lo}+\omega_{rf})t\right) + \cos\left((\omega_{lo}-\omega_{rf})t\right)\right]$$



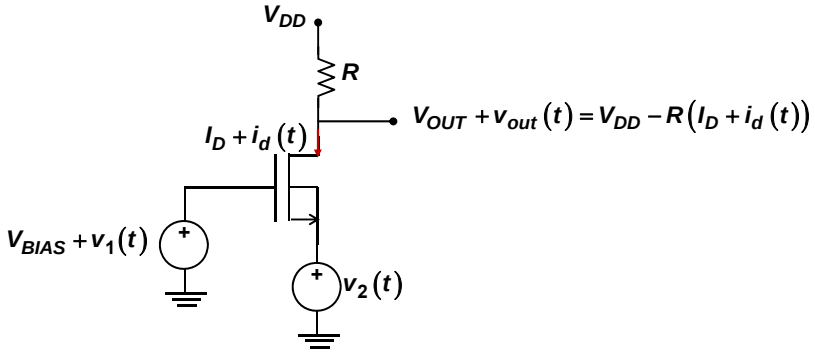
Mixer Conversion Gain:

$$\text{Conversion gain} = G_C = \frac{\frac{A}{2}v_{rf}v_{lo}}{v_{rf}} = \frac{A}{2}v_{lo}$$

Need a strong *LO* signal to obtain a good conversion gain

Need nonlinear components to realize voltage mixers and/or multipliers

FET is Not a Linear Device



Rough analysis (assuming operation in saturation and $\lambda_n \approx 0$):

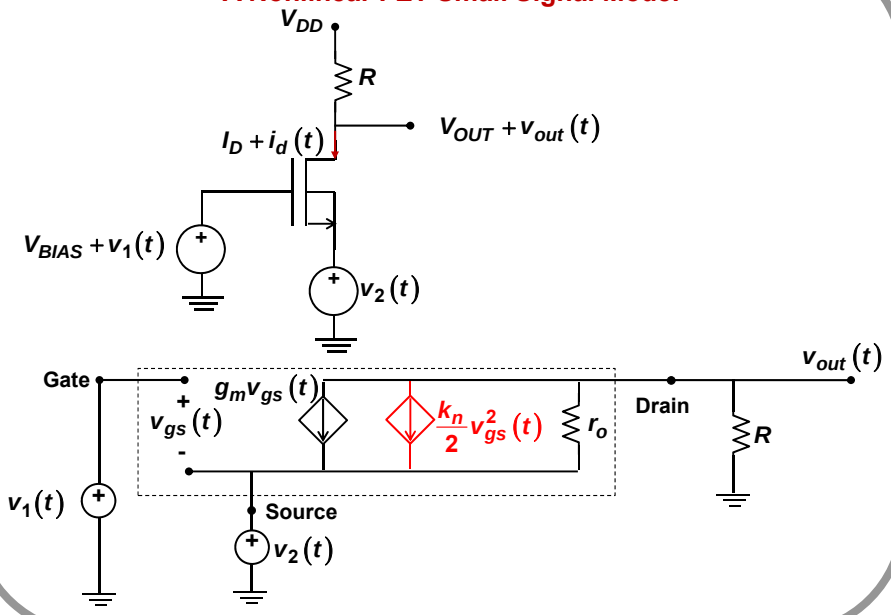
$$i_D = I_D + i_d(t)$$

$$\approx \frac{k_n}{2}\left[V_{BIAS}+v_1(t)-v_2(t)-V_{TN}\right]^2$$

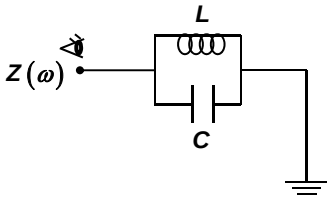
$$= \frac{k_n}{2}\left[V_B - V_{TN}\right]^2 + \frac{k_n}{2}\left[v_1(t)-v_2(t)\right]^2 + k_n\left[V_B - V_{TN}\right]\left[v_1(t)-v_2(t)\right]$$

$$\frac{k_n}{2}\left[v_1^2(t)+v_2^2(t)\right] - k_n v_1(t)v_2(t)$$ ← Product term !!

A Nonlinear FET Small Signal Model



An *LC* Tank Circuit

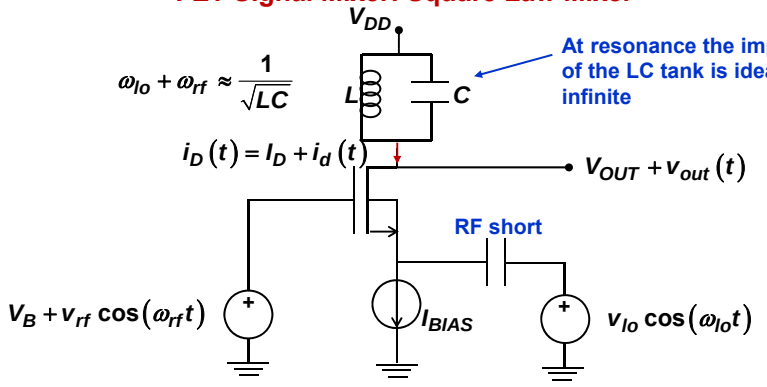


$$Z(\omega) = \frac{j\omega L \times \frac{1}{j\omega C}}{j\omega L + \frac{1}{j\omega C}} = \frac{j\omega L}{1 - \omega^2 LC}$$

Very large impedance at resonance when:

$$\omega = \frac{1}{\sqrt{LC}}$$

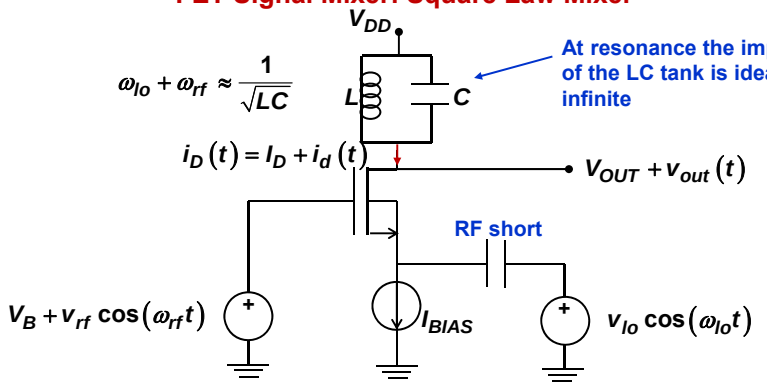
FET Signal Mixer: Square Law Mixer



Rough analysis (assuming $\lambda_n \approx 0$):

$$i_D \approx \frac{k_n}{2}\left[V_B+v_{rf}\cos(\omega_{RF}t)-v_{lo}\cos(\omega_{lo}t)-V_{TN}\right]^2$$
$$=\frac{k_n}{2}\left[V_B-V_{TN}\right]^2+\frac{k_n}{2}\left[v_{rf}\cos(\omega_{rf}t)-v_{lo}\cos(\omega_{lo}t)\right]^2$$
$$+k_n\left[V_B-V_{TN}\right]\left[v_{rf}\cos(\omega_{rf}t)-v_{lo}\cos(\omega_{lo}t)\right]$$

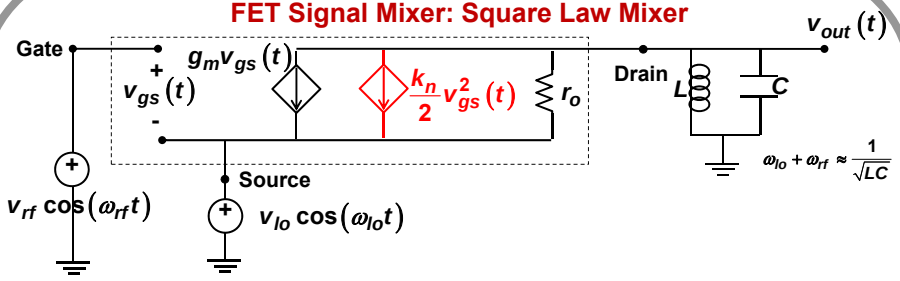
FET Signal Mixer: Square Law Mixer



Rough analysis (assuming $\lambda_n \approx 0$):

$$i_D \approx \frac{k_n}{2}\left[V_B-V_{TN}\right]^2+\frac{k_n}{4}\left[v_{rf}^2+v_{lo}^2\right]+\frac{k_n}{4}\left[v_{rf}^2\cos(2\omega_{rf}t)+v_{lo}^2\cos(2\omega_{lo}t)\right]$$
$$-k_n v_{rf}v_{lo}\cos(\omega_{rf}t)\cos(\omega_{lo}t) \quad \leftarrow \text{Product term !!}$$
$$+k_n\left[V_B-V_{TN}\right]\left[v_{rf}\cos(\omega_{rf}t)-v_{lo}\cos(\omega_{lo}t)\right]$$

FET Signal Mixer: Square Law Mixer



The dominant signal components at the outout near the frequency ω_{LO} are:

$$v_{out}(t) = \frac{k_n}{2} v_{rf} v_{lo} \mathrm{Re}\left\{ \frac{j\omega/C}{\frac{1}{LC} - \omega^2 + j\omega\frac{1}{r_o C}} e^{j\omega t} \right\}_{\omega=\omega_{lo}+\omega_{rf}}$$

Dominant term

$$+ \frac{k_n}{2} v_{rf} v_{lo} \mathrm{Re}\left\{ \frac{j\omega/C}{\frac{1}{LC} - \omega^2 + j\omega\frac{1}{r_o C}} e^{j\omega t} \right\}_{\omega=\omega_{lo}-\omega_{rf}}$$

$$+ g_m v_{lo} \mathrm{Re}\left\{ \frac{j\omega/C}{\frac{1}{LC} - \omega^2 + j\omega\frac{1}{r_o C}} e^{j\omega t} \right\}_{\omega=\omega_{lo}}$$

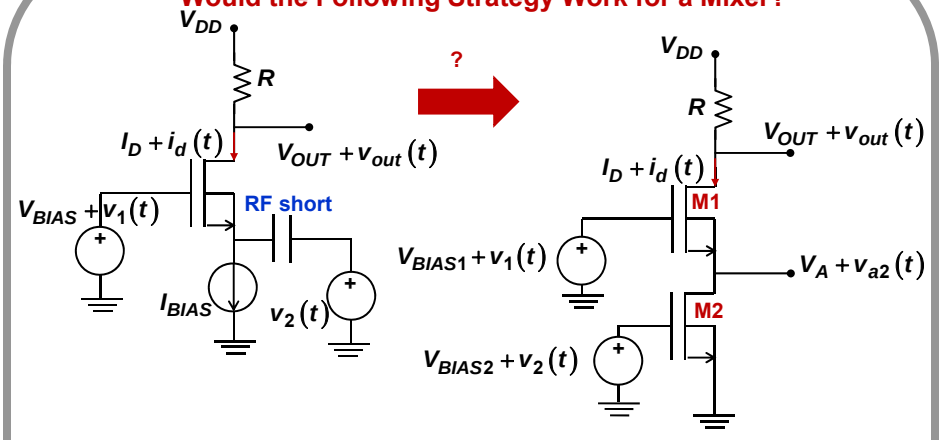
Not good

Conversion gain = G_C

$$\approx \frac{\frac{k_n}{2} v_{rf} v_{lo} r_o}{v_{rf}}$$

$$= \frac{k_n}{2} v_{lo} r_o$$

Would the Following Strategy Work for a Mixer?

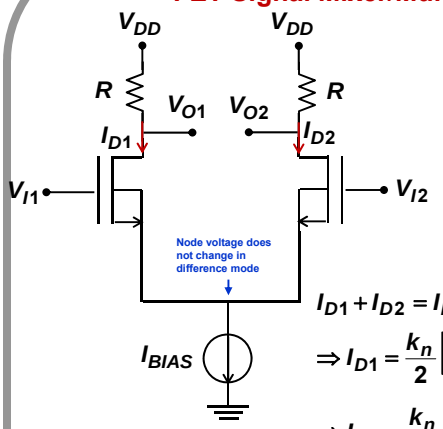


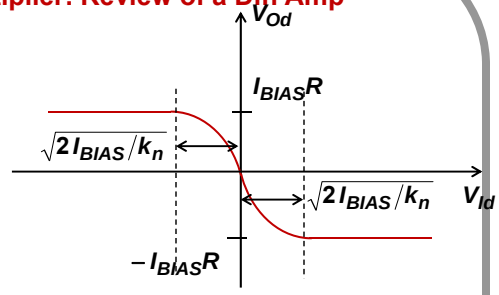
Since M1 and M2 must always have the same currents, once can show that:

$$V_A + v_{a2}(t) \approx \left[V_{BIAS1} + v_1(t)\right] - \left[V_{BIAS2} + v_2(t)\right] \qquad \text{(assuming } \lambda_n \approx 0\text{)}$$

So that the current $I_D + i_d(t)$ will have no (substantial) product term of the voltages v_1 and v_2

FET Signal Mixer/Multiplier: Review of a Diff Amp





$$I_{D1} + I_{D2} = I_{BIAS}$$

$$\Rightarrow I_{D1} = \frac{k_n}{2}\left[(V_{GS1} - V_{TN})^2\right] = \frac{I_{BIAS}}{2} + k_n \frac{V_{Id}}{4}\sqrt{4\frac{I_{BIAS}}{k_n} - V_{Id}^2}$$

$$\Rightarrow I_{D2} = \frac{k_n}{2}\left[(V_{GS2} - V_{TN})^2\right] = \frac{I_{BIAS}}{2} - k_n \frac{V_{Id}}{4}\sqrt{4\frac{I_{BIAS}}{k_n} - V_{Id}^2}$$

$$V_{Od} = V_{O1} - V_{O2} = -Rk_n \frac{(V_{I1} - V_{I2})}{2}\sqrt{4\frac{I_{BIAS}}{k_n} - (V_{I1} - V_{I2})^2}$$

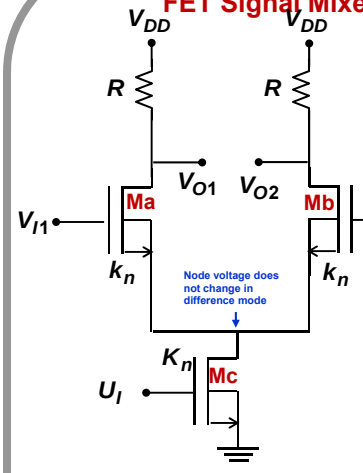
Assume small

Provided:

$$\sqrt{\frac{2I_{BIAS}}{k_n}} >> (V_{I1} - V_{I2})$$

$$\approx -Rk_n \frac{(V_{I1} - V_{I2})}{2}\sqrt{4\frac{I_{BIAS}}{k_n}}$$

FET Signal Mixer/Multiplier: Single-Balanced Mixer



A single-balanced mixer:

$$V_{Od} = V_{O1} - V_{O2} \approx -Rk_n \frac{(V_{I1} - V_{I2})}{2}\sqrt{4\frac{I_{BIAS}}{k_n}}$$

$$I_{BIAS} \approx \frac{K_n}{2}(U_I - V_{TN})^2$$

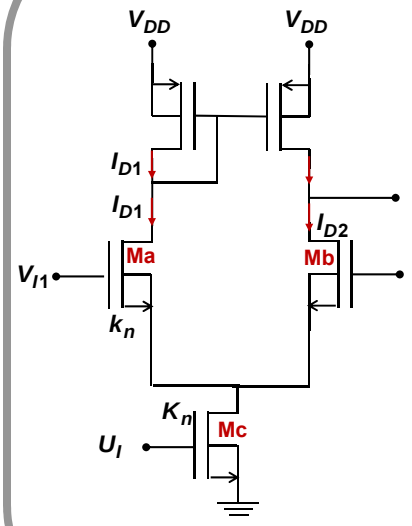
Product term

$$V_{Od} = V_{O1} - V_{O2} \approx -Rk_n \frac{(V_{I1} - V_{I2})}{2}\sqrt{2\frac{K_n}{k_n}}(U_I - V_{TN})$$

But still not quite what one would want……..

i) The input voltage U_I is not differential…….
ii) The two input voltages being multiplied don't appear symmetrically in the final answer
iii) There is an additional term proportional only to V_{I1}-V_{I2} in the output

FET Signal Mixer/Multiplier: Single-Balanced Mixer



$$V_{OUT} = k_n \frac{V_{Id}}{2} \sqrt{4 \frac{I_{BIAS}}{k_n}} \left(r_{on} \| r_{op} \right)$$

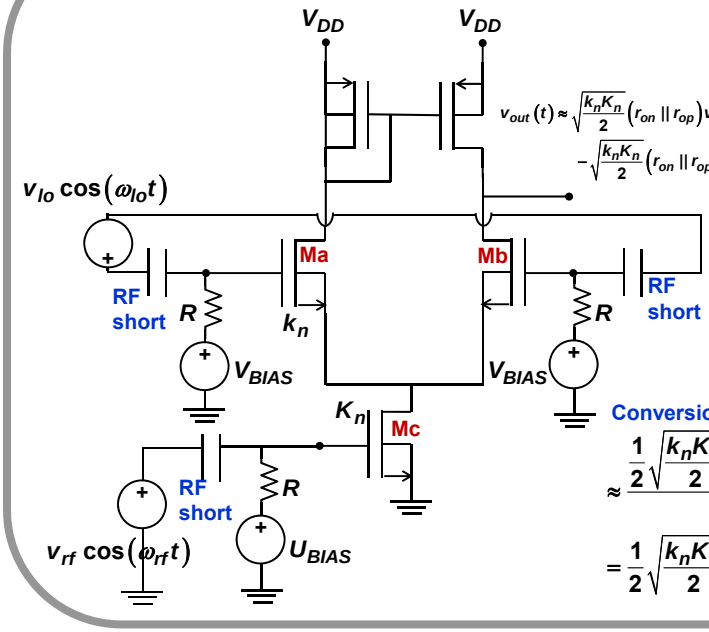
$$I_{BIAS} \approx \frac{K_n}{2} (U_I - V_{TN})^2$$

Product term

$$V_{OUT} = \sqrt{\frac{k_n K_n}{2}} V_{Id} (U_I - V_{TN}) \left(r_{on} \| r_{op} \right)$$

Much higher conversion gain with PFET current mirror on top!
And a single-ended output!

FET Signal Mixer/Multiplier: Single-Balanced Mixer



$$v_{out}(t) \approx \sqrt{\frac{k_n K_n}{2}} \left(r_{on} \| r_{op} \right) v_{lo} v_{rf} \cos(\omega_{rf} t) \cos(\omega_{lo} t)$$
$$- \sqrt{\frac{k_n K_n}{2}} \left(r_{on} \| r_{op} \right) (U_{BIAS} - V_{TN}) v_{lo} \cos(\omega_{lo} t)$$

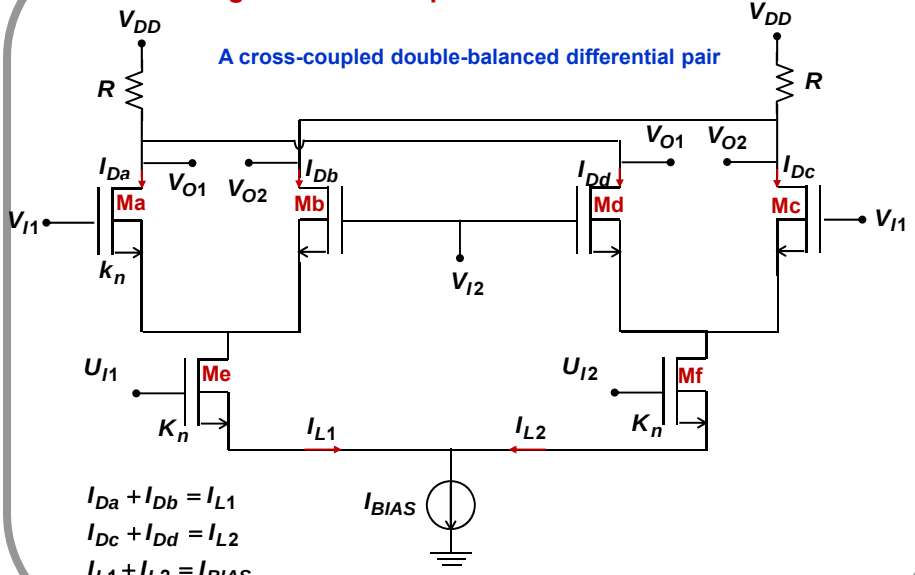
Not good

Conversion gain = G_C

$$\approx \frac{\frac{1}{2} \sqrt{\frac{k_n K_n}{2}} v_{RF} v_{LO} \left(r_{on} \| r_{op} \right)}{v_{RF}}$$

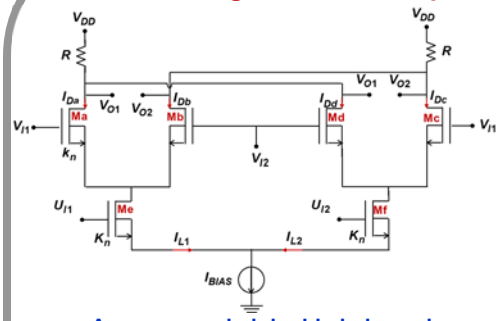
$$= \frac{1}{2} \sqrt{\frac{k_n K_n}{2}} v_{LO} \left(r_{on} \| r_{op} \right)$$

FET Signal Mixer/Multiplier: A Double-Balanced Mixer



$$I_{Da} + I_{Db} = I_{L1}$$
$$I_{Dc} + I_{Dd} = I_{L2}$$
$$I_{L1} + I_{L2} = I_{BIAS}$$

FET Signal Mixer/Multiplier: A Double-Balanced Mixer



A cross-coupled double-balanced differential pair

$$I_{Da} + I_{Db} = I_{L1}$$
$$I_{Dc} + I_{Dd} = I_{L2}$$
$$I_{L1} + I_{L2} = I_{BIAS}$$

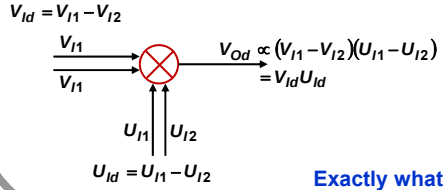
$$I_{Da} = \frac{k_n}{2}\left[(V_{GSa} - V_{TN})^2\right] \approx \frac{I_{L1}}{2} + k_n \frac{V_{Id}}{4}\sqrt{4\frac{I_{L1}}{k_n}}$$

$$I_{Db} = \frac{k_n}{2}\left[(V_{GSb} - V_{TN})^2\right] = \frac{I_{L1}}{2} - k_n \frac{V_{Id}}{4}\sqrt{4\frac{I_{L1}}{k_n}}$$

$$I_{Dc} = \frac{k_n}{2}\left[(V_{GSc} - V_{TN})^2\right] \approx \frac{I_{L2}}{2} + k_n \frac{V_{Id}}{4}\sqrt{4\frac{I_{L2}}{k_n}}$$

$$I_{Dd} = \frac{k_n}{2}\left[(V_{GSd} - V_{TN})^2\right] \approx \frac{I_{L2}}{2} - k_n \frac{V_{Id}}{4}\sqrt{4\frac{I_{L2}}{k_n}}$$

$$V_{Id} = V_{I1} - V_{I2}$$



$$V_{Od} = V_{O1} - V_{O2} = -(I_{Da} + I_{Dd})R + (I_{Dc} + I_{Db})R$$
$$\approx -Rk_n \frac{(V_{I1} - V_{I2})}{2}\left(\sqrt{4\frac{I_{L1}}{k_n}} - \sqrt{4\frac{I_{L2}}{k_n}}\right)$$
$$= -Rk_n \frac{(V_{I1} - V_{I2})}{2}\sqrt{2\frac{K_n}{k_n}}(U_{I1} - U_{I2})$$
$$= -R\sqrt{\frac{k_n K_n}{2}}(V_{I1} - V_{I2})(U_{I1} - U_{I2})$$

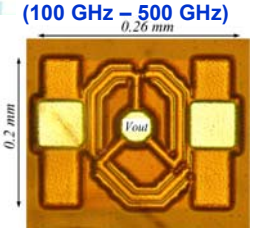
Exactly what one would want! → Product terms

Oscillators: Electronic, Photonic, and Spintronic

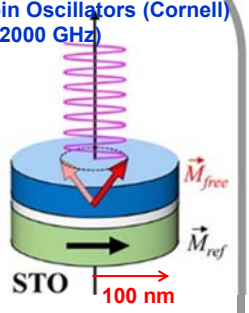
Photonic Oscillators (Lasers)
(2 THz – 2000 THz)

~ 1 m

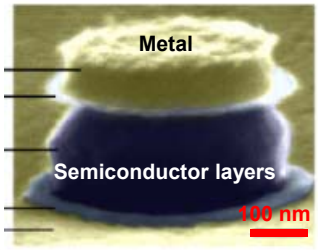
CMOS THz Oscillators
(Cornell)
(100 GHz – 500 GHz)



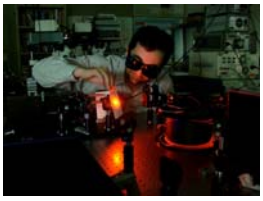
Electron Spin Oscillators (Cornell)
(100 MHz – 2000 GHz)



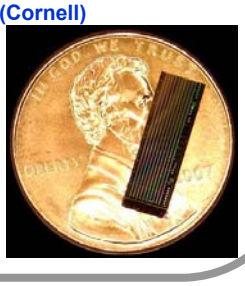
Plasmonic Nanopatch Spasers
(Cornell, UCB)



Fiber lasers (Cornell)

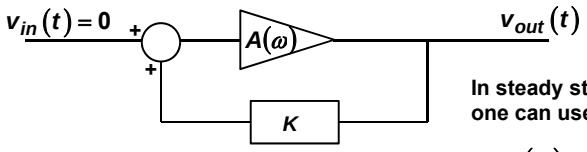


Semiconductor lasers
(Cornell)



Electrical Oscillators: A Phenomenological Introduction

Consider the following circuit with positive feedback:



In steady state operation (when one can use phasors):

$$v_{out}(\omega)=\frac{A(\omega)}{1-KA(\omega)}v_{in}(\omega)$$

$$\left[1-KA(\omega)\right]v_{out}(\omega)=A(\omega)v_{in}(\omega)$$

Loop gain: $A(\omega)K$

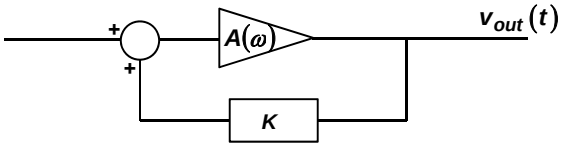
One can have a non-zero output at frequency ω, with no input, if at that frequency:

$$\left[1-KA(\omega)\right]v_{out}(\omega)=0$$
$$\Rightarrow 1-KA(\omega)=0$$
$$\Rightarrow A(\omega)K=1$$
$$\Rightarrow \left|A(\omega)K\right|=1 \quad \text{and} \quad \angle\left[A(\omega)K\right]=2\pi n \quad \{\, n=0,1,2...$$

For steady state oscillation, the loop gain must equal unity

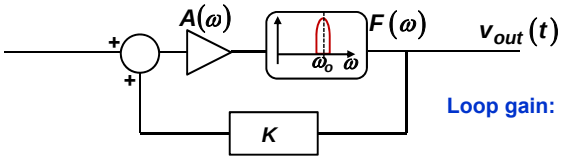
Electrical Oscillators: A Phenomenological Introduction

Consider the following circuit with positive feedback:



The unity loop gain condition $A(\omega)K = 1$ could be met (or almost met) at many different frequencies at the same time!

Add a bandwidth limiting element in the loop – a narrow bandpass filter:



Loop gain: $A(\omega)F(\omega)K$

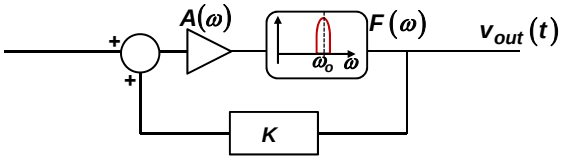
Now the condition for steady state oscillation at the frequency ω becomes:

$$\left[1 - KF(\omega)A(\omega)\right]v_{out}(\omega) = 0$$

$$\Rightarrow A(\omega)F(\omega)K = 1$$

→ **Will favor oscillation at frequency ω_o**

Electrical Oscillators: A Phenomenological Introduction



Now the condition for steady state oscillation at the frequency ω_o is: $A(\omega_o)F(\omega_o)K = 1$

But is the oscillation going to be stable?

Q: What if the loop gain is slightly larger than unity:

$$\left|A(\omega_o)F(\omega_o)K\right| > 1$$

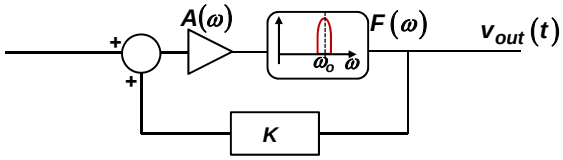
The oscillations will build up to infinity (phasor analysis not valid anymore because there is no steady state)

Q: What if the loop gain is slightly smaller than unity:

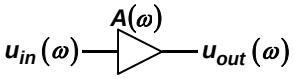
$$\left|A(\omega_o)F(\omega_o)K\right| < 1$$

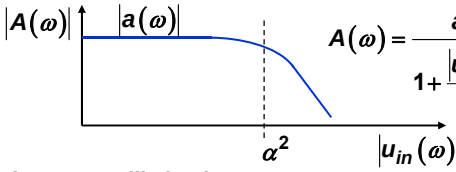
The oscillations might never build up

Electrical Oscillators: A Phenomenological Introduction



What if the gain $A(\omega)$ is a non-linear decreasing function of the input signal power:





$$A(\omega) = \frac{a(\omega)}{1 + \frac{|u_{in}(\omega)|^2}{\alpha^2}}$$

Then the condition for stable steady state oscillation becomes:

$$A(\omega_o)F(\omega_o)K = 1$$

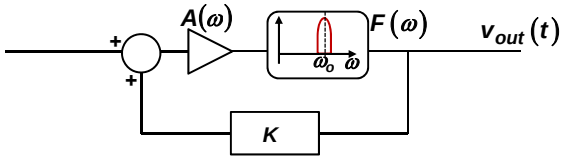
$$\Rightarrow \frac{a(\omega_o)}{1 + \frac{|u_{in}(\omega_o)|^2}{\alpha^2}} F(\omega_o)K = 1$$

Stable provided:

$$|a(\omega_o)F(\omega_o)K| > 1$$

The signal looping around in the oscillator will adjust its magnitude automatically such that the unity gain condition is met…..!!!

Electrical Oscillators: A Phenomenological Introduction



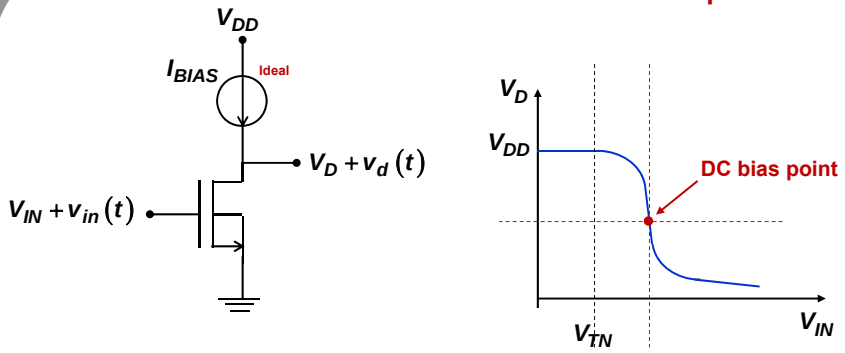
Conditions necessary (but not sufficient) for stable steady state oscillations:

1) The complex loop gain must equal unity

2) There must be a bandwidth limiting element (or a filter) in the loop

3) The magnitude of the loop gain must be a decreasing function of the loop signal power (this is called gain saturation)

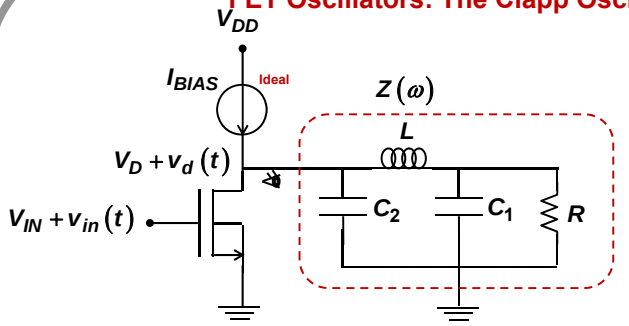
FET Oscillators: Gain Saturation in a CS Amplifier



Things to note:

- The small-signal output is 180 degrees out of phase with the small-signal input
- The magnitude of the gain can be pretty large (typically between 10-100)
- Gain decreases when the magnitude of the small signal input becomes large (this is gain saturation!!)

FET Oscillators: The Clapp Oscillator



$$Z(\omega) = \left[\left(\left(R \,||\, \frac{1}{j\omega C_1}\right) + j\omega L\right) || \left(\frac{1}{j\omega C_2}\right)\right] = \frac{R + (1 + j\omega C_1 R)\, j\omega L}{j\omega (C_1 + C_2) R \left[1 - \omega^2 \frac{C_1 C_2}{C_1 + C_2} L + \frac{1}{j\omega (C_1 + C_2) R} + j\omega \frac{C_2 L}{(C_1 + C_2) R}\right]}$$

Gain:

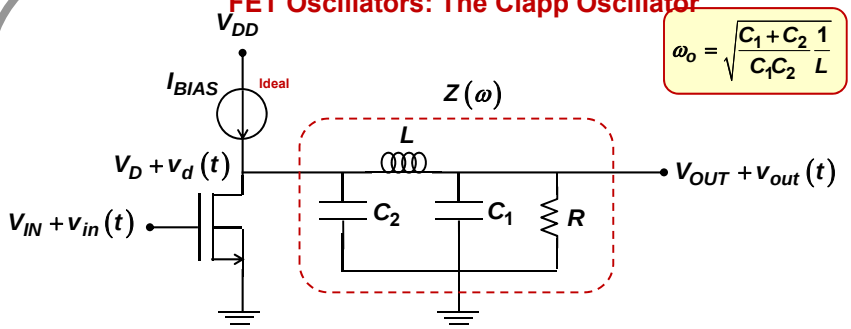
$$v_d(\omega) = -g_m \left(Z(\omega) \,||\, r_o\right) v_{in}(\omega) \approx -g_m Z(\omega) v_{in}(\omega)$$

Resonance at: $\omega_o = \sqrt{\frac{C_1 + C_2}{C_1 C_2} \frac{1}{L}}$

At resonance $|Z(\omega)|$ becomes large!
And the gain is large too!

FET Oscillators: The Clapp Oscillator

$$\omega_o = \sqrt{\frac{C_1 + C_2}{C_1 C_2}\frac{1}{L}}$$

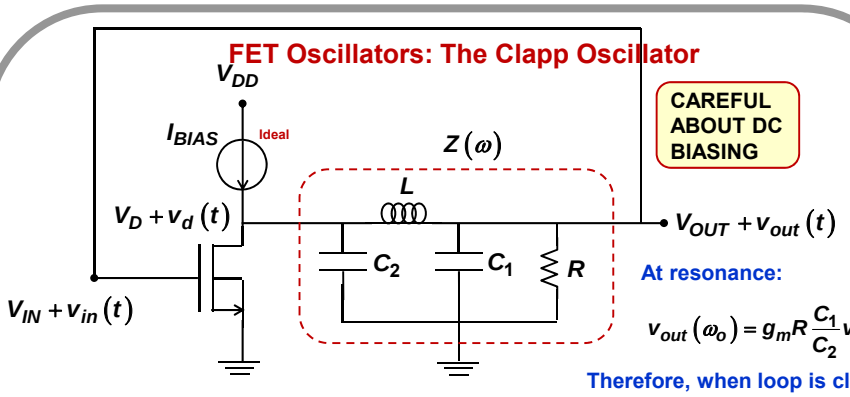


$$v_{out}(\omega) = \frac{\left(R \parallel \frac{1}{j\omega C_1}\right)}{\left(R \parallel \frac{1}{j\omega C_1}\right) + j\omega L} v_d(\omega) = -g_m Z(\omega) \frac{\left(R \parallel \frac{1}{j\omega C_1}\right)}{\left(R \parallel \frac{1}{j\omega C_1}\right) + j\omega L} v_{in}(\omega)$$

$$= \frac{-g_m R}{j\omega(C_1+C_2)R\left[1 - \omega^2 \frac{C_1 C_2}{C_1+C_2} L + \frac{1}{j\omega(C_1+C_2)R} + j\omega \frac{C_2 L}{(C_1+C_2)R}\right]} v_{in}(\omega)$$

At resonance: $v_{out}(\omega_o) = g_m R \frac{C_1}{C_2} v_{in}(\omega_o)$

FET Oscillators: The Clapp Oscillator



CAREFUL ABOUT DC BIASING

At resonance:

$$v_{out}(\omega_o) = g_m R \frac{C_1}{C_2} v_{in}(\omega_o)$$

What if we close the loop!? Would things work out?

Therefore, when loop is closed:

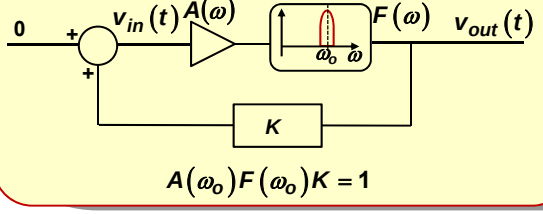
$$v_{out}(\omega_o) = v_{in}(\omega_o)$$

$$\Rightarrow \left[1 - g_m R \frac{C_1}{C_2}\right] v_{out}(\omega_o) = 0$$

Condition for oscillation:

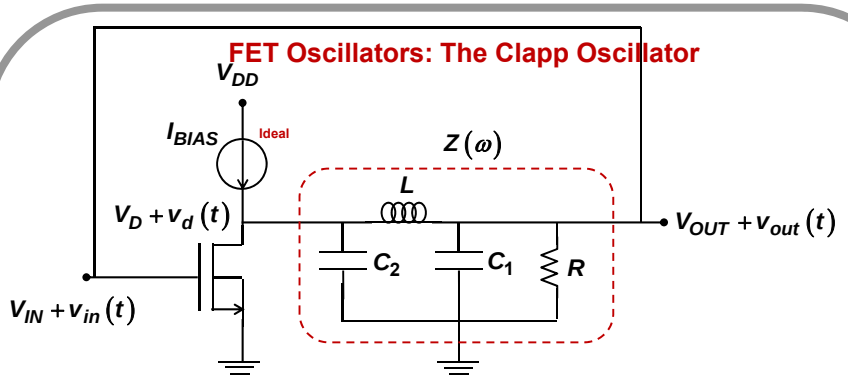
$$g_m R \frac{C_1}{C_2} = 1$$

Compare with:



$$A(\omega_o)F(\omega_o)K = 1$$

FET Oscillators: The Clapp Oscillator



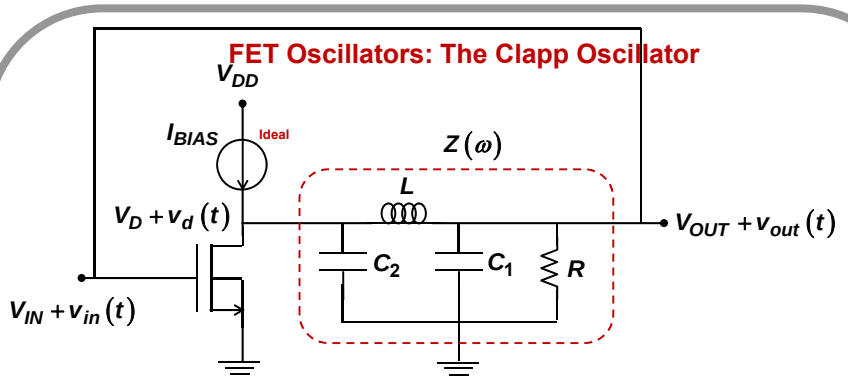
$$v_{out}(\omega) = \frac{-g_m R}{j\omega(C_1+C_2)R\left[1-\omega^2\frac{C_1C_2}{C_1+C_2}L+\frac{1}{j\omega(C_1+C_2)R}+j\omega\frac{C_2L}{(C_1+C_2)R}\right]}v_{in}(\omega)$$

Therefore, when loop is closed, and we have a stable oscillation: $v_{out}(\omega) = v_{in}(\omega)$

$$v_{out}(\omega) = \frac{-g_m R}{j\omega(C_1+C_2)R\left[1-\omega^2\frac{C_1C_2}{C_1+C_2}L+\frac{1}{j\omega(C_1+C_2)R}+j\omega\frac{C_2L}{(C_1+C_2)R}\right]}v_{out}(\omega)$$

$$\Rightarrow \left[j\omega(C_1+C_2)R\left(1-\omega^2\frac{C_1C_2}{C_1+C_2}L\right)+1-\omega^2C_2L+g_mR\right]v_{out}(\omega)=0$$

FET Oscillators: The Clapp Oscillator



$$\left[j\omega(C_1+C_2)R\left(1-\omega^2\frac{C_1C_2}{C_1+C_2}L\right)+1-\omega^2C_2L+g_mR\right]v_{out}(\omega)=0$$

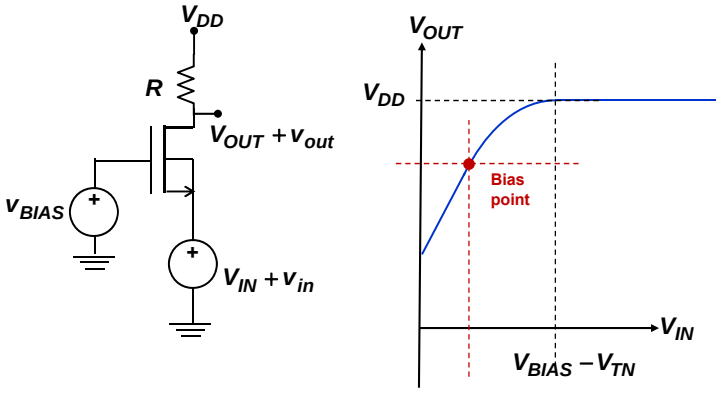
Imaginary part

$$\omega = \sqrt{\frac{C_1+C_2}{C_1C_2}\frac{1}{L}}$$

Real part

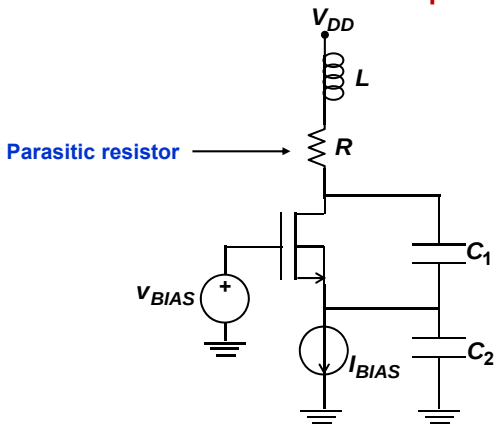
$$g_mR\frac{C_1}{C_2}=1$$

FET Oscillators: Gain Saturation in a CG Amplifier



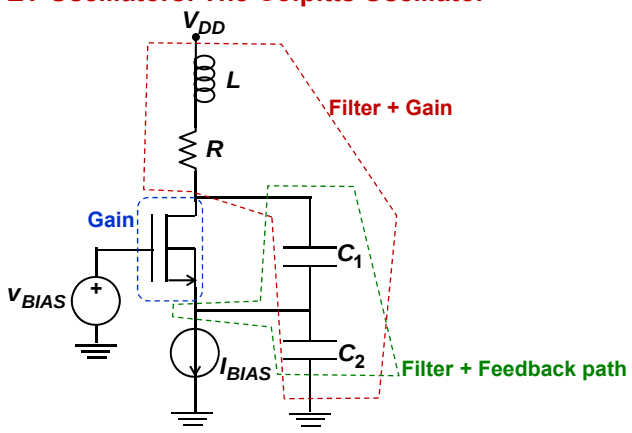
As the input small signal increase increases in strength, the gain experienced by it will decrease

FET Oscillators: The Colpitts Oscillator



A common gate FET stage connected in a positive feedback loop used can be used to realize an oscillator

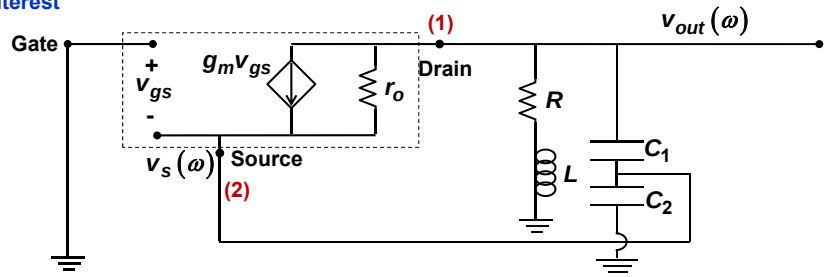
FET Oscillators: The Colpitts Oscillator



A common gate FET stage connected in a positive feedback loop used can be used to realize an oscillator

The Colpitts Oscillator: Small Signal Model

Assume the capacitors internal to the FET, C_{gs} and C_{gd}, are open at the frequencies of interest



KCL at (1):

$$\frac{v_{out}(\omega)}{j\omega L + R} - g_m v_s(\omega) + \frac{v_{out}(\omega) - v_s(\omega)}{r_o} + j\omega C_1\left[v_{out}(\omega) - v_s(\omega)\right] = 0$$

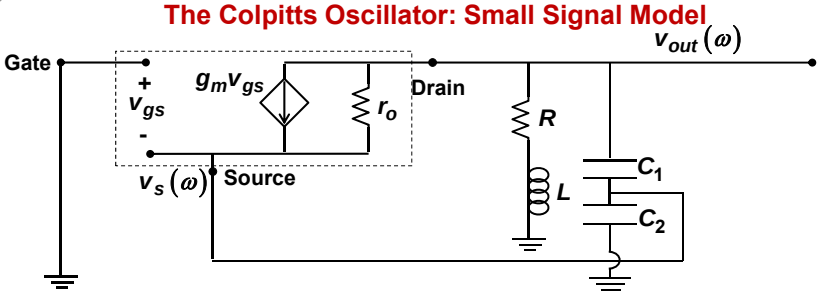
KCL at (2):

$$-j\omega C_2 v_s(\omega) - g_m v_s(\omega) + \frac{v_{out}(\omega) - v_s(\omega)}{r_o} + j\omega C_1\left[v_{out}(\omega) - v_s(\omega)\right] = 0$$

These give:

$$\Rightarrow \frac{v_{out}(\omega)}{j\omega L + R} = -j\omega C_2 v_s(\omega)$$

The Colpitts Oscillator: Small Signal Model



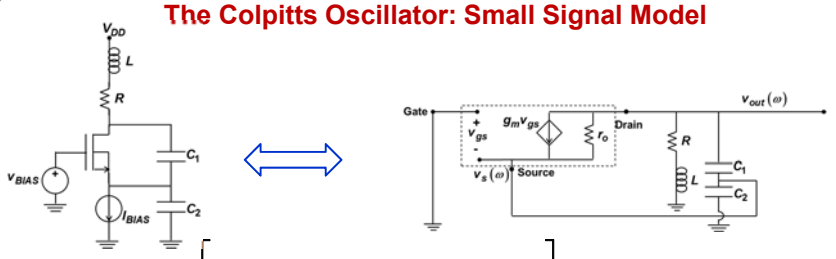
$$\left[j\omega L + \frac{1}{j\omega \dfrac{C_1 C_2}{C_1 + C_2}} + \cancel{\frac{R}{j\omega C_2 r_o}}^{\text{small}} + R - \frac{g_m}{\omega^2 C_1 C_2} + \cancel{\frac{L}{C_2 r_o}}^{\text{small}} \right] v_{out}(\omega) = 0$$

Note: The ignored quantities need not be small

Compare with:

$$\left[1 - KA(\omega)\right] v_{out}(\omega) = 0$$

The Colpitts Oscillator: Small Signal Model



$$\left[j\omega L + \frac{1}{j\omega \dfrac{C_1 C_2}{C_1 + C_2}} + R - \frac{g_m}{\omega^2 C_1 C_2} \right] = 0$$

This implies:

$$j\omega L + \frac{1}{j\omega \dfrac{C_1 C_2}{C_1 + C_2}} = 0$$

$$\Rightarrow \omega = \frac{1}{\sqrt{L C_{eq}}}$$

$$C_{eq} = \frac{C_1 C_2}{C_1 + C_2}$$

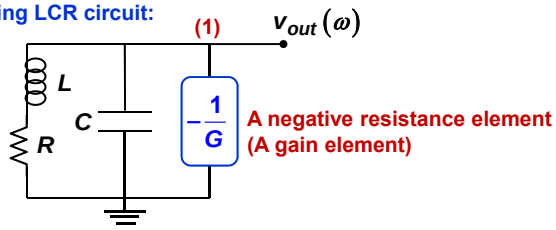
and:

$$R = \frac{g_m}{\omega^2 C_1 C_2} = g_m \frac{L}{C_1 + C_2}$$

The above implies that the FET gain (proportional to g_m) must balance the dissipation due to the resistor R

Electrical Oscillators: Another Viewpoint

Consider the following LCR circuit:



Doing KCL at node (1) gives:

small

$$\left[j\omega L + \frac{1}{j\omega C} - \frac{GR}{j\omega C} + R - G\frac{L}{C}\right] v_{out}(\omega) = 0$$

This implies:

$$j\omega L + \frac{1}{j\omega C} = 0$$

$$\Rightarrow \omega = \frac{1}{\sqrt{LC}}$$

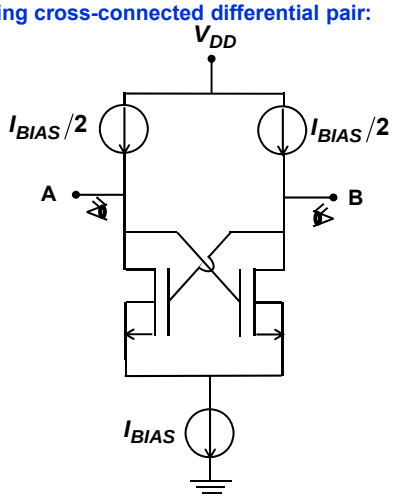
and:

$$R = G\frac{L}{C}$$

The above implies that the gain must balance the dissipation due to the resistor *R*

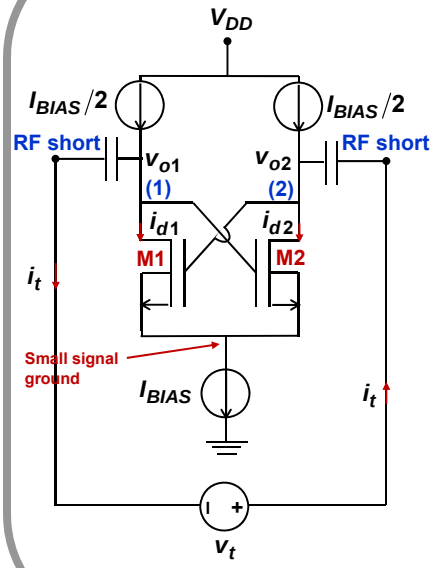
A Differential Pair Negative Resistance Element

Consider the following cross-connected differential pair:



Suppose we find the small signal resistance looking into the terminals A and B .....

A Differential Pair Negative Resistance Element



Forget the output conductance of the FETs for now

We have:

$$v_{o2} - v_{o1} = v_t$$

$$v_{gs1} - v_{gs2} = v_t = v_{id}$$

Therefore:

$$i_{d1} = g_m \frac{v_t}{2}$$

$$i_{d2} = -g_m \frac{v_t}{2}$$

And KCL gives at (1) and (2):

$$i_{d1} + i_t = 0$$

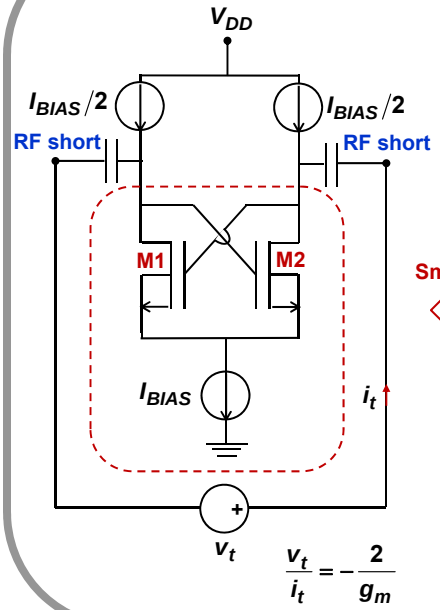
$$i_{d2} - i_t = 0$$

Therefore:

$$\frac{v_t}{i_t} = -\frac{2}{g_m}$$

Negative !!

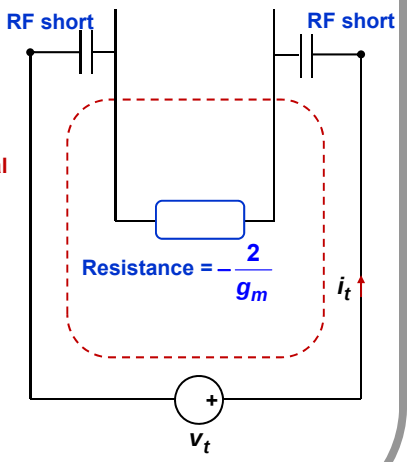
A Differential Pair Negative Resistance Element



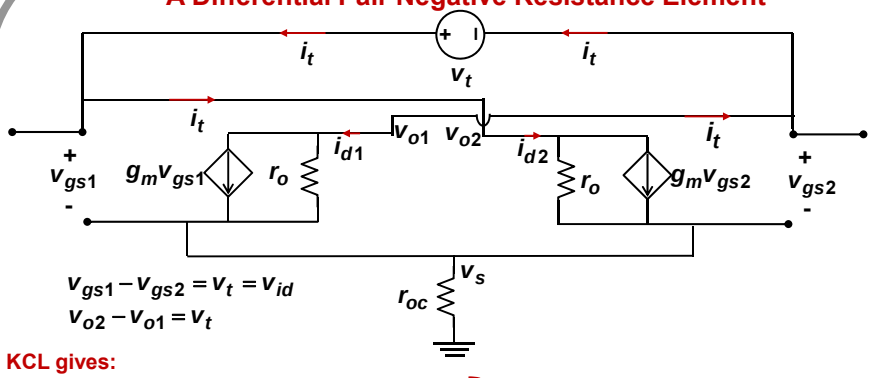
$$\frac{v_t}{i_t} = -\frac{2}{g_m}$$

Small signal

Equivalent small signal model



A Differential Pair Negative Resistance Element



KCL gives:

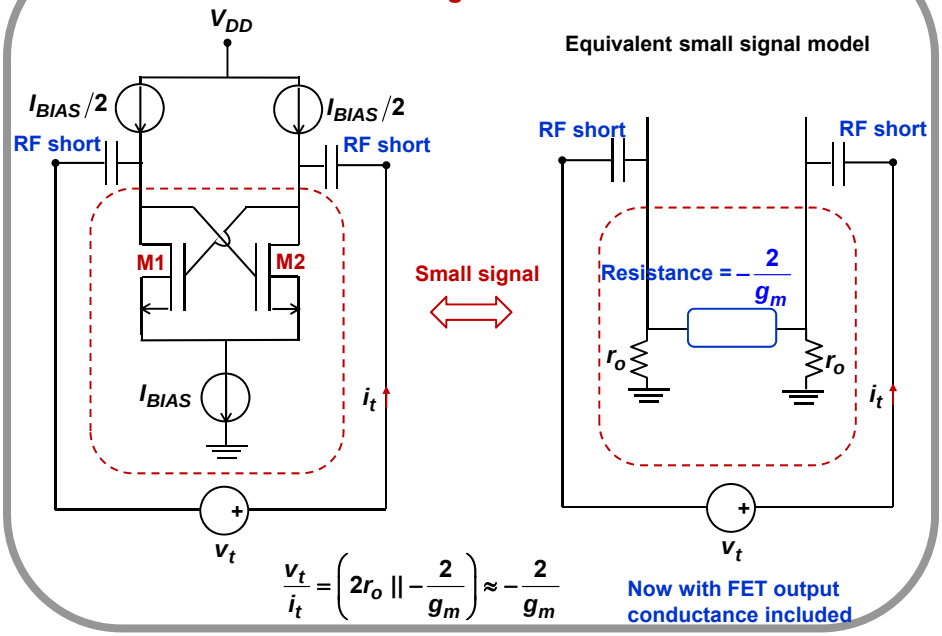
$$g_m v_{gs1} + g_o\left(v_{o1} - v_s\right) + i_t = 0$$
$$g_m v_{gs2} + g_o\left(v_{o2} - v_s\right) - i_t = 0$$

Subtracting the two gives:

$$g_m v_t - g_o v_t + 2i_t = 0$$

$$g_m v_t + g_o v_t + 2i_t = 0$$
$$\Rightarrow \frac{v_t}{i_t} = \frac{2}{\left(-g_m + g_o\right)} = \left(\frac{-2}{g_m} \| 2r_o\right)$$

A Differential Pair Negative Resistance Element

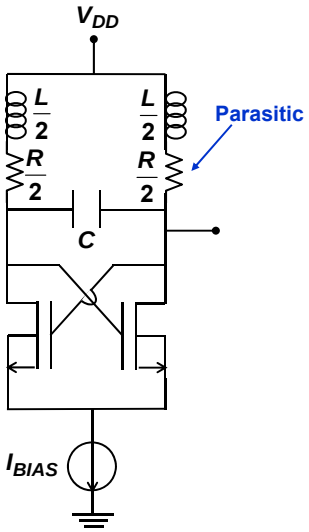


$$\frac{v_t}{i_t} = \left(2r_o \| -\frac{2}{g_m}\right) \approx -\frac{2}{g_m}$$

Now with FET output conductance included

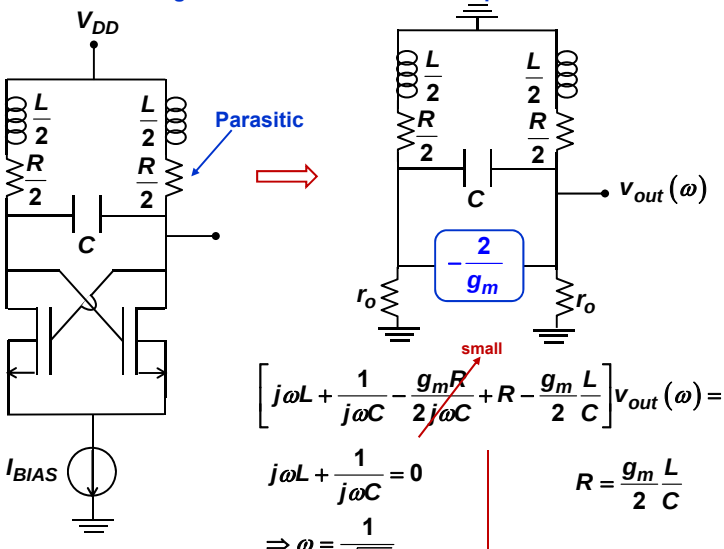
A Differential Pair Oscillator

Consider the following cross-connected differential pair:



A Differential Pair Oscillator

Consider the following cross-connected differential pair:



$g_m r_o >> 1$

small

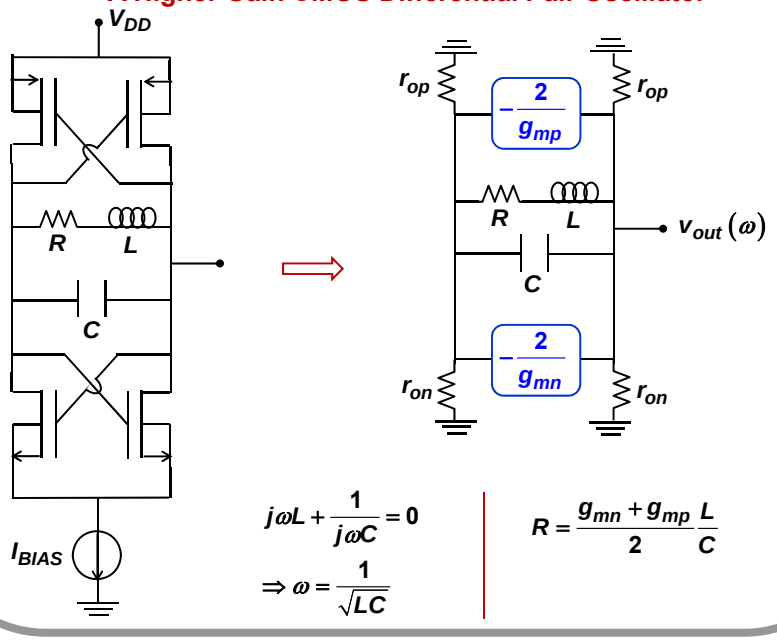
$$\left[j\omega L + \frac{1}{j\omega C} - \frac{g_m R}{2 j\omega C} + R - \frac{g_m}{2}\frac{L}{C} \right] v_{out}(\omega) = 0$$

$$j\omega L + \frac{1}{j\omega C} = 0$$

$$\Rightarrow \omega = \frac{1}{\sqrt{LC}}$$

$$R = \frac{g_m}{2}\frac{L}{C}$$

A Higher Gain CMOS Differential Pair Oscillator

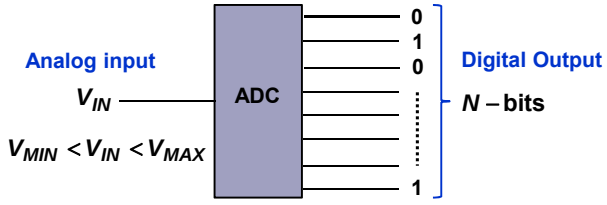


$$j\omega L + \frac{1}{j\omega C} = 0$$

$$\Rightarrow \omega = \frac{1}{\sqrt{LC}}$$

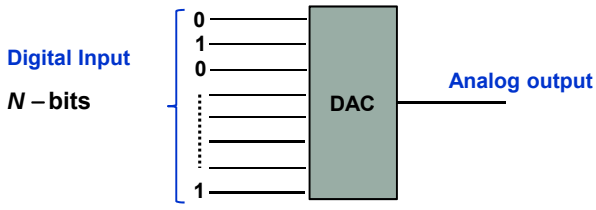
$$R = \frac{g_{mn} + g_{mp}}{2}\frac{L}{C}$$

Analog-to-Digital Converters(ADCs) and Digital-to-Analog Converters (DACs)

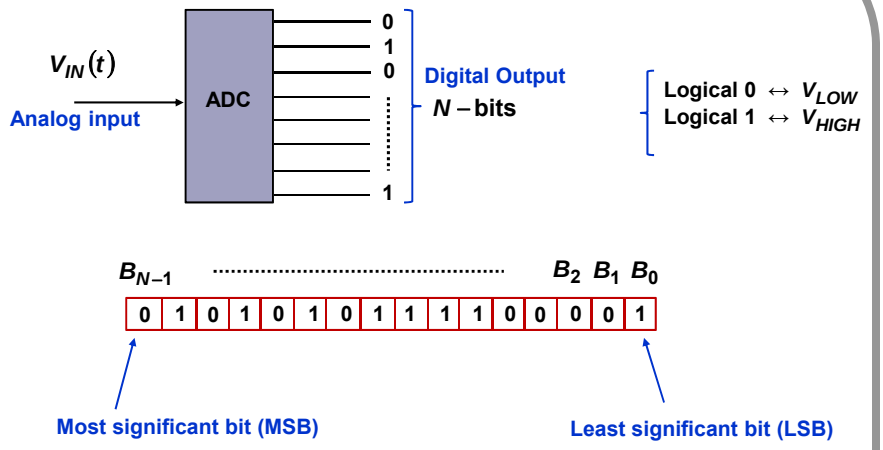


Resolution: $\frac{|V_{MAX} - V_{MIN}|}{2^N - 1}$

Dynamic Range: $20\log_{10}\left(\frac{|V_{MAX}|}{|V_{MIN}|}\right)$



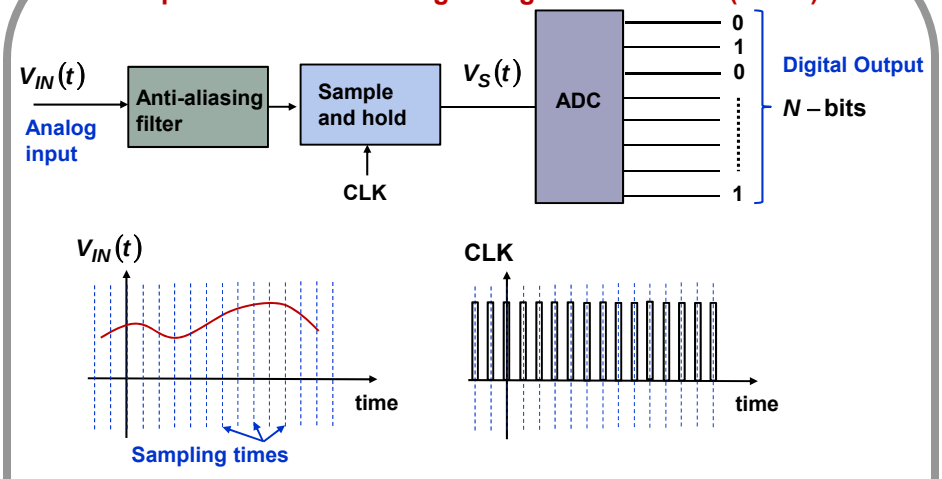
Analog-to-Digital Converters (ADCs)



Analog value, corresponding to a digital value, is:

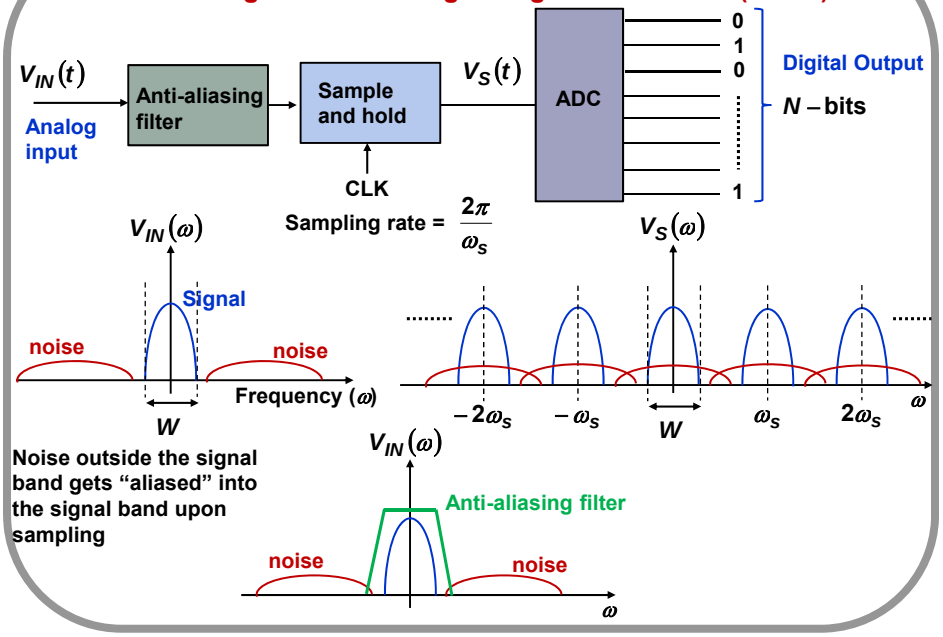
$$V_{MIN} + \frac{(V_{MAX} - V_{MIN})}{(2^N - 1)}\left[2^{N-1}B_{N-1} + 2^{N-2}B_{N-2} + ...2^2 B_2 + 2^1 B_1 + B_0\right]$$

Sample and Hold in Analog-to-Digital Converters (ADCs)

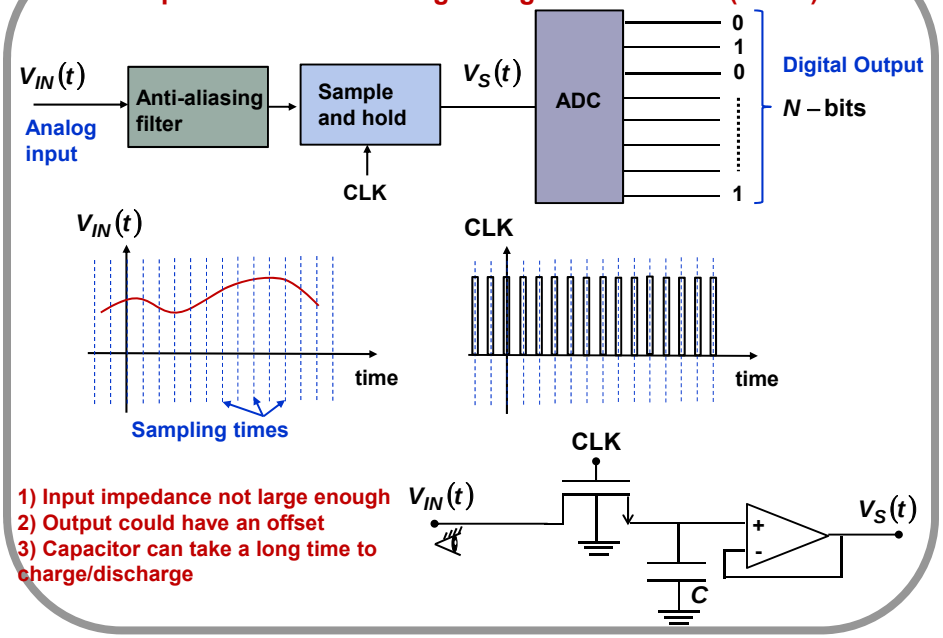


Sample the input waveform periodically and hold the sampled value in place till the next sampling event

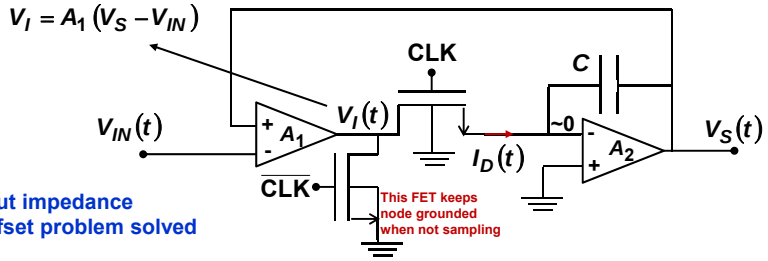
Anti-Aliasing Filter in Analog-to-Digital Converters (ADCs)



Sample and Hold in Analog-to-Digital Converters (ADCs)



A Better Sample and Hold Circuit



Large input impedance
Output offset problem solved

Suppose when the CLK is HIGH the current through the FET is (assuming linear region):

$$I_D = k_n\left(V_{GS} - V_{TN} - \frac{V_{DS}}{2}\right)V_{DS} \approx k_n(V_{CLK} - V_{TN})V_I = \frac{V_I}{R_n}$$

(V_{DS} small)

Then:

$$C\frac{d(0 - V_S)}{dt} = I_D = \frac{V_I}{R_n} = \frac{A_1(V_S - V_{IN})}{R_n}$$

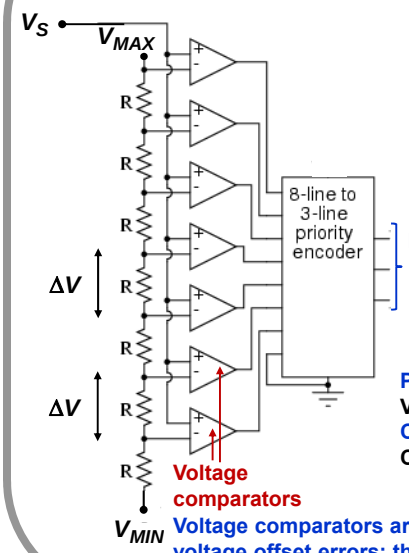
$$\Rightarrow \frac{dV_S}{dt} + \frac{A_1}{R_nC}V_S = \frac{A_1}{R_nC}V_{IN}$$

$$\Rightarrow V_S(t) = V_S(0)e^{-\frac{A_1}{R_nC}t} + V_{IN}\left(1 - e^{-\frac{A_1}{R_nC}t}\right)$$

V_S is pulled to V_{IN} and V_I is pulled to ~0 V within a very short time after CLK goes HIGH

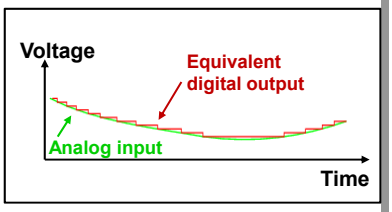
Flash Analog-to-Digital Converters (ADCs)

3-bit Flash ADC



Voltage resolution:

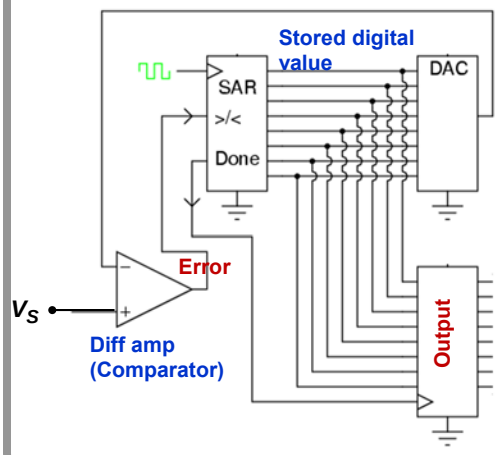
$$\Delta V = \frac{V_{MAX} - V_{MIN}}{2^N - 1}$$



Pros:
Very high speed architecture
Cons:
Component intensive (requires 2^N-1 comparators)

Voltage comparators are essentially diff amps that have very low voltage offset errors; the input voltage offset error needs to be much less than the resolution of the ADC

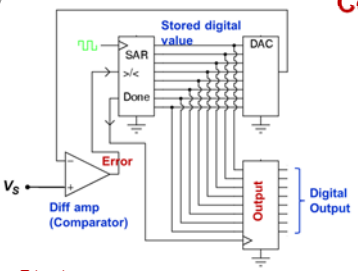
Successive Approximation Register (SAR) Analog-to-Digital Converters (ADCs)



Internal register keeps updating the stored digital value, compares the resulting analog value obtained from this digital value to the input analog value, until the stored value matches the input value

And then the stored value is placed in the output register

Successive Approximation Register (SAR) Analog-to-Digital Converters (ADCs)



Consider a 4-bit SAR-ADC with a 0-3 V input range

0000 => 0 Volts 1111 => 3 Volts

Resolution = 0.2 Volt

Suppose the input is 1.70 Volts

Start

SAR = 1000 → DAC = 1.60 V → Error = +1 → Stored value is smaller

SAR = 1111 → DAC = 3.00 V → Error = -1 → Stored value is larger

SAR = 1100 → DAC = 2.40 V → Error = +1 → Stored value is larger

SAR = 1010 → DAC = 2.00 V → Error = +1 → Stored value is larger

SAR = 1001 → DAC = 1.80 V → Error = +1 → Stored value is larger

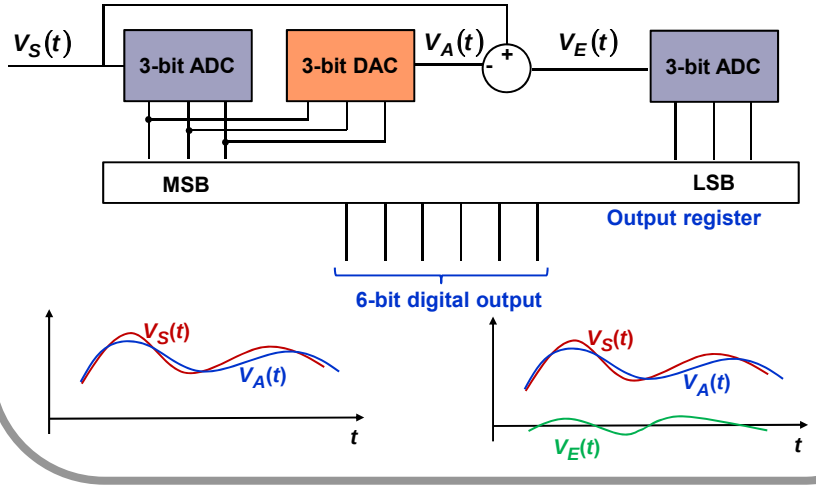
Produce output

Pros: Scalable to high resolutions Cons: Slower than flash

Pipelined Analog-to-Digital Converters (ADCs)

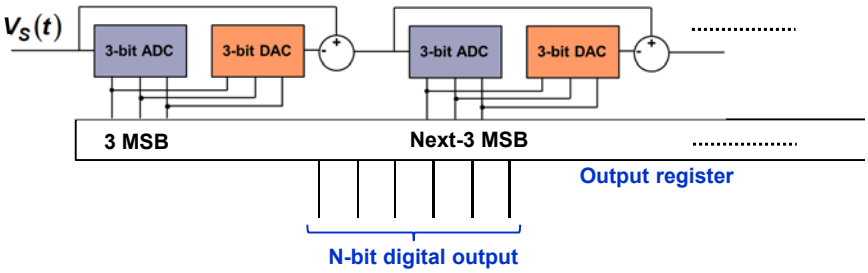
Main Idea: Use features of the flash architecture but scale to higher resolutions

Example: Build a 6-bit pipelined ADC from two 3-bit Flash ADCs



Pipelined Analog-to-Digital Converters (ADCs)

Can easily generalize:

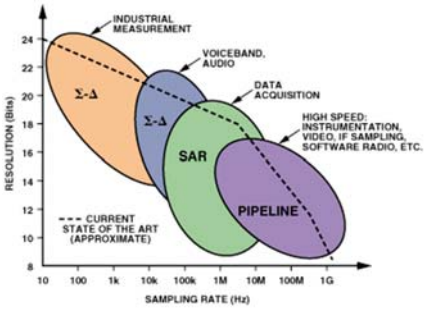


Pros:
Scalable to high resolutions
Fast

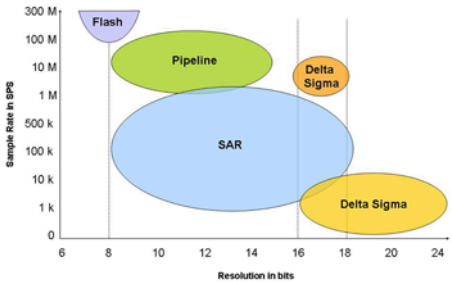
Cons:
Large power dissipation

Analog-to-Digital Converters (ADCs): State of the Art

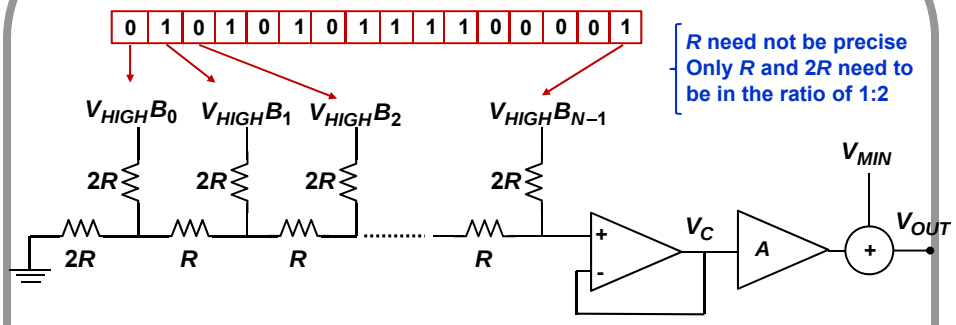
Walt Kester, Analog devices (2005)



William Klein, Texas Instruments (2007)



R/2R Ladder Digital-to-Analog Converters (DACs)



$$V_C = V_{HIGH}\left\{\frac{B_{N-1}}{2}+\frac{B_{N-2}}{4}+\frac{B_{N-3}}{8}+\ldots\ldots\ldots\frac{B_2}{2^{N-2}}+\frac{B_1}{2^{N-1}}+\frac{B_0}{2^N}\right\}$$

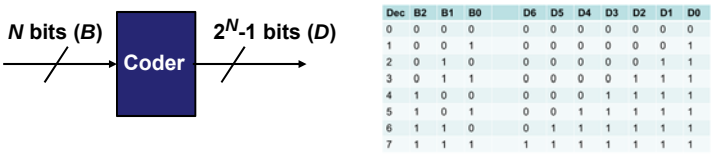
If:

$$A=\frac{(V_{MAX}-V_{MIN})}{2^N-1}\frac{2^N}{V_{HIGH}}$$

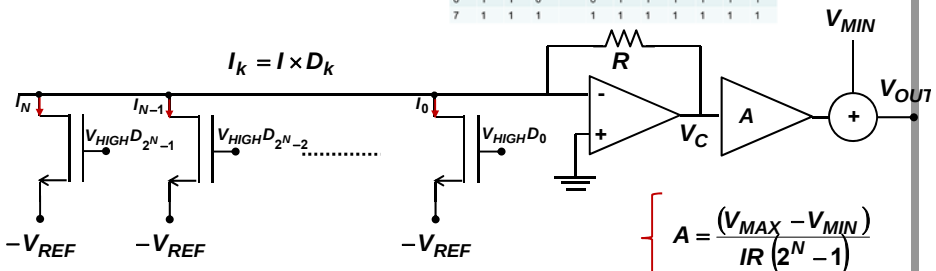
Then the output will be the desired analog output:

$$V_{OUT}=V_{MIN}+\frac{(V_{MAX}-V_{MIN})}{(2^N-1)}\left[2^{N-1}B_{N-1}+2^{N-2}B_{N-2}+\ldots\ldots 2^2B_2+2^1B_1+B_0\right]$$

Thermometer Code Digital-to-Analog Converters (DACs)



Dec	B2	B1	B0	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	0	0	0
1	0	0	1	0	0	0	0	0	0	1
2	0	1	0	0	0	0	0	0	1	1
3	0	1	1	0	0	0	0	1	1	1
4	1	0	0	0	0	0	1	1	1	1
5	1	0	1	0	0	1	1	1	1	1
6	1	1	0	0	1	1	1	1	1	1
7	1	1	1	1	1	1	1	1	1	1



$$A = \frac{(V_{MAX} - V_{MIN})}{IR\left(2^N - 1\right)}$$

$$V_C = IR\left(D_{2^N-1} + D_{2^N-2} + \ldots\ldots\ldots + D_1 + D_0\right)$$

$$V_C = IR\left[2^{N-1}B_{N-1} + 2^{N-2}B_{N-2} + \ldots\ldots + 2^2 B_2 + 2^1 B_1 + B_0\right]$$

$$V_{OUT} = V_{MIN} + \frac{(V_{MAX} - V_{MIN})}{\left(2^N - 1\right)}\left[2^{N-1}B_{N-1} + 2^{N-2}B_{N-2} + \ldots\ldots 2^2 B_2 + 2^1 B_1 + B_0\right]$$

Wireless Communications