Lecture 13

Biasing and Loading Single Stage FET Amplifiers

The Building Blocks of Analog Circuits - III

In this lecture you will learn:

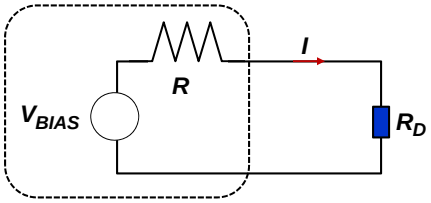
- Current biasing of circuits
- Current sources and sinks for CS, CG, and CD circuits

A Poor Man's Current Source

What if one wanted to bias a device with a current source?

.....but one only had a voltage source?

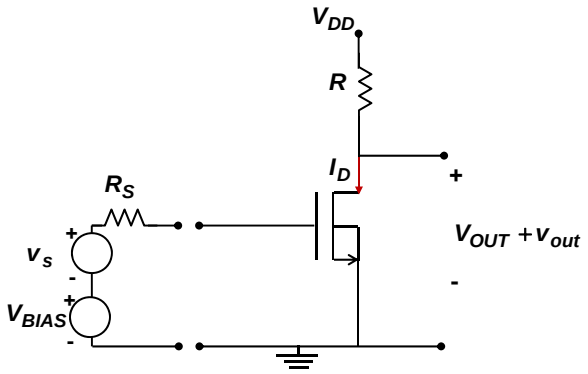
Solution: Use a large voltage source with a large resistor in series!



Poor man's current source

$$I = \frac{V_{BIAS}}{R + R_D} \approx \frac{V_{BIAS}}{R}$$

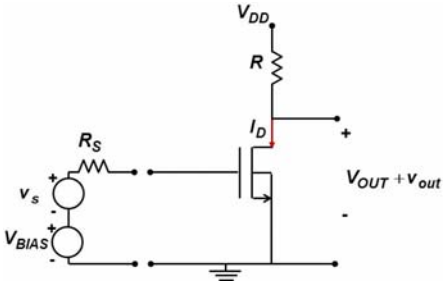
The Common Source Amplifier



Open circuit voltage gain:

$$A_v = \frac{v_{out}}{v_{in}} = -\frac{i_d R}{v_{in}} = -g_m (r_o \,||\, R)$$

The Common Source Amplifier: Problems



Open circuit voltage gain:

$$A_v = \frac{v_{out}}{v_{in}} = -g_m (r_o \,||\, R)$$

In saturation:

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \sqrt{2k_n I_D (1 + \lambda_n V_{DS})}$$

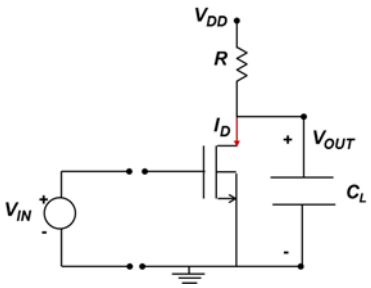
To achieve large gain one needs:

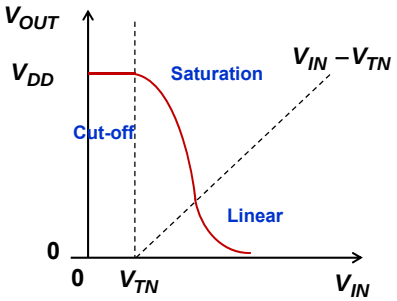
1) A large DC current bias I_D in order to get a large g_m
2) A large value of the resistor R

Both the above requirements cannot be met easily simultaneously:

- Not easy to realize large resistors in micro-chips
- A large resistor R will limit the maximum value of the DC current bias I_D (because the potential drop $I_D R$ can become large enough to put the FET in the linear region where g_m and the gain will be small)

The Digital Logic Inverter: Problems





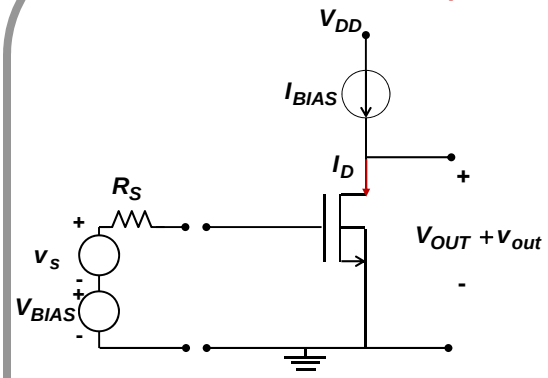
To achieve fast switching one needs:

1) A small resistor (because then the RC_L charging time will be smaller when the output switches from "0" to "1")

But

- A small resistor will require a very large current (to achieve a large potential drop across it) when the input is "1", and the NFET is turned on, and the output need to be low or "0" – and this means more power dissipation
- When the input is "1", and the NFET is turned on, there is constant static power dissipation

The Common Source Amplifier with a Current Source



What is needed is an ideal current source in the drain that can supply a large DC current and at the same time has a large small signal resistance

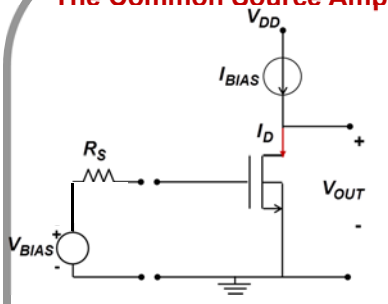
The incremental (or differential or small signal) resistance looking into an ideal current source is infinite

$$A_v = \frac{v_{out}}{v_{in}} = -g_m r_o$$

An ideal current source, of course, does not exist

But one can certainly do much better than using a resistor in the drain

The Common Source Amplifier with a Current Source: DC Biasing



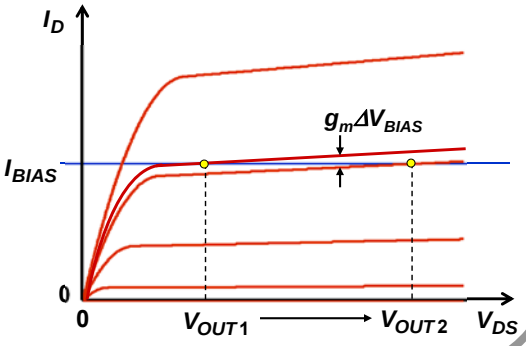
$$I_D = I_{BIAS} = \frac{W}{2L}\mu_n C_{ox}(V_{GS} - V_{TN})^2(1+\lambda_n V_{DS})$$

Suppose for V_{BIAS1} the output was V_{OUT1}

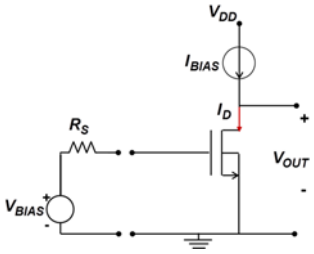
Suppose V_{BIAS1} is changed to a smaller value V_{BIAS2}

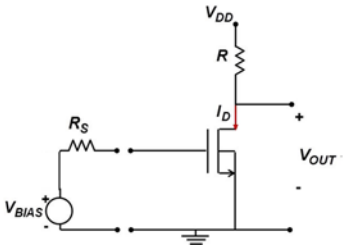
$$\Delta V_{BIAS} = V_{BIAS2} - V_{BIAS1} < 0$$

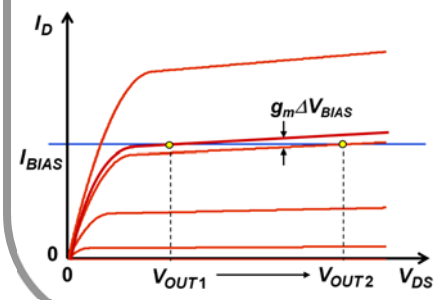
The output V_{OUT2} can be obtained graphically, as shown

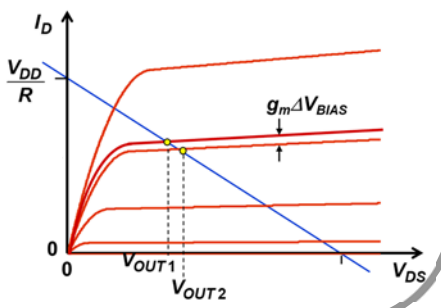


The Common Source Amplifier with a Current Source: DC Biasing

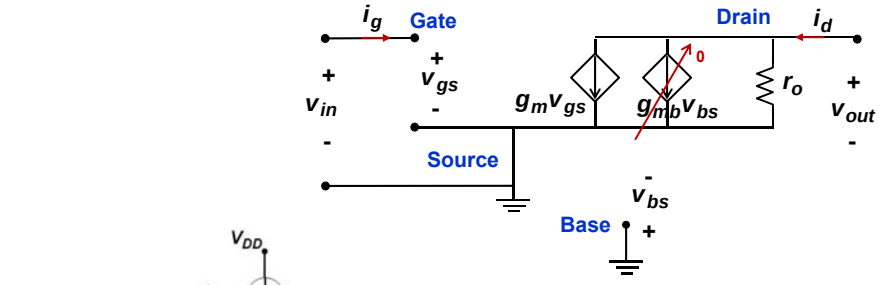


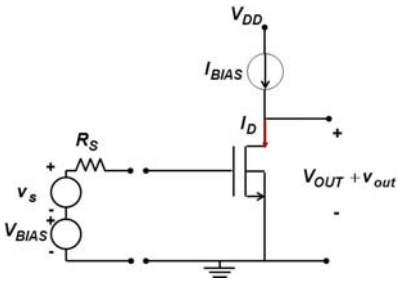






The CS Amplifier with a Current Source: Small Signal Analysis





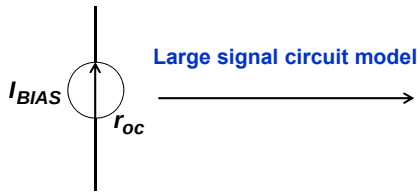
Open circuit voltage gain:

$$A_v = \frac{v_{out}}{v_{in}} = -g_m r_o \longrightarrow \text{Large}$$

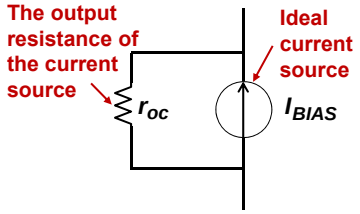
Output resistance:

$$R_{out} = r_o \longrightarrow \text{Large}$$

Large Signal Model of a Current Source

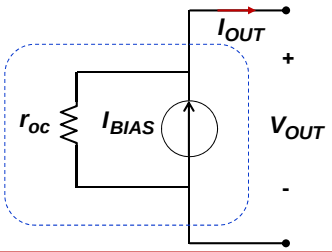


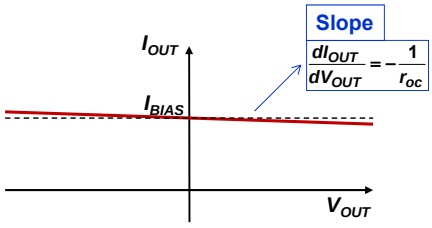
Large signal circuit model



A current source

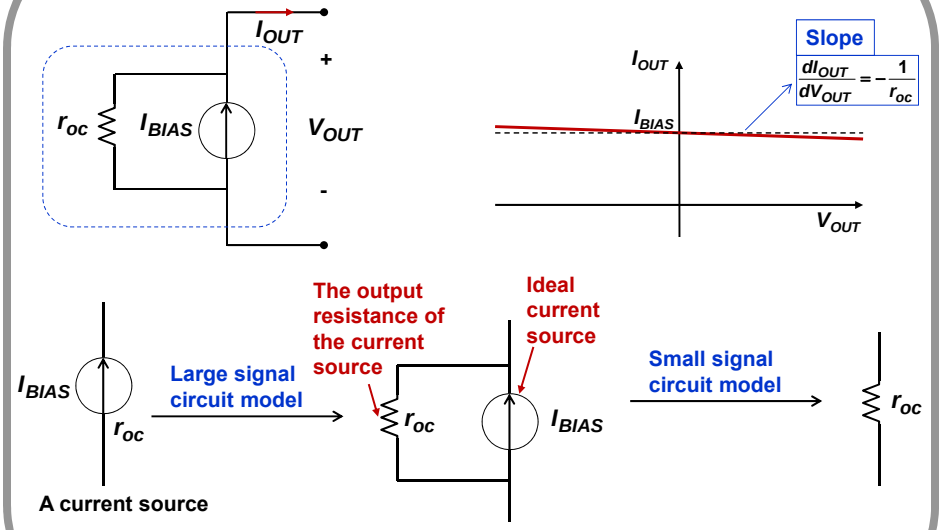
- A large signal model of a current source
- r_{oc} is large for a good current source and infinite for an ideal current source



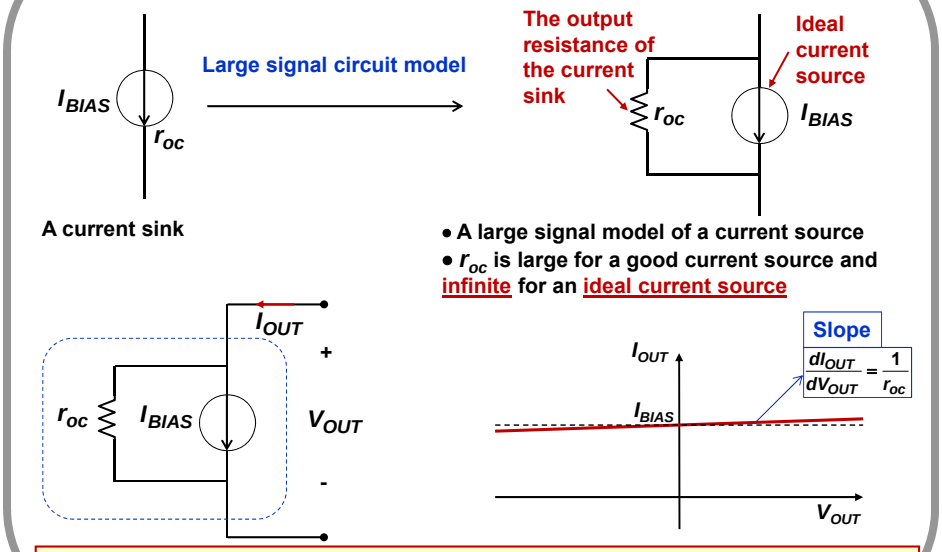


One can have any voltage at the at the output terminals of a good current source and the current delivered will remain mostly constant

Small Signal Model of a Current Source



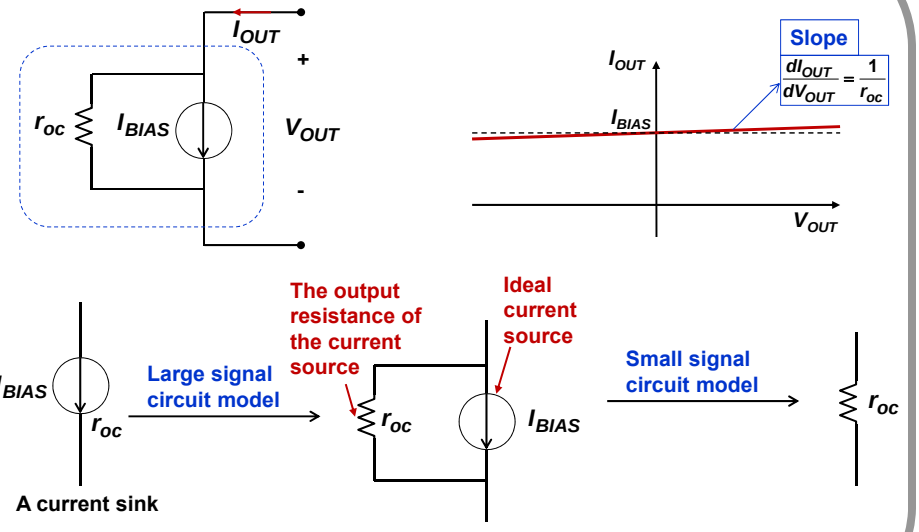
Large Signal Model of a Current Sink



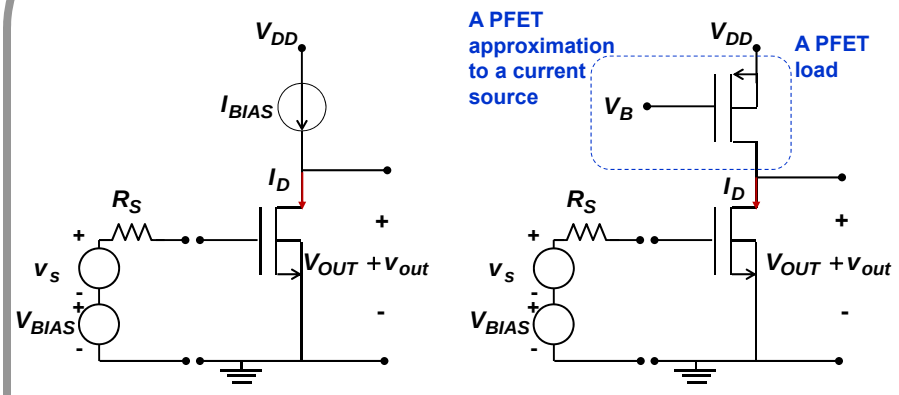
- A large signal model of a current source
- r_{oc} is large for a good current source and infinite for an ideal current source

One can have any voltage at the at the output terminals of a good current sink and the current dinked will remain mostly constant

Small Signal Model of a Current Sink



PFET Loaded NFET Common Source Amplifier



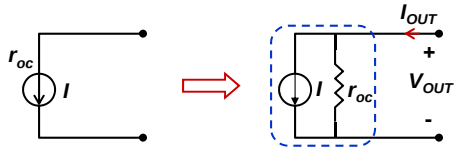
An ideal current source, of course, does not exist

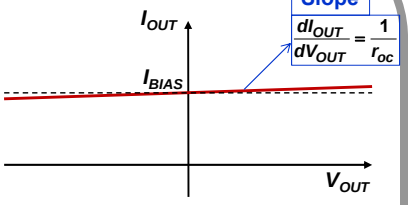
But one can certainly do much better than using a resistor in the drain

Use a PFET!

Current Sinks and NFET Transistors

Current Sink:

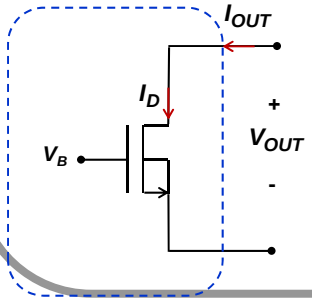


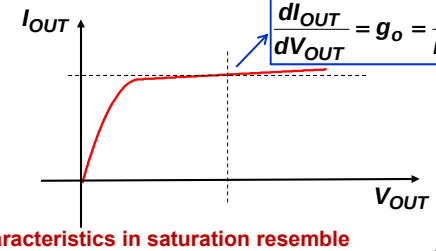


Slope

$$\frac{dI_{OUT}}{dV_{OUT}} = \frac{1}{r_{oc}}$$

One can have any voltage at the at the output terminals of a good current sink and the current sinked will remain mostly constant





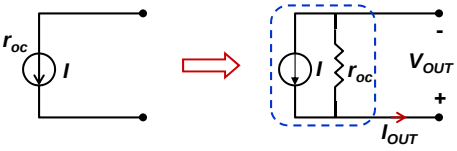
Slope

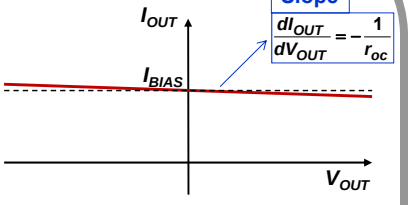
$$\frac{dI_{OUT}}{dV_{OUT}} = g_o = \frac{1}{r_o}$$

Characteristics in saturation resemble that of a non-ideal current source!

Current Sources and PFET Transistors

Current Sources:

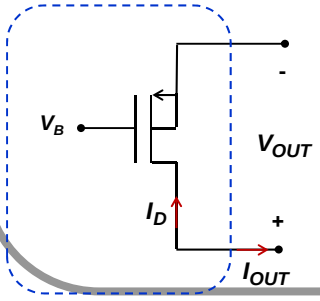


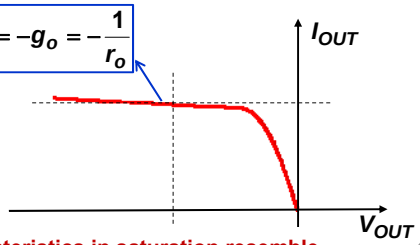


Slope

$$\frac{dI_{OUT}}{dV_{OUT}} = -\frac{1}{r_{oc}}$$

One can have any voltage at the at the output terminals of a good current source and the current delivered will remain mostly constant



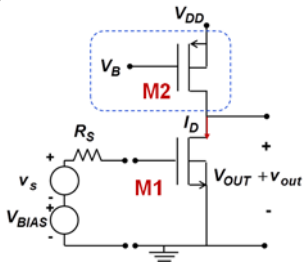


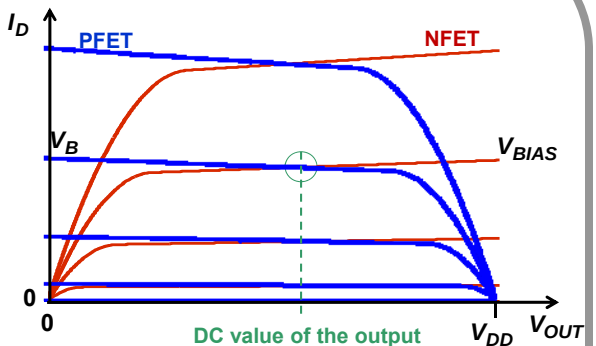
Slope

$$\frac{dI_{OUT}}{dV_{OUT}} = -g_o = -\frac{1}{r_o}$$

Characteristics in saturation resemble that of a non-ideal current source!

PFET Loaded NFET: Large Signal Analysis





$V_{DS1} = V_{OUT}$

$V_{DS2} = V_{OUT} - V_{DD}$

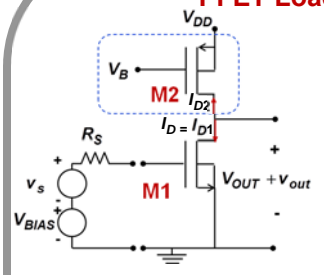
$I_{D1} = I_D = -I_{D2}$

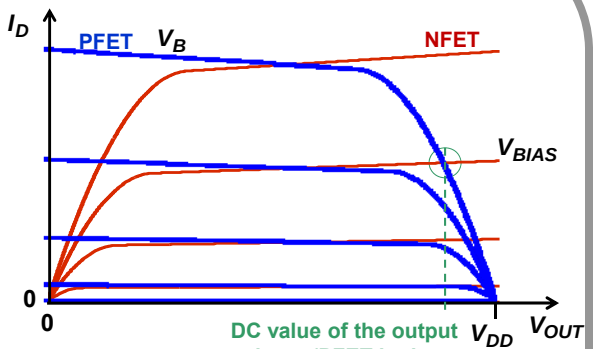
DC value of the output voltage (Both FETs in saturation)

Instead of the resistive load line, we now have the full I_D vs V_{DS} curves of the PFET

The biasing voltages need to be selected carefully, otherwise one of the transistors can go into the linear region!!

PFET Loaded NFET: Large Signal Analysis





$V_{DS1} = V_{OUT}$

$V_{DS2} = V_{OUT} - V_{DD}$

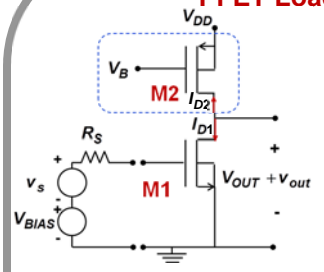
$I_{D1} = I_D = -I_{D2}$

DC value of the output voltage (PFET in the linear region)

Instead of the resistive load line, we now have the full I_D vs V_{DS} curves of the PMOS

The biasing voltages need to be selected carefully, otherwise one of the transistors can go into the linear region!!

PFET Loaded NFET: Large Signal Analysis



Assuming the biasing is correct, both the FETs are in saturation

Equate the drain current magnitudes of the two FETs

Then the only unknown will be V_{OUT} ; solve for it

Verify that the obtained value of V_{OUT} does indeed result in both the transistors being in saturation

NFET

$$I_{D1} = \frac{k_n}{2}(V_{GS1} - V_{TN})^2(1+\lambda_n V_{DS1}) = \frac{k_n}{2}(V_{BIAS} - V_{TN})^2(1+\lambda_n V_{OUT})$$

PFET

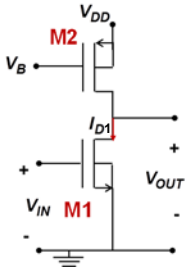
$$I_{D2} = -\frac{k_p}{2}(V_{GS2} - V_{TP})^2(1-\lambda_p V_{DS2}) = -\frac{k_p}{2}(V_B - V_{DD} - V_{TP})^2(1-\lambda_p(V_{OUT} - V_{DD}))$$

Equating:

$$I_{D1} = I_D = -I_{D2}$$

$$\Rightarrow \frac{k_n}{2}(V_{BIAS} - V_{TN})^2(1+\lambda_n V_{OUT}) = \frac{k_p}{2}(V_B - V_{DD} - V_{TP})^2(1+\lambda_p(V_{DD} - V_{OUT}))$$

PFET Loaded NFET: Transfer Curve

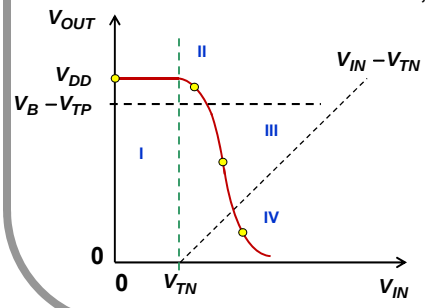


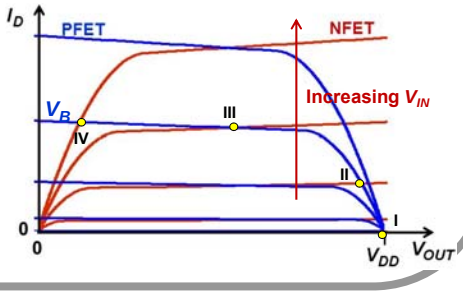
I: $V_{IN} < V_{TN}$
M1 cut-off

II: $V_{IN} > V_{TN}$ & $V_{OUT} > V_{IN} - V_{TN}$ & $V_{OUT} > V_B - V_{TP}$
M1 saturation, M2 Linear

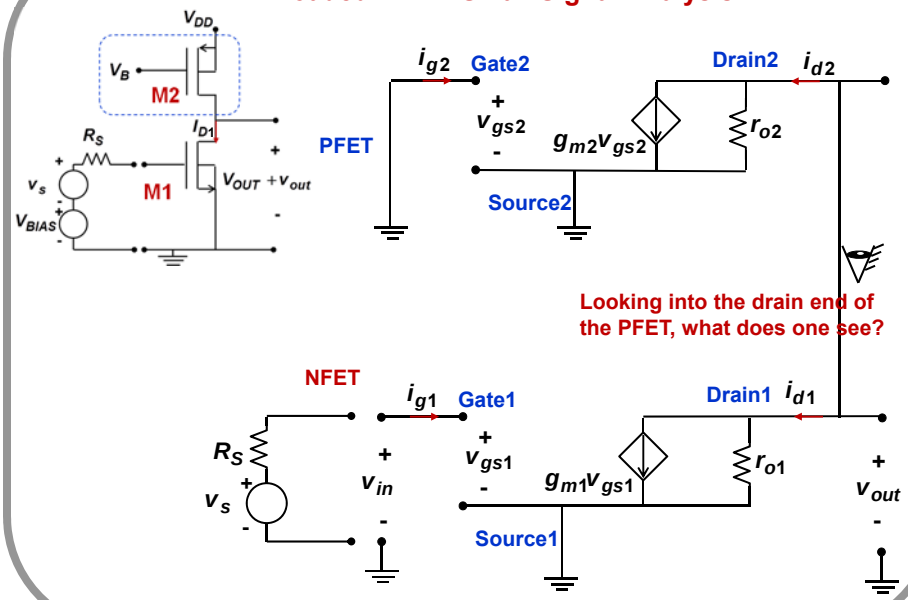
III: $V_{IN} > V_{TN}$ & $V_{OUT} > V_{IN} - V_{TN}$ & $V_{OUT} < V_B - V_{TP}$
M1 saturation, M2 saturation

IV: $V_{IN} > V_{TN}$ & $V_{OUT} < V_{IN} - V_{TN}$ & $V_{OUT} < V_B - V_{TP}$
M1 linear, M2 saturation

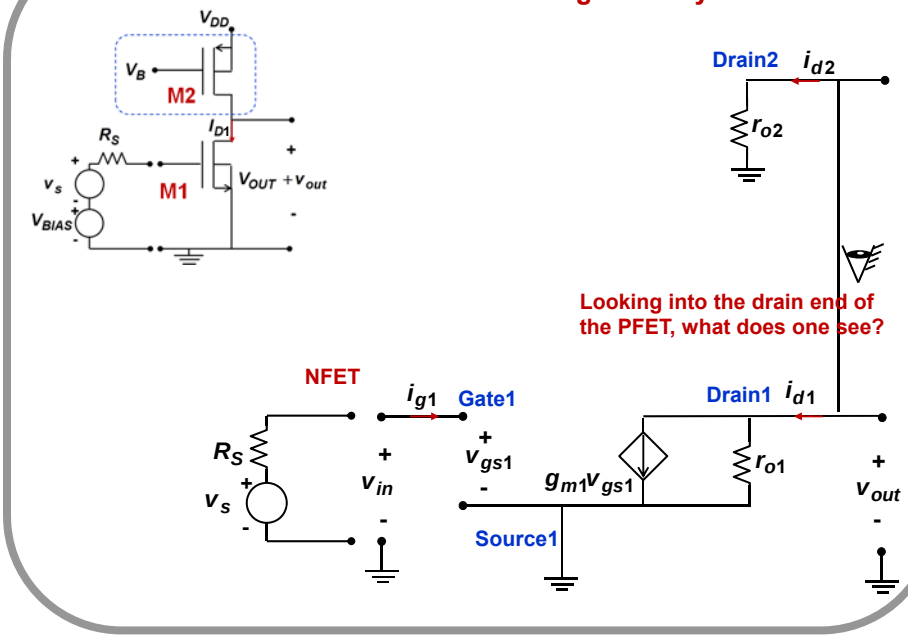




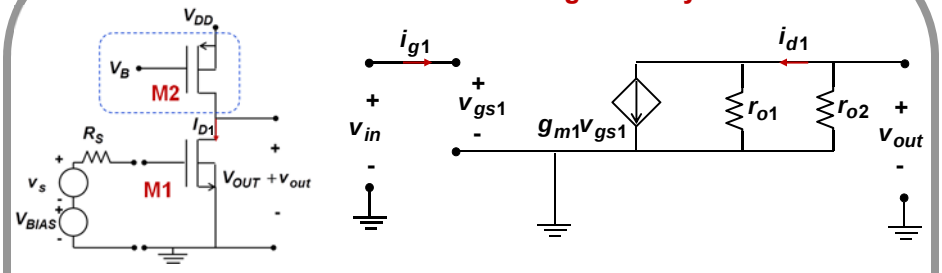
PFET Loaded NFET: Small Signal Analysis



PMOS Loaded NMOS: Small Signal Analysis



PFET Loaded NFET: Small Signal Analysis



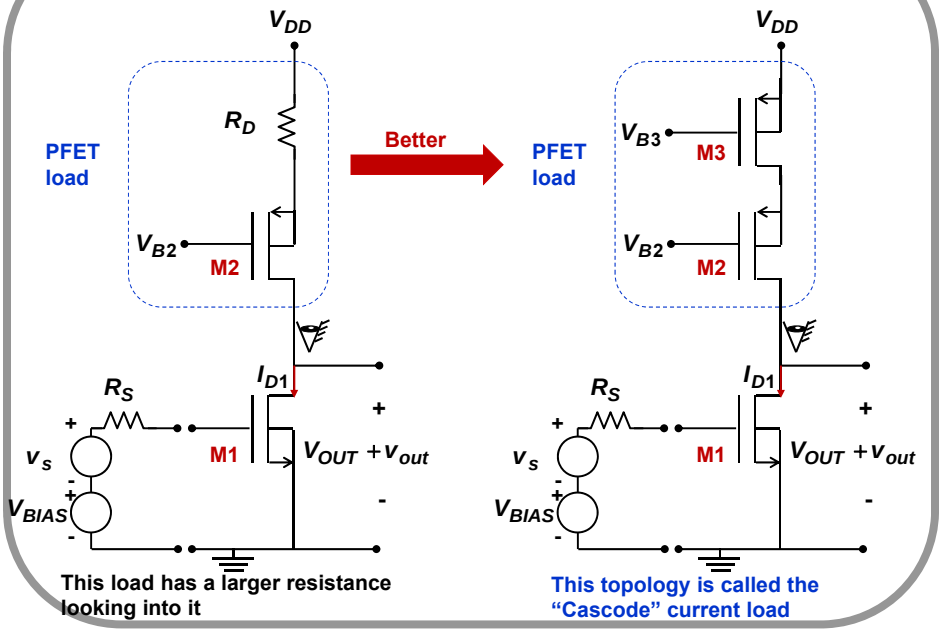
Open circuit voltage gain:

$$A_v = \frac{v_{out}}{v_{in}} = -g_{m1}(r_{o1} \| r_{o2})$$

Output resistance:

$$R_{out} = r_{o1} \| r_{o2}$$

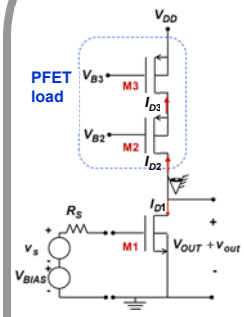
PFET Loaded NFET: The Cascode PFET Load

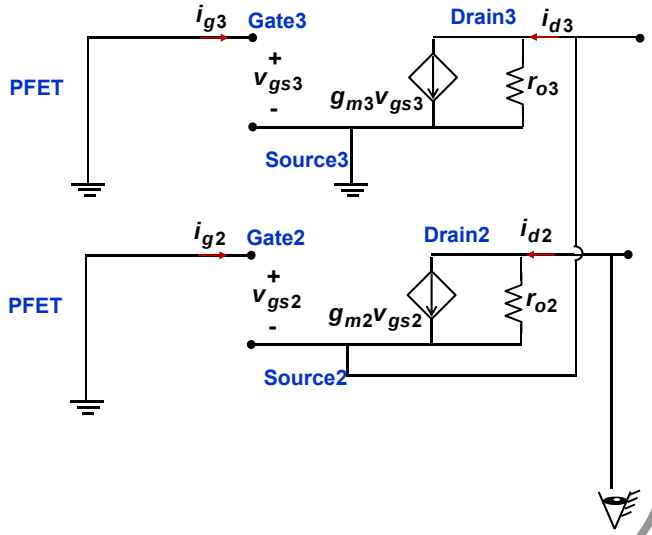


This load has a larger resistance looking into it

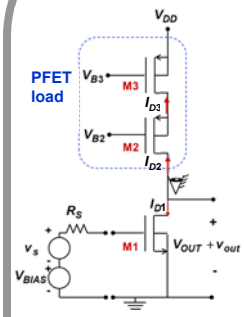
This topology is called the "Cascode" current load

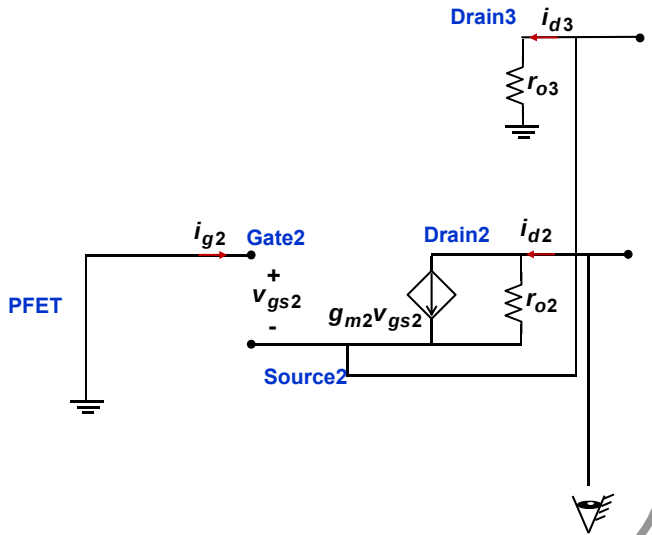
Cascode PEFT Load: Small Signal Analysis



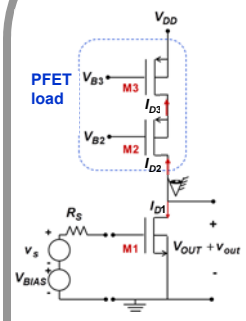


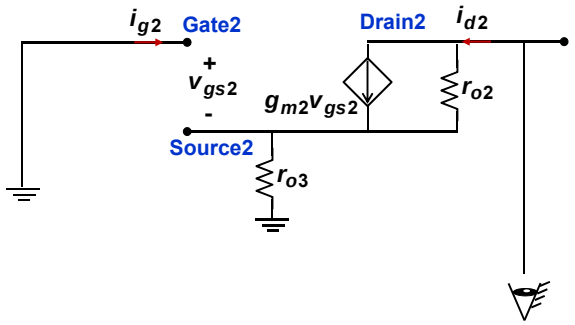
Cascode PFET Load: Small Signal Analysis





Cascode PFET Load: Small Signal Analysis



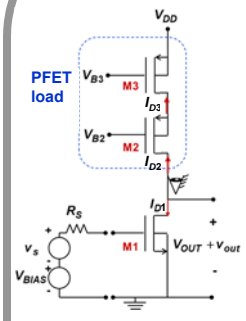


Resistance looking into the current source is:

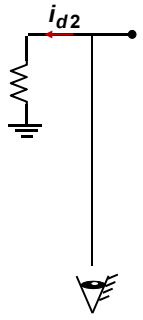
$$r_{o2}+r_{o3}+g_{m2}r_{o2}r_{o3}=r_{o2}+r_{o3}(1+g_{m2}r_{o2})\approx g_{m2}r_{o2}r_{o3}$$

Typically a good approximation

Cascode PFET Load: Small Signal Analysis



$$r_{o2}+r_{o3}(1+g_{m2}r_{o2})$$
$$\approx g_{m2}r_{o2}r_{o3}$$



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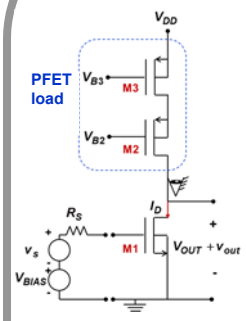
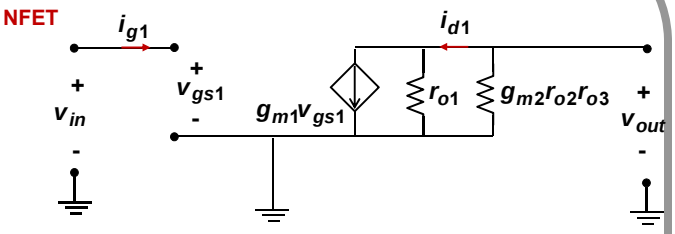
Typically a good approximation

Cascode PFET Load: Small Signal Analysis





Open circuit voltage gain:

$$A_v = \frac{v_{out}}{v_{in}} = -g_{m1}(r_{o1} \| (g_{m2}r_{o2}r_{o3})) \approx -g_{m1}r_{o1}$$

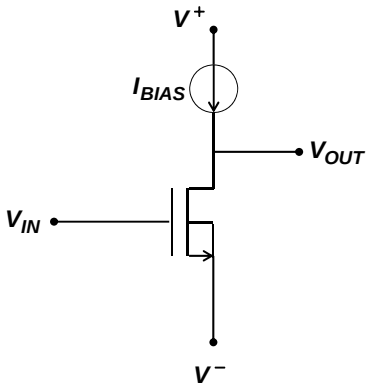
Typically a good approximation

Output resistance:

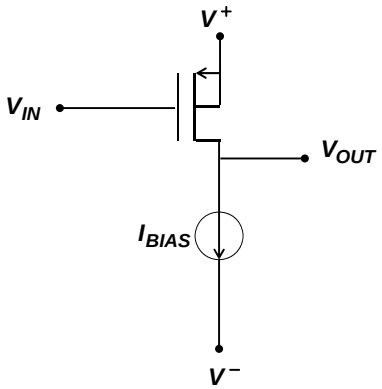
$$R_{out} = r_{o1} \| (g_{m2}r_{o2}r_{o3}) \approx r_{o1}$$

Typically a good approximation

The Common Source Amplifier: General Topology



NFET

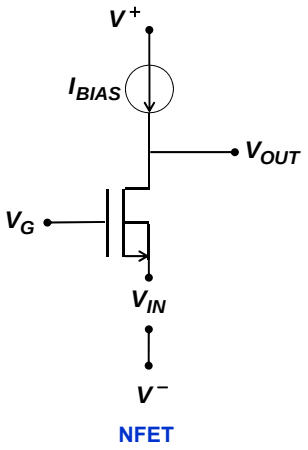


PFET

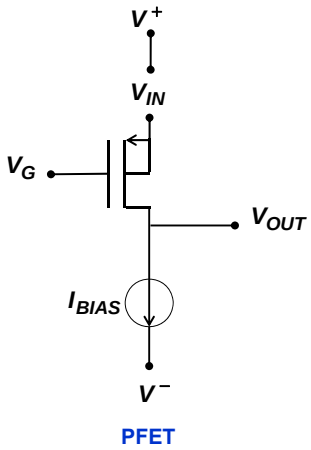
V^+ is the most positive voltage in the circuit
V^- is the most negative voltage in the circuit

- Large input resistance
- Large output resistance
- Large voltage gain
- Large current gain

The Common Gate Amplifier: General Topology



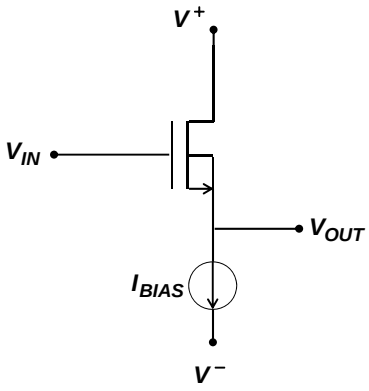
NFET



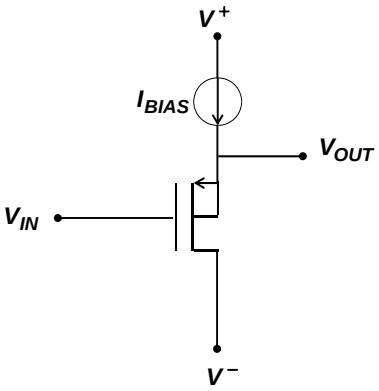
PFET

- Can have small input resistance
- Large output resistance
- Large voltage gain
- Small (unity) current gain

The Common Drain Amplifier: General Topology



NFET



PFET

- Large input resistance
- Small output resistance
- Small (less than unity) voltage gain

Chip-Based Current Sources and Voltage Sources

We have realized a decent load but ……

How does one generate voltage levels on a chip for biasing??

Current and voltage biasing of circuits require transistor based current and voltage sources on a chip!

What are the good figures of merit of chip-based voltage and current sources?