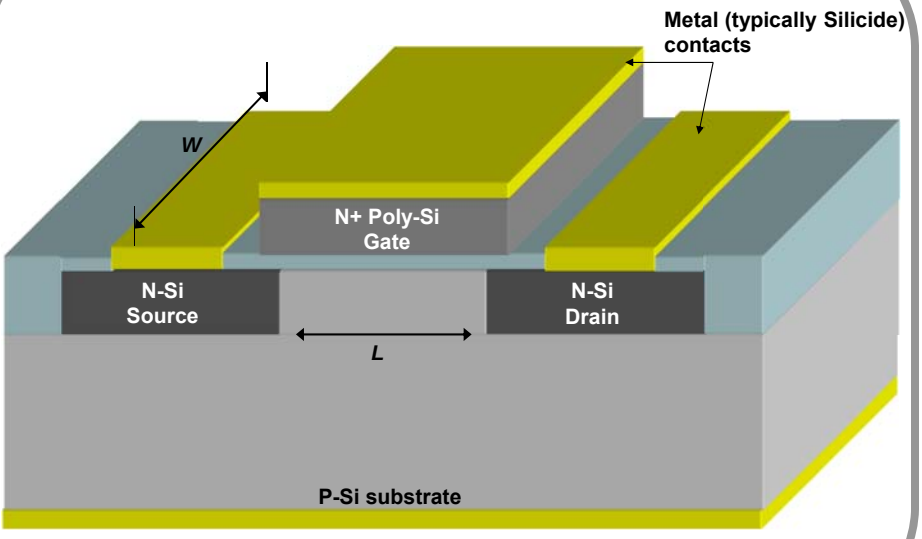
Lecture 10

Simple FET Circuits and Small Signal Models

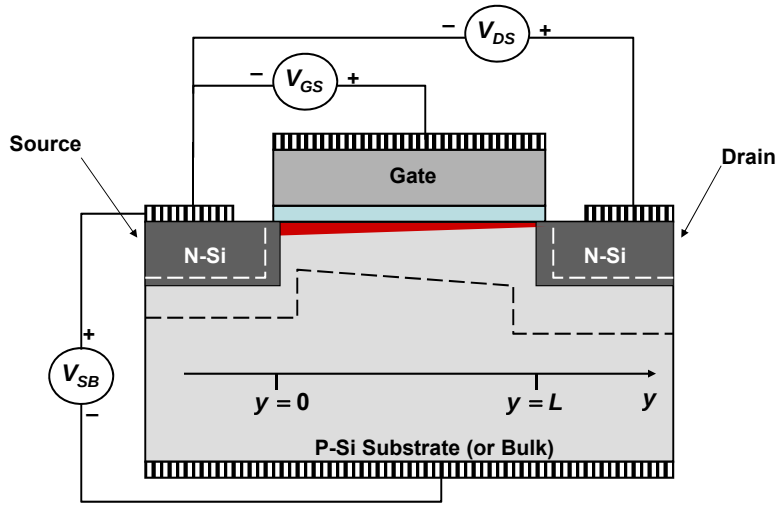
In this lecture you will learn:

- **The operation of simple MOS FET circuits**
- **Small signal circuit models of the MOS FETs**

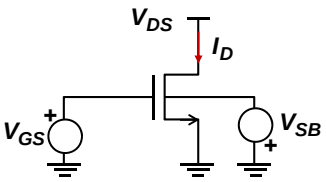
A NMOS Transistor in 3D

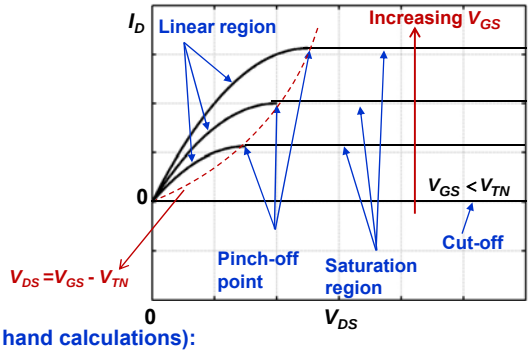


A NMOS Transistor: A Review



NMOS Transistor: A Review



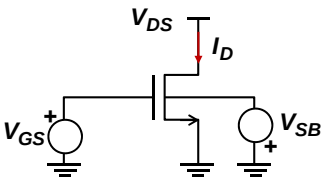


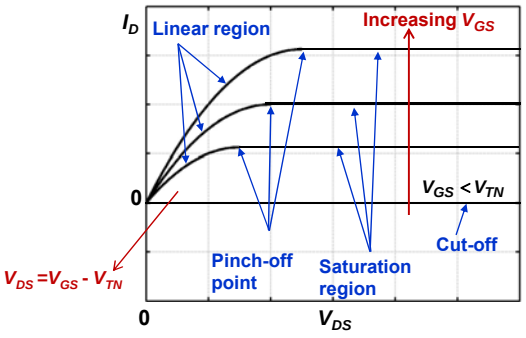
Simplified current model (good for hand calculations):

$$I_D = \begin{cases} 0 & \text{For } V_{GS} < V_{TN} \quad \text{Cut-off} \\ k_n\left[V_{GS} - V_{TN} - \frac{V_{DS}}{2}\right]V_{DS} & \text{For } 0 \le V_{DS} \le V_{GS} - V_{TN} \quad \text{Linear region} \\ \frac{k_n}{2}(V_{GS} - V_{TN})^2 & \text{For } 0 \le V_{GS} - V_{TN} \le V_{DS} \quad \text{Saturation region} \end{cases}$$

$$k_n = \frac{W}{L}\mu_n C_{ox}$$

NMOS Transistor: A Review



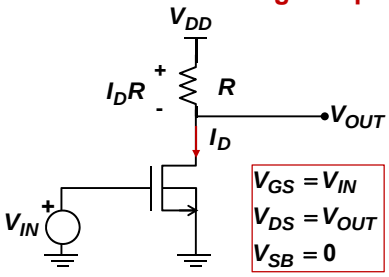


Better current model:

$$I_D = \begin{cases} 0 & \text{For } V_{GS} < V_{TN} \quad \text{Cut-off} \\ k_n\left[V_{GS} - V_{TN} - \frac{V_{DS}}{2}\right]V_{DS}(1+\lambda_n V_{DS}) & \text{For } 0 \le V_{DS} \le V_{GS} - V_{TN} \quad \text{Linear region} \\ \frac{k_n}{2}(V_{GS} - V_{TN})^2(1+\lambda_n V_{DS}) & \text{For } 0 \le V_{GS} - V_{TN} \le V_{DS} \quad \text{Saturation region} \end{cases}$$

$$k_n = \frac{W}{L}\mu_n C_{ox}$$

NFET Voltage Amplifier and Inverter



We need to find the relation between the output and the input voltage

1) $V_{IN} < V_{TN}$

The FET is in cut-off regime and $I_D = 0$ and consequently $V_{OUT} = V_{DD}$

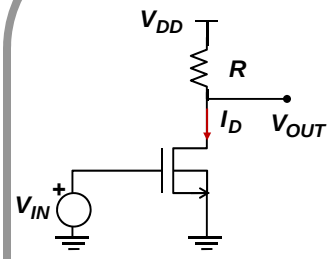
2) $V_{IN} > V_{TN}$

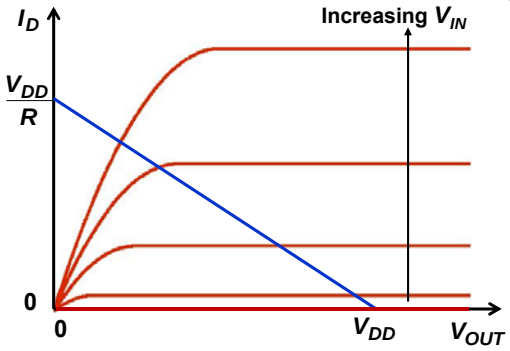
The FET is turned on and $I_D \neq 0$ and consequently $V_{OUT} = V_{DD} - I_D R < V_{DD}$

$V_{DS} > V_{GS} - V_{TN}$ (Saturation) $\longrightarrow$ $V_{OUT} > V_{IN} - V_{TN}$ (Saturation)

$V_{DS} < V_{GS} - V_{TN}$ (Linear) $\longrightarrow$ $V_{OUT} < V_{IN} - V_{TN}$ (Linear)

NFET Voltage Amplifier and Inverter: A Graphical Solution



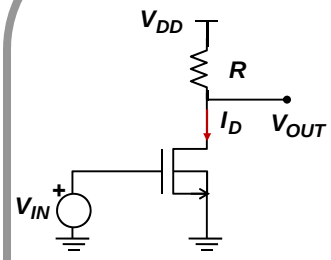


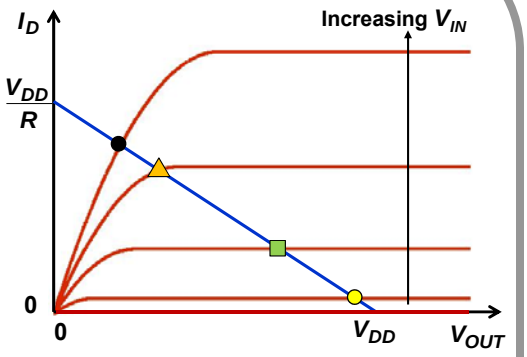
$$I_D = \frac{V_{DD} - V_{OUT}}{R}$$

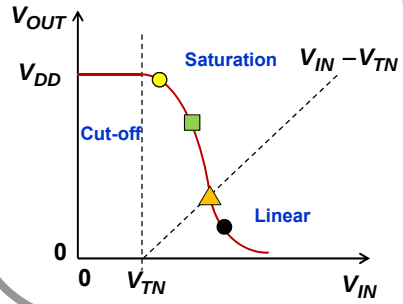
$$I_D = \begin{cases} 0 & \text{For } V_{IN} < V_{TN} \\ k_n\left[V_{IN} - V_{TN} - \frac{V_{OUT}}{2}\right]V_{OUT} & \text{For } 0 \le V_{OUT} \le V_{IN} - V_{TN} \\ \frac{k_n}{2}(V_{IN} - V_{TN})^2 & \text{For } 0 \le V_{IN} - V_{TN} \le V_{OUT} \end{cases}$$

$$k_n = \frac{W}{L}\mu_n C_{ox}$$

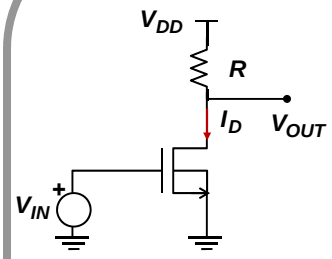
NFET Voltage Amplifier and Inverter: A Graphical Solution







NFET Voltage Amplifier and Inverter: Transfer Curve



1) Assume the FET is in the saturation regime:

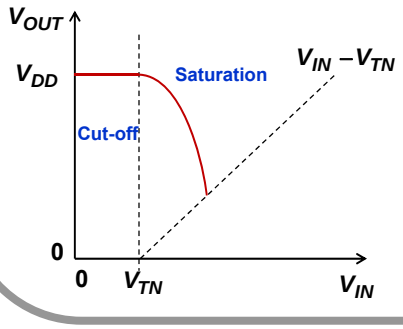
$$I_D = \frac{k_n}{2}(V_{IN} - V_{TN})^2$$

$$I_D = \frac{V_{DD} - V_{OUT}}{R}$$

Answer is:

$$V_{OUT} = V_{DD} - \frac{Rk_n}{2}(V_{IN} - V_{TN})^2$$

$$\Rightarrow \frac{dV_{OUT}}{dV_{IN}} = -Rk_n(V_{IN} - V_{TN})$$

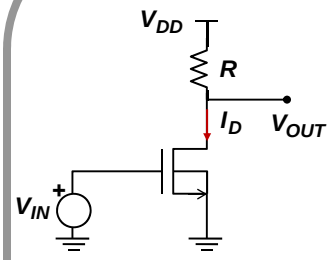


But the assumption that the FET is in saturation is only valid provided that:

$$V_{DS} > V_{GS} - V_{TN}$$

$$\Rightarrow V_{OUT} > V_{IN} - V_{TN}$$

NFET Voltage Amplifier and Inverter: Transfer Curve

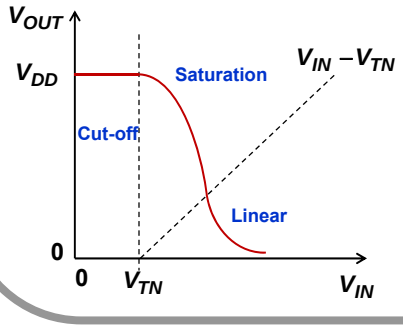


2) Now assume the FET is in the linear regime:

$$I_D = k_n\left[V_{IN} - V_{TN} - \frac{V_{OUT}}{2}\right]V_{OUT}$$

$$I_D = \frac{V_{DD} - V_{OUT}}{R}$$

Answer can be found by solving the above two equations for V_{OUT} vs V_{IN}

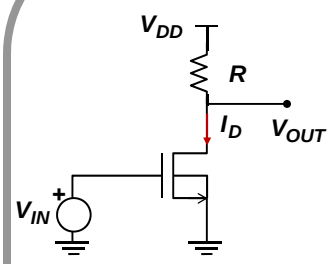


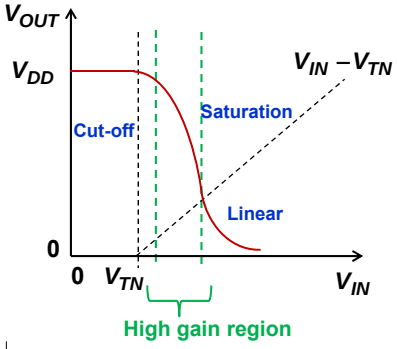
A high input voltage produces a low output voltage

A low input voltage produces a high output voltage

The device can therefore be used as a logical inverter!

NFET Voltage Amplifier and Inverter: Transfer Curve



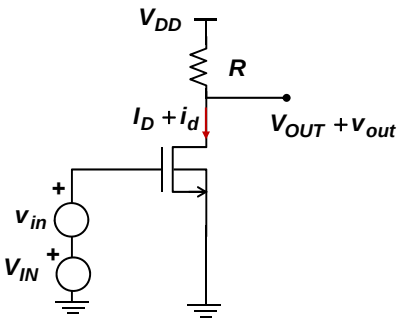


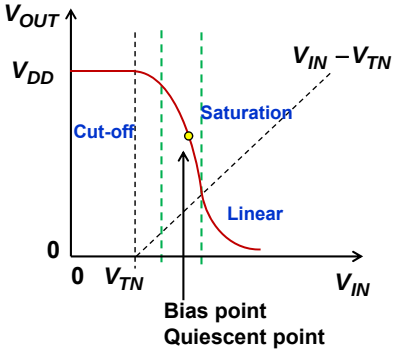
In the high gain region, the slope $\left|\frac{dV_{OUT}}{dV_{IN}}\right|$ can be much larger than unity!

This means a small change in the input voltage will produce a large change in the output voltage

The circuit can therefore be used as a voltage amplifier!

NFET Common Source (CS) Voltage Amplifier





What is: $\frac{v_{out}}{v_{in}} = ?$ → Voltage gain

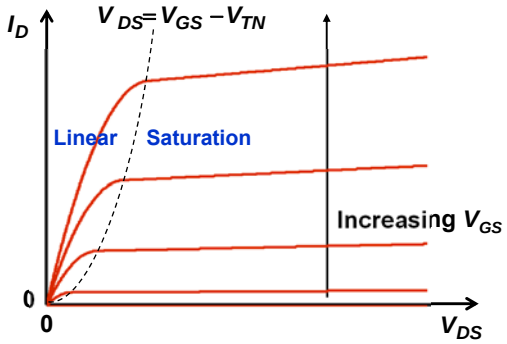
We need better techniques to calculate the voltage gain of such amplifier circuits

We need small signal models of the FETs!

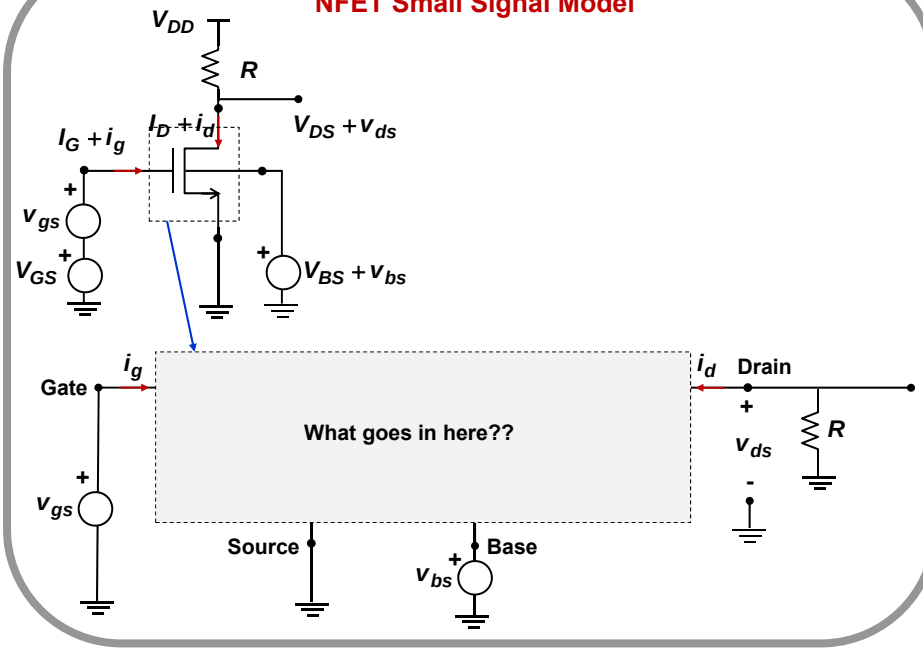
NFET Model with Channel Length Modulation Included

We will often use the following current model:

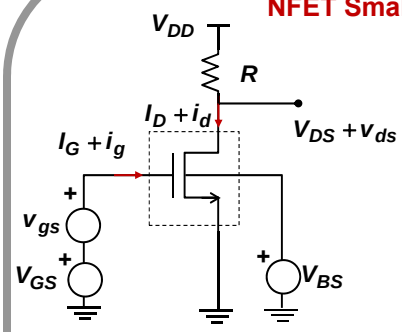
$$I_D = \begin{cases} 0 & \text{For } V_{GS} < V_{TN} \text{ (Cut-off region)} \\ k_n\left[V_{GS} - V_{TN} - \frac{V_{DS}}{2}\right]V_{DS}(1+\lambda_n V_{DS}) & \text{For } 0 \le V_{DS} \le V_{GS} - V_{TN} \text{ (Linear region)} \\ \frac{k_n}{2}(V_{GS} - V_{TN})^2(1+\lambda_n V_{DS}) & \text{For } 0 \le V_{GS} - V_{TN} \le V_{DS} \text{ (Saturation region)} \end{cases}$$



NFET Small Signal Model



NFET Small Signal Model – Part I

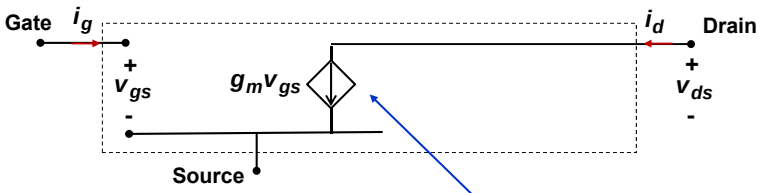


$$i_D = I_D + i_d$$
$$= I_D(V_{GS} + v_{gs})$$
$$= I_D + \frac{\partial I_D}{\partial V_{GS}} v_{gs}$$
$$= I_D + g_m v_{gs}$$

IEEE notation!

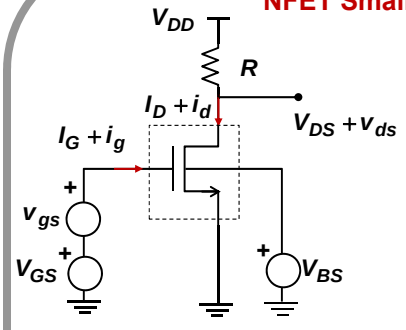
$$g_m = \frac{\partial I_D}{\partial V_{GS}}$$

Transconductance



A voltage-controlled current source

NFET Small Signal Model – Part II



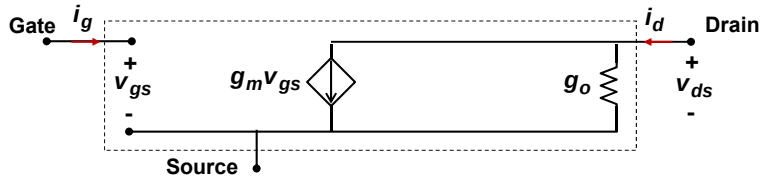
$$i_D = I_D + i_d = I_D(V_{GS} + v_{gs}, V_{DS} + v_{ds})$$
$$= I_D + \frac{\partial I_D}{\partial V_{GS}} v_{gs} + \frac{\partial I_D}{\partial V_{DS}} v_{ds}$$
$$= I_D + g_m v_{gs} + g_o v_{ds}$$

$$g_m = \frac{\partial I_D}{\partial V_{GS}}$$

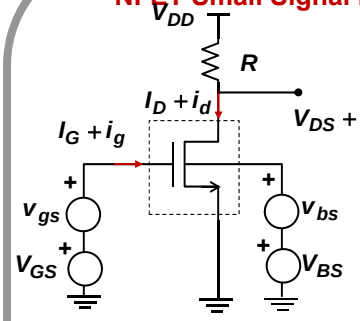
Transconductance

$$g_o = \frac{\partial I_D}{\partial V_{DS}}$$

Output conductance



NFET Small Signal Model – Part III – The Complete Model

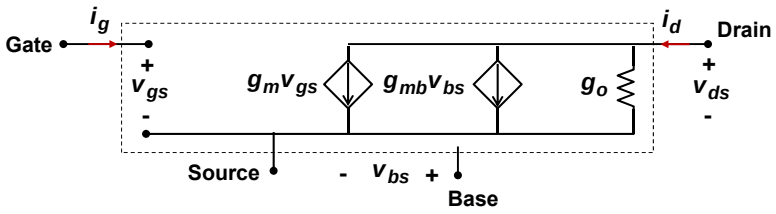


$$i_D = I_D + i_d = I_D(V_{GS} + v_{gs}, V_{DS} + v_{ds}, V_{BS} + v_{bs})$$
$$= I_D + \frac{\partial I_D}{\partial V_{GS}} v_{gs} + \frac{\partial I_D}{\partial V_{DS}} v_{ds} + \frac{\partial I_D}{\partial V_{BS}} v_{bs}$$
$$= I_D + g_m v_{gs} + g_o v_{ds} + g_{mb} v_{bs}$$

$g_m = \frac{\partial I_D}{\partial V_{GS}}$ Transconductance

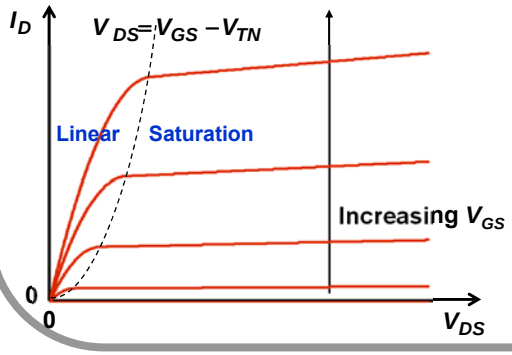
$g_o = \frac{\partial I_D}{\partial V_{DS}}$ Output conductance

$g_{mb} = \frac{\partial I_D}{\partial V_{BS}}$ Backgate conductance



NFET Model

$$I_D = \begin{cases} 0 & \text{For } V_{GS} < V_{TN} \text{ (Cut-off region)} \\ k_n\left[V_{GS} - V_{TN} - \frac{V_{DS}}{2}\right] V_{DS}(1 + \lambda_n V_{DS}) & \text{For } 0 \le V_{DS} \le V_{GS} - V_{TN} \text{ (Linear region)} \\ \frac{k_n}{2}(V_{GS} - V_{TN})^2(1 + \lambda_n V_{DS}) & \text{For } 0 \le V_{GS} - V_{TN} \le V_{DS} \text{ (Saturation region)} \end{cases}$$



$g_m = \frac{\partial I_D}{\partial V_{GS}}$ Transconductance

$g_o = \frac{\partial I_D}{\partial V_{DS}}$ Output conductance

$g_{mb} = \frac{\partial I_D}{\partial V_{BS}}$ Backgate conductance

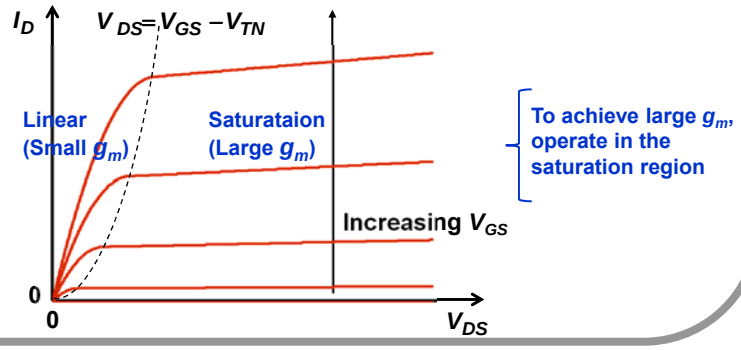
NFET: Transconductance

$$g_m = \frac{\partial I_D}{\partial V_{GS}}$$

Saturation: $g_m = \frac{\partial I_D}{\partial V_{GS}} = k_n (V_{GS} - V_{TN})(1 + \lambda_n V_{DS}) = \sqrt{2 k_n I_D (1 + \lambda_n V_{DS})}$

Linear: $g_m = \frac{\partial I_D}{\partial V_{GS}} = k_n V_{DS} (1 + \lambda_n V_{DS})$

Increases only as the square-root of the current



To achieve large g_m, operate in the saturation region

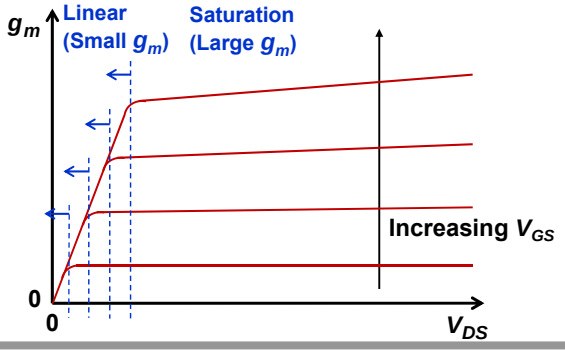
NFET: Transconductance

$$g_m = \frac{\partial I_D}{\partial V_{GS}}$$

Saturation: $g_m = \frac{\partial I_D}{\partial V_{GS}} = k_n (V_{GS} - V_{TN})(1 + \lambda_n V_{DS}) = \sqrt{2 k_n I_D (1 + \lambda_n V_{DS})}$

Linear: $g_m = \frac{\partial I_D}{\partial V_{GS}} = k_n V_{DS} (1 + \lambda_n V_{DS})$

Increases only as the square-root of the current

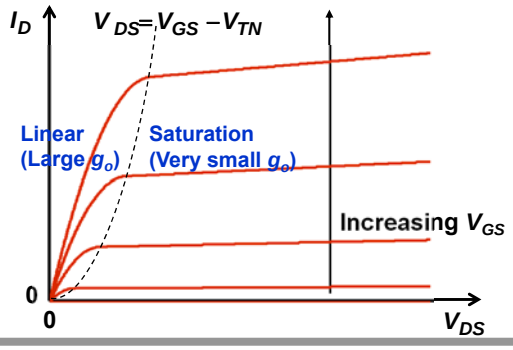


NFET: Output Conductance

$$g_o = \frac{\partial I_D}{\partial V_{DS}}$$

Saturation: $g_o = \frac{\partial I_D}{\partial V_{DS}} = \frac{k_n}{2}(V_{GS} - V_{TN})^2 \lambda_n = \lambda_n I_D$

Linear: $g_o = \frac{\partial I_D}{\partial V_{DS}} = \lambda_n I_D + k_n (V_{GS} - V_{TN} - V_{DS})(1 + \lambda_n V_{DS})$

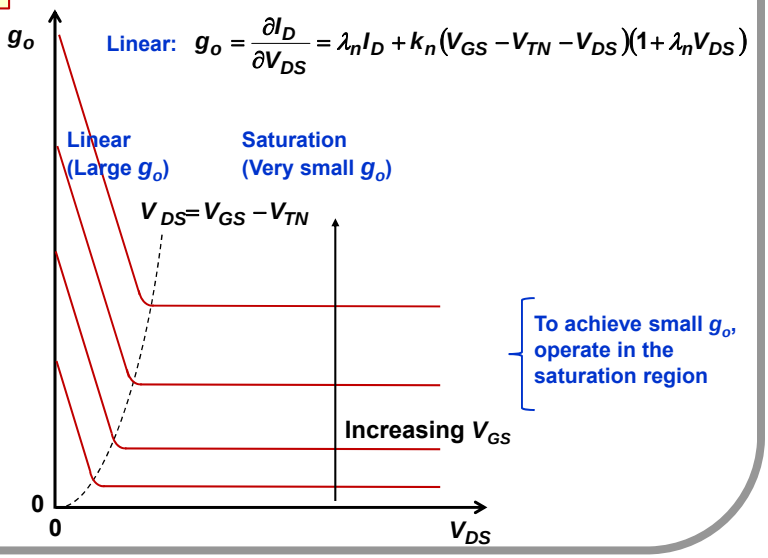


NFET: Output Conductance

$$g_o = \frac{\partial I_D}{\partial V_{DS}}$$

Saturation: $g_o = \frac{\partial I_D}{\partial V_{DS}} = \frac{k_n}{2}(V_{GS} - V_{TN})^2 \lambda_n = \lambda_n I_D$

Linear: $g_o = \frac{\partial I_D}{\partial V_{DS}} = \lambda_n I_D + k_n (V_{GS} - V_{TN} - V_{DS})(1 + \lambda_n V_{DS})$



NFET: Backgate Conductance

Recall that the threshold voltage depends on the source-to-bulk voltage V_{SB}:

$$V_{TN} = V_{TN}(V_{SB}=0) + \gamma_n\left(\sqrt{-2\phi_p + V_{SB}} - \sqrt{-2\phi_p}\right)$$

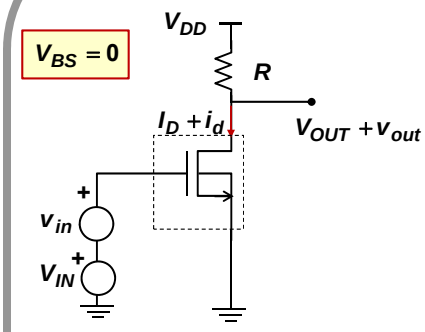
$$\gamma_n = \frac{\sqrt{2\,\varepsilon_S q N_a}}{C_{ox}}$$ = Backgate effect (or the body effect) parameter

$$g_{mb} = \frac{\partial I_D}{\partial V_{BS}} = \frac{\partial I_D}{\partial V_{TN}}\frac{\partial V_{TN}}{\partial V_{BS}}$$

Saturation: $$g_{mb} = \frac{\partial I_D}{\partial V_{TN}}\frac{\partial V_{TN}}{\partial V_{BS}} = -\frac{\partial I_D}{\partial V_{GS}}\frac{\partial V_{TN}}{\partial V_{BS}} = g_m\frac{\gamma_n}{2\sqrt{-2\phi_p - V_{BS}}}$$

Linear: $$g_{mb} = \frac{\partial I_D}{\partial V_{TN}}\frac{\partial V_{TN}}{\partial V_{BS}} = -\frac{\partial I_D}{\partial V_{GS}}\frac{\partial V_{TN}}{\partial V_{BS}} = g_m\frac{\gamma_n}{2\sqrt{-2\phi_p - V_{BS}}}$$

NFET Common Source (CS) Voltage Amplifier



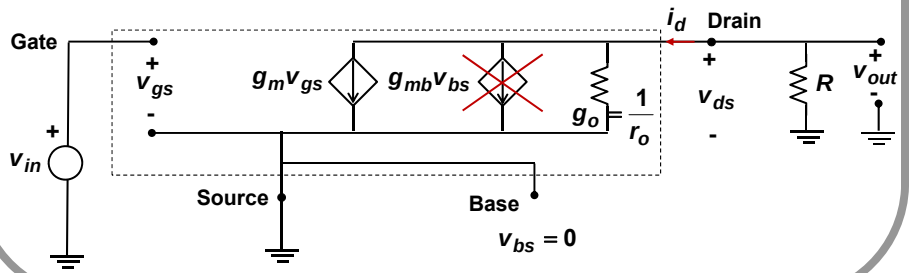
$$v_{gs} = v_{in}$$

$$i_d = g_m v_{gs} + \frac{v_{out}}{r_o} = -\frac{v_{out}}{R}$$

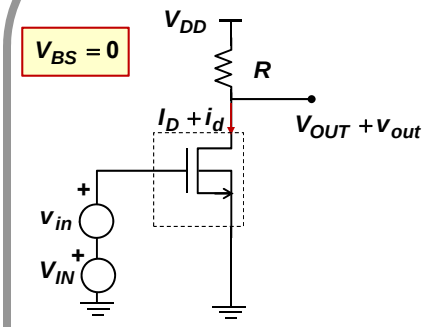
$$\Rightarrow v_{out} = -g_m(r_o \,||\, R)v_{gs} = --g_m(r_o \,||\, R)v_{in}$$

$$\Rightarrow A_v = \frac{v_{out}}{v_{in}} = -g_m(r_o \,||\, R)$$

Voltage gain



NFET Common Source (CS) Voltage Amplifier



$$v_{gs} = v_{in}$$

$$i_d = g_m v_{gs} + \frac{v_{out}}{r_o} = -\frac{v_{out}}{R}$$

$$\Rightarrow v_{out} = -g_m (r_o \| R) v_{gs} = --g_m (r_o \| R) v_{in}$$

$$\Rightarrow A_v = \frac{v_{out}}{v_{in}} = -g_m (r_o \| R)$$

Voltage gain

$$\frac{1}{r_o \| R} = \frac{1}{r_o} + \frac{1}{R}$$

$$\Rightarrow r_o \| R = \frac{R}{1 + g_o R}$$

$$\Rightarrow A_v = \frac{v_{out}}{v_{in}} = -g_m (r_o \| R) = -g_m \frac{R}{1 + g_o R}$$

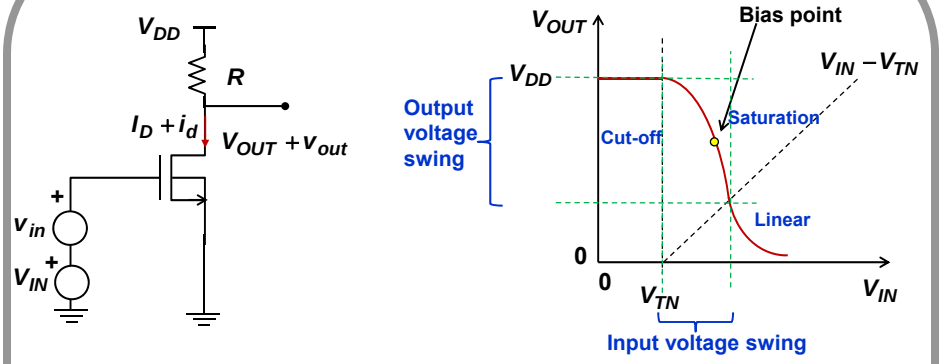
A Note on Small Signal Modeling

When making a small signal model out of a complicated nonlinear signal remember that:

1) All DC voltage sources in the circuit become short circuits

2) All DC current sources in the circuit become open circuits

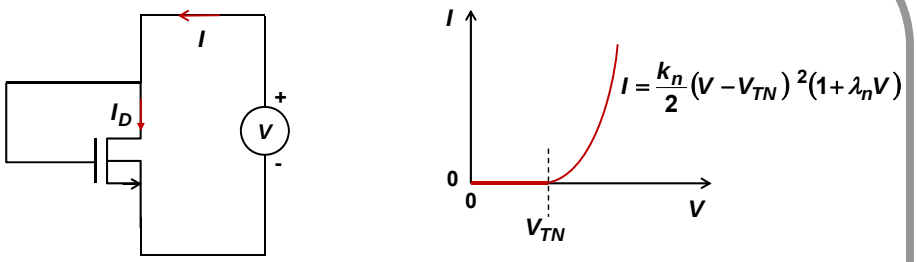
NFET CS Amplifier: Limits of Output Voltage Swing



Minimum output voltage and maximum input voltage:
If the output voltage becomes too small (happens when the input voltage becomes too large), the FET will go into the linear region (in the linear region the gain is small)

Maximum output voltage and minimum input voltage:
If the input voltage becomes too small the FET will go into cut-off

The Diode-Connected NFET



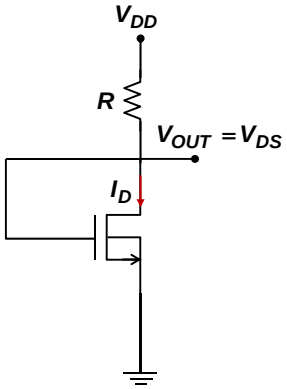
The gate and the drain of the FET are tied together

Since:

$$V_{DG} = 0$$
$$\Rightarrow V_{DS} = V_{GS}$$
$$\Rightarrow V_{DS} > V_{GS} - V_{TN}$$

$\Rightarrow$ The FET is always operating in saturation when not in cut-off (i.e. provided $V_{GS} > V_{TN}$)

The Diode-Connected NFET



Finding V_{OUT}:

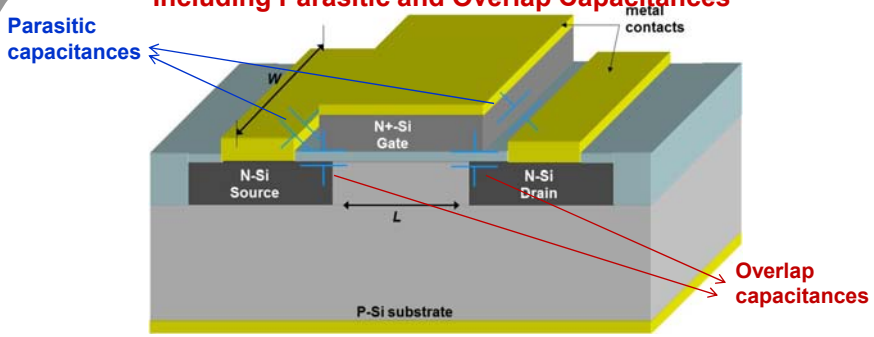
$$I_D = \frac{k_n}{2}(V_{GS} - V_{TN})^2(1 + \lambda_n V_{DS})$$

$$\Rightarrow \frac{k_n}{2}(V_{OUT} - V_{TN})^2(1 + \lambda_n V_{OUT}) = \frac{V_{DD} - V_{OUT}}{R}$$

$$\Rightarrow \frac{k_n}{2}(V_{OUT} - V_{TN})^2 \approx \frac{V_{DD} - V_{OUT}}{R}$$

The above equation can be solved for V_{OUT}

Including Parasitic and Overlap Capacitances

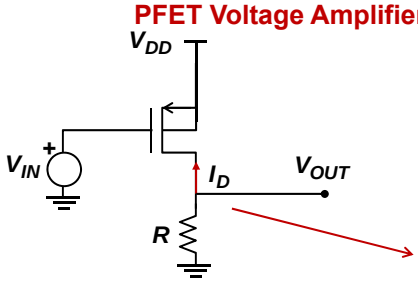


In Saturation:

$$C_{gs} = \left.\frac{\partial Q_G}{\partial V_{GS}}\right|_{V_{DS},V_{SB}} = \frac{2}{3}WLC_{ox} + WC_{ov} + WC_p \neq \frac{2}{3}WLC_{ox}$$

$$C_{gd} = \left.\frac{\partial Q_G}{\partial V_{GD}}\right|_{V_{GS},V_{SB}} = WC_{ov} + WC_p \neq 0$$

PFET Voltage Amplifier and Inverter



We need to find the relation between the output and the input voltage

$I_D < 0$ and actual current is flowing out of the drain

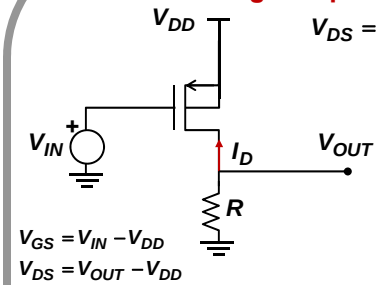
1) $V_{GS} = V_{IN} - V_{DD} > V_{TP}$

The FET is in cut-off regime and $I_D = 0$ and consequently $V_{OUT} = 0$

2) $V_{GS} = V_{IN} - V_{DD} < V_{TP}$

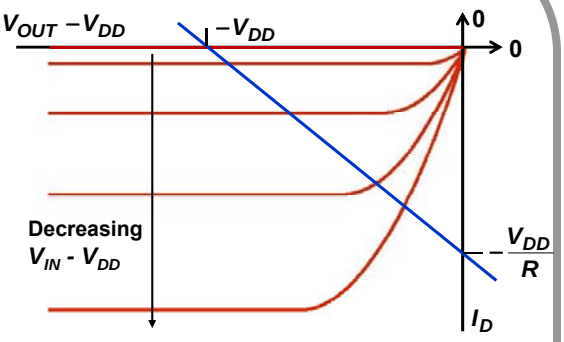
The FET is turned on and $I_D \neq 0$ and consequently $V_{OUT} = -I_D R$

PFET Voltage Amplifier and Inverter: A Graphical Solution



$V_{GS} = V_{IN} - V_{DD}$

$V_{DS} = V_{OUT} - V_{DD}$

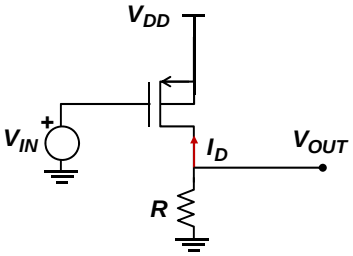


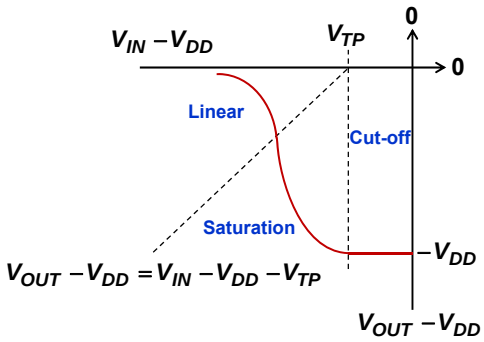
$$I_D = -\frac{V_{OUT}}{R}$$

$$I_D = \begin{cases} 0 & \text{For } V_{IN} - V_{DD} > V_{TP} \\ -k_p\left[V_{IN} - V_{DD} - V_{TP} - \frac{V_{OUT} - V_{DD}}{2}\right](V_{OUT} - V_{DD}) & \text{For } 0 \geq V_{OUT} - V_{DD} \geq V_{IN} - V_{DD} - V_{TP} \\ -\frac{k_p}{2}(V_{IN} - V_{DD} - V_{TP})^2 & \text{For } 0 \geq V_{IN} - V_{DD} - V_{TP} \geq V_{OUT} - V_{DD} \end{cases}$$

$$k_p = \frac{W}{L}\mu_p C_{ox}$$

PFET Voltage Amplifier and Inverter: Transfer Curve



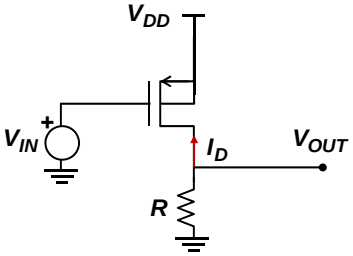


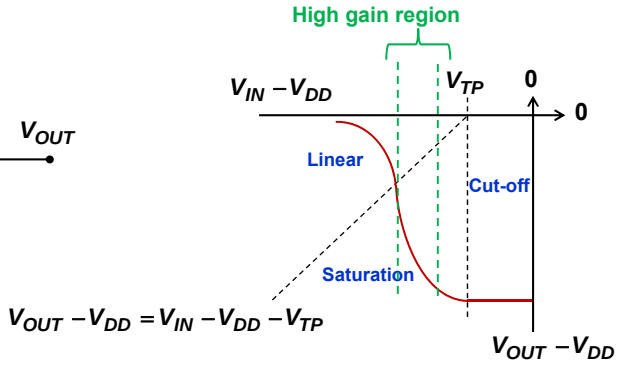
A high input voltage produces a low output voltage

A low input voltage produces a high output voltage

The device can therefore be used as a logical inverter!

PFET Voltage Amplifier and Inverter: Transfer Curve



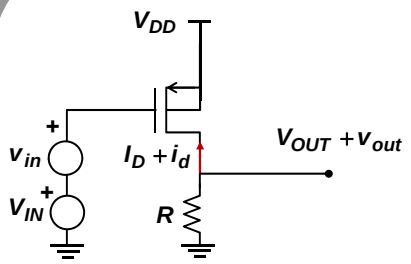


In the high gain region, the slope $\left|\frac{dV_{OUT}}{dV_{IN}}\right|$ can be larger than unity!

This means a small change in the input voltage will produce a large change in the output voltage

The circuit can therefore be used as a voltage amplifier!

PFET Common Source (CS) Voltage Amplifier



$$v_{gs} = v_{in}$$

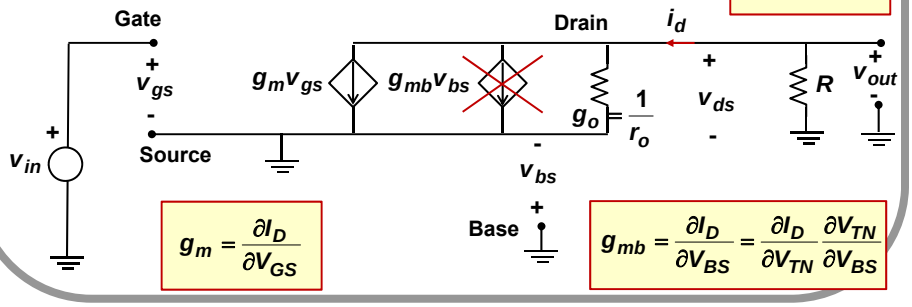
$$i_d = g_m v_{gs} + \frac{v_{out}}{r_o} = -\frac{v_{out}}{R}$$

$$\Rightarrow v_{out} = -g_m (r_o \,||\, R) v_{gs}$$

$$\Rightarrow A_v = \frac{v_{out}}{v_{in}} = -g_m (r_o \,||\, R)$$

Voltage gain

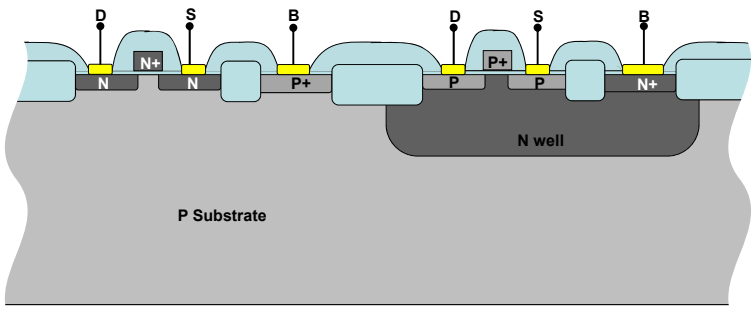
$$g_o = \frac{\partial I_D}{\partial V_{DS}}$$



$$g_m = \frac{\partial I_D}{\partial V_{GS}}$$

$$g_{mb} = \frac{\partial I_D}{\partial V_{BS}} = \frac{\partial I_D}{\partial V_{TN}} \frac{\partial V_{TN}}{\partial V_{BS}}$$

The Standard CMOS Process



The NFETs and the PFETs can be realized on the same P-substrate by making a N-well inside the substrate for the PFETs

The Double-Well CMOS Process