Lecture #30

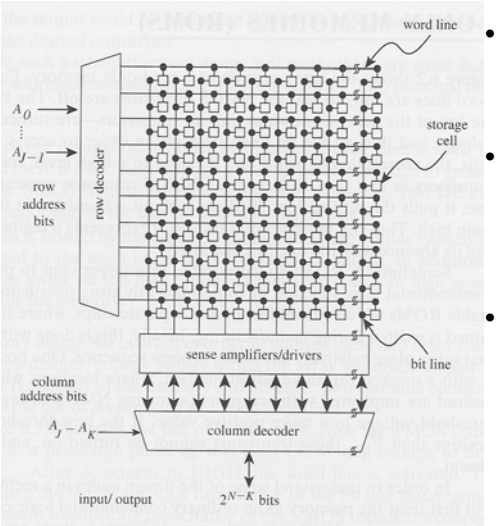
ANNOUNCEMENT

- Review Session: Thu. May 15, 2-5 PM, 277 Cory

OUTLINE

- Charge coupled devices

Memory Organization



- Some address bits are used by row decoder to select one word line
- Information in storage cells along that word line is passed to the column decoder
- Decoder selects bits (according to the remaining address bits) to be presented at the output

Storage of Charge Beneath MOS Gate

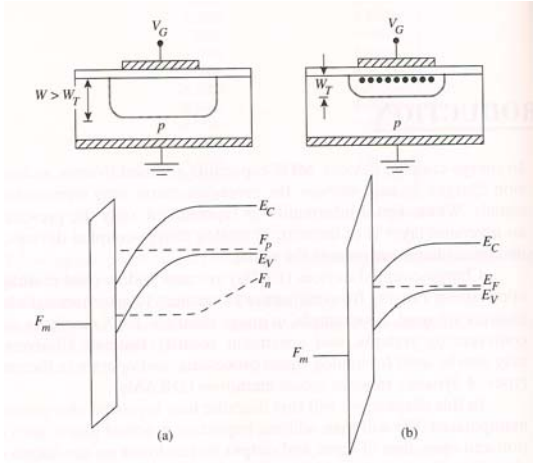


Figure 4.1. MOS band diagrams (a) just after switching from accumulation to deep depletion and (b) after equilibrium has been restored.

Transfer of Charge Between MOS Gates

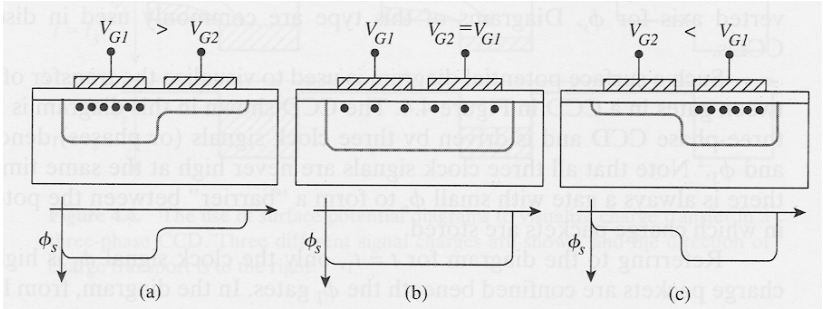


Figure 4.2. Transfer of inversion charge between two adjacent MOS capacitors: (a) V_{G2} small so that charge is confined beneath the left-hand gate; (b) equal gate voltages $V_{G1} = V_{G2}$, resulting in sharing of charge between the gates; and (c) V_{G1} small so that charge is transferred to the right-hand electrode. Also shown is the surface potential as a function of position.

Charge Coupled Device

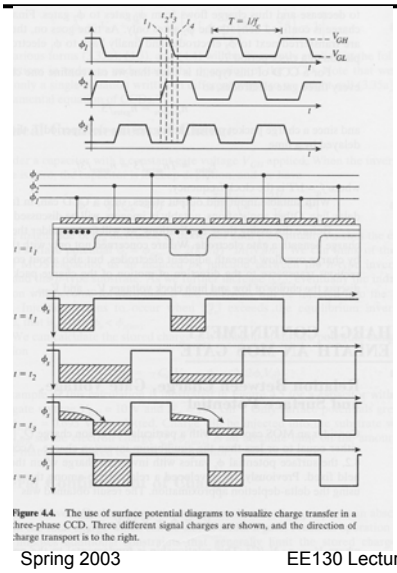


Figure 4.4. The use of surface potential diagrams to visualize charge transfer in a three-phase CCD. Three different signal charges are shown, and the direction of charge transport is to the right.

- Array of closely-spaced MOS capacitors
  - Transfer of stored inversion charge along surface, into the device output, under proper control of gate biases
- Applications include memory, signal processing, imaging

CCD Imager

1. Entire CCD array is biased into deep depletion, then exposed to a focused image for a time interval
2. Channel under each gate (“pixel”) becomes charged to a level corresponding to the brightness at that location
3. Stored charge (analog signal) is clocked out to sense amplifiers at the edges of the CCD array