Lecture #28

ANNOUNCEMENTS

- Quiz #6 next Thursday (May 8)
  - Topics covered: MOSFET
  - Closed book; calculator, 6 pages of notes allowed

OUTLINE

- MOSFET scaling
- CMOS technology
- Silicon on Insulator technology

Reading: Reader Part III, Chapter 4

Short-Channel MOSFET V_T

- For short-channel MOSFETs, V_T is usually defined as the gate voltage at which the maximum barrier for electrons at the surface equals $2\psi_B$. This is lower than the long-channel V_T by an amount

$$\Delta V_T = \frac{24T_{oxe}}{W_{dm}}\sqrt{\psi_{bi}(\psi_{bi}+V_{DS})}\,e^{-\pi L/2(W_{dm}+3T_{oxe})}$$

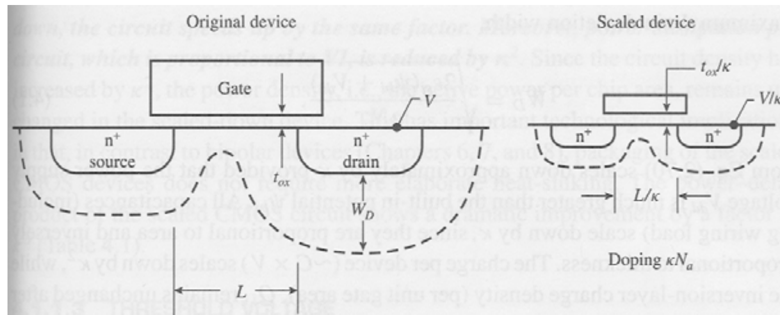
$$\text{where}\quad \psi_{bi} = \frac{E_G}{2q}+\psi_B$$

Note: This equation assumes that $r_j > W_{dm}$

➔ **To minimize V_T roll-off, N_{body} should be high enough to ensure that $L_{min} > 2W_{dm}$**

Constant-Field Scaling

- Voltages and MOSFET dimensions are scaled by the same factor κ>1, so that the electric field remains unchanged



Constant-Field Scaling (cont.)

	MOSFET Device and Circuit Parameters	Multiplicative Factor ($\kappa > 1$)
Scaling assumptions	Device dimensions (t_{ox}, L, W, x_j)	$1/\kappa$
	Doping concentration (N_a, N_d)	κ
	Voltage (V)	$1/\kappa$
Derived scaling behavior of device parameters	Electric field ($\mathscr{E}$)	1
	Carrier velocity (v)	1
	Depletion-layer width (W_d)	$1/\kappa$
	Capacitance ($C = \varepsilon A/t$)	$1/\kappa$
	Inversion-layer charge density (Q_i)	1
	Current, drift (I)	$1/\kappa$
	Channel resistance (R_{ch})	1
Derived scaling behavior of circuit parameters	Circuit delay time ($\tau \sim CV/I$)	$1/\kappa$
	Power dissipation per circuit ($P \sim VI$)	$1/\kappa^2$
	Power–delay product per circuit ($P\tau$)	$1/\kappa^3$
	Circuit density ($\propto 1/A$)	κ^2
	Power density (P/A)	1

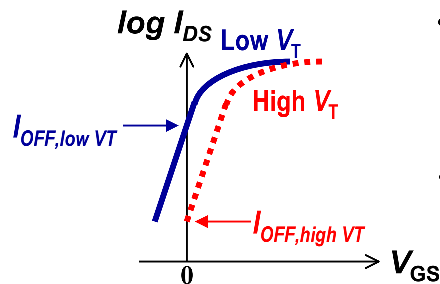
- Circuit speed improves by κ
- Power dissipation per function is reduced by κ^2

V_T Design Trade-Off

- Low V_T is desirable for high ON current:

$$I_{dsat} \propto (V_{dd} - V_t)^{\eta} \qquad 1 < \eta < 1.5$$

- But V_T is needed for low OFF current:



- Non-scaling factors:
  - kT/q
  - E_G
  - T_{inv}

→ V_T cannot be scaled aggressively!

- Since V_T cannot be scaled down aggressively, the power-supply voltage (V_{DD}) has not been scaled down in proportion to the MOSFET channel length

Feature Size (μm)	Power-Supply Voltage (V)	Gate Oxide Thickness (Å)	Oxide Field (MV/cm)
2	5	350	1.4
1.2	5	250	2.0
0.8	5	180	2.8
0.5	3.3	120	2.8
0.35	3.3	100	3.3
0.25	2.5	70	3.6

Generalized Scaling

- Electric field intensity increases by a factor α>1
- $\underline{N}_{body}$ must be scaled up by α to control short-channel effects

	MOSFET Device and Circuit Parameters	Multiplicative Factor ($\kappa > 1$)	
Scaling assumptions	Device dimensions (t_{ox}, L, W, x_j)	$1/\kappa$	
	Doping concentration (N_a, N_d)	$\alpha\kappa$	
	Voltage (V)	α/κ	
Derived scaling behavior of device parameters	Electric field ($\mathscr{E}$)	α	
	Depletion-layer width (W_d)	$1/\kappa$	
	Capacitance ($C = \varepsilon A/t$)	$1/\kappa$	
	Inversion-layer charge density (Q_i)	α	
		Long Ch.	Vel. Sat.
	Carrier velocity (v)	α	1
	Current, drift (I)	α^2/κ	α/κ
Derived scaling behavior of circuit parameters	Circuit delay time ($\tau \sim CV/I$)	$1/\alpha\kappa$	$1/\kappa$
	Power dissipation per circuit ($P \sim VI$)	α^3/κ^2	α^2/κ^2
	Power–delay product per circuit ($P\tau$)	α^2/κ^3	
	Circuit density ($\propto 1/A$)	κ^2	
	Power density (P/A)	α^3	α^2

- Reliability and power density are issues

CMOS Technology

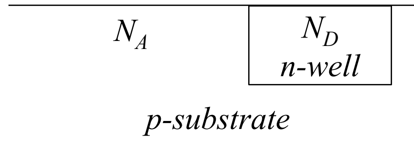
Both n-channel and p-channel MOSFETs are fabricated on the same chip ($V_{Tp} = -V_{Tn}$)

- Primary advantage:
  - Lower average power dissipation
    - In steady state, either the NMOS or PMOS device is off, so there is no d.c. current path between V_{DD} and GND
- Disadvantages:
  - More complex (expensive) process
  - Latch-up problem

Need p-regions (for NMOS) and n-regions (for PMOS) on the wafer surface, *e.g.*:

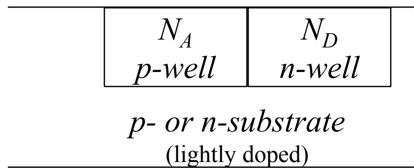
Single-well technology

- n-well must be deep enough to avoid vertical punch-through



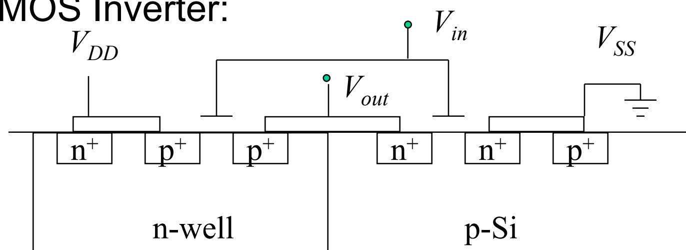
Twin-well technology

- Wells must be deep enough to avoid vertical punch-through

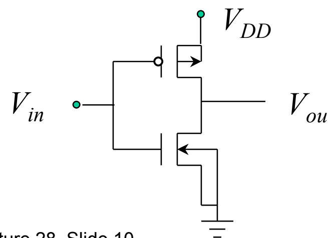


CMOS Latch-up

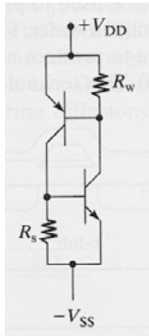
CMOS Inverter:



Equivalent circuit:



Coupled parasitic npn and pnp bipolar transistors:



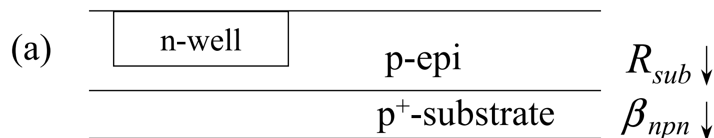
If either BJT enters the active mode, the SCR will enter into the forward conducting mode (large current flowing between V_{DD} and GND) if $\beta_{npn}\beta_{pnp} > 1$

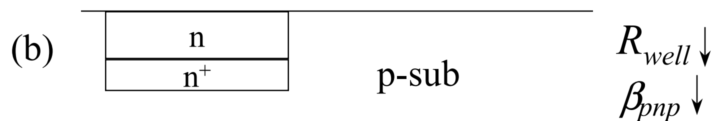
=> circuit burnout!

Latch-up is triggered by a <u>transient</u> increase in current, caused by
- transient currents (ionizing radiation, impact ionization, *etc.*)
- voltage transients
  - *e.g.* negative voltage spikes which forward-bias the pn junction momentarily

How to Prevent CMOS Latchup

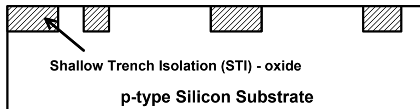
1. Reduce minority-carrier lifetimes in well/substrate
2. Use highly doped substrate or wells:



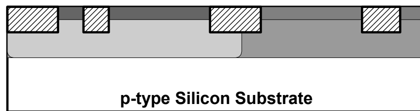


"retrograde well"

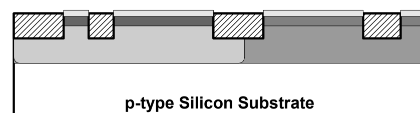
Modern CMOS Fabrication Process



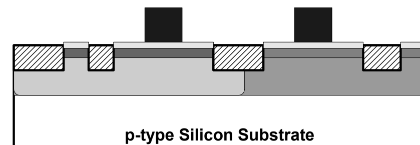
- A series of lithography, etch, and fill steps are used to create silicon islands isolated by oxide



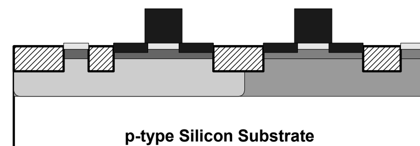
- Lithography and implant steps are used to set NMOS and PMOS doping levels



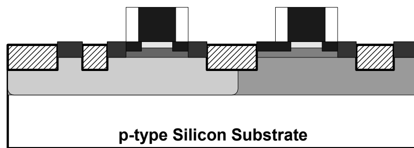
- A thin gate oxide is grown



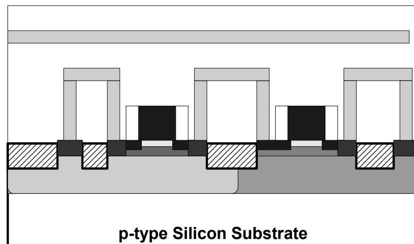
- Poly-Si is deposited and patterned to form gate electrodes



- Lithography and implantation is used to form NLDD and PLDD regions

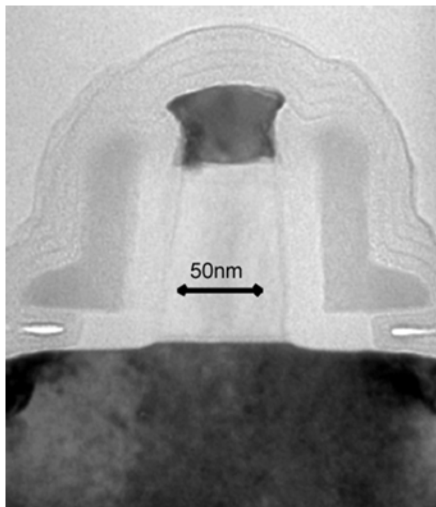


- A series of steps is used to form the deep source / drain regions as well as body contacts



- A series of steps is used to encapsulate the devices and form metal interconnections between them.

Intel's 90 nm CMOS Technology



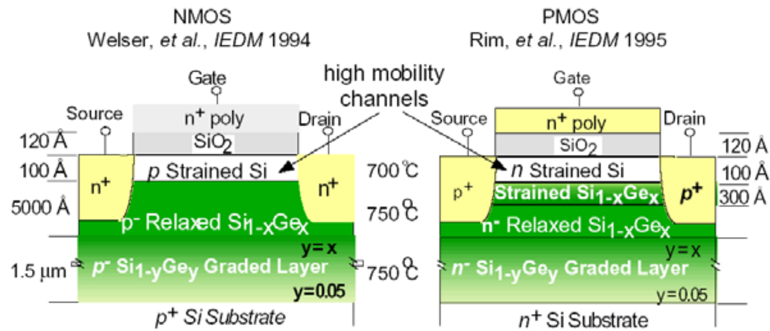
To be used for volume manufacturing of ICs on 300 mm wafers beginning this year

- L_{gate} = 50 nm
- T_{ox} = 1.2 nm
- Strained Si channel

Strained Si

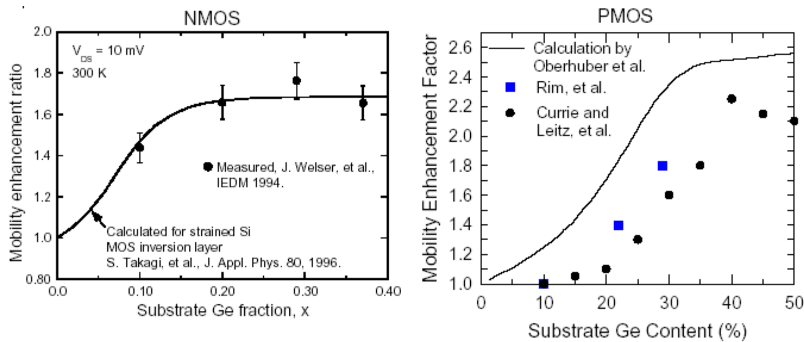
$$I_{Dsat} \propto v \times Q_{inv}$$

→ I_{Dsat} can be increased by enhancing field-effect mobilities, by straining the Si channel:

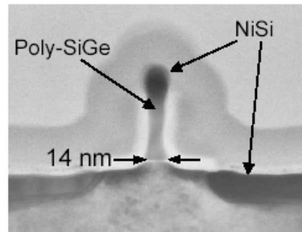


Courtesy of J. Hoyt, MIT

Mobility Enhancement with Strain

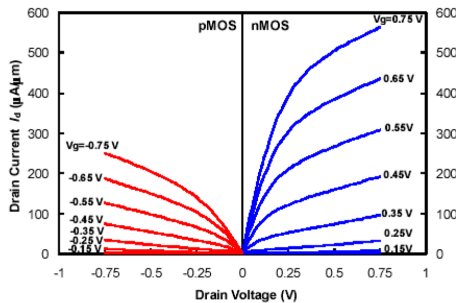


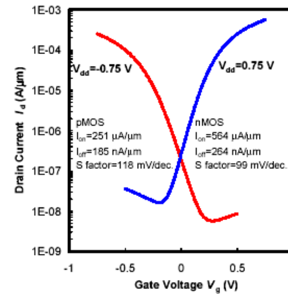
14 nm CMOSFETs



Hokazono *et al.*, Toshiba Corporation, presented at the *International Electron Devices Meeting* (San Francisco, CA) Dec. '02

- 1.3 nm SiO_xN_y gate dielectric
- Poly-$Si_{0.9}Ge_{0.1}$ gate





Silicon on Insulator (SOI) Technology

- Advantages over bulk-Si:
  - very low junction capacitance
  - no body effect
  - soft-error immunity