Lecture #27

ANNOUNCEMENTS

- Design Project: Your BJT design should meet the performance specifications to within 10% at both 300K and 360K.

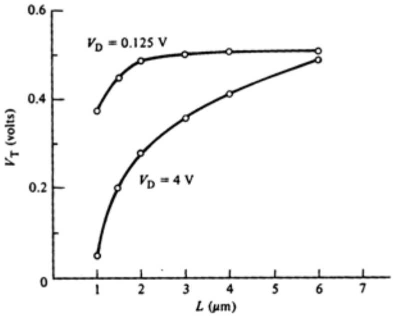
  (β_{dc}> 45, f_T > 18 GHz, V_A > 9 V and $V_{punchthrough}$ > 9 V)

OUTLINE

- Short channel effect
- Drain-induced barrier lowering
- Excess current effects
- Parasitic source/drain resistance

The Short Channel Effect (SCE)

“V_T roll-off”



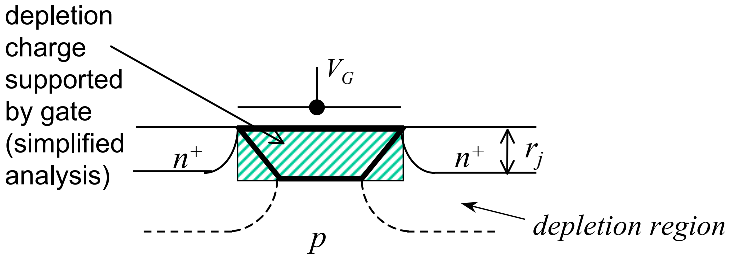
- |V_T| decreases with L
  - Effect is exacerbated by high values of |V_{DS}|
- This is undesirable (*i.e.* we want to minimize it!) because circuit designers would like V_T to be invariant with transistor dimensions and biasing conditions

Qualitative Explanation of SCE

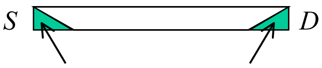
- Before an inversion layer forms beneath the gate, the surface of the Si underneath the gate must be depleted (to a depth W_{dm})
- The source & drain pn junctions assist in depleting the Si underneath the gate
  - – Portions of the depletion charge in the channel region are balanced by charge in S/D regions, rather than by charge on the gate

$\Rightarrow$ less gate charge is required to reach inversion (*i.e.* $|V_T|$ decreases)

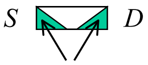
The smaller the *L*, the greater percentage of charge balanced by the S/D pn junctions:



Large L:

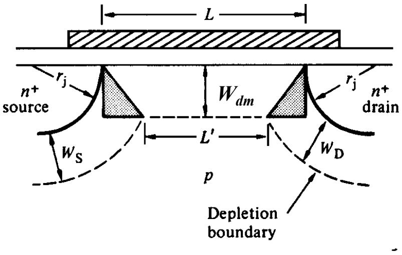


Small L:



First-Order Analysis of SCE

- The gate supports the depletion charge in the trapezoidal region. This is smaller than the rectangular depletion region underneath the gate, by the factor $$1-\frac{L+L'}{2L}$$



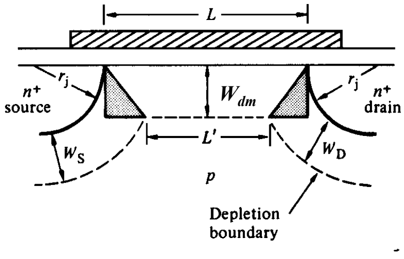
- This is the factor by which the depletion charge Q_{dep} is reduced from the ideal
- One can deduce from simple geometric analysis that $L' = L - 2r_j\left[\sqrt{1+\frac{2W_{dm}}{r_j}}-1\right]$

V_T Roll-Off: First-Order Model

$$\left|V_T\right| - \left|V_{T(long-channel)}\right| \equiv \Delta V_T = \frac{-qN_A W_{dm}}{C_{oxe}}\frac{r_j}{L}\left(\sqrt{1+\frac{2W_{dm}}{r_j}}-1\right)$$

Minimize ΔV_T by

- reducing T_{oxe}
- reducing r_j
- increasing N_A
(trade-offs: degraded *m, μ*)



⇒ **MOSFET vertical dimensions should be scaled along with horizontal dimensions!**

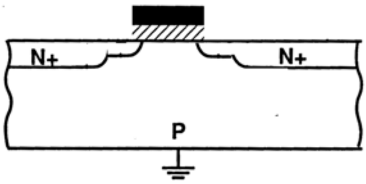
Source and Drain Structure

- To minimize SCE, we want shallow (small r_j) S/D regions -- but the parasitic resistance of these regions will increase when r_j is reduced.

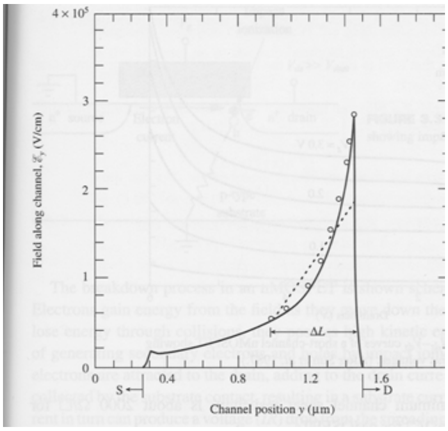
$$R_{source}, R_{drain} \propto \rho / W r_j$$

where ρ = resistivity of the S/D regions

- Shallow S/D “extensions” may be used to effectively reduce r_j without increasing the S/D sheet resistance too much

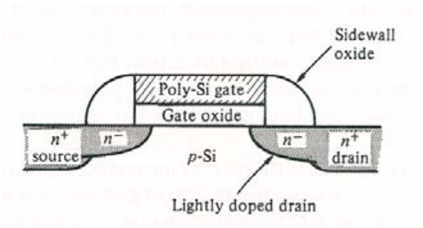


Electric Field Along Channel



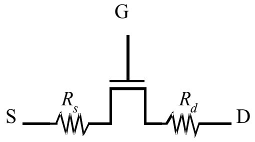
- The lateral electric field peaks at the drain.
  - $\mathcal{E}_{peak}$ can be as high as 10^6 V/cm
- High E-field causes several problems:
  - impact ionization
    - → substrate current
  - damage to gate-oxide interface and bulk

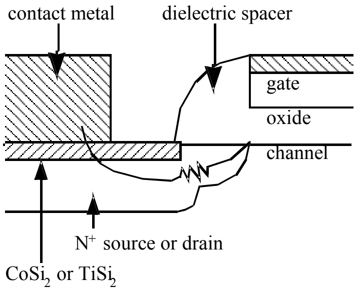
Lightly Doped Drain Structure



- Lower pn junction doping results in lower peak E-field
  - ✓ Hot-carrier effects reduced
  - ✗ Series resistance increased

Parasitic Source-Drain Resistance

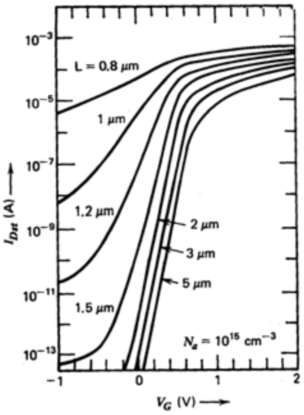




- If $I_{Dsat0} \propto V_{GS} - V_T$, $I_{Dsat} = \dfrac{I_{Dsat0}}{1 + \dfrac{I_{Dsat0} R_s}{(V_{GS} - V_T)}}$
  - I_{Dsat} is reduced by about 15% in a 0.1μm MOSFET.
  - $V_{Dsat} = V_{Dsat0} + I_{Dsat}(R_s + R_d)$

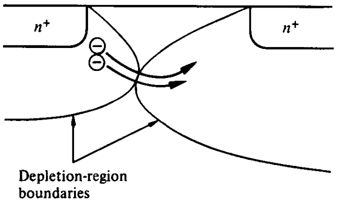
Drain Induced Barrier Lowering (DIBL)

- As the source & drain get closer, they become electrostatically coupled, so that the drain bias can affect the potential barrier to carrier flow at the source junction → subthreshold current increases.

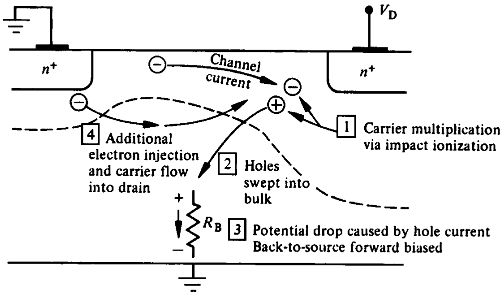


Excess Current Effects

- Punchthrough



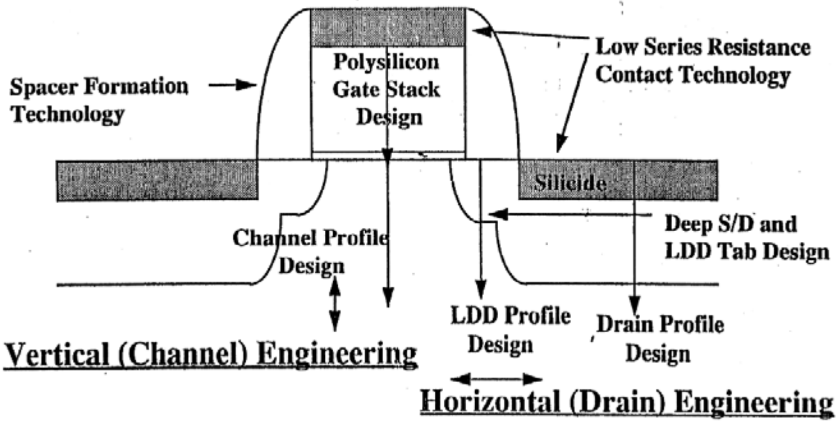
- Parasitic BJT action



Summary: MOSFET OFF State *vs.* ON State

- **Sub-threshold regime ($V_{GS} < V_T$):**
  - I_{DS} is limited by the rate at which carriers diffuse across the source pn junction
  - Subthreshold swing S, DIBL are issues
- **ON state ($V_{GS} > V_T$):**
  - I_{DS} is limited by the rate at which carriers drift across the channel
  - Punchthrough and parasitic BJT effects are of concern, particularly at high drain bias
    - I_{Dsat} increases rapidly with V_{DS}
  - Parasitic series resistances reduce drive current
    - source resistance R_S reduces effective V_{GS}
    - source and drain resistances R_S and R_D reduce effective V_{DS}

SUBMICRON DEVICE STRUCTURE AND DESIGN



Spacer Formation Technology

Polysilicon Gate Stack Design

Low Series Resistance Contact Technology

Silicide

Deep S/D and LDD Tab Design

Channel Profile Design

LDD Profile Design

Drain Profile Design

Vertical (Channel) Engineering

Horizontal (Drain) Engineering