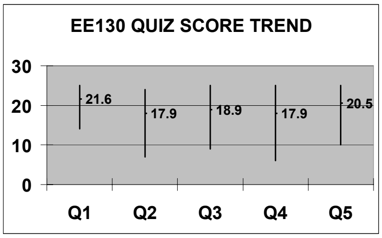
Lecture #25

- Design Project:
  - – Due in class (5 PM) on **Thursday May 1st**
    - 20 pt penalty for late submissions, accepted until 5 PM on 5/8
  - – Your BJT design does not need to meet the performance specifications when W_B and N_B are varied by +/- 10%
  - – Equation for ΔE_G assumes N_E is in cm^{-3} and T is in K
- Quiz#5 Results:

  (undergrad.'s only)
  N=60
  Mean=20.5
  Std.Dev.=3.6

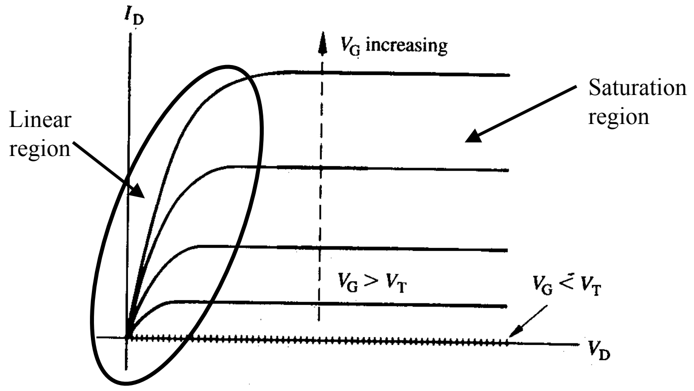


OUTLINE

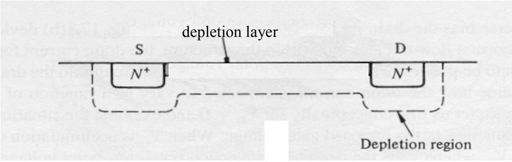
- NMOSFET *I-V*
- Effective mobility
- Transconductance
- PMOSFET *I-V*
- Subthreshold current

Ideal MOSFET *I-V* Characteristics

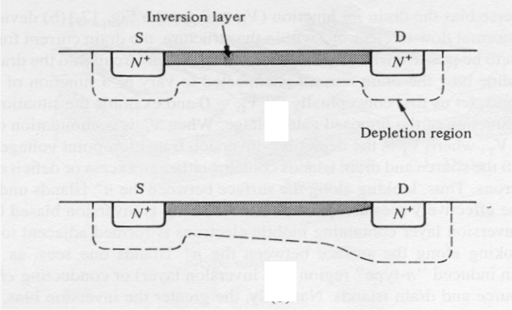
(Enhancement Mode NMOS Transistor)



Review: Qualitative Operation of the NMOSFET



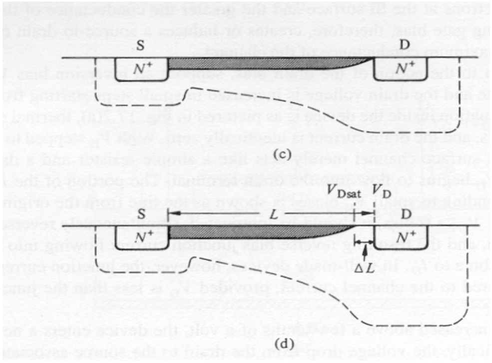
The potential barrier to electron flow from the source into the channel is lowered by applying $V_{GS} > V_T$

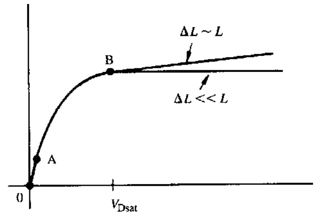


Electrons flow from the source to the drain by drift, when $V_{DS}>0$. ($I_{DS} > 0$.)

The channel potential varies from V_S at the source end to V_D at the drain end.

(The inversion layer can be modeled as a resistor.)





When V_D is increased to be equal to V_G-V_T, the inversion-layer charge density at the drain end of the channel equals zero, *i.e.* the channel becomes “pinched off”

As V_D is increased above V_G-V_T, the length ΔL of the “pinch-off” region increases. The voltage applied across the inversion layer is always $V_{Dsat}=V_{GS}-V_T$, and so the current saturates:

$$I_{Dsat} = I_{DS}\Big|_{V_{DS}=V_{Dsat}}$$

If ΔL is significant compared to L, then I_{DS} will increase slightly with increasing $V_{DS}>V_{Dsat}$, due to “channel-length modulation”

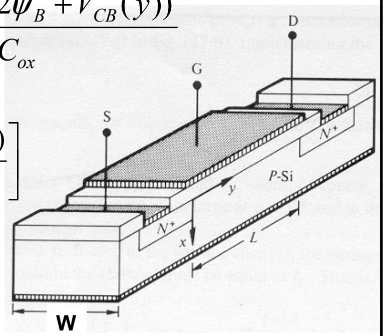
NMOSFET *I-V* Characteristics

- $V_D > V_S$
- Current in the channel flows by drift
- Channel voltage $V_C(y)$ varies continuously between the source and the drain

$$V_T = V_{FB} + V_C(y) + 2\psi_B + \frac{\sqrt{2qN_A\varepsilon_{Si}(2\psi_B + V_{CB}(y))}}{C_{ox}}$$

- Channel inversion charge

$$Q_{inv}(y) = -C_{oxe}\left[V_G - V_{FB} - V_C(y) - 2\psi_B - \frac{Q_{dep}(y)}{C_{oxe}}\right]$$



1^{st}-Order Approximation

- Neglect variation of Q_{dep} with *y*

$$Q_{dep} = \sqrt{2qN_A\varepsilon_{Si}(2\psi_B + V_{SB})}$$

$$\Rightarrow \quad Q_{inv} = -C_{oxe}\left[V_G - V_T + V_S - V_C\right]$$

where V_T **= threshold voltage at the source end**:

$$V_T = V_{FB} + V_S + 2\psi_B + \frac{\sqrt{2qN_A\varepsilon_{Si}(2\psi_B + V_{SB})}}{C_{ox}}$$

NMOSFET Current (1^{st}-order approx.)

- Consider an incremental length *dy* in the channel. The voltage drop across this region is

$$dV_C = I_{DS}dR = I_{DS}\frac{dy}{\sigma W T_{inv}} = I_{DS}\frac{dy}{q\mu_{eff}nWT_{inv}} = -\frac{I_{DS}dy}{Q_{inv}\mu_{eff}W}$$

$$\int_0^L I_{DS}dy = -\int_{V_S}^{V_D}\mu_{eff}WQ_{inv}(V_C)dV_C$$

$$I_{DS} = -\frac{W}{L}\mu_{eff}\int_{V_S}^{V_D}Q_{inv}(V_C)dV_C$$

$$I_{DS} = \frac{W}{L}\mu_{eff}C_{oxe}\left[V_{GS} - V_T - \frac{V_{DS}}{2}\right]V_{DS}$$ in the linear region

$$I_{DS} = I_{Dsat} = \frac{W}{2L}C_{oxe}\mu_{eff}(V_{GS} - V_T)^2$$ in the saturation region

Effective Mobility

$$I_{DS} = WQ_{inv}v = WQ_{inv}\mu_{eff}\mathcal{E} = WQ_{inv}\mu_{eff}\left(\frac{V_{DS}}{L}\right)$$

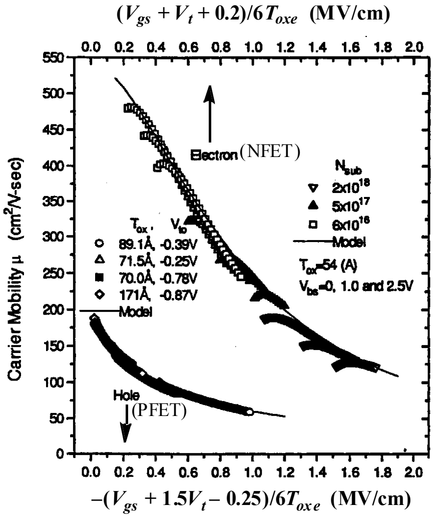
$$= (W/L)\mu_{eff}C_{oxe}(V_G - V_T)V_{DS}$$

where μ_{eff} is the ***effective electron mobility***

The NMOSFET can be modelled as a resistor at low V_{DS}:

$$R_{DS} = \frac{V_{DS}}{I_{DS}} = \frac{L}{W\mu_{eff}C_{oxe}(V_G - V_T)}$$

μ_{eff} *vs.* Effective Normal Field



Scattering mechanisms:

- coulombic scattering
- phonon scattering
- surface roughness scattering

The “Body Effect”

V_T is a function of V_{SB}:

$$V_T = V_{T0} + \frac{\sqrt{2qN_A\varepsilon_{Si}}}{C_{oxe}}\left(\sqrt{2\psi_B + V_{SB}} - \sqrt{2\psi_B}\right)$$
$$= V_{T0} + \gamma\left(\sqrt{2\psi_B + V_{SB}} - \sqrt{2\psi_B}\right)$$

where γ is the ***body effect parameter***

When the source-body pn junction is reverse-biased, $|V_T|$ increases. Usually, we want to minimize γ so that $I_{Dsat} \propto |V_{GS} - V_T|$ will be the same for all transistors in a circuit

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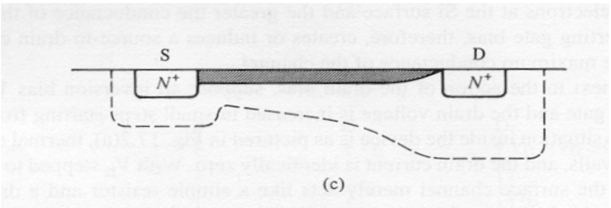
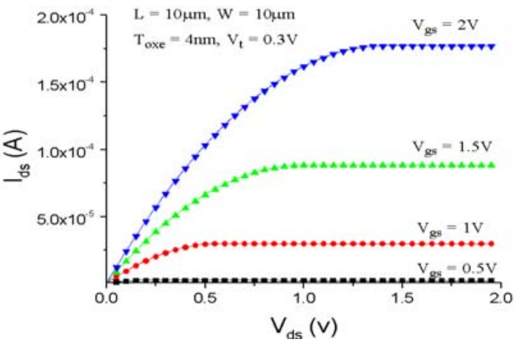
Problem with the “Square Law Theory”

- Assumes that gate charge is purely balanced by inversion charge
- Ignores variation in depletion width with distance y



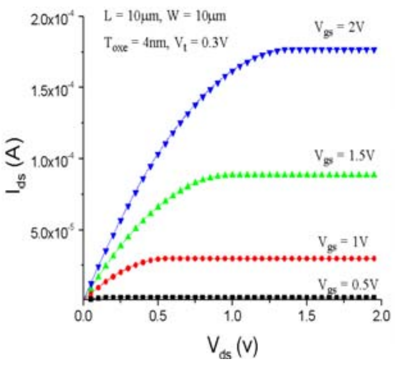
Modified Model



$$I_{DS} = \frac{W}{L} C_{oxe} \mu_{eff} (V_{GS} - V_T - \frac{m}{2} V_{DS}) V_{DS}$$

$$\text{where } m = 1 + \frac{C_{dm}}{C_{oxe}} = 1 + \frac{3T_{oxe}}{W_{dm}} \quad \text{since } \varepsilon_{Si} = 3\varepsilon_{SiO_2}$$

Modified Model: I_{Dsat} & Transconductance



- saturation region:

$$V_D \geq V_{Dsat} = \frac{V_{GS} - V_T}{m}$$

$$\boxed{I_{Dsat} = \frac{W}{2mL} C_{oxe} \mu_{eff} (V_{GS} - V_T)^2}$$

- transconductance: $g_m = dI_{DS}/dV_{GS}$

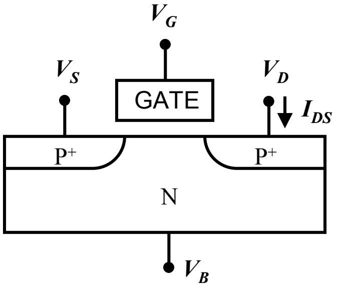
$$g_{msat} = \frac{W}{mL} C_{oxe} \mu_{eff} (V_{GS} - V_T)$$

MOSFET V_T Measurement

- V_T can be determined by plotting I_{DS} *vs.* V_{GS}, using a low value of V_{DS}

P-Channel MOSFET

- The PMOSFET turns on when $V_{GS} < V_{Tp}$
  - – Holes flow from SOURCE to DRAIN
    - ⇒ DRAIN is biased at a ***lower*** potential than the SOURCE



- **V_{DS} < 0**
- **I_{DS} < 0**
- $|I_{DS}|$ increases with
  - $|V_{GS} - V_{Tp}|$
  - $|V_{DS}|$ (linear region)

- In CMOS technology, the threshold voltages are usually symmetric: $V_{Tp} = -V_{Tn}$

PMOSFET *I-V*

- Linear region: $0 < |V_{DS}| < \dfrac{|V_{GS} - V_{Tp}|}{m}$

$$I_{DS} = -\frac{W}{L} C_{oxe} \mu_{p,eff} (V_{GS} + V_{Tp} - \frac{m}{2} V_{DS}) V_{DS}$$

- Saturation region: $|V_{DS}| > \dfrac{|V_{GS} - V_{Tp}|}{m}$

$$I_{DS} = I_{Dsat} = -\frac{W}{2mL} C_{oxe} \mu_{p,eff} (V_{GS} - V_{Tp})^2$$

$m = 1 + (3T_{\text{oxe}}/W_{\text{dm}})$ is the bulk-charge factor

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Sub-Threshold Leakage Current

- We had previously assumed that there is no channel current when $V_{\text{GS}} < V_{\text{T}}$. This is incorrect.
- Consider V_{S} close to $2\psi_{\text{B}}$: There is some inversion charge at the surface, which gives rise to subthreshold current flowing between the source and drain:

$$I_{DS} = \mu_{eff} C_{oxe} \frac{W}{L} (m-1) \left(\frac{kT}{q}\right)^2 e^{q(V_G - V_T)/mkT} (1 - e^{-qV_{DS}/kT})$$

Sub-Threshold Slope *S*

$$S \equiv \left(\frac{d(\log_{10} I_{DS})}{dV_{GS}} \right)^{-1}$$

$$= \frac{kT}{q} \ln(10)(1 + \frac{C_{dm}}{C_{oxe}})$$

V_T Design Tradeoff