Lecture #22

OUTLINE

The MOS Capacitor

- Capacitance
- Effect of Oxide Charges

Reading: Course Reader (Part III, Chap. 2)

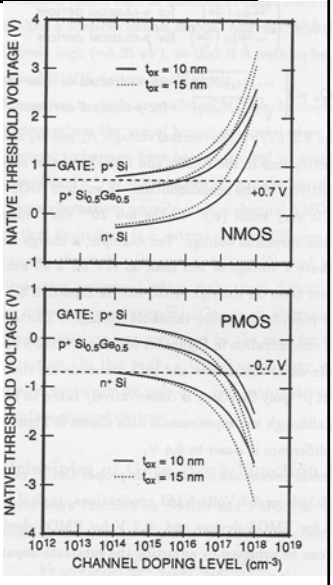
Review: Threshold Voltage

- For p-type Si ("NMOS"):

$$V_T = V_{FB} + 2\psi_B + \frac{\sqrt{2qN_A\varepsilon_{Si}(2\psi_B)}}{C_{ox}}$$

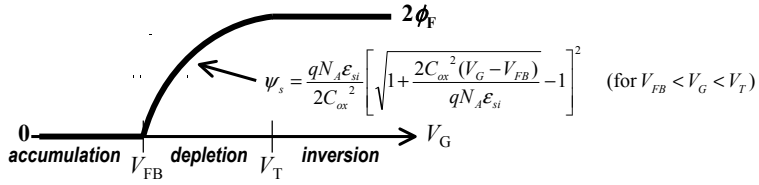
- For n-type Si ("PMOS"):

$$V_T = V_{FB} + 2\psi_B - \frac{\sqrt{2qN_D\varepsilon_{Si}|2\psi_B|}}{C_{ox}}$$

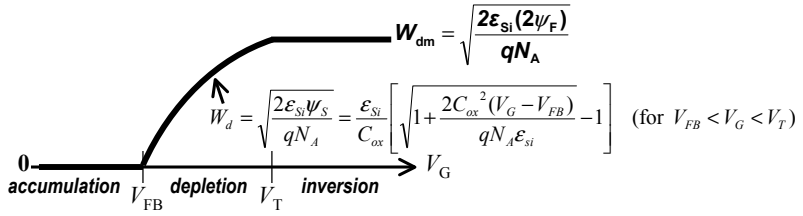


ψ_s and W_d vs. V_G (p-type Si)

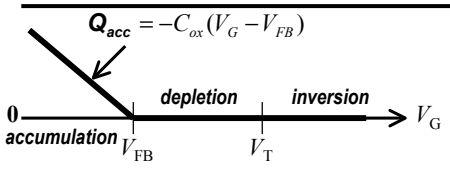
ψ_s:

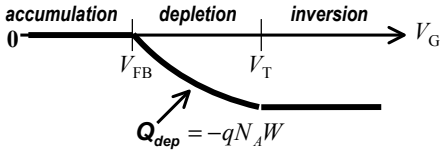


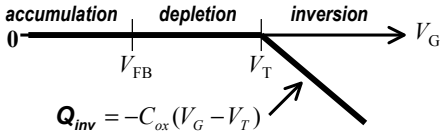
W_d:



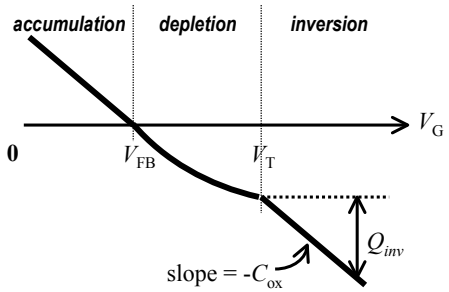
Total Charge Density in Si, Q_s



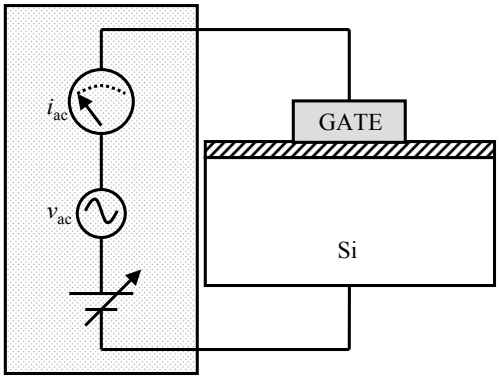




$$Q_s = Q_{acc} + Q_{dep} + Q_{inv}$$



MOS Capacitance Measurement



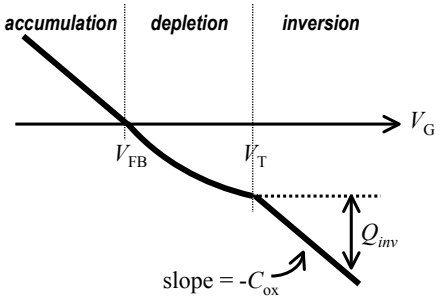
C-V Meter MOS Capacitor

- V_G is scanned slowly
- Capacitive current due to v_{ac} is measured

$$i_{ac} = C\frac{dv_{ac}}{dt}$$

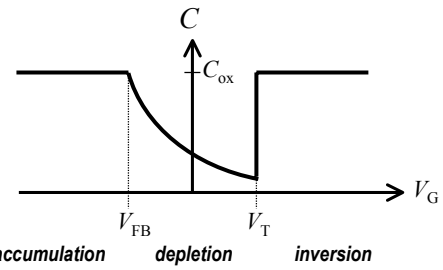
$$C = \left|\frac{dQ_{GATE}}{dV_G}\right| = \left|\frac{dQ_s}{dV_G}\right|$$

MOS *C-V* Characteristics (p-type Si)



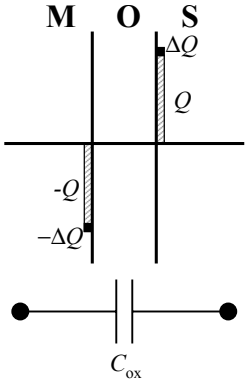
$$C = \left|\frac{dQ_s}{dV_G}\right|$$

Ideal *C-V* curve:



Capacitance in Accumulation (p-type Si)

- As the gate voltage is varied, incremental charge is added/subtracted to/from the gate and substrate.
- The incremental charges are separated by the gate oxide.



$$C = \left| \frac{dQ_{acc}}{dV_G} \right| = C_{ox}$$

Flat-Band Capacitance

- At the flat-band condition, variations in V_G give rise to the addition/subtraction of incremental charge in the substrate, at a depth L_D
- L_D is the "extrinsic Debye Length"
  - characteristic shielding distance, or the distance where the electric field emanating from a perturbing charge falls off by a factor of 1/e

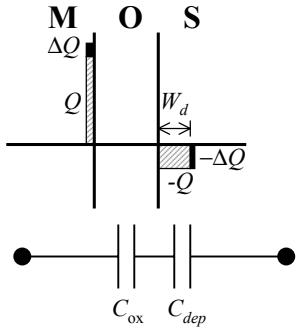
$$L_D = \sqrt{\frac{\varepsilon_{Si} kT}{q^2 N_A}}$$

$$\frac{1}{C_{FB}} = \frac{1}{C_{ox}} + \frac{L_D}{\varepsilon_{Si}}$$

Capacitance in Depletion (p-type Si)

- As the gate voltage is varied, the width of the depletion region varies.

→ Incremental charge is effectively added/subtracted at a depth W_d in the substrate.



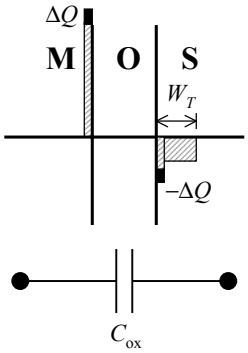
$$C = \left|\frac{dQ_{dep}}{dV_G}\right| = \sqrt{\frac{1}{C_{ox}^{\ 2}} + \frac{2(V_G - V_{FB})}{qN_A\varepsilon_{Si}}}$$

$$\frac{1}{C} = \frac{1}{C_{ox}} + \frac{1}{C_{dep}} = \frac{1}{C_{ox}} + \frac{W_d}{\varepsilon_{Si}}$$

Capacitance in Inversion (p-type Si)

CASE 1: Inversion-layer charge can be supplied/removed quickly enough to respond to changes in the gate voltage.

→ Incremental charge is effectively added/subtracted at the surface of the substrate.



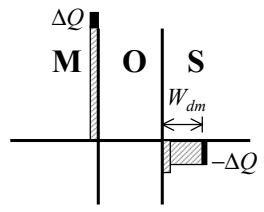
Time required to build inversion-layer charge = $2N_A\tau_o/n_i$, where
τ_o = minority-carrier lifetime at surface

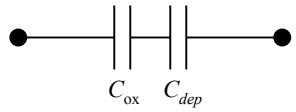
$$C = \left|\frac{dQ_{inv}}{dV_G}\right| = C_{ox}$$

Capacitance in Inversion (p-type Si)

CASE 2: Inversion-layer charge cannot be supplied/removed quickly enough to respond to changes in the gate voltage.

→ Incremental charge is effectively added/subtracted at a depth W_d in the substrate.





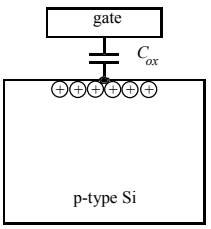
$$\frac{1}{C} = \frac{1}{C_{ox}} + \frac{1}{C_{dep}}$$

$$= \frac{1}{C_{ox}} + \frac{W_{dm}}{\varepsilon_{Si}}$$

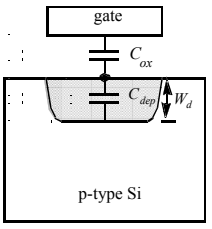
$$= \frac{1}{C_{ox}} + \sqrt{\frac{2(2\psi_B)}{qN_A\varepsilon_{Si}}} \equiv \frac{1}{C_{\min}}$$

Supply of Substrate Charge (p-type Si)

Accumulation:

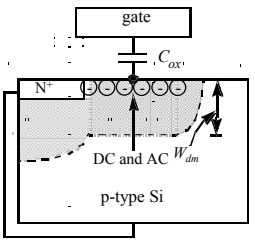


Depletion:

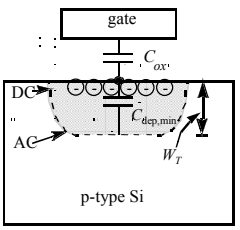


Inversion:

Case 1

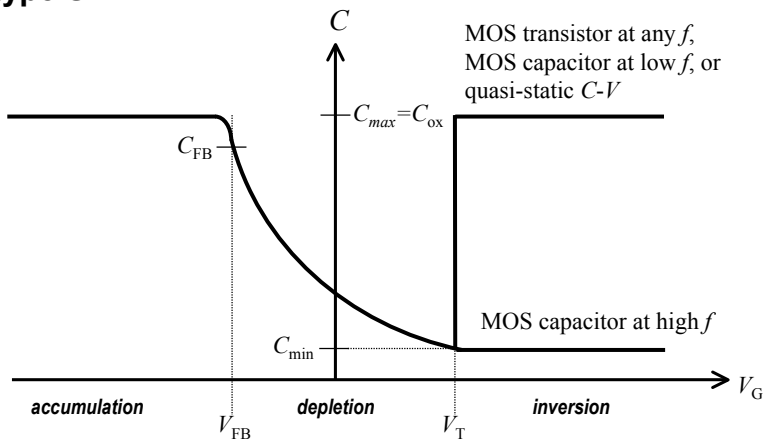


Case 2



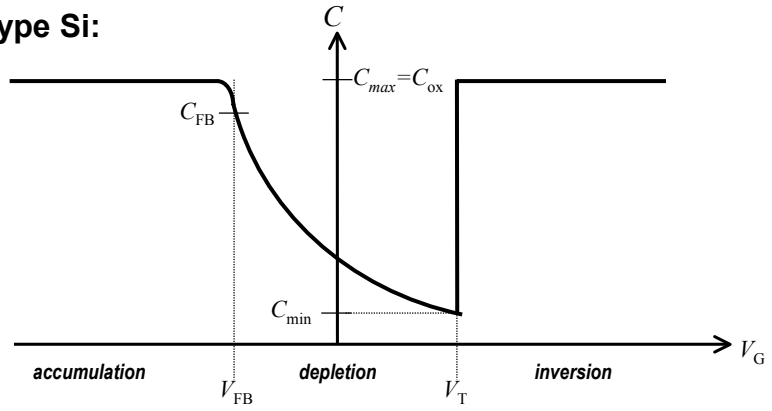
Capacitor *vs.* Transistor *C-V* (or LF *vs.* HF *C-V*)

p-type Si:



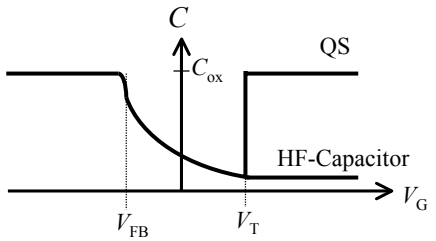
Quasi-Static *C-V* Measurement

p-type Si:



The quasi-static *C-V* characteristic is obtained by **slowly** ramping the gate voltage (< 0.1V/s), while measuring the gate current I_G with a very sensitive DC ammeter. *C* is calculated from $I_G = C \cdot dV_G/dt$.

Examples: *C-V* Characteristics



Does the QS or the HF-capacitor C-V characteristic apply?

(1) MOS capacitor, f=10kHz.

(2) MOS transistor, f=1MHz.

(3) MOS capacitor, slow V_G ramp.

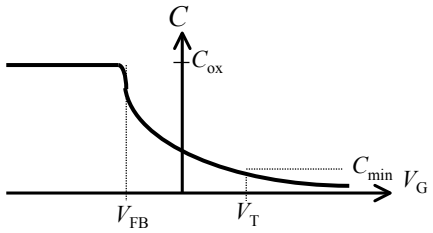
(4) MOS transistor, slow V_G ramp.

Deep Depletion

- If V_G is scanned quickly, Q_{inv} cannot respond to the change in V_G. The increase in substrate charge density Q_s must then come from an increase in depletion charge density Q_{dep}

  $\Rightarrow$ depletion depth W_d increases as V_G increases

  $\Rightarrow$ C decreases as V_G increases

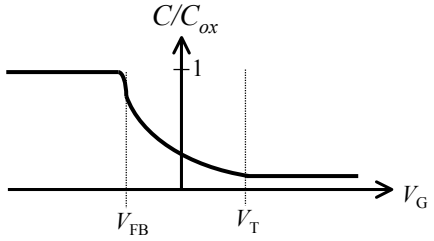


Parameter Extraction from *C-V*

From a single *C-V* measurement, we can extract much information about the MOS device.

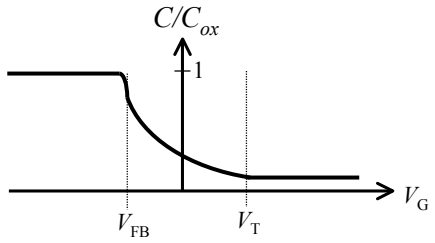
- Suppose we know that the gate-electrode material is heavily doped n-type poly-Si (Φ_M=4.05eV), and that the gate dielectric is SiO_2 (ε_r=3.9):
  - From $C_{max} = C_{ox}$ we determine the oxide thickness t_{ox}
  - From C_{min} and C_{ox} we determine substrate doping (by iteration)
  - From substrate doping and C_{ox} we calculate the flat-band capacitance C_{FB}
  - From the *C-V* curve, we can find $V_{FB} = V_G\big|_{C=C_{FB}}$
  - From Φ_M, Φ_S, C_{ox}, and V_{FB} we can determine Q_f

Example: Effect of Doping



- How would *C-V* characteristic change if substrate doping N_A were increased?
  - V_{FB}
  - V_T
  - C_{min}

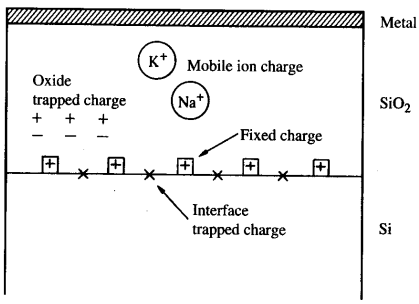
Example: Effect of Oxide Thickness



- How would *C-V* characteristic change if oxide thickness t_{ox} were decreased?
  - V_{FB}
  - V_T
  - C_{min}

Oxide Charges

In real MOS devices, there is always some charge in the oxide and at the Si/oxide interface.



- In the oxide:
  - Trapped charge Q_{ot}
    - High-energy electrons and/or holes injected into oxide
  - Mobile charge Q_M
    - Alkali-metal ions, which have sufficient mobility to drift in oxide under an applied electric field
- At the interface:
  - Fixed charge Q_F
    - Excess Si (?)
  - Trapped charge Q_{it}
    - Dangling bonds

Effect of Oxide Charges

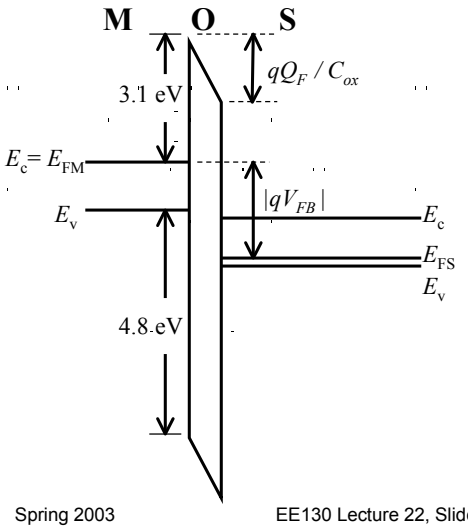
- In general, charges in the oxide cause a shift in the gate voltage required to reach the threshold condition:

$$\Delta V_T = -\frac{1}{\varepsilon_{SiO_2}} \int_0^{t_{ox}} x \rho_{ox}(x) dx$$

(*x* defined to be 0 at metal-oxide interface)

- In addition, they may alter the field-effect mobility of mobile carriers (in a MOSFET) due to Coulombic scattering

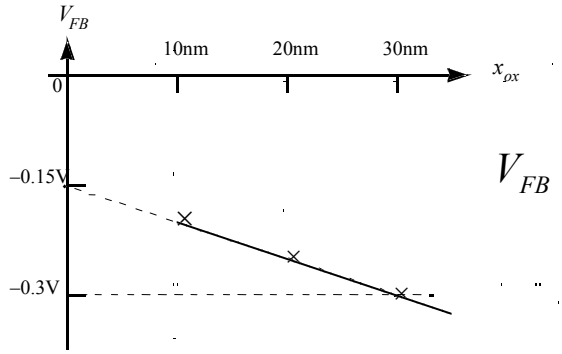
Fixed Oxide Charge Q_F



$$V_{FB} = \phi_{MS} - \frac{Q_F}{C_{ox}}$$

Determination of Q_F

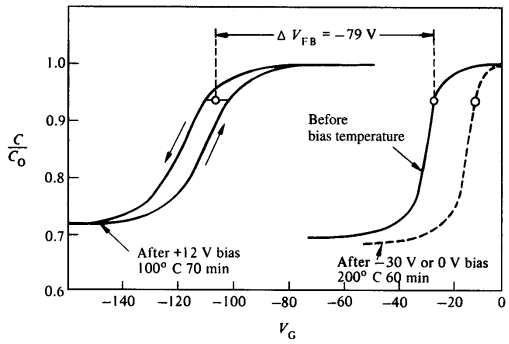
Measure *C-V* characteristics of capacitors with different oxide thicknesses. Plot V_{FB} as a function of t_{ox}.



$$V_{FB} = \phi_{MS} - \frac{t_{ox}}{\varepsilon_{SiO_2}} Q_F$$

Mobile Ions

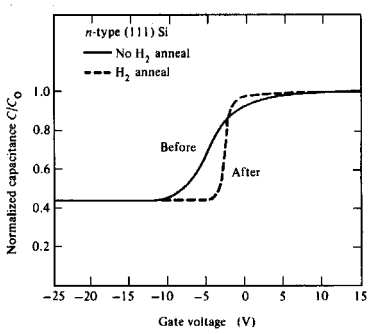
- Odd shifts in *C-V* characteristics were once a mystery:

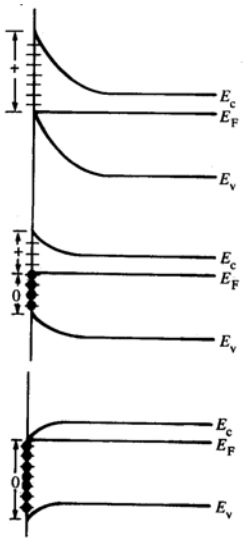


$$\Delta V_{FB} = -\frac{Q_M}{C_{ox}}$$

- Source of problem: Mobile charge moving to/away from interface, changing charge centroid

Interface Traps





Traps cause "sloppy" *C-V* and also greatly degrade mobility in channel

$$\Delta V_G = -\frac{Q_{IT}(\psi_S)}{C_{ox}}$$