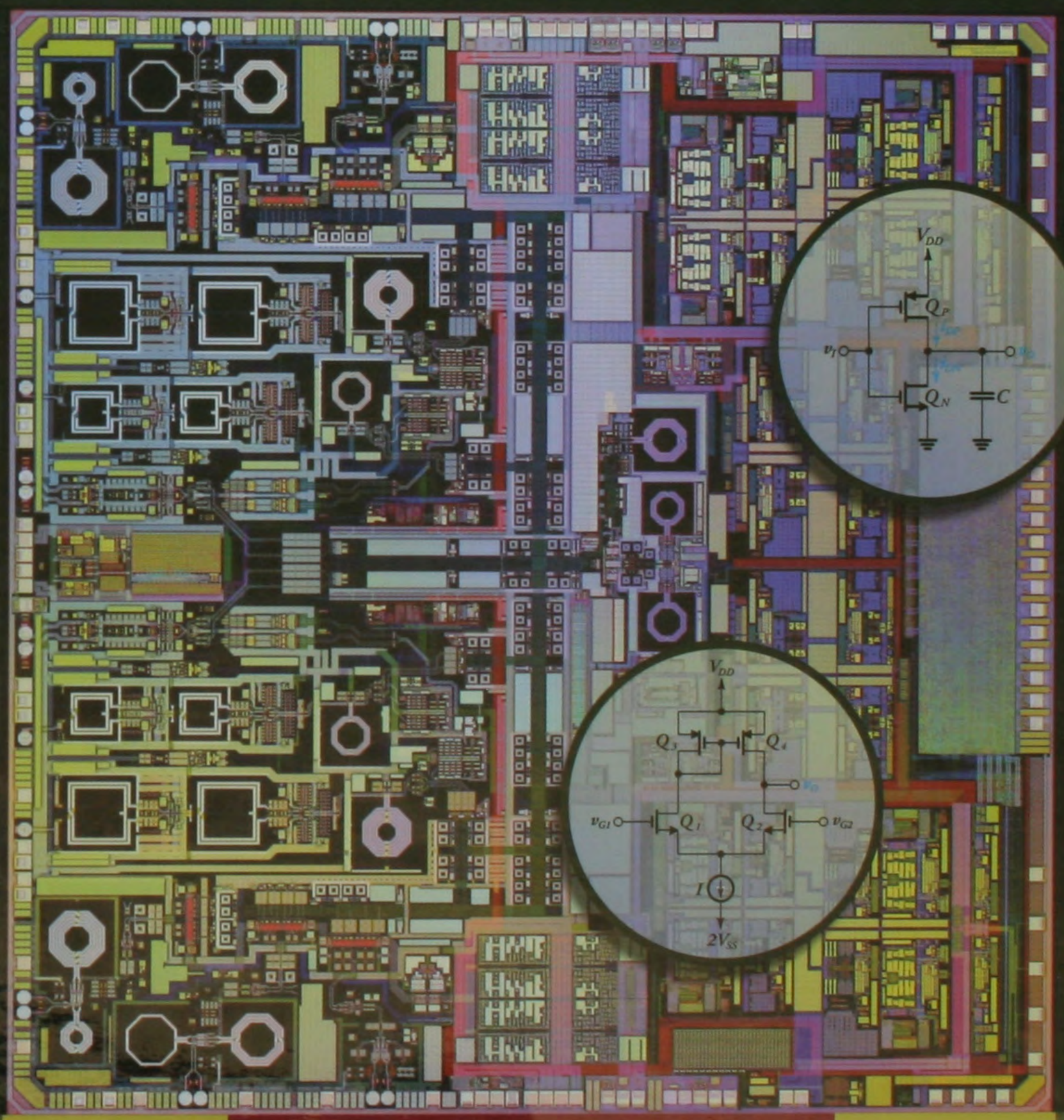
Enclosed DVD includes stu
versions of Nati
Instruments™ Multi
software and Cad
PSpice® softw
See the
c

SEDRA/SMITH

Microelectronic Circuits



SIXTH EDITION

Microelectronic Circuits

SIXTH EDITION

Microelectronic Circuits

Adel S. Sedra
University of Waterloo

Kenneth C. Smith
University of Toronto

New York Oxford
OXFORD UNIVERSITY PRESS
2010

Oxford University Press, Inc., publishes works that further Oxford University's objective of excellence in research, scholarship, and education.

Oxford New York
Auckland Cape Town Dar es Salaam Hong Kong Karachi
Kuala Lumpur Madrid Melbourne Mexico City Nairobi
New Delhi Shanghai Taipei Toronto

With offices in
Argentina Austria Brazil Chile Czech Republic France Greece
Guatemala Hungary Italy Japan Poland Portugal Singapore
South Korea Switzerland Thailand Turkey Ukraine Vietnam

Published by Oxford University Press, Inc.
198 Madison Avenue, New York, New York 10016
http://www.oup.com

Oxford is a registered trademark of Oxford University Press

Library of Congress Cataloging-in-Publication Data

Sedra, Adel S.
Microelectronic circuits / Adel S. Sedra, Kenneth C. Smith.—6th ed.
p. cm.—(The Oxford series in electrical and computer engineering)
ISBN 978-0-19-532303-0
1. Electronic circuits. 2. Integrated circuits. I. Smith, Kenneth Carless. II. Title.
TK7867.S39 2010
621.3815—dc22

2009042633

Cover Photo: The device is a fully integrated triple-band, dual-arm WiMAX RFIC targeted at broadband wireless access applications, including fixed and mobile terminals, as well as pico and femto base stations. The multiple frequency bands enable equipment to be readily adapted to different regional requirements, while the dual-arm (dual-channel) arrangement allows the use of Multiple-Input/Multiple-Output (MIMO) technology. It illustrates the high degree of integration required by the latest wireless standards, incorporating high-quality Phase-Locked Loops, Radio Frequency Low-Noise Amplifiers, Mixers, and Power Amplifier stages, as well as programmable baseband filters and digital circuitry for control and calibration. (Photo credit: PMC-Sierra, the premier Internet infrastructure solutions provider. NASDAQ:PMCS) **Circuits:** Analog (Active-loaded Differential Amplifier). Digital (CMOS Inverter).

Printing number: 9 8 7 6 5 4 3 2 1

Printed in the United States of America
on acid-free paper

BRIEF TABLE OF CONTENTS

Preface xxii

PART I **DEVICES AND BASIC CIRCUITS** 2

1 Signals and Amplifiers 4
2 Operational Amplifiers 52
3 Semiconductors 124
4 Diodes 164
5 MOS Field-Effect Transistors (MOSFETs) 230
6 Bipolar Junction Transistors (BJTs) 350

PART II **INTEGRATED-CIRCUIT AMPLIFIERS** 490

7 Building Blocks of Integrated-Circuit Amplifiers 492
8 Differential and Multistage Amplifiers 586
9 Frequency Response 686
10 Feedback 802
11 Output Stages and Power Amplifiers 910
12 Operational Amplifier Circuits 974

PART III **DIGITAL INTEGRATED CIRCUITS** 1058

13 CMOS Digital Logic Circuits 1060
14 Advanced MOS and Bipolar Logic Circuits 1142
15 Memory Circuits 1202

PART IV **FILTERS AND OSCILLATORS** 1252

16 Filters and Tuned Amplifiers 1254
17 Signal Generators and Waveform-Shaping Circuits 1334

Appendixes

A VLSI Fabrication Technology **A-1** (on DVD)
B SPICE Device Models and Design and Simulation Examples Using PSpice® and Multisim™ **B-1** (on DVD)
C Two-Port Network Parameters **C-1** (on DVD)
D Some Useful Network Theorems **D-1** (on DVD)
E Single-Time-Constant Circuits **E-1** (on DVD)
F *s*-Domain Analysis: Poles, Zeros, and Bode Plots **F-1** (on DVD)
G Bibliography **G-1** (on DVD)
H Standard Resistance Values and Unit Prefixes **H-1**
I Answers to Selected Problems **I-1**

Index **IN-1**

TABLE OF CONTENTS

Preface xxii

PART I DEVICES AND BASIC CIRCUITS 2

1 Signals and Amplifiers 4
Introduction 5
1.1 Signals 6
1.2 Frequency Spectrum of Signals 9
1.3 Analog and Digital Signals 11
1.4 Amplifiers 14
1.4.1 Signal Amplification 14
1.4.2 Amplifier Circuit Symbol 15
1.4.3 Voltage Gain 15
1.4.4 Power Gain and Current Gain 16
1.4.5 Expressing Gain in Decibels 17
1.4.6 Amplifier Power Supplies 17
1.4.7 Amplifier Saturation 19
1.4.8 Symbol Convention 20
1.5 Circuit Models for Amplifiers 21
1.5.1 Voltage Amplifiers 22
1.5.2 Cascaded Amplifiers 24
1.5.3 Other Amplifier Types 26
1.5.4 Relationships Between the Four Amplifier Models 27
1.5.5 Determining R_i and R_o 27
1.5.6 Unilateral Models 28
1.6 Frequency Response of Amplifiers 30
1.6.1 Measuring the Amplifier Frequency Response 30
1.6.2 Amplifier Bandwidth 31
1.6.3 Evaluating the Frequency Response of Amplifiers 31
1.6.4 Single-Time-Constant Networks 33
1.6.5 Classification of Amplifiers Based on Frequency Response 38
Summary 41
Problems 42

2 Operational Amplifiers 52
Introduction 53
2.1 The Ideal Op Amp 54
2.1.1 The Op-Amp Terminals 54
2.1.2 Function and Characteristics of the Ideal Op Amp 55
2.1.3 Differential and Common-Mode Signals 57
2.2 The Inverting Configuration 58
2.2.1 The Closed-Loop Gain 59
2.2.2 Effect of the Finite Open-Loop Gain 61
2.2.3 Input and Output Resistances 62
2.2.4 An Important Application: The Weighted Summer 65
2.3 The Noninverting Configuration 67
2.3.1 The Closed-Loop Gain 67
2.3.2 Effect of the Finite Open-Loop Gain 69
2.3.3 Input and Output Resistances 69
2.3.4 The Voltage Follower 69
2.4 Difference Amplifiers 71
2.4.1 A Single Op-Amp Difference Amplifier 72
2.4.2 A Superior Circuit: The Instrumentation Amplifier 76
2.5 Integrators and Differentiators 80
2.5.1 The Inverting Configuration with General Impedances 80
2.5.2 The Inverting Integrator 82
2.5.3 The Op-Amp Differentiator 87
2.6 DC Imperfections 88
2.6.1 Offset Voltage 89
2.6.2 Input Bias and Offset Currents 93
2.6.3 Effect of V_{OS} and I_{OS} on the Operation of the Inverting Integrator 96
2.7 Effect of Finite Open-Loop Gain and Bandwidth on Circuit Performance 97
2.7.1 Frequency Dependence of the Open-Loop Gain 97

2.7.2 Frequency Response of the Closed-Loop Amplifier 99
2.8 Large-Signal Operation of Op Amps 102
2.8.1 Output Voltage Saturation 102
2.8.2 Output Current Limits 102
2.8.3 Slew Rate 104
2.8.4 Full-Power Bandwidth 106
Summary 107
Problems 108

3 Semiconductors 124
Introduction 125
3.1 Intrinsic Semiconductors 125
3.2 Doped Semiconductors 126
3.3 Current Flow in Semiconductors 132
3.3.1 Drift Current 132
3.3.2 Diffusion Current 135
3.3.3 Relationship Between D and μ 138
3.4 The *pn* Junction with Open-Circuit Terminals (Equilibrium) 138
3.4.1 Physical Structure 138
3.4.2 Operation with Open-Circuit Terminals 139
3.5 The *pn* Junction with Applied Voltage 145
3.5.1 Qualitative Description of Junction Operation 145
3.5.2 The Current–Voltage Relationship of the Junction 147
3.5.3 Reverse Breakdown 152
3.6 Capacitive Effects in the *pn* Junction 154
3.6.1 Depletion or Junction Capacitance 154
3.6.2 Diffusion Capacitance 156
Summary 157
Problems 159

4 Diodes 164
Introduction 165
4.1 The Ideal Diode 166
4.1.1 Current–Voltage Characteristic 166
4.1.2 A Simple Application: The Rectifier 167
4.1.3 Another Application: Diode Logic Gates 170
4.2 Terminal Characteristics of Junction Diodes 173
4.2.1 The Forward-Bias Region 175
4.2.2 The Reverse-Bias Region 178
4.2.3 The Breakdown Region 178
4.3 Modeling the Diode Forward Characteristic 179
4.3.1 The Exponential Model 179
4.3.2 Graphical Analysis Using the Exponential Model 180
4.3.3 Iterative Analysis Using the Exponential Model 180
4.3.4 The Need for Rapid Analysis 181
4.3.5 The Constant-Voltage-Drop Model 181
4.3.6 The Ideal-Diode Model 183
4.3.7 The Small-Signal Model 184
4.3.8 Use of the Diode Forward Drop in Voltage Regulation 187
4.4 Operation in the Reverse Breakdown Region—Zener Diodes 189
4.4.1 Specifying and Modeling the Zener Diode 190
4.4.2 Use of the Zener as a Shunt Regulator 191
4.4.3 Temperature Effects 194
4.4.4 A Final Remark 194
4.5 Rectifier Circuits 194
4.5.1 The Half-Wave Rectifier 195
4.5.2 The Full-Wave Rectifier 197
4.5.3 The Bridge Rectifier 199
4.5.4 The Rectifier with a Filter Capacitor—The Peak Rectifier 200
4.5.5 Precision Half-Wave Rectifier—The Super Diode 206
4.6 Limiting and Clamping Circuits 207
4.6.1 Limiter Circuits 207
4.6.2 The Clamped Capacitor or DC Restorer 210
4.6.3 The Voltage Doubler 212
4.7 Special Diode Types 213
4.7.1 The Schottky-Barrier Diode (SBD) 213
4.7.2 Varactors 214
4.7.3 Photodiodes 214
4.7.4 Light-Emitting Diodes (LEDs) 214
Summary 215
Problems 216

5 MOS Field-Effect Transistors (MOSFETs) 230
Introduction 231
5.1 Device Structure and Physical Operation 232

5.1.1 Device Structure 232
5.1.2 Operation with Zero Gate Voltage 234
5.1.3 Creating a Channel for Current Flow 234
5.1.4 Applying a Small v_{DS} 236
5.1.5 Operation as v_{DS} is Increased 239
5.1.6 Operation for $v_{DS} \geq v_{OV}$ 242
5.1.7 The *p*-Channel MOSFET 244
5.1.8 Complementary MOS or CMOS 246
5.1.9 Operating the MOS Transistor in the Subthreshold Region 246
5.2 Current–Voltage Characteristics 247
5.2.1 Circuit Symbol 247
5.2.2 The i_D–v_{DS} Characteristics 248
5.2.3 The i_D–v_{GS} Characteristic 250
5.2.4 Finite Output Resistance in Saturation 253
5.2.5 Characteristics of the *p*-Channel MOSFET 256
5.3 MOSFET Circuits at DC 258
5.4 Applying the MOSFET in Amplifier Design 268
5.4.1 Obtaining a Voltage Amplifier 268
5.4.2 The Voltage Transfer Characteristic (VTC) 268
5.4.3 Biasing the MOSFET to Obtain Linear Amplification 269
5.4.4 The Small-Signal Voltage Gain 270
5.4.5 Determining the VTC by Graphical Analysis 274
5.4.6 Locating the Bias Point Q 275
5.5 Small-Signal Operation and Models 276
5.5.1 The DC Bias Point 276
5.5.2 The Signal Current in the Drain Terminal 277
5.5.3 Voltage Gain 279
5.5.4 Separating the DC Analysis and the Signal Analysis 279
5.5.5 Small-Signal Equivalent Circuit Models 280
5.5.6 The Transconductance g_m 282
5.5.7 The T Equivalent Circuit Model 287
5.5.8 Summary 290
5.6 Basic MOSFET Amplifier Configurations 291
5.6.1 The Three Basic Configurations 292
5.6.2 Characterizing Amplifiers 293
5.6.3 The Common-Source Configuration 294
5.6.4 The Common-Source Amplifier with a Source Resistance 297
5.6.5 The Common-Gate Amplifier 300
5.6.6 The Common-Drain Amplifier or Source Follower 302
5.6.7 Summary and Comparisons 305
5.7 Biasing in MOS Amplifier Circuits 306
5.7.1 Biasing by Fixing V_{GS} 307
5.7.2 Biasing by Fixing V_G and Connecting a Resistance in the Source 308
5.7.3 Biasing Using a Drain-to-Gate Feedback Resistance 311
5.7.4 Biasing Using a Constant-Current Source 312
5.7.5 A Final Remark 314
5.8 Discrete-Circuit MOS Amplifiers 314
5.8.1 The Basic Structure 314
5.8.2 The Common-Source (CS) Amplifier 316
5.8.3 The Common-Source Amplifier with a Source Resistance 318
5.8.4 The Common-Gate Amplifier 318
5.8.5 The Source Follower 321
5.8.6 The Amplifier Bandwidth 322
5.9 The Body Effect and Other Topics 323
5.9.1 The Role of the Substrate—The Body Effect 323
5.9.2 Modeling the Body Effect 324
5.9.3 Temperature Effects 325
5.9.4 Breakdown and Input Protection 325
5.9.5 Velocity Saturation 326
5.9.6 The Depletion-Type MOSFET 326
Summary 328
Problems 329

6 Bipolar Junction Transistors (BJTs) 350
Introduction 351
6.1 Device Structure and Physical Operation 352
6.1.1 Simplified Structure and Modes of Operation 352
6.1.2 Operation of the *npn* Transistor in the Active Mode 353
6.1.3 Structure of Actual Transistors 361
6.1.4 Operation in the Saturation Mode 362

6.1.5 The *pnp* Transistor 364
6.2 Current–Voltage Characteristics 365
6.2.1 Circuit Symbols and Conventions 365
6.2.2 Graphical Representation of Transistor Characteristics 370
6.2.3 Dependence of i_C on the Collector Voltage—The Early Effect 371
6.2.4 An Alternative Form of the Common-Emitter Characteristics 374
6.3 BJT Circuits at DC 378
6.4 Applying the BJT in Amplifier Design 396
6.4.1 Obtaining a Voltage Amplifier 396
6.4.2 The Voltage Transfer Characteristic (VTC) 397
6.4.3 Biasing the BJT to Obtain Linear Amplification 397
6.4.4 The Small-Signal Voltage Gain 399
6.4.5 Determining the VTC by Graphical Analysis 401
6.4.6 Locating the Bias Point Q 402
6.5 Small-Signal Operation and Models 403
6.5.1 The Collector Current and the Transconductance 404
6.5.2 The Base Current and the Input Resistance at the Base 406
6.5.3 The Emitter Current and the Input Resistance at the Emitter 407
6.5.4 Voltage Gain 408
6.5.5 Separating the Signal and the DC Quantities 409
6.5.6 The Hybrid-π Model 410
6.5.7 The T Model 411
6.5.8 Small-Signal Models of the *pnp* Transistor 412
6.5.9 Application of the Small-Signal Equivalent Circuits 412
6.5.10 Performing Small-Signal Analysis Directly on the Circuit Diagram 419
6.5.11 Augmenting the Small-Signal Model to Account for the Early Effect 420
6.5.12 Summary 422
6.6 Basic BJT Amplifier Configurations 422
6.6.1 The Three Basic Configurations 424
6.6.2 Characterizing Amplifiers 425
6.6.3 The Common-Emitter Amplifier 427
6.6.4 The Common-Emitter Amplifier with an Emitter Resistance 432
6.6.5 The Common-Base (CB) Amplifier 436
6.6.6 The Common-Collector Amplifier or Emitter Follower 438
6.6.7 Summary and Comparisons 445
6.7 Biasing in BJT Amplifier Circuits 446
6.7.1 The Classical Discrete-Circuit Biasing Arrangement 447
6.7.2 A Two-Power-Supply Version of the Classical Bias Arrangement 450
6.7.3 Biasing Using a Collector-to-Base Feedback Resistor 451
6.7.4 Biasing Using a Constant-Current Source 452
6.8 Discrete-Circuit BJT Amplifier 453
6.8.1 The Basic Structure 453
6.8.2 The Common-Emitter Amplifier 455
6.8.3 The Common-Emitter Amplifier with an Emitter Resistance 457
6.8.4 The Common-Base Amplifier 459
6.8.5 The Emitter Follower 460
6.8.6 The Amplifier Frequency Response 461
6.9 Transistor Breakdown and Temperature Effects 463
6.9.1 Transistor Breakdown 463
6.9.2 Dependence of β on I_C and Temperature 464
Summary 465
Problems 466

PART II INTEGRATED-CIRCUIT AMPLIFIERS 490

7 Building Blocks of Integrated-Circuit Amplifiers 492
Introduction 493
7.1 IC Design Philosophy 494
7.2 The Basic Gain Cell 495
7.2.1 The CS and CE Amplifiers with Current-Source Loads 495
7.2.2 The Intrinsic Gain 496
7.2.3 Effect of the Output Resistance of the Current-Source Load 499
7.2.4 Increasing the Gain of the Basic Cell 505

7.3 The Cascode Amplifier 506
7.3.1 Cascoding 506
7.3.2 The MOS Cascode 507
7.3.3 Distribution of Voltage Gain in a Cascode Amplifier 514
7.3.4 The Output Resistance of a Source-Degenerated CS Amplifier 517
7.3.5 Double Cascoding 518
7.3.6 The Folded Cascode 519
7.3.7 The BJT Cascode 520
7.3.8 The Output Resistance of an Emitter-Degenerated CE Amplifier 524
7.3.9 BiCMOS Cascodes 525
7.4 IC Biasing—Current Sources, Current Mirrors, and Current-Steering Circuits 526
7.4.1 The Basic MOSFET Current Source 527
7.4.2 MOS Current-Steering Circuits 530
7.4.3 BJT Circuits 532
7.5 Current-Mirror Circuits with Improved Performance 537
7.5.1 Cascode MOS Mirrors 538
7.5.2 A Bipolar Mirror with Base-Current Compensation 539
7.5.3 The Wilson Current Mirror 539
7.5.4 The Wilson MOS Mirror 542
7.5.5 The Widlar Current Source 543
7.6 Some Useful Transistor Pairings 546
7.6.1 The CC-CE, CD-CS, and CD-CE Configurations 546
7.6.2 The Darlington Configuration 549
7.6.3 The CC-CB and CD-CG Configurations 550
Summary 553

Appendix 7.A Comparison of the MOSFET and BJT 554
7.A.1 Typical Values of IC MOSFET Parameters 554
7.A.2 Typical Values of IC BJT Parameters 556
7.A.3 Comparison of Important Characteristics 557
7.A.4 Combining MOS and Bipolar Transistors: BiCMOS Circuits 568
7.A.5 Validity of the Square-Law MOSFET Model 569
Problems 569

8 Differential and Multistage Amplifiers 586
Introduction 5587
8.1 The MOS Differential Pair 588
8.1.1 Operation with a Common-Mode Input Voltage 589
8.1.2 Operation with a Differential Input Voltage 593
8.1.3 Large-Signal Operation 594
8.2 Small-Signal Operation of the MOS Differential Pair 599
8.2.1 Differential Gain 599
8.2.2 The Differential Half-Circuit 601
8.2.3 The Differential Amplifier with Current-Source Loads 603
8.2.4 Cascode Differential Amplifier 604
8.2.5 Common-Mode Gain and Common-Mode Rejection Ratio (CMRR) 605
8.3 The BJT Differential Pair 612
8.3.1 Basic Operation 613
8.3.2 Input Common-Mode Range 615
8.3.3 Large-Signal Operation 616
8.3.4 Small-Signal Operation 618
8.3.5 Common-Mode Gain and CMRR 624
8.4 Other Nonideal Characteristics of the Differential Amplifier 629
8.4.1 Input Offset Voltage of the MOS Differential Amplifier 629
8.4.2 Input Offset Voltage of the Bipolar Differential Amplifier 632
8.4.3 Input Bias and Offset Currents of the Bipolar Differential Amplifier 634
8.4.4 A Concluding Remark 635
8.5 The Differential Amplifier with Active Load 635
8.5.1 Differential to Single-Ended Conversion 636
8.5.2 The Active-Loaded MOS Differential Pair 637
8.5.3 Differential Gain of the Active-Loaded MOS Pair 638
8.5.4 Common-Mode Gain and CMRR 641
8.5.5 The Bipolar Differential Pair with Active Load 644
8.6 Multistage Amplifiers 651
8.6.1 A Two-Stage CMOS Op Amp 651
8.6.2 A Bipolar Op Amp 657

Summary 666
Problems 667

9 Frequency Response 686
Introduction 687
9.1 Low-Frequency Response of the CS and CE Amplifiers 689
9.1.1 The CS Amplifier 689
9.1.2 The CE Amplifier 694
9.2 Internal Capacitive Effects and the High-Frequency Model of the MOSFET and the BJT 701
9.2.1 The MOSFET 701
9.2.2 The BJT 706
9.3 High-Frequency Response of the CS and CE Amplifiers 711
9.3.1 The Common-Source Amplifier 712
9.3.2 The Common-Emitter Amplifier 717
9.4 Useful Tools for the Analysis of the High-Frequency Response of Amplifiers 721
9.4.1 The High-Frequency Gain Function 721
9.4.2 Determining the 3-dB Frequency f_H 721
9.4.3 Using Open-Circuit Time Constants for the Approximate Determination of f_H 724
9.4.4 Miller's Theorem 727
9.5 A Closer Look at the High-Frequency Response of the CS and CE Amplifiers 731
9.5.1 The Equivalent Circuit 731
9.5.2 Analysis Using Miller's Theorem 732
9.5.3 Analysis Using Open-Circuit Time Constants 735
9.5.4 Exact Analysis 737
9.5.5 Adapting the Formulas for the Case of the CE Amplifier 741
9.5.6 The Situation when R_{sig} is Low 742
9.6 High-Frequency Response of the CG and Cascode Amplifiers 746
9.6.1 High-Frequency Response of the CG Amplifier 746
9.6.2 High-Frequency Response of the MOS Cascode Amplifier 750
9.6.3 High-Frequency Response of the Bipolar Cascode Amplifier 755
9.7 High-Frequency Response of the Source and Emitter Followers 756
9.7.1 The Source Follower 756
9.7.2 The Emitter Follower 758
9.8 High-Frequency Response of Differential Amplifiers 760
9.8.1 Analysis of the Resistively Loaded MOS Amplifier 760
9.8.2 Analysis of the Active-Loaded MOS Amplifier 765
9.9 Other Wideband Amplifier Configurations 770
9.9.1 Obtaining Wideband Amplification by Source and Emitter Degeneration 770
9.9.2 The CD-CS, CC-CE and CD-CE Configurations 773
9.9.3 The CC-CB and CD-CG Configurations 777
9.10 High-Frequency Response of Multistage Amplifiers 779
9.10.1 Frequency Response of the Two-Stage CMOS Op Amp 780
9.10.2 Frequency Response of the Bipolar Op Amp of Section 8.6.2. 783
Summary 784
Problems 785

10 Feedback 802
Introduction 803
10.1 The General Feedback Structure 804
10.2 Some Properties of Negative Feedback 809
10.2.1 Gain Desensitivity 809
10.2.2 Bandwidth Extension 810
10.2.3 Noise Reduction 811
10.2.4 Reduction in Nonlinear Distortion 813
10.3 The Four Basic Feedback Topologies 814
10.3.1 Voltage Amplifiers 814
10.3.2 Current Amplifiers 816
10.3.3 Transconductance Amplifiers 819
10.3.4 Transresistance Amplifiers 821
10.3.5 A Concluding Remark 822
10.4 The Feedback Voltage-Amplifier (Series-Shunt) 823
10.4.1 The Ideal Case 823
10.4.2 The Practical Case 825
10.4.3 Summary 827
10.5 The Feedback Transconductance-Amplifier (Series-Series) 834

10.5.1 The Ideal Case 834
10.5.2 The Practical Case 836
10.5.3 Summary 836
10.6 The Feedback Transresistance-Amplifier (Shunt-Shunt) 846
10.6.1 The Ideal Case 846
10.6.2 The Practical Case 848
10.6.3 Summary 855
10.7 The Feedback Current-Amplifier (Shunt-Series) 855
10.7.1 The Ideal Case 855
10.7.2 The Practical Case 856
10.8 Summary of the Feedback Analysis Method 863
10.9 Determining the Loop Gain 863
10.9.1 An Alternative Approach for Finding $A\beta$ 865
10.9.2 Equivalence of Circuits from a Feedback-Loop Point of View 866
10.10 The Stability Problem 868
10.10.1 The Transfer Function of the Feedback Amplifier 868
10.10.2 The Nyquist Plot 869
10.11 Effect of Feedback on the Amplifier Poles 870
10.11.1 Stability and Pole Location 871
10.11.2 Poles of the Feedback Amplifier 872
10.11.3 Amplifier with a Single-Pole Response 872
10.11.4 Amplifier with a Two-Pole Response 873
10.11.5 Amplifier with Three or More Poles 877
10.12 Stability Study Using Bode Plots 879
10.12.1 Gain and Phase Margins 879
10.12.2 Effect of Phase Margin on Closed-Loop Response 880
10.12.3 An Alternative Approach for Investigating Stability 881
10.13 Frequency Compensation 884
10.13.1 Theory 884
10.13.2 Implementation 885
10.13.3 Miller Compensation and Pole Splitting 886
Summary 890
Problems 890

11 Output Stages and Power Amplifiers 910
Introduction 911
11.1 Classification of Output Stages 912
11.2 Class A Output Stage 913
11.2.1 Transfer Characteristic 913
11.2.2 Signal Waveforms 915
11.2.3 Power Dissipation 915
11.2.4 Power Conversion Efficiency 917
11.3 Class B Output Stage 918
11.3.1 Circuit Operation 918
11.3.2 Transfer Characteristic 919
11.3.3 Power-Conversion Efficiency 920
11.3.4 Power Dissipation 921
11.3.5 Reducing Crossover Distortion 923
11.3.6 Single-Supply Operation 924
11.4 Class AB Output Stage 924
11.4.1 Circuit Operation 924
11.4.2 Output Resistance 926
11.5 Biasing the Class AB Circuit 929
11.5.1 Biasing Using Diodes 929
11.5.2 Biasing Using the V_{BE} Multiplier 931
11.6 CMOS Class AB Output Stages 933
11.6.1 The Classical Configuration 933
11.6.2 An Alternative Circuit Utilizing Common-Source Transistors 936
11.7 Power BJTs 943
11.7.1 Junction Temperature 944
11.7.2 Thermal Resistance 944
11.7.3 Power Dissipation versus Temperature 944
11.7.4 Transistor Case and Heat Sink 946
11.7.5 The BJT Safe Operating Area 949
11.7.6 Parameter Values of Power Transistors 950
11.8 Variations on the Class AB Configuration 950
11.8.1 Use of Input Emitter Followers 951
11.8.2 Use of Compound Devices 952
11.8.3 Short-Circuit Protection 954
11.8.4 Thermal Shutdown 955
11.9 IC Power Amplifiers 955
11.9.1 A Fixed-Gain IC Power Amplifier 956
11.9.2 Power Op Amps 960
11.9.3 The Bridge Amplifier 960

11.10 MOS Power Transistors 962
11.10.1 Structure of the Power MOSFET 962
11.10.2 Characteristics of Power MOSFETs 963
11.10.3 Temperature Effects 964
11.10.4 Comparison with BJTs 965
11.10.5 A Class AB Output Stage Utilizing Power MOSFETs 965
Summary 967
Problems 968

12 Operational Amplifier Circuits 974
Introduction 975
12.1 The Two Stage CMOS Op Amp 976
12.1.1 The Circuit 977
12.1.2 Input Common-Mode Range and Output Swing 977
12.1.3 Voltage Gain 978
12.1.4 Common-Mode Rejection Ratio (CMRR) 981
12.1.5 Frequency Response 981
12.1.6 Slew Rate 984
12.1.7 Power-Supply Rejection Ratio (PSRR) 986
12.1.8 Design Tradeoffs 987
12.2 The Folded Cascode CMOS Op Amp 991
12.2.1 The Circuit 991
12.2.2 Input Common-Mode Range and Output Swing 993
12.2.3 Voltage Gain 994
12.2.4 Frequency Response 996
12.2.5 Slew Rate 997
12.2.6 Increasing the Input Common-Mode Range: Rail-to-Rail Input Operation 999
12.2.7 Increasing the Output Voltage Range: The Wide-Swing Current Mirror 1000
12.3 The 741 Op-Amp Circuit 1002
12.3.1 Bias Circuit 1002
12.3.2 Short-Circuit Protection Circuitry 1004
12.3.3 The Input Stage 1004
12.3.4 The Second Stage 1004
12.3.5 The Output Stage 1005
12.3.6 Device Parameters 1005
12.4 DC Analysis of the 741 1006
12.4.1 Reference Bias Current 1007
12.4.2 Input-Stage Bias 1007
12.4.3 Input Bias and Offset Currents 1010
12.4.4 Input Offset Voltage 1010
12.4.5 Input Common-Mode Range 1010
12.4.6 Second-Stage Bias 1011
12.4.7 Output-Stage Bias 1011
12.4.8 Summary 1012
12.5 Small-Signal Analysis of the 741 1013
12.5.1 The Input Stage 1013
12.5.2 The Second Stage 1019
12.5.3 The Output Stage 1022
12.6 Gain, Frequency Response, and Slew Rate of the 741 1026
12.6.1 Small-Signal Gain 1026
12.6.2 Frequency Response 1027
12.6.3 A Simplified Model 1028
12.6.4 Slew Rate 1029
12.6.5 Relationship Between f_t and SR 1030
12.7 Modern Techniques for the Design of BJT Op Amps 1031
12.7.1 Special Performance Requirements 1031
12.7.2 Bias Design 1033
12.7.3 Design of Input Stage to Obtain Rail-to-Rail V_{ICM} 1035
12.7.4 Common-Mode Feedback to Control the DC Voltage at the Output of the Input Stage 1041
12.7.5 Output-Stage Design for Near Rail-to-Rail Output Swing 1045
Summary 1050
Problems 1051

PART II DIGITAL INTEGRATED CIRCUITS 1058

13 CMOS Digital Logic Circuits 1060
Introduction 1061
13.1 Digital Logic Inverters 1062
13.1.1 Function of the Inverter 1062
13.1.2 The Voltage Transfer Characteristic (VTC) 1062
13.1.3 Noise Margins 1064
13.1.4 The Ideal VTC 1066
13.1.5 Inverter Implementation 1066
13.1.6 Power Dissipation 1078

13.1.7 Propagation Delay 1080
13.1.8 Power-Delay and Energy-Delay Products 1084
13.1.9 Silicon Area 1085
13.1.10 Digital IC Technologies and Logic-Circuit Families 1086
13.1.11 Styles for Digital-System Design 1088
13.1.12 Design Abstraction and Computer Aids 1088
13.2 The CMOS Inverter 1089
13.2.1 Circuit Operation 1089
13.2.2 The Voltage-Transfer Characteristic 1092
13.2.3 The Situation When Q_N and Q_P are Not Matched 1094
13.3 Dynamic Operation of the CMOS Inverter 1098
13.3.1 Determining the Propagation Delay 1099
13.3.2 Determining the Equivalent Load Capacitance C 1104
13.3.3 Inverter Sizing 1107
13.3.4 Dynamic Power Dissipation 1109
13.4 CMOS Logic-Gate Circuits 1110
13.4.1 Basic Structure 1110
13.4.2 The Two-Input NOR Gate 1113
13.4.3 The Two-Input NAND Gate 1114
13.4.4 A Complex Gate 1115
13.4.5 Obtaining the PUN from the PDN and Vice Versa 1115
13.4.6 The Exclusive-OR Function 1115
13.4.7 Summary of the Synthesis Method 1117
13.4.8 Transistor Sizing 1117
13.4.9 Effects of Fan-In and Fan-Out on Propagation Delay 1121
13.5 Implications of Technology Scaling: Issues in Deep-Submicron Design 1122
13.5.1 Scaling Implications 1123
13.5.2 Velocity Saturation 1124
13.5.3 Subthreshold Conduction 1129
13.5.4 Wiring—The Interconnect 1130
Summary 1132
Problems 1134

14 Advanced MOS and Bipolar Logic Circuits 1142
Introduction 1143
14.1 Pseudo-NMOS Logic Circuits 1144
14.1.1 The Pseudo-NMOS Inverter 1144
14.1.2 Static Characteristics 1145
14.1.3 Derivation of the VTC 1146
14.1.4 Dynamic Operation 1149
14.1.5 Design 1149
14.1.6 Gate Circuits 1150
14.1.7 Concluding Remarks 1150
14.2 Pass-Transistor Logic Circuits 1152
14.2.1 An Essential Design Requirement 1153
14.2.2 Operation with NMOS Transistors as Switches 1154
14.2.3 Restoring the Value of V_{OH} to V_{DD} 1158
14.2.4 The Use of CMOS Transmission Gates as Switches 1159
14.2.5 Pass-Transistor Logic Circuit Examples 1164
14.2.6 A Final Remark 1166
14.3 Dynamic MOS Logic Circuits 1166
14.3.1 The Basic Principle 1167
14.3.2 Nonideal Effects 1170
14.3.3 Domino CMOS Logic 1173
14.3.4 Concluding Remarks 1175
14.4 Emitter-Coupled Logic (ECL) 1175
14.4.1 The Basic Principle 1175
14.4.2 ECL Families 1176
14.4.3 The Basic Gate Circuit 1177
14.4.4 Voltage-Transfer Characteristics 1180
14.4.5 Fan-Out 1185
14.4.6 Speed of Operation and Signal Transmission 1185
14.4.7 Power Dissipation 1186
14.4.8 Thermal Effects 1187
14.4.9 The Wired-OR Capability 1190
14.4.10 Final Remarks 1190
14.5 BiCMOS Digital Circuits 1190
14.5.1 The BiCMOS Inverter 1191
14.5.2 Dynamic Operation 1193
14.5.3 BiCMOS Logic Gates 1193
Summary 1195
Problems 1196

15 Memory Circuits 1202
Introduction 1203
15.1 Latches and Flip-Flops 1204
15.1.1 The Latch 1204
15.1.2 The SR Flip-Flop 1206
15.1.3 CMOS Implementation of SR Flip-Flops 1207

15.1.4 A Simpler CMOS Implementation of the Clocked SR Flip-Flop 1211
15.1.5 D Flip-Flop Circuits 1212
15.2 Semiconductor Memories: Types and Architectures 1214
15.2.1 Memory-Chip Organization 1215
15.2.2 Memory-Chip Timing 1217
15.3 Random-Access Memory (RAM) Cells 1217
15.3.1 Static Memory (SRAM) Cell 1218
15.3.2 Dynamic Memory (DRAM) Cell 1225
15.4 Sense Amplifiers and Address Decoders 1227
15.4.1 The Sense Amplifier 1227
15.4.2 The Row-Address Decoder 1235
15.4.3 The Column-Address Decoder 1237
15.4.4 Pulse-Generation Circuits 1238
15.5 Read-Only Memory (ROM) 1240
15.5.1 A MOS ROM 1240
15.5.2 Mask-Programmable ROMs 1242
15.5.3 Programmable ROMs (PROMs and EPROMs) 1243
Summary 1246
Problems 1247

PART IV FILTERS AND OSCILLATORS 1252

16 Filters and Tuned Amplifiers 1254
Introduction 1255
16.1 Filter Transmission, Types, and Specification 1256
16.1.1 Filter Transmission 1256
16.1.2 Filter Types 1257
16.1.3 Filter Specification 1257
16.2 The Filter Transfer Function 1260
16.3 Butterworth and Chebyshev Filters 1263
16.3.1 The Butterworth Filter 1263
16.3.2 The Chebyshev Filter 1267
16.4 First-Order and Second-Order Filter Functions 1270
16.4.1 First-Order Filters 1271
16.4.2 Second-Order Filter Functions 1271
16.5 The Second-Order LCR Resonator 1279
16.5.1 The Resonator Natural Modes 1279
16.5.2 Realization of Transmission Zeros 1280
16.5.3 Realization of the Low-Pass Function 1280
16.5.4 Realization of the High-Pass Function 1282
16.5.5 Realization of the Bandpass Function 1282
16.5.6 Realization of the Notch Functions 1282
16.5.7 Realization of the All-Pass Function 1284
16.6 Second-Order Active Filters Based on Inductor Replacement 1285
16.6.1 The Antoniou Inductance-Simulation Circuit 1285
16.6.2 The Op Amp-RC Resonator 1286
16.6.3 Realization of the Various Filter Types 1288
16.6.4 The All-Pass Circuit 1289
16.7 Second-Order Active Filters Based on the Two-Integrator-Loop Topology 1293
16.7.1 Derivation of the Two-Integrator-Loop Biquad 1293
16.7.2 Circuit Implementation 1295
16.7.3 An Alternative Two-Integrator-Loop Biquad Circuit 1297
16.7.4 Final Remarks 1298
16.8 Single-Amplifier Biquadratic Active Filters 1299
16.8.1 Synthesis of the Feedback Loop 1299
16.8.2 Injecting the Input Signal 1302
16.8.3 Generation of Equivalent Feedback Loops 1304
16.9 Sensitivity 1307
16.9.1 A Concluding Remark 1309
16.10 Switched-Capacitor Filters 1310
16.10.1 The Basic Principle 1310
16.10.2 Practical Circuits 1312
16.10.3 A Final Remark 1315
16.11 Tuned Amplifiers 1315
16.11.1 The Basic Principle 1315
16.11.2 Inductor Losses 1317
16.11.3 Use of Transformers 1319
16.11.4 Amplifiers with Multiple Tuned Circuits 1320

16.11.5 The Cascode and the CC-CB Cascade 1321
16.11.6 Synchronous Tuning 1321
16.11.7 Stagger-tuning 1323
Summary 1327
Problems 1328

17 Signal Generators and Waveform-Shaping Circuits 1334
Introduction 1335
17.1 Basic Principles of Sinusoidal Oscillators 1336
17.1.1 The Oscillator Feedback Loop 1336
17.1.2 The Oscillation Criterion 1337
17.1.3 Nonlinear Amplitude Control 1339
17.1.4 A Popular Limiter Circuit for Amplitude Control 1339
17.2 Op-Amp–RC Oscillator Circuits 1342
17.2.1 The Wien-Bridge Oscillator 1342
17.2.2 The Phase-Shift Oscillator 1344
17.2.3 The Quadrature Oscillator 1346
17.2.4 The Active-Filter-Tuned Oscillator 1347
17.2.5 A Final Remark 1349
17.3 LC and Crystal Oscillators 1349
17.3.1 LC-Tuned Oscillators 1349
17.3.2 Crystal Oscillators 1353
17.4 Bistable Multivibrators 1355
17.4.1 The Feedback Loop 1355
17.4.2 Transfer Characteristics of the Bistable Circuit 1356
17.4.3 Triggering the Bistable Circuit 1358
17.4.4 The Bistable Circuit as a Memory Element 1358
17.4.5 A Bistable Circuit with Noninverting Transfer Characteristics 1359
17.4.6 Application of the Bistable Circuit as a Comparator 1360
17.4.7 Making the Output Levels More Precise 1361
17.5 Generation of Square and Triangular Waveforms Using Astable Multivibrators 1363
17.5.1 Operation of the Astable Multivibrator 1363
17.5.2 Generation of Triangular Waveforms 1366
17.6 Generation of a Standardized Pulse—The Monostable Multivibrator 1367
17.7 Integrated-Circuit Timers 1369
17.7.1 The 555 Circuit 1369
17.7.2 Implementing a Monostable Multivibrator Using the 555 IC 1370
17.7.3 An Astable Multivibrator Using the 555 IC 1372
17.8 Nonlinear Waveform-Shaping Circuits 1374
17.8.1 The Breakpoint Method 1375
17.8.2 The Nonlinear-Amplification Method 1377
17.9 Precision Rectifier Circuits 1378
17.9.1 Precision Half-Wave Rectifier—The "Superdiode" 1378
17.9.2 An Alternative Circuit 1379
17.9.3 An Application: Measuring AC Voltages 1380
17.9.4 Precision Full-Wave Rectifier 1382
17.9.5 A Precision Bridge Rectifier for Instrumentation Applications 1384
17.9.6 Precision Peak Rectifiers 1385
17.9.7 A Buffered Precision Peak Detector 1385
17.9.8 A Precision Clamping Circuit 1386
Summary 1386
Problems 1387

Appendixes 1396
VLSI Fabrication Technology (by Wai Tung Ng) A-1 (on DVD)
B SPICE Device Models and Design and Simulation Examples Using PSpice® and Multisim™ B-1 (on DVD)
C Two-Port Network Parameters C-1 (on DVD)
D Some Useful Network Theorems D-1 (on DVD)
E Single-Time-Constant Circuits E-1 (on DVD)
F *s*-Domain Analysis: Poles, Zeros, and Bode Plots F-1 (on DVD)
G Bibliography G-1 (on DVD)
H Standard Resistance Values and Unit Prefixes H-1
I Answers to Selected Problems I-1

Index IN-1

TABLES

FOR REFERENCE AND STUDY

Table 1.1 The Four Amplifier Types 26
Table 1.2 Frequency Response of STC Networks 34
Table 2.1 Characteristics of the Ideal Op Amp 56
Table 3.1 Summary of Important Equations in Semiconductor Physics 159
Table 5.1 Regions of Operation of the Enhancement NMOS Transistor 249
Table 5.2 Regions of Operation of the Enhancement PMOS Transistor 257
Table 5.3 Small-Signal Equivalent-Circuit Models for the MOSFET 290
Table 5.4 Characteristics of MOSFET Amplifiers 306
Table 6.1 BJT Modes of Operation 353
Table 6.2 Summary of the BJT Current–Voltage Relationships in the Active Mode 367
Table 6.3 Conditions and Models for the Operation of the BJT in Various Modes 379
Table 6.4 Small-Signal Models of the BJT 423
Table 6.5 Characteristics of BJT Amplifiers 446
Table 7.1 Gain Distribution in the MOS Cascode Amplifier for Various Values of R_L 516
Table 7.A.1 Typical Values of CMOS Device Parameters 554
Table 7.A.2 Typical Parameter Values for BJTs 556
Table 7.A.3 Comparison of the MOSFET and the BJT 557
Table 9.1 The MOSFET High-Frequency Model 706
Table 9.2 The BJT High-Frequency Model 711
Table 10.1 Summary of Relationships for the Four Feedback-Amplifier Topologies 864
Table 12.1 DC Collector Currents of the 741 Circuit (μA) 1013
Table 13.1 Important Parameters of the VTC of the Logic Inverter 1065
Table 13.2 Implications of Device and Voltage Scaling 1123
Table 13.3 Summary of Important Characteristics of the CMOS Logic Inverter 1133
Table 14.1 Regions of Operation of the Pseudo-NMOS Inverter 1147
Table 16.1 Design Data for the Second Order Circuits Based on Inductor Simulation 1292
Table 16.2 Design Data for the the Tow–Thomas Biquad 1298

PREFACE

Microelectronic Circuits, sixth edition, is intended as a text for the core courses in electronic circuits taught to majors in electrical and computer engineering. It should also prove useful to engineers and other professionals wishing to update their knowledge through self-study.

As was the case with the first five editions, the objective of this book is to develop in the reader the ability to analyze and design electronic circuits, both analog and digital, discrete and integrated. While the application of integrated circuits is covered, emphasis is placed on transistor circuit design. This is done because of our belief that even if the majority of those studying this book were not to pursue a career in IC design, knowledge of what is inside the IC package would enable intelligent and innovative application of such chips. Furthermore, with the advances in VLSI technology and design methodology, IC design itself is becoming accessible to an increasing number of engineers.

Prerequisites

The prerequisite for studying the material in this book is a first course in circuit analysis. As a review, some linear circuits material is included here in the appendices: specifically, two-port network parameters in Appendix C; some useful network theorems in Appendix D; single-time-constant circuits in Appendix E; and *s*-domain analysis in Appendix F. No prior knowledge of physical electronics is assumed. All required semiconductor device physics is included, and Appendix A provides a brief description of IC fabrication. All these appendices can be found on the DVD that accompanies this book.

Emphasis on Design

It has been our philosophy that circuit design is best taught by pointing out the various trade-offs available in selecting a circuit configuration and in selecting component values for a given configuration. The emphasis on design has been increased in this edition by including more design examples, simulation examples, exercise problems, and end-of-chapter problems. Those exercises and end-of-chapter problems that are considered "design-oriented" are indicated with a D. Also, considerable material is provided on the most valuable design aid, SPICE, including Appendix B, which is available on the DVD so that it can be offered in searchable format, and in the full detail it deserves while not crowding other topics out of the text.

New to This Edition

Although the philosophy and pedagogical approach of the first five editions have been retained, several changes have been made to both organization and coverage.

1. **Four-Part Organization.** The book has been reorganized into four Parts. Part I: *Devices and Basic Circuits* (Chapters 1-6) provides a coherent and comprehensive single-semester introductory course in electronics. Similarly, Part II: *Integrated-Circuit Amplifiers* (Chapters 7-12) presents a rich package of material suitable for a second course. Part III: *Digital Integrated Circuits* (Chapters 13-15) represents a nearly self-contained coverage of digital electronics that can be studied after Chapters 5 (MOSFETs) and 6 (BJTs), or even only 5 if the emphasis is on MOS digital circuits—extremely helpful for teaching Computer Engineering students. Finally, Part IV: *Filters and Oscillators* (Chapters 16-17), deals with more specific application-oriented material that can be used to supplement a second course on analog circuits, be part of a third course, or used as reading and reference material to support student design projects. More on course design is given below.
2. **Flexible organization.** The most important feature of this edition is its flexible organization. Some manifestations of this flexibility are:
   - **MOSFETs and BJTs**. Chapter 5 (MOSFETs) and Chapter 6 (BJTs) are written to be completely independent of each other and thus can be taught in whatever order the instructor desires. Because the two chapters have identical structures, the chapter taught second can be covered much faster.
   - **Robust Digital Coverage**. The digital material has been grouped together in the new Part III, updated, and expanded. It can be covered at various points in the first or second course. All that is needed by way of background is the material on the two transistor types (Chapters 5 and 6) or even just Chapter 5 since most digital electronics today is MOS-based.
   - **Semiconductors as Needed**. The required material on semiconductor physics has been grouped together in a short chapter (Chapter 3) that can be taught, skipped, or assigned as reading material, depending on the background of the students and the instructor's teaching philosophy. This chapter serves as a primer on the basics, or as a refresher, depending on whether students have had a prior course in semiconductors.
   - **Op-amps Anywhere**. The op-amp chapter (Chapter 2) can be taught at any point in the first or second course, or skipped altogether if this material is taught in other courses.
   - **Frequency Response**. The material on amplifier frequency response has been grouped together into a single chapter (Chapter 9). The chapter is organized in a way that allows coverage of as few sections as the instructor deems necessary. Also, some of the basic material (Sections 9.1 to 9.3) can be covered earlier (after Chapters 5 or 6) as part of the first course.
   - **"Must-Cover" Topics First.** Each chapter is organized so that the essential "must-cover" topics are placed first, and the more specialized material appears last. More specialized material that can be skipped on a first reading, while the student is first learning the basics, is marked with a ⊕. Once the students understand the core concepts, they can return to these important but specialized topics.

3. **Streamlined MOSFETs and BJTs**. Chapters 5 (MOSFETs) and 6 (BJTs) have been rewritten to increase the clarity of presentation and emphasize essential topics. Also, these chapters are now shorter and can be covered faster.
4. **Cascode Configuration**. A novel and intuitively appealing approach is used to introduce the cascode configuration in Chapter 7.
5. **Comparison of MOSFETs and BJTs**. The insightful comparison of the MOSFET and the BJT has been moved to an appendix attached to Chapter 7. The appendix also includes an update of the device parameter values corresponding to various generations of fabrication process technologies. This appendix provides a good review and a reference that can be consulted at various points in a second course.
6. **Feedback**. The feedback chapter (Chapter 10) has been rewritten to increase clarity. Also, a large number of new examples, mostly MOS-based, are included.
7. **Class AB Amplifiers**. New material on MOSFET class AB amplifiers is included in Chapter 11.
8. **Low-Voltage Bipolar Design**. While the classical 741 op-amp circuit is retained, a new section on modern techniques for the design of low-voltage bipolar op amps has been added to Chapter 12.
9. **Deep-Submicron Design**. In addition to augmenting and consolidating the material on digital electronics in Part III, a new section on technology scaling (Moore's Law) and deep-submicron design issues has been added (Chapter 13).
10. **MOS Emphasis**. Throughout the book, greater emphasis is placed on MOS circuits to reflect the current dominance of the MOSFET in electronics.
11. **Bonus Reading on DVD**. Supplementary material on a wide variety of topics that were included in previous editions is made available on the DVD accompanying the book (see a listing below).
12. **Examples, Exercises, and Problems**. The number of Examples has been increased. Also, the in-chapter Exercises and end-of-chapter Problems have been updated with parameter values of current technologies so students work with a real-world perspective on technology. More Exercises and Problems, of a greater variety, have been added.
13. **Summary Tables**. As a study aid and for easy reference, many summary tables are included. See the complete List of Summary Tables after the Table of Contents.
14. **Learning Objectives**. A new section (In This Chapter You Will Learn…) has been added at the beginning of each chapter to focus attention on the major learning objectives of the chapter.
15. **SPICE**. A significant number of new simulation examples using National Instruments™ Multisim™ are added to the Cadence PSpice® simulation examples. Together with a section describing the SPICE device models, these design and simulation examples are grouped together in Appendix B. They can also be found together with other simulation files in the Lab-on-a-Disc on the DVD.
16. **Simulation**. A number of end-of-chapter Problems in each chapter are marked with the SIM icon SIM as simulation problems. Students attempting these problems will find considerable additional guidance on the DVD.
17. **Key Equations**. All equations that will be cross-referenced and used again are numbered. Particularly important equations are marked with a special icon.

As well as the structural differences described above, new coverage is included on all of the following technical topics.

- Entirely rewritten coverage of semiconductors (Chapter 3)
- MOSFET and BJT chapters extensively rewritten and restructured, with new figures and examples (Chapter 5 and 6)
- The basic gain cell (Chapter 7)
- The cascode amplifier (Chapter 7)
- CC-CE, CD-CS, and CD-CE transistor configurations (Chapter 7)
- CMRR (Chapter 8)
- The differential amplifier with active load (Chapter 8)
- Determining the output resistance R_o (Chapter 8)
- All new sections on frequency response (Chapter 9)
- Many, many new MOS examples of feedback (Chapter 10)
- CMOS class AB output stages (Chapter 11)
- Rejection ratios (CMRR and PSRR) (Chapter 12)
- Modern techniques for the design of BJT op amps (Section 12.7)
- Digital logic inverters (Chapter 13)
- The CMOS inverter (Chapter 13)
- Deep submicron design and technology scaling (Moore's Law) (Section 13.5)

The DVD and the Website

A DVD accompanies this book. It contains much useful supplementary information and material intended to enrich the student's learning experience. These include

1. Student versions of both Cadence PSpice® and National Instruments™ Multisim™.
2. The input files for all the PSpice® and Multisim™ examples in this book.
3. Step-by-step guidance to help with the simulation Examples and end-of-chapter Problems identified with a SIM icon.
4. A link to the book's website, offering PowerPoint slides of every figure in this book that students can print and carry to class to facilitate taking notes.
5. Bonus text material of specialized topics not covered in the current edition of the textbook. These include:
   - Junction Field-Effect Transistors (JFETs)
   - Gallium Arsenide (GaAs) devices and circuits
   - Transistor-Transistor Logic (TTL) circuits
   - Analog-to-Digital and Digital-to-Analog converter circuits
6. Appendices for the book:
   - Appendix A: VLSI Fabrication Technology
   - Appendix B: SPICE Device Models and Design and Simulation Examples Using PSpice® and Multisim™
   - Appendix C: Two-Port Network Parameters
   - Appendix D: Some Useful Network Theorems
   - Appendix E: Single-Time-Constant Circuits
   - Appendix F: *s*-domain Analysis: Poles, Zeroes, and Bode Plots
   - Appendix G: Bibliography

A website for the book has been set up (www.oup.com/us/sedrasmith, or www.sedrasmith.org). Its content will change frequently to reflect new developments in the field. On the site, PowerPoint-based slides of all the figures in the text are available for easy note-taking. The website also features datasheets for hundreds of useful devices to help in laboratory experiments, links to industrial and academic websites of interest, and a message center to communicate with the authors and with Oxford University Press.

Exercises and End-of-Chapter Problems

Over 475 Exercises are integrated throughout the text. The answer to each exercise is given below the exercise so students can check their understanding of the material as they read. Solving these exercises should enable the reader to gauge his or her grasp of the preceding material. In addition, more than 1450 end-of-chapter Problems, 55% of which are new or revised in this edition, are provided. The problems are keyed to the individual chapter sections and their degree of difficulty is indicated by a rating system: difficult problems are marked with an asterisk (*); more difficult problems with two asterisks (**); and very difficult (and/or time consuming) problems with three asterisks (***). We must admit, however, that this classification is by no means exact. Our rating no doubt depended to some degree on our thinking (and mood!) at the time a particular problem was created. Answers to sample problems are given in Appendix I, so students have a checkpoint to tell if they are working out the problems correctly. Complete solutions for all exercises and problems are included in the *Instructor's Solutions Manual*, which is available from the publisher to those instructors who adopt the book.

As in the previous five editions, many examples are included. The examples, and indeed most of the problems and exercises, are based on real circuits and anticipate the applications encountered in designing real-life circuits. This edition continues the use of numbered solution steps in the figures for many examples, as an attempt to recreate the dynamics of the classroom.

Course Organization

The book contains sufficient material for a sequence of two single-semester courses (each of 40-50 lecture hours). The organization of the book provides considerable flexibility for course design. In the following, we suggest various possibilities for the two courses. This is also laid out in an easy-to-follow visual form at the beginning of the Instructor's Edition of the book.

The First Course

At the core of the first course are Chapters 4 (Diodes), 5 (MOSFETs), and 6 (BJTs). Of these three, the MOSFET chapter is the one that has to be covered most thoroughly. If it is covered before the BJT, and we recommend that it should be, then the BJT chapter can be covered much faster. If time does not permit, some of the later sections in Chapter 4 can be skipped. Chapter 1 (Signals and Amplifiers) deserves some treatment in class. Although the signal concepts can be assigned as out-of-class reading, the amplifier material should be discussed. However, if frequency response is not emphasized in the first course, Section 1.6 can be skipped.

Around this core, one can build three possible curricula for the first course:

1. *Standard*: Chapters 1–6. Here, some or all of Chapter 2 (Op Amps) can be delayed. Also, the decision as to how much to cover of Chapter 3 (Semiconductors) will

depend on the students' background and the instructor's philosophy. If desired, this course can be supplemented by the material on amplifier frequency response in Sections 9.1–9.3.

2. *Digital Orientation*: Chapters 1 (without Section 1.6), 4 (without the later applications sections), all of 5, 6 (perhaps focusing only on the early sections), Section 9.2, and Chapters 13, 14, and 15. If time constraints are a concern, coverage of 6 can be shortened; Section 13.5 on Moore's Law and deep-submicron design can be skipped, and Sections 14.4 and 14.5 that depend on BJTs can be omitted. This course is ideal for Computer Engineering students.
3. *Analog Orientation*. Chapters 1, 4 (perhaps without all of the later, more application-oriented sections), 5, 6, 7 (without the advanced material in 7.6), 8, 9 (including at least 9.1–9.3, and the instructor's selection of other topics), and 10 (a selection of topics). This is a heavy course, and assumes that the students have previously covered op amps and maybe diodes, as well as device physics. This course is ideal where the first electrical engineering course is a hybrid of circuits and basic electronics, and where students have taken a semiconductor device physics course.

The Second Course

There are three possibilities for the second course:

1. *Standard*: Chapters 7–12. If time does not permit, some of the later sections in Chapter 9 can be skipped. Also, some of the more advanced topics in Chapters 11 and 12 can be skipped. If desired, some material from Chapter 16 (Filters) and Chapters 17 (Oscillators) can be included. This course ideally follows the "Standard First Course" outlined above.
2. *Analog and Digital Combination*: Chapters 7, 8, 9 (selection of topics); 10 (selection of topics), 13 (perhaps without Section 13.5 on technology scaling), 14 (omitting 14.4 and 14.5 if time is short), and 15 (selection of topics).
3. *Electrical Follow-up*: Chapters 6, 7, 8, 9, 10, and a choice of topics as time allows, selected from Chapters 11 and 12. This course is ideal for Electrical Engineering students who took a first semester with a "Digital Orientation" outlined above to accommodate Computer Engineering students.

Supplementary Material/Third Course

Chapters 16 (Filters) and 17 (Oscillators) contain material that can be used to supplement a third course on analog circuits. As well, this material is highly design-oriented and can be used to aid students who are pursuing design projects.

Chapters 13, 14, and 15 can be used as about half (15 hours of lecture) of a senior level course on digital IC design.

An Outline for the Reader

Part I, *Devices and Basic Circuits*, includes the most fundamental and essential topics for the study of electronic circuits. At the same time, it constitutes a complete package for a first course on the subject.

Chapter 1. The book starts with an introduction to the basic concepts of electronics in Chapter 1. Signals, their frequency spectra, and their analog and digital forms are presented.

Amplifiers are introduced as circuit building blocks and their various types and models are studied. This chapter also establishes some of the terminology and conventions used throughout the text.

Chapter 2. Chapter 2 deals with operational amplifiers, their terminal characteristics, simple applications, and practical limitations. We chose to discuss the op amp as a circuit building block at this early stage simply because it is easy to deal with and because the student can experiment with op-amp circuits that perform nontrivial tasks with relative ease and with a sense of accomplishment. We have found this approach to be highly motivating to the student. We should point out, however, that part or all of this chapter can be skipped and studied at a later stage (for instance, in conjunction with Chapter 8, Chapter 10, and/or Chapter 12) with no loss of continuity.

Chapter 3. Chapter 3 provides an overview of semiconductor concepts at a level sufficient for understanding the operation of diodes and transistors in later chapters. Coverage of this material is useful in particular for students who have had no prior exposure to device physics. Even those with such a background would find a review of Chapter 3 beneficial as a refresher. The instructor can choose to cover this material in class or assign it for outside reading.

Chapter 4. The first electronic device, the diode, is studied in Chapter 4. The diode terminal characteristics, the circuit models that are used to represent it, and its circuit applications are presented. Depending on the time available in the course, some of the diode applications (e.g., Section 4.6) can be skipped. Also, the brief description of special diode types (Section 4.7) can be left for the student to read.

Chapters 5 and 6. The foundation of electronic circuits is established by the study of the two transistor types in use today: the MOS transistor in Chapter 5 and the bipolar transistor in Chapter 6. These are the two most important chapters of the book. ***These two chapters have been written to be completely independent of one another and thus can be studied in either order, as desired.*** Furthermore, the two chapters have the same structure, making it easier and faster to study the second device, as well as to draw comparisons between the two device types.

Each of Chapters 5 and 6 begins with a study of the device structure and its physical operation, leading to a description of its terminal characteristics. Then, to allow the student to become very familiar with the operation of the transistor as a circuit element, a large number of examples are presented of dc circuits utilizing the device. We then ask: How can the transistor be used as an amplifier? To answer the question we consider the large-signal operation of the basic common-source (common-emitter) circuit and use it to delineate the regions over which the device can be used as a linear amplifier, from those regions where it can be used as a switch. We then pursue the small-signal operation of the transistor and develop circuit models for its representation. The various configurations in which the transistor can be used as an amplifier are then studied and contrasted. This is followed by a study of methods to bias the transistor to operate as an amplifier in discrete-circuit applications. We then put everything together by presenting complete practical discrete-circuit transistor amplifiers. The last section of each of Chapters 5 and 6 deals with second-order effects that are included for completeness, but that can be skipped if time does not permit detailed coverage.

After the study of Part I, the reader will be fully prepared to study either integrated-circuit amplifiers in Part II, or digital integrated circuits in Part III.

Part II, *Integrated-Circuit Amplifiers*, is devoted to the study of practical amplifier circuits that can be fabricated in the integrated-circuit (IC) form. Its six chapters constitute a coherent treatment of IC amplifier design and can thus serve as a second course in electronic circuits.

Chapter 7. Beginning with a brief introduction to the philosophy of IC design, Chapter 7 presents the basic circuit building blocks that are used in the design of IC amplifiers. We start with the basic gain cell comprising a common-source (common-emitter) transistor loaded with a current source, and ask: How can we increase its voltage gain? This leads naturally to the concept of cascoding and its use in the cascode amplifier and the cascode current source. We then consider the methods used for biasing IC amplifiers. The chapter concludes, as do most chapters in the book, with advanced topics (Sections 7.5 and 7.6) that can be skipped if the instructor is pressed for time.

Chapter Appendix 7.A. Chapter 7 includes an appendix that provides a comprehensive compilation and comparison of the properties of the MOSFET and the BJT. The comparison is aided by the inclusion of typical parameter values of devices fabricated with modern process technologies. This appendix can be consulted at any point from Chapter 7 on, and should serve as a concise review of the important characteristics of both transistor types.

MOS and Bipolar. Throughout Part II, both MOS and bipolar circuits are presented side-by-side. Because the MOSFET is by far the dominant device, its circuits are presented first. Bipolar circuits are discussed to the same depth but occasionally more briefly.

Chapter 8. The most important IC building block, the differential pair, is the main topic of Chapter 8. The last section of Chapter 8 is devoted to the study of multistage amplifiers.

Chapter 9. Chapter 9 presents a comprehensive treatment of the important subject of amplifier frequency response. Here, Sections 9.1, 9.2, and 9.3 contain essential material; Sections 9.4 and 9.5 provide an in-depth treatment of very useful new tools; and Sections 9.6 to 9.10 present the frequency response analysis of a variety of amplifier configurations that can be studied as and when needed. A selection of the latter sections can be made depending on the time available and the instructor's preference.

Chapter 10. The fourth of the essential topics of Part II, feedback, is the subject of Chapter 10. Both the theory of negative feedback and its application in the design of practical feedback amplifiers are presented. We also discuss the stability problem in feedback amplifiers and treat frequency compensation in some detail.

Chapter 11. In Chapter 11 we switch gears from dealing with small-signal amplifiers to those that are required to handle large signals and large amounts of power. Here we study the different amplifier classes—A, B, and AB—and their realization in bipolar and CMOS technologies. We also consider power BJTs and power MOSFETs, and study representative IC power amplifiers. Depending on the availability of time, some of the later sections (e.g., 11.8–11.10 on special applications) can be skipped in a first reading.

Chapter 12. Finally, Chapter 12 brings together all the topics of Part II in an important application; namely, the design of operational amplifier circuits. We study both CMOS and bipolar op amps. In the latter category, besides the classical and still timely 741 circuit, we present modern techniques for the design of low-voltage op amps (Section 12.7).

Part III, *Digital Integrated Circuits*, provides a brief but nonetheless comprehensive and sufficiently detailed study of digital IC design. Our treatment is almost self-contained, requiring for the most part only a thorough understanding of the MOSFET material presented in Chapter 5. Thus, Part III can be studied right after Chapter 5. The only exceptions to this are the last two sections in Chapter 14 which require knowledge of the BJT (Chapter 6). Also, knowledge of the MOSFET internal capacitances (Section 9.2.2) will be needed.

Chapter 13. Chapter 13 is the foundation of Part III. It begins with digital logic inverters (Section 13.1), and then concentrates on the bread-and-butter topics of digital IC design: the CMOS inverter (Sections 13.2 and 13.3) and CMOS logic gates (Section 13.4). The last section (13.5) deals with the implications of technology scaling (Moore's law) and discusses important issues in deep-submicron technologies. With the possible exception of Section 13.5, the material in Chapter 13 is the minimum needed to learn something meaningful about digital circuits.

Chapter 14. Chapter 14 builds on the foundation established in Chapter 13 and presents three important types of MOS logic circuits. As well, a significant family of bipolar logic circuits, emitter-coupled logic, is studied. The chapter concludes with an interesting digital circuit technology that attempts to combine the best attributes of bipolar and CMOS: BiCMOS.

Chapter 15. Digital circuits can be broadly divided into logic and memory circuits. The latter is the subject of Chapter 15.

Part IV, *Filters and Oscillators*, is intentionally oriented toward applications and systems. The two topics illustrate powerfully and dramatically the application of both negative and positive feedback.

Chapter 16. Chapter 16 deals with the design of filters, which are important building blocks of communication and instrumentation systems. A comprehensive, design-oriented treatment of the subject is presented. The material provided should allow the reader to perform a complete filter design, starting from specification and ending with a complete circuit realization. A wealth of design tables is included.

Chapter 17. Chapter 17 deals with circuits for the generation of signals with a variety of waveforms: sinusoidal, square, and triangular. We also present circuits for the nonlinear shaping of waveforms.

Appendices. The eight appendices contain much useful background and supplementary material. We wish to draw the reader's attention in particular to the first two: Appendix A provides a concise introduction to the important topic of IC fabrication technology including IC layout. Appendix B provides SPICE device models as well as a large number of design and simulation examples in PSpice® and Multisim™. The examples are keyed to the book chapters. These Appendices and a great deal more material on these simulation examples can be found on the DVD accompanying the book.

Ancillaries

A complete set of ancillary materials is available with this text to support your course.

For the Instructor

The *Instructor's Solutions Manual* provides complete worked solutions to all the exercises in each chapter and all the end-of-chapter problems in the text.

The *Instructor's Resource CD* is bound into the *Instructor's Solutions Manual* so instructors can find all their support materials in one place. The *Resource CD* contains PowerPoint-based slides of every figure in the book and each corresponding caption. The slides can be projected in class, added to a course management system, printed as overhead transparencies, or used as handouts. The CD also contains complete solutions and instructor's support for the Lab-on-a-Disc simulation problems. (ISBN 9780195340303)

For the Student and Instructor

The *DVD* included with every new copy of the textbook contains Lab-on-a-Disc simulation activities in Multisim™ and PSpice® for many of the simulation Examples and Problems in the text. It also contains a Student Edition of Cadence PSpice® v. 16.2 Demo software, and a Student Edition of National Instruments™ Multisim™ version 10.1.1, both of which can be

run by students on their own computers so they can practice their coursework wherever they happen to study. Bonus text topics, the Appendices, and a link to the book's website featuring manufacturer datasheets and PowerPoint-based slides of all of the book's illustrations, complete the DVD.

Acknowledgments

Many of the changes in this sixth edition were made in response to feedback received from instructors who adopted the fifth edition. We are grateful to all those who took the time to write to us. In addition, dozens of reviewers provided detailed commentary on the fifth edition and suggested many of the changes that we have incorporated in this revision. They are listed later; to all of them, we extend our sincere thanks.

A number of individuals made significant contributions to this edition. Sam Emaminejad and Muhammad Faisal prepared the Multisim™ and new PSpice® simulations and helped with many aspects of the manuscript preparation. Olivier Trescases of the University of Toronto and his students helped immensely, independently testing all the simulations in the Lab-on-a-Disc. Wai-Tung Ng of the University of Toronto rewrote Appendix A. Gordon Roberts of McGill University gave us permission to use some of the examples from the book *SPICE* 2nd edition, by Roberts and Sedra. Sima Dimitrijev of Griffith University undertook a detailed review of Chapter 3 on semiconductor devices, and David Pulfrey of the University of British Columbia offered suggestions as well. As in the previous edition, Anas Hamoui of McGill University was the source of many good ideas. Jim Somers of Sonora Designworks prepared discs for the student and instructor support materials. Jennifer Rodrigues typed all the revisions with skill and good humor and assisted with many of the logistics. Linda Lyman assisted with more details than we can possibly list here, and has been invaluable. Laura Fujino assisted in proofreading, and perhaps most importantly, in keeping one of us (KCS) focused. To all of these friends and colleagues we say thank you.

We are also grateful to the following colleagues and friends who have provided many helpful suggestions: Anthony Chan-Carusone, University of Toronto; Roman Genov, University of Toronto; David Johns, University of Toronto; Ken Martin, University of Toronto; David Nairn, University of Waterloo; Wai-Tung Ng, University of Toronto; Khoman Phang, University of Toronto; Gordon Roberts, McGill University; and Ali Sheikholeslami, University of Toronto.

The authors would like to thank Cadence and National Instruments for allowing Oxford University Press to distribute the PSpice® and Multisim™ software with this book. Mark Walters of National Instruments in particular has been very supportive. We are grateful to PMC Sierra for the excellent cover photo (which is fully described on the copyright page of this book, for readers who are interested in the intriguing technology shown here).

A large number of people at Oxford University Press contributed to the development of this edition and its various ancillaries. We would like to specifically mention Art Director Paula Schlosser and designers Dan Niver, Binbin Li, and Annika Sarin, Senior Copywriter Jill Crosson, as well as Susanne Arrington, Andy Battle, Brian Black, Sonya Borders, Gigi Brienza, Jim Brooks, Chris Critelli, Michael Distler, Diane Erickson, Ned Escobar, Adam Glazer, Chris Hellstrom, Andrea Hill, Adriana Hurtado, Holly Lewis, Jenny Lupica, Johanna Marcelino, Bill Marting, Laura Mahoney, Joella Molway, Preeti Parasharami, Emily Pillars, Terry Retchless, Kim Rimmer, Linda Roths, Sarah Smith, Patrick Thompson, Adam Tyrell, Euan White, and David Wright.

We wish to extend special thanks to our Publisher at Oxford University Press, John Challice, and to the hardworking editorial team of Engineering Associate Editor Rachael Zimmermann and Editorial Director Patrick Lynch, who have meticulously prepared all the ancillary support for this book. Steve Cestaro, Director of Editorial, Design, and Production, pulled out all the stops on this edition. Barbara Mathieu, Senior Production Editor, worked quietly, cheerfully, and tirelessly to bring this book to completion under significant pressure, making a difficult job look easy with grace and creativity. And last but certainly not least, a special note of thanks and gratitude to our Development Editor, Danielle Christensen, who was our main point of contact with OUP throughout the entire project and who managed the project with creativity, thoughtfulness, and dedication.

Finally, we wish to thank our families for their support and understanding, and to thank all the students and instructors who have valued this book throughout its history.

Adel S. Sedra
Kenneth C. (KC) Smith

Problem Solvers and Accuracy Checkers, Solutions Manual

Mandana Amiri, University of British Columbia, BC
Alok Berry, George Mason University, VA
Marc Cahay, University of Cincinnati, OH
Yun Chiu, University of Illinois–Urbana-Champaign, IL
Norman Cox, Missouri University of Science and Technology, MO
John Davis, University of Texas–Austin, TX
Michael Green, University of California–Irvine, CA
Roger King, University of Toledo, OH
Clark Kinnaird, Southern Methodist University, TX
Robert Krueger, University of Wisconsin–Milwaukee, WI
Shahriar Mirabbasi, University of British Columbia, BC
Daniel Moore, Rose-Hulman Institute of Technology, IN
Kathleen Muhonen, The Pennsylvania State University, PA
Angela Rasmussen, University of Utah, UT
Roberto Rosales, University of British Columbia, BC
John Wilson, Royal Military College, ON

Reviewers of the Sixth Edition

Elizabeth Brauer, Northern Arizona University, AZ
Martin Brooke, Duke University, NC
Yun Chiu, University of Illinois–Urbana-Champaign, IL
Norman Cox, Missouri University of Science and Technology, MO
Robert Bruce Darling, University of Washington, WA
John Davis, University of Texas–Austin, TX
Christopher DeMarco, University of Wisconsin–Madison, WI
Robert Engelken, Arkansas State University, AR
Ethan Farquhar, University of Tennessee, TN
Patrick Fay, University of Notre Dame, IN
George Giakos, University of Akron, OH
John Gilmer, Wilkes University, PA
Tayeb Giuma, University of North Florida, FL
Michael Green, University of California–Irvine, CA
Steven de Haas, California State University–Sacramento, CA
Anas Hamoui, McGill University, QC
William Harrell, Clemson University, SC
Reid Harrison, University of Utah, UT
Timothy Horiuchi, University of Maryland–College Park, MD
Mohammed Ismail, The Ohio State University, OH
Paul Israelson, Utah State University, UT
Zhenhua Jiang, University of Miami, FL
Seongsin M. Kim, University of Alabama, AL
Roger King, University of Toledo, OH
Clark Kinnaird, Southern Methodist University, TX
Tsu-Jae King Liu, University of California–Berkeley, CA
Yicheng Lu, Rutgers University, NJ
David Nairn, University of Waterloo, ON
Thomas Matthews, California State University–Sacramento, CA
Ken Noren, University of Idaho, ID
Brita Olson, California Polytechnic University–Pomona, CA
Martin Peckerar, University of Maryland–College Park, MD
Khoman Phang, University of Toronto, ON
Mahmudur Rahman, Santa Clara University, CA
John Ringo, Washington State University, WA
Norman Scheinberg, City College, NY

Kuang Sheng, Rutgers University, NJ
Andrew Szeto, San Diego State University, CA
Joel Therrien, University of Massachusetts–Lowell, MA
Len Trombetta, University of Houston, TX
Mustapha C.E. Yagoub, University of Ottawa, ON
Donna Yu, North Carolina State University, NC
Jiann-Shiun Yuan, University of Central Florida, FL
Sandra Yost, University of Detroit–Mercy, MI
Jianhua (David) Zhang, University of Illinois–Urbana-Champaign, IL

Reviewers of Prior Editions

Maurice Aburdene, Bucknell University, PA
Michael Bartz, University of Memphis, TN
Patrick L. Chapman, University of Illinois—Urbana-Champaign, IL
Roy H. Cornely, New Jersey Institute of Technology, NJ
Dale L. Critchlow, University of Vermont, VT
Artice Davis, San Jose State University, CA
Eby G. Friedman, University of Rochester, NY
Paul M. Furth, New Mexico State University, NM
Rhett T. George, Jr., Duke University, NC
Roobik Gharabagi, St. Louis University, MO
Steven de Haas, California State University—Sacramento, CA
Reza Hashemian, Northern Illinois University, IL
Ward J. Helms, University of Washington, WA
Richard Hornsey, York University, ON
Hsiung Hsu, The Ohio State University, OH
Robert Irvine, California State Polytechnic University—Pomona, CA
Steve Jantzi, Broadcom
Marian Kazimierczuk, Wright State University, OH
John Khoury, Columbia University, NY
Jacob B. Khurgin, The Johns Hopkins University, MD
Roger King, University of Toledo, OH
Robert J. Krueger, University of Wisconsin—Milwaukee, WI
Joy Laskar, Georgia Institute of Technology, GA
David Luke, University of New Brunswick, NB
Un-Ku Moon, Oregon State University, OR
Bahram Nabet, Drexel University, PA
Dipankar Nagchoudhuri, Indian Institute of Technology—Delhi, India
David Nairn, Analog Devices
Joseph H. Nevin, University of Cincinnati, OH
Rabin Raut, Concordia University, QC
John A. Ringo, Washington State University, WA
Zvi S. Roth, Florida Atlantic University, FL
Mulukutla Sarma, Northeastern University, MA
John Scalzo, Louisiana State University, LA
Pierre Schmidt, Florida International University, FL
Richard Schreier, Analog Devices
Dipankar Sengupta, Royal Melbourne Institute of Technology, Australia
Ali Sheikholeslami, University of Toronto, ON
Michael L. Simpson, University of Tennessee, TN
Karl A. Spuhl, Washington University in St. Louis, MO
Charles Sullivan, Dartmouth College, NH
Daniel van der Weide, University of Delaware, DE
Gregory M. Wierzba, Michigan State University, MI
Alex Zaslavsky, Brown University, RI

Microelectronic Circuits

INDEX

References marked **P** are study Problems; **S** are points in the chapter Summary; and Appendix pages found on the DVD are shown as **B-17**.

Numbers

2-port network parameter. *See* Two-port network parameter
2-input (NAND) gate. *See* Two-input NAND gate
2-input (NOR) gate. *See* Two-input NOR gate
2-integrator-loop biquad, 1293–1295
2-integrator-loop filter, PSpice example, **B71–B74**
2-stage CMOS op amp. *See* Two-stage CMOS op amp
3-dB frequency
  bandwidth, 322–323, 462
  determining, 692–693, 721–723, 784S, 790–792**P**
  example, 36–37
  open-circuit time constants, 724–727
  single-time-constant (STC) network, 33, 34, 35
553 circuit, 1369–1370
  553 timer, 1369, 1371
  astable multivibrator using, 1372–1374
  monostable multivibrator using, 1370–1372
6T cell, 1218, 1246**S**
741 op amp. PSpice example, **B15–B18**
741 op-amp circuit, 1002–1005, 1050**S**, 1053**P**
  bias circuit, 1002–1004
  dc analysis, 1006–1013, 1050**S**, 1053–1054**P**
  dc collector currents, 1013
  device parameters, 1005
  frequency response, 1027–1028
  input bias current, 1010
  input offset current, 1010
  input resistance, 1019–1020
  input stage, 1004, 1013–1016
  input stage bias, 1007–1010
  output resistance, 1020–1021
  output short-circuit protection, 1026
  output stage, 1005, 1022–1026
  output-stage bias, 1011–1012
  output voltage limits, 1022–1023
  reference bias current, 1007
  second stage, 1004–1005, 1019–1021
  second-stage bias, 1011
  short-circuit protection circuitry, 1004
  simplified model, 1028–1029
  slew rate, 1029–1030
  small-signal analysis, 1013–1026, 1050**S**, 1054–1055**P**
  small-signal gain, 1026–1027
  small-signal model, 1023–1025
  Thévenin equivalent circuit, 1021
  transconductance, 1020
  unity-gain bandwidth and slew rate, 1030–1031

A

Abrupt junction, 155
Ac (capacitively coupled) amplifier, 40
Acceptor, 131
Access transistors, 1218
Ac circuits, 44–45**P**
Ac ground
  common-emitter amplifier, 455
  common-source amplifier, 316
Active-filler design, pole control, 877
Active filter. *See* Second-order active filter
Active-filter-tuned oscillator, 1347–1349, 1386**S**
  PSpice example, **B77–B79**
Active loaded, 495
  MOS amplifier, 637–638, 765–769
Active mode
  base current, 356–357
  BJT, 352, 353
  BJT current-voltage relationships, 367
  collector current, 356
  current flow, 354–356
  emitter current, 357–358
  equivalent-circuit model, 358–359
  MOSFET and BJT, 557, 559
  operation of BJT, 379
  operation of *npn* transistor, 353–361, 465**S**
  operation of pnp transistor, 364–365
  recapitulation, 358–359
Active-RC filter, 1256
Active region, MOSFET and BJT, 559
Ac voltages, precision rectifier measuring, 1380–1382
ADC (analog-to-digital converter), 13–14, 41**S**
Address decoder, 1235–1237, 1246**S**, 1249–1250**P**
  column-address decoder, 1237
  row-address decoder, 1235–1237
Advanced logic circuit
  BiCMOS digital, 1190–1194, 1195**S**, 1201**P**
  dynamic MOS, 1166–1175, 1195**S**, 1199**P**
  emitter-coupled logic (ECL), 1175–1190, 1195**S**, 1199–1201**P**
  pass-transistor, 1152–1166, 1195**S**, 1197–1199**P**
  pseudo-NMOS, 1144–1152, 1195**S**, 1196–1197**P**
All-pass (AP) circuit, second-order filter, 1289, 1292, 1293
All-pass (AP) filter, 1271, 1273, 1278
All-pass function, realization, 1281, 1284
All-pole filter, 1263
Amount of feedback, 804, 805, 890S
Amplification, 3
  biasing MOSFET for linear, 269–270
Amplifier, 3, 46**P**
  applying BJT in, design, 396–403, 475–477**P**
  applying MOSFET in, design, 268–276, 337–339**P**
  BJT, configurations, 422–445, 466S, 481–483**P**
  buffer, 23, 439
  cascaded, 24–26
  cascode, 506–526
  cascode differential, 604–605
  CB (common-base), 424, 425, 436–438, 466**S**, 483**P**
  CC (common-collector), 424, 425, 438–443, 466**S**
  CC–CB, 550–551
  CC–CE, 546–547
  CD–CE, 546–547
  CD–CG, 550–551
  CD–CS, 546–547
  CE (common-emitter), 424, 427–430, 466**S**, 481–483**P**
  CE with emitter resistance, 432–435
  CG (common-gate), 292, 300–302, 328S, 341–343**P**
  characterizing, 293–294, 425–426
  circuit models for, 21–30, 46–49**P**
  circuit symbol, 15
  common-source (CS), 292, 294–297, 297–300, 328**S**, 341–343**P**
  current, 816–819, 855–863, 903–906**P**
  difference, 71–80, 115–118**P**
  differential, nonideal characteristics, 629–635, 677–678**P**
  differential, with active load, 635–650, 678–682**P**
  discrete-circuit BJT, 453–462, 466**S**, 486–489**P**
  discrete-circuit MOS, 314–323, 328**S**, 345–347**P**
  emitter follower, 424, 425, 438–443, 466**S**
  error, 937
  expressing gain in decibels, 17
  feedback topologies, 814–822, 893–894**P**
  frequency response, 30–40
  frequency-response based classification, 38–40, 41**S**
  frequency response of, 30–40, 49–51**P**, 322–323, 461–462
  gain, 15
  high-frequency response analysis, 721–731, 790–792**P**
  instrumentation, 76–80, 108**S**
  multistage, 651–665, 682–685**P**
  operational transconductance, 995
  power gain and current gain, 16–17
  power supplies, 17–19
  relationship between four models, 27
  saturation, 19, 20
  sense, 1227–1235, 1246**S**, 1249–1250**P**
  signal amplification, 14–15
  single-pole response, 872–873
  source-drain, 293, 302–305, 328**S**, 341–343**P**
  symbol convention, 20–21
  three or more poles, 877–879
  transconductance, 819–820, 834–846, 899–901**P**
  transresistance, 821–822, 846–855, 901–903**P**
  tuned, 1315–1327, 1328**S**, 1332–1333**P**
  two-pole response, 873–877
  types, 26–27, 41**S**
  voltage, 22–23, 814–816, 864
  voltage gain, 15–16
  wideband configurations, 770–779

Amplifier bandwidth, 31, 32
  frequency response, 322–323
Amplifier circuit, biasing in MOS, 306–314, 328**S**, 343–345**P**
Amplifier frequency response, measuring, 30–31
Amplifier pole
  feedback and, 870–879, 907–908**P**
  poles of feedback amplifier, 872
  single-pole response, 872–873
  stability and pole location, 871–872
  three or more poles, 877–879
  two-pole response, 873–877
Amplifier transfer function, $T(\omega)$, 32
Amplitude, symmetrical square-wave signal, 9–10
Amplitude control
  limiter circuit, 1339–1341
  nonlinear, 1339
Amplitude response, amplifier, 31
Analog circuit, 12
Analog signal, 11–12, 41**S**, 45–46**P**
Analog-to-digital converter (A/D or ADC), 13–14, 41**S**
Angular frequency, ω, 9
Anisotropic etching, **A4**
Anode, diode, 166
Antoniou inductance simulation circuit, 1285–1286
Applied voltage, *pn* junction with, 145–154, 161**P**
Astable multivibrator, 1336, 1363–1367, 1386**S**, 1391**P**
  553 IC, 1372–1374
  operation, 1363–1365
  triangular waveform, 1366–1367
Attenuation function, 1256
Audio band, 10
Autotransformer, 1318
Avalanche effect, *pn* junction breakdown, 153

B

Balanced manner, 600, 622
Bandgap energy, 128
Bandpass (BP) circuit, design data, 1290, 1292
Bandpass (BP) filter, 40, 1257, 1258, 1276
Bandpass amplifier, 40
Bandpass function, realization, 1281, 1282
Band-reject, 1257, 1258
Bandstop (BS) filter, 1257, 1258
Bandwidth
  BJT amplifier, 462
  circuit performance, 97–102, 122–123**P**
  full-power, 106, 107, 108**S**
  ideal op amp, 56
  unity-gain, 98, 107–108**S**
Bandwidth extension, feedback, 810–811
Bandwidth-shrinkage factor, 1322
Barkhausen criterion, 1337
Barrier, depletion region, 140
Base (B), terminal, 28, 352
Base-charging capacitance, BJT, 707
Base current
  input resistance at base, 406–407
  npn transistor in active mode, 356–357
Base-current compensation, bipolar mirror, 539, 553**S**
Base-emitter junction capacitance, BJT, 707
Base-width modulation effect, 372
Bias circuit
  741 op-amp circuit, 1002–1004
  two-stage CMOS op amp, 655–657
Bias current, reference, of 741 op-amp circuit, 1007
Bias design, BJT op amp, 1033–1035
Biasing
  BJT amplifier circuits, 446–453, 483–486**P**
  BJT circuit, 532–536
  BJT for linear amplification, 397–399
  class AB circuit, 929–933, 967**S**, 969–970**P**
  class AB circuit using V_{BE} multiplier, 931–932
  collector-to-base feedback resistor, 451–452
  constant-current source, 312–313, 452–453
  drain-to-gate feedback resistor, 311–312
  fixing gate voltage and connecting resistance, 308–311
  IC (integrated circuit) amplifier, 526–537, 553**S**, 576–580**P**
  MOS amplifier circuits, 306–314, 328**S**, 343–345**P**
  MOSFET for linear amplification, 269–270
  using diodes, 929–930
Bias point Q, 270, 275, 276, 398, 402–403
BiCMOS (bipolar CMOS) circuit
  bipolar and MOS transistor, 568–569
  fabrication, **A1**
  IC technology, 1086, 1088
  SiGe, process, **A13**, **A14**
  VLSI process, **A12**
BiCMOS cascodes, 525–526, 553S
BiCMOS digital circuit, 1190–1194, 1195**S**, 1201**P**
  BiCMOS inverter, 1191–1193
  dynamic operation, 1193
  equivalent circuit, 1193, 1194
  logic gates, 1193–1194
  two-input NAND gate, 1193, 1194
Bilinear transfer function, 1271
Binary, number system, 12–13
Bipolar cascode amplifier, high frequency response, 755–756, 785**S**, 794–795**P**
Bipolar differential amplifier
CMRR (common-mode rejection ratio), 647–648
  common-mode gain, 647–648
  differential gain, 644–647
  input bias and offset currents, 634–635
  input offset voltage, 632–634
  pair with active load, 644–650
  systemic input offset voltage, 648–650
Bipolar junction transistor. *See* BJT (bipolar junction transistor)
Bipolar mirror, base-current compensation, 539, 553**S**
Bipolar op amp
  analysis using current gains, 664–665
  frequency response, 783–784
  multistage amplifier, 657–665, 666**S**
Biquad, 1293
Biquadratic transfer function, 1271
Bistable circuit, 1203
Bistable multivibrator, 1336, 1386**S**
Bistable multivibrators, 1355–1362, 1390–1391**P**
  bistable circuit as comparator, 1360–1361
  bistable circuit as memory element, 1358
  bistable circuit with noninverting transfer characteristics, 1359
  feedback loop, 1355–1356
  output level precision, 1361, 1362
  Schmitt trigger, 1358
  transfer characteristics of bistable circuit, 1356–1358
  triggering bistable circuit, 1358
Bit lines, memory chip, 1215
BJT (bipolar junction transistor), 28
  amplifier configurations, 422–445, 424–425, 465**S**, 481–483**P**
  amplifier frequency response, 461–462
  applying, in amplifier design, 396–403, 475–477**P**
  base-charging capacitance, 707
  base current, 356–357, 406–407
  base-emitter junction capacitance, 707
  biasing, amplifier circuits, 446–453, 483–486**P**
  biasing, for linear amplification, 397–399
  biasing using collector-to-base feedback resistor, 451–452
  biasing using constant-current source, 452–453
  bias point Q, 402–403
  BJT cascode, 520–524
  CB (common-base) amplifier, 424, 425, 436–438, 458–459, 466**S**
  CC (common-collector) amplifier, 424, 425, 438–443, 466**S**
  CE (common-emitter) amplifier, 424, 427–430, 432–435, 455–456, 457–458, 466**S**
  characterizing amplifiers, 425–426, 446
  circuit, 532–536
  circuits at dc, 378–394, 465**S**, 471–475**P**
  circuit symbols, 365–367
  classical discrete-circuit bias arrangement, 447–449
  collector-base junction capacitance, 707
  collector-base reverse current (ICBO), 367
  collector current, 356, 404–406
  common-emitter characteristic, 374–376
  common-emitter current gain, 374
  comparison to MOSFET, 554–569, 583–585**P**
  conventions, 365–367
  current flow, 354–356
  current-voltage characteristics, 365–378, 468–471**P**
  cutoff frequency, 708–710
  dependence of i_C on collector voltage, 371–373, 465**S**
  diffusion capacitance, 707
  discrete-circuit, amplifiers, 453–462, 466**S**, 486–489**P**
  Early effect, 371–373, 420–421, 465**S**
  emitter current, 357–358, 407–408
  emitter follower, 424, 425, 438–443, 460–461, 466**S**
  equivalent-circuit models, 358–359
  high-frequency hybrid model, 707–708
  high-frequency model, 706–711, 784–785**S**, 788**P**
  hybrid-π model, 410–411, 707–708
  IC (integrated circuit) parameters, 556–557
  IC technology, 1086, 1087
  input resistance at base, 406–407
  input resistance at emitter, 407–408
  internal capacitance, 706–711, 785**S**, 788**P**
  models, 403–422, 477–481**P**
  models for operation modes, 379
  obtaining voltage amplifier, 396
  operation in saturation mode, 362–363
  operation modes, 352–353, 465**S**, 466–468**P**
  operation of *npn* transistor, 353–361
  parameter values, 556
  pnp transistor, 364–365, 465**S**
  power, 943–950, 970–971**P**
  PSpice example, **B26–B27**
  recapitulation, 358–359
  safe operating area, 949–950
  saturation resistance, 374–376
  saturation voltage, 374–376
  separating signal and dc quantities, 409–410
  small-signal analysis from circuit diagram, 419–420
  small-signal equivalent circuits, 412
  small-signal models, 423
  small-signal models for Early effect, 420–421
  small-signal models of *pnp* transistor, 412
  small-signal operation, 403–422, 477–481**P**
  small-signal voltage gain, 399–400
  SPICE simulation, 378, 466**P**
  structure, 352–353, 465**S**, 466–468**P**

  structure of transistors, 361
  temperature effects, 464, 465
  three-terminal device, 231–232, 351–352
  T model, 411–412
  transconductance, 404–406
  transistor breakdown, 463–464
  transistor characteristics, 370, 371
  two-power supply bias arrangement, 450–451
  voltage gain, 408–409
  voltage transfer characteristic (VTC), 397
  VTC by graphical analysis, 401–402
BJT differential pair, 612–628, 672–676**P**
  basic operation, 613–614
  CMRR (common-mode rejection ratio), 624–626
  collector currents, 619–620
  common-mode gain, 624–626
  common-mode input resistance, 626
  configuration, 612, 613
  differential half-circuit, 622–624
  differential voltage gain, 622
  input common-mode range, 615
  input differential resistance, 621–622
  large-signal operation, 616–617
  small-signal operation, 618–624
BJT model
  parameters BF and BR in SPICE, **B12**
  SPICE, **B9–B12**
  SPICE Gummel–Poon model, **B11**
  SPICE parameters, **B11**
BJT op amp (operational amplifier)
  bias design, 1033–1035
  buffer/driver stage, 1046
  common-mode feedback, 1041
  controlling dc voltage at output of input stage, 1041–1043
  current in inactive transistor, 1047–1049
  design, 1031–1049, 1050**S**, 1056–1057**P**
  design of input stage for rail-to-rail V_{ICM}, 1035–1038
  device parameters, 1033
  near rail-to-rail output signal swing, 1033
  near rail-to-rail output swing, 1045–1049
  output-stage design, 1045–1049
  performance requirements, 1031–1033
  rail-to-rail input common-mode range, 1032–1033
  Schottky barrier diode, 1043
Bode plot, **F3–F6**, **F6–F7P**
  closed-loop response, 880–881
  frequency response, 33, 34, 35
  gain margin, 879–880
  investigating stability, 881–883
  phase margin, 879–880
  stability study using, 879–883, 908**P**
Body, MOSFET, 232–233
Body effect
  model, 324–325
  MOSFETs, 323–325, 347**P**
Body-effect parameter, 324
Body transconductance, 324–325
Boot-strapped follower, 489**P**
Bound charge, 130
Breakdown
  BJT, 463–464
  MOSFET, 325–326
Breakdown diode, 190
Breakdown region, junction diode, 178–179
Breakdown voltage, diode, 178
Break frequency, STC networks, 35
Breakpoint method, sine-wave shaping, 1375–1377
Brick-wall responses, 1257
Bridge amplifier, configuration, 960–962
Bridge rectifier, 199–200, 216**S**
Buffer amplifier, 23, 47**P**, 439
Buffer/driver stage, BJT op amp, 1046
Buffered precision peak detector, 1385–1386
Butterworth filter, 1263–1267, 1327**S**, 1329**P**
Bypass capacitor
  amplifier, 784**S**
  common-emitter amplifier, 455
  common-source amplifier, 316, 693–694

C

Capacitances
  BJT, 707–710
  MOSFET, 701–703
  MOSFET and BJT, 559
Capacitive effects, *pn* junction, 154–157, 159**S**, 161–162**S**
Capacitively coupled amplifier, 39, 40
Capacitor
  common-emitter (CE) amplifier, 694–699, 699–701
  common-emitter amplifier, 694–699
  VLSI process, **A10–A11**
Carrier concentration in intrinsic silicon, 157
Carrier concentration in *n*-type silicon, 157
Carrier concentration in *p*-type silicon, 157
Carrier-depletion region, 139
Carrier diffusion, 135–137, 158**S**
Carrier drift, 132–133, 158**S**
Carrier transport, **B10**
Cascaded amplifier, model, 24–26, 47**P**
Cascading dynamic logic gates, 1172
Cascode
  MOS mirrors, 538, 553**S**
  term, 506n.1
  tuned amplifier, 1321
Cascode amplifier, 506–526, 553**S**, 572–574**P**
  BiCMOS cascodes, 525–526, 553**S**
  bipolar, 755–756
  BJT cascode, 520–524
  cascoding, 408–409
  double cascoding, 518, 519, 553**S**
  folded cascode, 519–520
  high frequency response, 750–756, 785**S**, 794–795**P**
  MOS, 750–755
  MOS cascode, 507–512
  output resistance of emitter-degenerated CE amplifier, 524–525
  output resistance of source-degenerated CS amplifier, 517–518
  voltage gain distribution, 514–517
Cascode differential amplifier, 604–605
Cascoding
  current-buffering action, 505, 506–507
  double, 518, 519, 553**S**
Cathode, diode, 166
CC–CB cascade, tuned amplifier, 1321
CC–CB configuration, 550–551, 777–779
CC–CE configuration, 546–547, 773–777
CC–CG configuration, 550–551
CD–CE configuration, 546–547, 773
CD–CG configuration, 777–779
CD–CS configuration, 546–547, 773
Center frequency, 1274
  response peak, 39, 40
Center-tapped, 197
Channel, MOSFET, 234–236
Channel-length modulation, 254, 255, 328**S**
Channel pinch-off, 242, 249
Characteristic equation, 1337, 1338
  feedback-amplifier pole, 872
Charge sharing, dynamic logic circuit, 1171–1172
Charge stored in depletion layer, 141–145, 158
Chebyshev filter, 1267–1270, 1327**S**, 1329**P**
  PSpice example, **B69–B71**
Chemical vapor deposition (CVD), IC fabrication, **A5–A6**
Circuit
  AC, 44–45**P**
  analysis, 44**P**
  basics, 42**P**
  biasing in BJT amplifier, 446–453
  BJT, 532–536
  BJT, at dc, 378–394, 465**S**, 471–475**P**
  design data for second-order filters, 1288–1289, 1292–1293
  equivalence of, from feedback-loop point, 866–867
  feedback triple, 842, 843
  folded-cascode CMOS op amp, 991–993
  monostable multivibrator, 1239–1240
  MOSFET, at dc, 258–267
  op amp performance, 97–102, 122–123**P**
  precision rectifier circuit, 1378–1386, 1386**S**, 1394–1395**P**
  pulse-generation, 1238–1240
  rectifier, 194–207, 225–227**P**
  switched-capacitor (SC), 1311, 1312–1315
  symbols, 365–367
  Thévenin-equivalent, 43**P**
  two-stage CMOS op-amp, 977
  voltage doubler, 212–213
Circuit diagram, small-signal analysis from, 419–420
Circuit implementation, second-order active filter, 1295–1297
Circuit model
  amplifiers, 21–30, 46–49**P**
  cascaded amplifiers, 24–26
  determining R_i and R_o, 27
  relationship between four amplifier models, 27
  unilateral, 28–30
  voltage amplifiers, 22–23
Circuit operation
  class AB output stage, 924–926
  class B output stage, 918–919
  CMOS inverter, 1089–1092
Circuit symbol
  amplifier, 15
  MOSFET, 247–248, 256
  MOSFET and BJT, 557
  operational amplifier, 54
Clamped capacitor, 211
Clamping circuit, 210–212, 216**S**, 227–229**P**
  precision, 1386
Class AB output stage, 924–928, 967**S**, 969**P**
  biasing, 929–933
  biasing using diodes, 929–930
  biasing using V_{BE} multiplier, 931–932
  circuit operation, 924–926
  classification, 912, 913
  CMOS, 933–943
  compound devices, 952–953
  configuration variations, 950–955, 967**S**, 971–973**P**
  Darlington configuration, 952–953, 967**S**
  input emitter followers, 951
  output resistance, 926–927
  power MOSFETs, 965–966, 967**S**
  short-circuit protection, 954, 955
  thermal shutdown, 955, 956
Class A output stage, 913–918, 967**S**, 967–968**P**
  classification, 912, 913
  power-conversion efficiency, 917–918
  power dissipation, 915–916
  signal waveforms, 915
  transfer characteristic, 913–915
Class B bipolar output stage, Multisim example, **B112–B118**
Class B BJT output stage, PSpice example, **B50–B55**
Class B output stage, 918–924, 967**S**, 968–969**P**

Class B output stage *(continued)*
circuit operation, 918–919
classification, 912, 913
power-conversion efficiency, 920–921
power dissipation, 921–922
reducing crossover distortion, 923
single-supply operation, 924
transfer characteristic, 919–920
Class C, amplifier stage, 912, 913
Classical sensitivity function, 1307
Classification, output stages, 912–913
Clean room, oxidation, A2
Clear field, VLSI layout, A15, A16
Clipper, 208
Clock, 1203
Clocked set/reset flip-flop, CMOS implementation, 1211, 1212
Closed-loop amplifier, frequency response of, 99–102
Closed-loop gain
definition, G, 59
inverting configuration, 59–61
noninverting configuration, 67–68
Closed-loop response, phase margin, 880–881
Closed-loop transfer function, feedback, 868
Closure resistance, 275
CMOS (complementary MOS), 246
circuit of folded-cascode, 991–993
circuit of two-stage, 977
class AB output stages, 933–943, 967**S**, 969**P**
common-mode rejection ratio (CMRR) of two-stage, 981
design trade-offs of two-stage, 987–988
fabrication, A1
folded-cascode CMOS op amp, 991–1001, 1050**S**, 1052–1053**P**
frequency response of folded-cascode, 996–997
frequency response of two-stage, 981–984
IC technology, 1086–1087
implementation of clocked set/reset (SR) flip-flops, 1211, 1212
implementation of SR flip-flops, 1207–1211
input common-mode range of folded-cascode, 993–994, 999–1000
input common-mode range of two-stage, 977–978
Multisim example of, CS amplifier, B88–B92
output swing of folded-cascode, 993–994
output swing of two-stage, 977–978
output voltage range of folded-cascode, 1000–1001
phase margin, 982–984
power-supply rejection ratio (PSRR), 986–987
PSpice example, B40–B43
PSpice example of CS amplifier, B29, B30–B33
rail-to-rail input operation of folded-cascode, 999–1000
simplified equivalent circuit, 982
slew rate (SR) of folded-cascode, 997
SR of two-stage, 984–986
twin-well, process, A7–A9
two-stage, op amp, 651–657, 666**S**, 976–991, 1050**S**, 1051–1052**P**
values of CMOS device parameters, 554–555
voltage gain of folded-cascode, 994–996
voltage gain of two-stage, 978–980
wide-swing current mirror of folded-cascode, 1000–1001
CMOS (complementary MOS) class AB output stage
classical, 933–936
common-source transistors, 936–943
output resistance, 937–939
voltage transfer characteristic, 939–941
CMOS (complementary MOS) inverter, 1089–1098, 1132**S**, 1136–1138**P**
circuit operation, 1089–1092
dynamic operation, 1098–1110, 1132**S**
dynamic power dissipation, 1109–1110
equivalent load capacitance C, 1104–1107
inverter sizing, 1107–1109
Multisim example, B123–B127
n-channel Q_N and *p*-channel Q_P MOSFETs unmatched, 1094–1095
pass-transistor control, 1158–1159
propagation delay, 1099–1104
PSpice example, B60–B63
voltage-transfer characteristic (VTC), 1092–1094, 1129, 1133
CMOS (complementary MOS) logic circuit, 1110–1121, 1132**S**, 1138–1139**P**
basic structure, 1110–1113
characteristics, 1133
CMOS inverter, 1089–1098, 1132**S**, 1136–1138**P**
CMOS logic-gate circuit, 1110–1121, 1132**S**, 1138–1139**P**
complex gate, 1115
deep-submicron design, 1122–1131, 1139–1141**P**
digital logic inverters, 1062–1089, 1132**S**, 1134–1136**P**
dynamic operation of CMOS inverter, 1098–1110, 1132**S**
exclusive OR function, 1115–1116
fan-in and fan-out on propagation delay, 1121
inverter output resistance, 1133
noise margins, 1133
propagation delay, 1133
pull-down network (PDN), 1110, 1111, 1132**S**
pull-up network (PUN), 1110, 1111, 1112, 1132**S**
PUN and PDN networks, 1115
synthesis method, 1117
technology scaling, 1122–1131, 1139–1141**P**
transistor sizing, 1117–1120
two-input NAND gate, 1114–1115
two-input NOR gate, 1113, 1114
CMOS logic gate, Domino, 1173–1175, 1195**S**
CMOS transmission gate
configuration, 1153
equivalent resistance, 1161–1164
switches in PTL circuit, 1159–1164
CMRR (common-mode rejection ratio), B3
active-loaded differential amplifier, 641–644
bipolar differential pair, 647–648
BJT differential pair, 624–626
definition, 72, 109**P**
g_m mismatch, 608–610
MOS differential pair, 605–612
two-stage CMOS op amp, 981
Coincidence function, 1138**P**
Collector (C), terminal, 28, 352
Collector-base junction (CBJ)
BJT, 352, 353, 465**S**
operation of BJT, 379
Collector-base junction capacitance, BJT, 707
Collector-base reverse current (ICBO), 367
Collector current
BJT, 404–406
BJT differential pair, 619–620
npn transistor in active mode, 356
Collector-to-base feedback resistor, biasing, 451–452
Colpitts oscillator, 1349, 1350
Column-address decoder, 1237, 1246**S**
Column decoder, memory chip, 1216
Combinational circuit, 1203
Common-base (CB) amplifier
BJT, 424, 425, 436–438, 466**S**, 483**P**
characteristics, 446
discrete-circuit BJT, 458–459
Common-base current gain, 358
Common-collector (CC) amplifier
BJT, 424, 425, 438–443, 466**S**
emitter follower, 438, 446
Common-drain (CD) amplifier
BJT, 424, 425, 436–438, 466**S**, 483**P**
characteristic parameters, 303–305
MOSFET, 293, 302–305, 328**S**, 341–343**P**
need for voltage buffers, 302–303
Common-emitter (CE) amplifier
adapting formulas for, 741–742
alternative gain expressions, 429–430
analysis on circuit, 430
BJT, 424, 427–430, 466**S**, 481–483**P**
capacitors, 694–699
characteristic parameters, 427–428, 446
discrete-circuit BJT, 455–456
gain cell of, with current-source load, 495–496
high-frequency response, 717–720, 789–790**P**
lower 3-dB frequency, 699
low frequency response, 694–701, 785–787**P**
Multisim example, B85–B88
output resistance of emitter-degenerated, 524–525
overall voltage gain, 428–429
PSpice example, B27–B30
values for three capacitors, 699–701
with emitter resistance, 432–435, 457–458
Common-emitter characteristics, 372, 374–376
Common-emitter circuit, transistor amplifier, 28
Common-emitter configuration, 372
Common-emitter current gain, 357, 374
Common-gate (CG) amplifier
characteristics, 306
discrete-circuit MOS, 318, 320
high frequency response, 746–750, 785**S**, 794–795**P**
MOSFET, 292, 300–302, 341–343**P**
Common-mode feedback, 1017, 1041
dc voltage at output of input stage, 1041–1043
Common-mode gain
active-loaded differential amplifier, 641–644
bipolar differential pair, 647–648
BJT differential pair, 624–626
MOS differential pair, 605–612
Common-mode half-circuit, 607, 624
Common-mode input resistance, 626
Common-mode input resistance (R_{icm}), B3
Common-mode input signal, ideal op amp, 57–58
Common-mode range, 116**P**
Common-mode rejection, 1231
op amp, 55
Common-mode rejection ratio. *See* CMRR (common-mode rejection ratio)
Common-mode voltage, MOS differential pair, 589–590
Common-source (CS) amplifier
analysis from circuit diagram, 297
characteristic parameters of, 295–296, 306
coupling and bypass capacitors, 693–694
discrete-circuit MOS, 316–317
exact analysis of high frequency, 737–741
gain cell of, with current-source load, 495–496
high-frequency response, 713–717, 789–790**P**
lower 3-dB frequency, 692–693
low-frequency response, 689–694, 785–787**P**
low resistance R_{sig}, 742–745
MOSFET, 292, 294–297, 328**S**, 341–343**P**
Multisim example, B75–B84, B100–B103, B103–B107
output resistance of source-degenerated, 517–518
overall voltage gain, 296
pole frequencies by inspection, 693
PSpice example, B23–B25, B29, B30–B33
resistance in source lead, 318, 319
with source resistance, 297–300, 318, 319
V_o/V_{sig}, 689–692
Common-source transistors
circuit utilizing, 936–943
output resistance, 937–939
voltage transfer characteristic, 939–941
Comparator, bistable circuit as, 1360–1361
Comparison circuit, 806
Complementary circuits, 1289
Complementary manner, 600, 622
Complementary pass-transistor logic (CPL), 1165
Complementary switch, inverter, 1068
Complementary transformation, 1303
Complex frequency variables, 32
Complex gate, CMOS logic circuit, 1115
Compound device, class AB output stage, 952–953
Computer aids, digital systems, 1088–1089
Concentration gradient, 135
Concentration profile, 135
Conduction interval, 203
Conductivity, σ, 133
Configuration
CC–CB amplifiers, 550–551, 777–779
CC–CE amplifier, 546–547, 773–777
CD–CE amplifier, 546–547, 773
CD–CG amplifier, 777–779
CD–CS amplifier, 546–547, 773
two-stage CMOS op-amp, 976
wideband amplifier, 770–779
Conjugate pairs, F2
Constant-current source
basic MOSFET, 527–530
biasing, 452–453
biasing a MOSFET, 312–313
Constant-voltage-drop model, diode, 181–182, 215**S**
Corner frequency, F4
STC networks, 35
Coupling capacitor
amplifier, 38–40, 784**S**
common-emitter amplifier, 456
common-source amplifier, 316, 693–694
Covalent bond, 126, 127
Crossover distortion, 919
class B output stage reducing, 923
Crystal oscillator, 1353–1355, 1386**S**, 1389–1390**P**
Pierce oscillator, 1354, 1355
Current, inactive transistor of BJT op amp, 1047–1049
Current amplifier, 27, 41**S**
circuit model, 26
feedback, 855–863, 903–906**P**
topology, 816–819, 864
Current buffer, 505
Current buffering, 506
Current conveyor, 585**P**, 973**P**
Current crowding, BJT safe operating area, 949
Current divider, 43**P**
Current flow
diffusion current, 135–137, 158**S**
drift current, 132–133, 158**S**
MOSFET, 234–236
npn transistor in active mode, 354–356
semiconductor, 132–138, 158**S**, 159–160**P**
Current gain, 16, 17, 528, 664–665
Current mirror, 528
BJT circuit, 532–534
cascode MOS, 538, 553**S**
differential MOS amplifier with, load, 1233–1235
MOS amplifier, 313
wide-swing, of folded-cascode CMOS op amp, 1000–1001
Wilson, 539–541, 553**S**
Current-mirror circuit, 537–546, 580–582**P**
Current-mixing, current-sampling topology, 816–817
Current-mixing, voltage-sampling topology, 821–822
Current-mode logic (CML), 1177
bipolar circuit, 1087
Current signal, 9
Current sink, 531
Current source, 531
BJT current mirror, 535
Widlar, 543–546, 553**S**
Current-source load, output resistance, 499–500
Current-source loaded, 495
Current-source loads
CS and CE amplifiers with, 495–496
differential amplifier with, 603
Current steering, 527
BJT circuit, 535–536
Current-steering circuit, MOS, 530–532
Current transfer ratio, 528
Current-voltage
BJT, 365–378, 465**S**, 468–471**P**
circuit symbols, 365–367
collector-base reverse current (I_{CBO}), 367
conventions, 365–367
diode, 166–167
Early effect, 371–373, 465**S**
MOSFET, 247–258, 328**S**, 331–334**P**
MOSFET and BJT, 557, 559–560
Current-voltage relationship, 158
junction, 147–152
Cut-in voltage, junction diode, 176
Cut off, diode, 166
Cutoff frequency, BJT, 708–710
Cutoff mode
BJT, 352, 353
operation of BJT, 379

D

DAC (digital-to-analog converter), 14, 46**P**
Dark field, VLSI layout, A15, A16
Darlington configuration, 549, 550, 553**S**
class AB output stage, 952–953, 967**S**
Darlington pair, 549
Dc amplifier, 40, 56
Dc analysis, 741 op-amp circuit, 1006–1031, 1050**S**, 1053–1054**P**
Dc bias point, 276–277
Dc collector currents, 741 op-amp circuit, 1013
Dc components, separating signal and, 409–410
Dc emitter–degeneration resistor, B27
Dc imperfections
input bias current (I_B), 93–95, 107**S**
input offset currents (I_{os}), 93–95, 107**S**
inverting integrator operation, 95–97
offset voltage (V_{os}), 89–92
op amp, 88–97, 120–122**P**
Dc operating point, 270, 398
Dc power supply, PSpice example, B18–B22
Dc restoration, 211
Dc restorer, 210–212, 216**S**
Dc voltage
common-mode feedback controlling, 1041–1043
MOSFET circuits, 258–267
Dead band, 919
Decibel, expressing gain in, 17
Deep-submicron design. *See* Technology scaling
Degeneration resistance, 309
Degenerative feedback, negative, 803
Depletion capacitance, 158
BJT, 707
pn junction, 154–155
Depletion-layer capacitance, MOSFET, 701, 702–703
Depletion region
open-circuit terminals, 139–140, 159**S**
width of and charge stored in, 141–143, 159**S**
Depletion-type MOSFET, 326–327, 328**S**, 347**P**
Desensitivity factor, feedback, 809
Design
bias, of BJT op amp, 1033–1035
BJT op amp, 1031–1049, 1050**S**, 1056–1057**P**
circuit data for second-order filters, 1288–1289, 1292–1293
input stage for rail-to-rail V_{ICM}, 1035–1038
output stage, for near rail-to-rail output swing, 1045–1049
pass-transistor logic (PTL) circuit, 1153–1154
pseudo-NMOS logic circuit, 1149–1150
Design abstraction, digital systems, 1088–1089
Design of dc power supply, PSpice example, B18–B22
Design parameters
BJT op amp, 1033
MOSFET and BJT, 559, 565–566
Design philosophy, IC (integrated circuit), 493, 494
Design trade-offs, two-stage CMOS op amp, 987–988
D flip-flop circuit, 1212–1214
Difference amplifier
CMRR (common-mode rejection ratio), 72
operational amp, 71–80, 115–118**P**
single op-amp, 72–75
superior circuit, 76–80
Difference-mode, MOS differential pair, 593
Differential amplifier
active-loaded MOS differential pair, 637–638
bipolar differential pair with active load, 644–650
BJT, 612–628, 672–676**P**
CMRR (common-mode rejection ratio), 641–644
common-mode gain, 641–644
differential gain of active-loaded MOS pair, 638–641
differential to single-ended conversion, 636
frequency response, 760–769, 796**P**
input bias and offset currents of bipolar, 634–635
input offset voltage of bipolar, 632–634
input offset voltage of MOS pair, 629–631
MOS, 588–612, 667–672**P**
MOS differential pair, 588–598, 603
nonideal characteristics, 629–635, 677–678**P**
preference to single-ended, 587–588
with active load, 635–650, 678–682**P**
Differential and multistage amplifier
BJT differential pair, 612–628
MOS differential pair, 588–598
Differential gain, *A*, 56
active-loaded MOS pair, 638–641
bipolar differential pair, 644–647
determining, 641
MOS differential pair, 599–601
Differential gain at dc, B3
Differential half-circuit
BJT differential pair, 622–624
MOS differential pair, 601–602
Differential-in
bipolar op amp, 657

Differential-in *(continued)*
op amp, 636
Differential-input, single-ended-output amplifier, 55
Differential-input resistance (R_{id}), 75, B3
Differential input signal
ideal op amp, 57–58
MOS differential pair, 593
Differential input voltage, MOS differential pair, 593–594
Differential-out
bipolar op amp, 657
op amp, 636
Differential output, 600
Differential-pair configuration
BJT, 612–628, 666**S**, 672–676**P**
MOS, 588–598, 666**S**, 667–668**P**
small-signal operation of MOS, 599–612, 666**S**, 668–672**P**
Differential voltage gain, BJT differential pair, 622
Differentiator, op amp, 80, 85, 87–88, 118–120**P**
Differentiator time-constant, 88
Diffusion, IC fabrication, A4–A5
Diffusion capacitance, 158
BJT, 707
pn junction, 155–157
Diffusion constant, 136
Diffusion constant and mobility, 138, 157
Diffusion current
open-circuit terminals, 139, 159**S**
semiconductor, 135–137, 158**S**
Diffusion current density, 157
Diffusion length, holes, 148
Diffusivity, 136
Digital circuit, 14
Digital IC technologies, inverter, 1086–1088
Digital logic inverter, 1062–1089, 1132**S**, 1134–1136**P**
BiCMOS, 1086, 1088
bipolar, 1086, 1087
CMOS, 1086–1087
computer aids, 1088–1089
design abstraction, 1088–1089
digital IC technologies, 1086–1088
digital-system design, 1088
energy-delay product (EDP), 1084–1085
function, 1062
gallium arsenide (GaAs), 1086, 1088
ideal VTC, 1066
inverter implementation, 1066–1069
logic circuit families, 1086–1088
noise margins, 1064–1065
power-delay product (PDP), 1084–1085
power dissipation, 1078–1080
propagation delay, 1080–1084
silicon area, 1085–1086
voltage-transfer characteristic (VTC), 1062–1064
Digital signal, 12, 41**S**, 45–46**P**
Digital-system design, 1088
Digital-to-analog converter (D/A or DAC), 14, 46**P**
Digitized signal amplitude, 12
Digit line, memory chip, 1215
Diode, 165–216
biasing class AB circuit, 929–930, 969–970**P**
breakdown region, 178–179, 215**S**
bridge rectifier, 199–200
clamped capacitor, 210–212, 227–229**P**
constant-voltage-drop model, 181–182
current-voltage characteristic, 166–167
DC restorer, 210–212
diode logic gates, 170–171
exponential model, 179, 180–181
forward-bias region, 175–177
full-wave rectifier, 197–199
graphic analysis, 180
half-wave rectifier, 195–197
ideal, 166–173, 216–219**P**
ideal-diode model, 183
iterative analysis, 180–181
laser, 215
light-emitting, (LEDs), 214–215
limiter circuits, 207–210, 227–229**P**
modeling forward characteristic, 179–189, 221–224**P**
operation in reverse breakdown region-zener diode, 189–194, 224–225**P**
peak rectifier, 200–205
photodiodes, 214
precision half-wave rectifier, 206–207
rapid analysis, 181
rectifier, 167–168
rectifier circuits, 194–207, 225–227**P**
rectifier with filter capacitor, 200–205
reverse-bias region, 178
Schottky-barrier, (SBD), 213–214
small-signal model, 184–187
superdiode, 206–207
terminal characteristics of junction, 173–179, 219–221**P**
varactors, 214
voltage doubler, 212–213
voltage regulation, 187
Diode-connected transistor, 260
Diode forward drop, voltage regulation, 187
Diode logic gates, 170–171
Diode model, SPICE, B4–B5
Diode small-signal conductance, 186
Diode small-signal resistance, 186
Direct-coupled amplifier, op amp, 56
Directly coupled (dc) amplifier, IC technology, 39, 40
Discrete circuit, electronic device, 5
Discrete-circuit bias, classical arrangement, 447–449
Discrete-circuit BJT amplifier, 453–462, 466**S**, 486–489**P**
CB (common-base), 458–459
CE (common-emitter), 455–456
CE with emitter resistance, 457–458
emitter follower, 460–461
frequency response, 461–462
structure, 453–454
Discrete-circuit MOS amplifier, 314–323, 328**S**, 345–347**P**
CG (common-gate) amplifier, 318, 320
CS (common-source) amplifier, 316–317
frequency response, 322–323
source follower, 321–322
structure, 314, 316
Discrete CS amplifier, Multisim example, B100–B103
Discrete-time signal, 12
Discretized signal amplitude, 12
Distortion, waveform, 15
DMOS (double-diffused MOS), transistor, 962–963, 967**S**
Dominant pole, 99
Dominant-pole response, 721
Domino CMOS logic, 1173–1175, 1195**S**
Donor, 130
Dopants, A5
Doped semiconductor, 129–132, 158**S**, 159**P**
n type, 129
p type, 129
Double-anode zener, 209
Double cascoding, 518, 519, 553**S**
Double limiter, 208
Drain, n^+, of MOSFET, 232–233
Drain diffusion, MOSFET, 701
Drain terminal, signal current, 277–279
Drain-to-gate feedback resistor, biasing, 311–312
Drift current
and equilibrium, 140–141, 159**S**
semiconductor, 132–133, 158**S**
Drift current density, 157
Driver, memory chip, 1216
Dry etching, A4
Dry oxidation, A2
Dummy cell, 1231
Duty cycle, 211, 1374
Dynamic memory, 1204
Dynamic MOS logic circuit, 1166–1175, 1195**S**, 1199**P**
basic principle, 1167–1168
cascading dynamic logic gates, 1172
charge sharing, 1171–1172
Domino CMOS logic, 1173–1175
evaluation phase, 1167
nonideal effects, 1170–1173
output voltage decay, 1170–1171
periodically refreshed, 1166
precharge phase, 1167
Dynamic operation
BiCMOS inverter circuit, 1193, 1194
CMOS inverter, 1098–1110, 1132**S**
pseudo-NMOS logic circuit, 1149
Dynamic power dissipation, 1078
CMOS inverter, 1109–1110
Dynamic random-access memory (DRAM) cell, 1217, 1225–1227, 1246**S**
differential operation in, 1231–1232
Dynamic resistance, 191
Dynamic sequential circuit, 1204

E

Early effect, 378
dependence of current on collector voltage, 371–373, 465**S**
small-signal models, 420–421
Early voltage, 372
Ebers–Moll model, B9
Edge triggered, 1212
Effective base width, 372
Effective voltage, 235
Efficiency (η), amplifier power, 18
Einstein relationship, 138
Electron-current density, 136
Elmore delay formula, 1163
Emission coefficient, B4
Emitter (E)
terminal, 28, 352
wideband amplification by, 770–773
Emitter-base junction (EBJ)
BJT, 352, 353, 465**S**
operation of BJT, 379
Emitter-coupled logic (ECL), 587, 1175–1190, 1195**S**, 1199–1201**P**
basic gate circuit, 1177–1180
basic principle, 1175–1176
circuit of 10K logic-gate family, 1178
current-mode logic (CML), 1177
families, 1176–1177
fan-out, 1185
manufacturers' specifications, 1184–1185
noise margins, 1183
NOR transfer curve, 1183–1184
OR transfer curve, 1181–1182
power dissipation, 1186–1187
PSpice example, B64–B69
signal transmission, 1185–1186
speed of operation, 1185–1186
thermal effects, 1187
voltage-transfer characteristic (VTC), 1180–1185
wired-OR capability, 1190

Emitter current
input resistance at emitter, 407–408
npn transistor in active mode, 357–358
Emitter-degenerated CE amplifier, output resistance, 524–525
Emitter degeneration resistance, 435
Emitter follower
BJT, 424, 425, 438–443, 466**S**
characteristic parameters, 439–441
characteristics, 446
discrete-circuit BJT, 460–461
high-frequency response, 758–760, 785**S**, 795–796**P**
overall voltage gain, 441–442
Thévenin representation of, output, 442–443
voltage buffers, 438–439
Emitter resistance, 407
common-emitter amplifier with, 432–435, 457–458
PSpice example, B27–B30
Energy-delay product (EDP), digital logic inverter, 1084–1085
Enhancement-mode operation, 239
Enhancement-type MOSFET, 239
Epitaxial layer, A5
Epitaxy, A5
Equations, summary of important, 157–158
Equiripple, 1259
Equivalence, 1138**P**
Equivalent circuit
BiCMOS inverter, 1193, 1194
high-frequency response, 731–732
ideal op amp, 56
two-stage CMOS op amp, 982
Equivalent-circuit model, npn transistor in active mode, 358–359
Equivalent feedback loop, generation, 1303–1307
Equivalent-load capacitance *C*, CMOS inverter, 1104–1107
Equivalent resistance, CMOS transmission gate, 1161–1164
Erasable programmable ROM (PROM), 1240, 1243–1245, 1246**S**
Error amplifiers, 937
Error signal, 806
Etching, A3, A4
Evaluation phase, 1167
Excess concentration, holes, 148
Exclusive-OR (XOR) function, CMOS logic circuit, 1115–1116
Exponential model
diode, 179
graphical analysis using, 180
iterative analysis using, 180–181

F

Fan-in, propagation delay, 1121
Fan-out
emitter-coupled logic (ECL), 1185
inverters, 1134**P**
propagation delay, 1121
Feedback, 802–890, 890–909**P**
amplifier poles, 870–879, 890**S**, 907–908**P**
analysis method, 863
bandwidth extension, 810–811
basic topologies, 814–822, 893–894**P**
current amplifier, 816–819, 864
equivalent of circuits from feedback-loop point, 866–867
frequency compensation, 884–886, 908–909**P**
gain desensitivity, 809
general, structure, 804–809, 890–891**P**
ideal series-shunt amplifier, 823–825
ideal series-shunt transconductance amplifier, 834–836
ideal shunt-series current amplifier, 855–856
ideal shunt-shunt transresistance amplifier, 846–848
interference reduction, 811–812
loop gain, 863, 865–868, 890**S**, 906–907**P**
Miller compensation, 886–889
negative, properties, 809–814, 890**S**, 891–893**P**
Nyquist plot, 869–870
pole splitting, 886–889, 890**S**
practical series-shunt amplifier, 825–827
practical series-shunt transconductance amplifier, 836, 837
practical shunt-series current amplifier, 856–858
practical shunt-shunt transresistance amplifier, 848–849
reduction in nonlinear distortion, 813–814
series-shunt transconductance amplifier, 834–846, 899–901
series-shunt voltage amplifier, 823–833, 894–899**P**
shunt-series current amplifier, 855–863, 903–906**P**
shunt-shunt transresistance amplifier, 846–855, 901–903**P**
SPICE simulations, 890**P**, 895**P**, 901**P**, 906**P**, 909**P**
stability problem, 868–870, 890**S**, 907**P**
stability study using Bode plots, 879–883, 908**P**
transconductance amplifier, 819–820, 864
transfer function of amplifier, 868–869
transresistance amplifier, 821–822, 864
voltage amplifier, 814–816, 864
Feedback amplifier
PSpice example, B46–B50
transfer function, 868–869
Feedback factor β, 805
Feedback loop
bistable multivibrator, 1355–1356
generation of equivalent, 1303–1307
oscillator, 1336–1337
single-amplifier biquadratic active filter, 1299–1302
Feedback transfer function, 868
Feedback triple, 842, 843
Field-programmable gate array (FPGA), 1088
Filter. *See also* Second-order active filter; Single-amplifier biquadratic active filter
all-pass function, 1281, 1284–1285
bandpass function, 1281, 1282
Butterworth filter, 1263–1267, 1327**S**, 1329**P**
Chebyshev filter, 1267–1270, 1327**S**, 1329**P**
first-order, 1271, 1272, 1273, 1327**S**
first-order and second-order, functions, 1270–1278, 1327**S**, 1329–1330**P**
high-pass function, 1281, 1282
low-pass function, 1280, 1281, 1282
notch functions, 1281, 1282–1284
passive sensitivities, 1308
resonator natural modes, 1279–1280
second-order, 1271, 1274–1275, 1276–1278
second-order active, based on inductor replacement, 1285–1293, 1328**S**, 1331**P**
second-order active, based on two-integrator-loop topology, 1293–1299, 1328**S**, 1331**P**
second-order LCR resonator, 1279–1285, 1327**S**, 1330–1331**P**
sensitivity, 1307–1309, 1328**S**, 1332**P**
single-amplifier biquadratic active, 1299–1307, 1328**S**, 1331–1332**P**
specification, 1257–1260, 1327**S**
switched-capacitor, 1310–1315, 1328**S**, 1332**P**
transfer function, 1260–1263, 1327**S**, 1329**P**
transmission, 1256–1257, 1327**S**, 1328–1329**P**
transmission zeros, 1280, 1281
types, 1257
Filter approximation, 1259
Filter capacitor, 200
rectifier with, 200–205
Filter order, 1260
Finite open-loop gain
circuit performance, 97–102, 122–123**P**
op amp, 61–62, 69
First-order filter, 1271, 1272, 1273, 1327**S**
First-order function, *s*-domain, F2–F3
Fixed-gain IC (integrated circuit), power amplifier, 956–959, 967**S**
Flash memories, 1245
Flat gain, 1275
Flip-flop, 1206–1214, 1246**S**, 1246–1247**P**
CMOS implementation of clocked set/reset (SR), 1211, 1212
CMOS implementation of SR, 1207–1211
D, circuit, 1212–1214
set/reset (SR), 1206–1207
Floating gate, 1244
Floating-gate transistor, 1244, 1245
Folded cascode
CMOS op amp, 991–1001, 1050**S**, 1052–1053**P**
IC (integrated circuit) amplifier, 519–520, 553**S**
Folded-cascode amplifier
Multisim example, B92–B95
PSpice example, B40–B46
Folded-cascode CMOS op amp
circuit, 991–993
frequency response, 996–997
input common-mode range, 993–994, 999–1000
operational transconductance amplifier (OTA), 995
output swing, 993–994
output voltage range, 1000–1001
rail-to-rail input operation, 999–1000
slew rate, 997
structure, 992
voltage gain, 994–996
wide-swing current mirror, 1000–1001
Forced ratio, 363
Forward base-transit time, 707
Forward bias, *pn* junction, 145–147
Forward-biased diode, 166
Forward-bias region, junction diode, 175–177
Forward current, 158
Fourier series, signal, 9–10
Fourier transform, 9, 10
Free electron, 126, 127, 158**S**
Frequency, magnitude of gain of CE amplifier vs., 688
Frequency compensation, 97, 878, 884–886, 908–909**P**
implementation, 885–886
Miller compensation, 886–889
pole splitting, 886–889, 890**S**
theory, 884–885
Frequency dependence, open-loop gain, 97–99, 107–108**S**
Frequency response
3-dB frequency, 721–723, 784–785**S**, 790–792**P**
741 op-amp circuit, 1027–1028, 1055–1056**P**
active-loaded MOS amplifier, 765–769
analysis tools of high-, of amplifiers, 721–731
bipolar op amp, 783–784
BJT high-frequency model, 706–711
differential amplifiers, 760–769
equivalent circuit, 731–732

Frequency response *(continued)*
exact circuit analysis, 737–741
folded-cascode CMOS op amp, 996–997
formulas for common-emitter (CE) amplifier, 741–742
high-, of bipolar cascode amplifier, 755–756
high-, of CE amplifier, 717–720, 731–745
high-, of CG (common-gate) amplifier, 746–750
high-, of CS (common-source) amplifier, 713–717, 731–745
high-, of emitter follower, 758–760
high-, of MOS cascode amplifier, 750–755
high-, of source follower, 756–758
high-frequency gain function, 721
high-frequency models, 701–711
internal capacitive effects, 701–711
low-, of CE amplifier, 694–701
low-, of CS amplifier, 689–694
low resistance R_{sig}, 742–745
Miller's theorem, 727–731, 732–735
MOSFET high-frequency model, 701–706
Multisim examples, B100–B103, B103–B107
multistage amplifier, 779–784
open-circuit time constants, 735–737
open-circuit time constants for upper 3-dB frequency, 724–727
PSpice example, B40–B43
resistively loaded MOS amplifier, 760–765
STC circuits, E6–E10
two-stage CMOS op amp, 780–783, 981–984
wideband amplifier configurations, 770–779
Frequency response of amplifier, 49–51**P**
amplifier bandwidth, 31, 32
amplifier classification based on, 38–40
BJT, 461–462
closed-loop amplifier, 99–102
evaluating, 31–32
measuring, 30–31, 41**S**
MOSFET, 322–323
single-time-constant (STC) networks, 33–35
Frequency-selection function, 1257
Frequency-selective network, 1336
Frequency spectrum of signals, 9–11, 45**P**
Full-power bandwidth, 106, 108**S**
Full-wave rectifier, 197–199, 215–216**S**
precision, 1382–1384
Function generators, 1336
Fundamental frequency, 10

G
Gain
741 op-amp circuit, 1026–1027, 1055–1056**P**
current gain, 16, 17
distribution in MOS cascode amplifier, 516
expressing in decibels, 17
increasing, of basic cell, 505–506
magnitude of, of CE amplifier vs. frequency, 688
power gain, 16–17
single-time-constant (STC) circuit, 33–35, 41**S**
voltage gain, 15–16
with feedback, 805
Gain-bandwidth (GB), frequency response, 323, 462
Gain-bandwidth product (GB), 98n.5, 101, 107–108**S**, 565, 744
Gain cell, IC amplifiers, 495–506, 553**S**, 569–572**P**
Gain desensitivity, negative feedback, 809
Gain expressions, BJT amplifier, 429–430
Gain function, 1256
high-frequency, 721
Gain margin, stability using Bode plots, 879–880
Gain-reduction factor, amount of feedback, 804
Gallium arsenide (GaAs), IC technology, 1086, 1088
Gate-capacitance parameters, MOSFET model, B7–B9
Gate capacitive effect, MOSFET, 701, 702
Gate circuit
emitter-coupled logic (ECL), 1177–1180
pseudo-NMOS logic circuit, 1150
Gate electrode, MOSFET, 232–233
Gate-to-source voltage, biasing, 307
Gate voltage, biasing, 308–311
Generation, 128
G_m-reduction method, 1031
Graded junction, 155
Grading coefficient, 155
Grounded-emitter circuit, transistor amplifier, 28
Gummel–Poon model, SPICE BJT model, B11

H
Half-wave rectifier, 195–197, 215**S**
precision, 1378–1379
Hard limiter, 208
Hartley oscillator, 1349, 1350
Heat sink, power BJT, 946–949
High frequency
3-dB frequency, 721–723
adapting formulas for CE (common-emitter) amplifier, 741–742
analysis tools for amplifiers, 721–731, 790–792**P**
bipolar cascode amplifier, 755–756, 785**S**, 794–795**P**
BJT model, 706–711, 784–785**S**, 788**P**
CE amplifier, 717–720, 731–745, 789–790**P**
CG (common-gate) amplifier, 746–750, 785**S**, 794–795**P**
CS (common-source) amplifier, 713–717, 731–745, 789–790**P**
CS amplifier with low resistance R_{sig}, 742–745
emitter follower, 758–760, 785**S**, 795–796**P**
equivalent circuit, 731–732
exact analysis of, in CS amplifier, 737–741
gain function, 721
gain of amplifier vs., 688
Miller's theorem, 727–731, 792**P**
MOS cascode amplifier, 750–755, 785**S**, 794–795**P**
MOSFET model, 703, 704, 784–785**S**, 788**P**
open-circuit time constants, 724–727, 735–737
response of CS and CE amplifiers, 731–745, 792–794**P**
source follower, 756–758, 785**S**, 795–796**P**
High-frequency hybrid model, BJT, 707–708
High-frequency model, MOSFET and BJT, 558, 564–565
High pass (HP), single time-constant (STC) networks, 33, 34, 35, 41**S**
High-pass (HP) circuit
design data, 1290, 1292
frequency response of STC circuits, E8–E10
pulse response, E14–E15
STC circuit, E4–E6
step response, E11–E12
High-pass (HP) filter, 1257, 1258, 1272, 1276
High-pass function, realization, 1281, 1282
High-pass notch (HPN) circuit, design data, 1291, 1293
High-pass notch (HPN) filter, 1277
Hole, 126, 127, 158**S**
Hole lifetime, 156
Hole mobility, 132
Hot electrons, A8
Hot spots, 949
Hybrid-π model
BJT, 410–411, 423, 707–708
MOSFET and BJT, 557, 561
T model, 288, 328**S**

I
IC (integrated-circuit) amplifier
basic gain cell, 495–506, 553**S**, 569–572**P**
basic MOSFET current source, 527–530
biasing, 526–537, 553**S**, 576–580**P**
BiCMOS cascodes, 525–526
bipolar mirror, 539, 553**S**
BJT cascode, 520–524
BJT circuits, 532–536
BJT parameters, 556–557
cascode amplifier, 506–526, 553**S**, 572–574**P**
cascode MOS mirrors, 538
CS and CE amplifiers with current-source loads, 495–496
current-mirror circuits, 537–546, 553**S**, 580–582**P**
Darlington configuration, 549, 550, 553**S**
design, A1, 40
design philosophy, 493, 494
double cascoding, 518, 519
folded cascode, 519–520
increasing gain of basic cell, 505–506
MOS cascode, 507–512
MOS current-steering circuits, 530–532
output resistance of current-source load, 499–500
output resistance of emitter-degenerated CE amplifier, 524–525
output resistance of source-degenerated CS amplifier, 517–518
power, 955–962, 967**S**, 973**P**
transistor pairings, 546–551, 553**S**, 582–583**P**
voltage gain distribution in cascode amplifier, 514–517
Widlar current source, 543–546, 553**S**
Wilson current mirror, 539–541, 553**S**
Wilson MOS mirror, 542–543, 553**S**
Ideal diode, 166–173, 183, 215**S**, 216–219**P**
Ideal operational amplifier, 54–58, 107**S**, 108–109**P**
Impedances, inverting configuration with, 80
Inactive transistor, BJT op amp, 1047–1049
Incremental diffusion capacitance C_d, 156–157
Incremental resistance, 186, 191
Inductorless filter, 1256
Inductor loss, tuned amplifier, 1317–1318
Infinite bandwidth, ideal op amp, 56
Input bias, bipolar differential amplifier, 634–635
Input bias current, 634
741 op-amp circuit, 1010
Input bias current (I_B), B3, 93–95, 96, 107**S**
Input common-mode range, B39
741 op-amp circuit, 1010
BJT differential pair, 615
design of input stage for rail-to-rail V_{ICM}, 1035–1038
folded-cascode CMOS op amp, 993–994, 999–1000
MOS differential pair, 590
two-stage CMOS op-amp, 977–978
Input differencing circuit, 806
Input differential resistance, BJT differential pair, 621–622
Input emitter follower, class AB output stage, 951
Input offset current, 634–635
741 op-amp circuit, 1010
Input offset current (I_{os}), B3, 93–95, 107**S**
inverting integrator operation, 95–97, 107**S**
Input offset voltage, 629
741 op-amp circuit, 1010
bipolar differential amplifier, 632–634
bipolar differential pair, 648–650
MOS differential pair, 629–631
two-stage CMOS op amp, 654–655
Input offset voltage (V_{os}), B3, 89–92, 107**S**
inverting integrator operation, 95–97, 107**S**
Input protection, MOSFET, 325–326
Input resistance
741 op-amp circuit, 1019–1020
MOSFET and BJT, 558
op amp, 62–65, 69
R_i, 22
Input signal, single-amplifier biquadratic active filter, 1302–1303
Input sinusoid (V_i), 30
Input stage
741 op-amp circuit, 1004, 1013–1016
common-mode feedback controlling dc voltage, 1041–1043
design for rail-to-rail V_{ICM}, 1035–1038
Input-stage bias, 741 op-amp circuit, 1007–1010
Instantaneous power dissipation, 915
Instrumentation amplifier, 76–80, 108**S**
Insulated-gate field-effect transistor (IGFET), 234
Integrated circuit, 125, 158**S**
Integrated circuit (IC), first, operational amplifier, 53
Integrated-circuit (IC) technology
IC chip, 5
microelectronics, 5–6
Integrated-circuit timer, 1369–1374, 1386**S**, 1392**P**
553 circuit, 1369–1370
astable multivibrator using 553 IC, 1372–1374
monostable multivibrator using 553 IC, 1370–1372
Integrated devices, A9
Integrator frequency, 83, 84
Integrators
inverting configuration with impedances, 80
inverting integrator, 80–85
op amp, 80–88, 108**S**, 118–120**P**
Integrator time constant, 82
Interconnect
inverter, 1105
technology scaling, 1130–1131
Interference reduction, feedback, 811–812
Internal capacitance, 38
BJT model, 706–711, 785**S**, 788**P**
MOSFET model, 701–706, 785**S**, 788**P**
Internally compensated op amps, 97
Intrinsic gain
basic gain cell, 496–498
MOSFET and BJT, 558, 561, 562
Intrinsic semiconductors, 126–129, 158**S**, 159**P**
Invention
BJT (bipolar junction transistor), 351–352
MOSFET, 352
Inversion layer, channel, 235
Inverter
BiCMOS, 1191–1193
digital logic inverter, 1062–1089, 1132**S**, 1134–1136**P**
dynamic operation of CMOS, 1098–1110, 1132**S**
equivalent load capacitance, 1104–1107
implementation, 1066–1069
output resistance, 1133
propagation delay, 1099–1104
pseudo-NMOS, 1144–1145
static characteristics of pseudo-NMOS, 1145–1146
Inverting configuration
analysis, 60
closed-loop gain, 59–61
finite open-loop gain, 61–62
general impedances, 80
input resistance, 62–65
negative feedback, 58
op amp (operation amplifier), 58–67, 109–113**P**
output resistance, 62–65
positive feedback, 58
weighted-summer circuit, 65–67
Inverting input terminal, 55, 56
Inverting integrator
offset current, 95–97, 107**S**
offset voltage, 95–97, 107**S**
op amp, 80–85
i_o, output current, 7
Ion implantation, IC fabrication, A5
Isotropic etching, A4

J
Junction
current-voltage relationship of, 147–152
description of operation, 145–147
Junction breakdown, 152
Junction built-in voltage, 141, 157, 159**S**
Junction capacitance
MOSFET, 702–703
pn junction, 154–155
Junction diode
breakdown region, 178–179
forward-bias region, 175–177, 215**S**
reverse-bias region, 178
terminal characteristics, 173–179, 219–221**P**
Junction temperature, 911
power BJT, 944

K
KHN biquad, 1295, 1296
Knee current, 190

L
Large-signal differential transfer characteristic, B35
Large-signal equivalent circuit, MOSFET, 250, 251
Large-signal models, 359
Large-signal operation
BJT differential pair, 616–617
full-power bandwidth, 106, 107
MOS differential pair, 594–598
op amp (operational amplifier), 102–107, 123**P**
output current limits, 102, 103–104
output voltage saturation, 102, 103–104
slew rate (SR), 104–105, 106, 107, 123**P**
Laser diode, 215
Latch, memory, 1204–1206, 1246**S**, 1246–1247**P**
Lateral *pnp* transistor, A12, 556
Layout, VLSI, A14–A16
LC-tuned oscillator, 1349–1352, 1386**S**, 1389–1390**P**
Colpitts oscillator, 1349, 1350
Hartley oscillator, 1349, 1350
Least significant bit (LSB), 13
Light-emitting diode (LED), 126, 214–215
Lightly doped drain (LDD), A8
Limiter circuit, 207–210, 216**S**, 227–229**P**
amplitude control, 1339–1341
Linear amplification
biasing BJT, 397–399
biasing MOSFET, 269–270
Linear amplifier, 15, 16
Linearity, 15
Linearized amplifier transfer, 813
Linear macromodel, op-amp, B1–B3
Linear oscillators, 1336
Line regulation, 192
Load, signal source, 6
Load line, graphical analysis, 180
Load regulation, 192
Load resistance, 396
MOSFET, 268
Local oxidation of silicon (LOCOS), A7
Logarithmic amplifier, 1393
Logic AND function, 170
Logic circuit. *See* Advanced logic circuit; BiCMOS digital circuit; CMOS (complementary MOS) logic circuit; Dynamic MOS logic circuit; Emitter-coupled logic (ECL); Pass-transistor logic circuit; Pseudo-NMOS logic circuit
Logic-circuit families, digital logic inverter, 1086–1088
Logic gate, BiCMOS, 1193, 1194
Logic inverter. *See* also Digital logic inverter
digital, 1062–1089, 1132**S**, 1134–1136**P**
Logic OR function, 170
Loop gain, PSpice example, B46–B50
Loop gain, $A\beta$
alternative approach, 865–866
determining, 809**S**, 863, 865–868, 906–907**P**
equivalence of circuits from feedback-loop point, 866–867
feedback amplifier, 805, 890**S**
Low frequency
3-dB frequency, 692–693
common-emitter amplifier, 694–701, 785–787**P**
common-source amplifier, 689–694, 785–787**P**
gain of amplifier vs., 688
Low-frequency small-signal model, MOSFET and BJT, 557, 561
Low-frequency T model, MOSFET and BJT, 558
Low pass (LP), single time-constant (STC) networks, 33, 34, 41**S**
Low-pass (LP) circuit
design data, 1290, 1292
frequency response of STC circuits, E6–E8
pulse response, E13–E14
STC circuit, E4–E6
step response, E10–E11
Low-pass (LP) filter, 1257, 1258, 1272, 1276
single time-constant networks, 33
Low-pass amplifier, 40
Low-pass function, realization, 1280, 1281, 1282
Low-pass notch (LPN) circuit, design data, 1291, 1293
Low-pass notch (LPN) filter, 1277
Lowpass-to-bandpass transformation, 1324

M
Macromodel, B1
Magnitude
amplifier, 31, 35
(V_o/V_i), 31
Magnitude response, frequency response of STC networks, 34
Main memory, 1214
Majority charge, 130
Manufacturer, emitter-coupled logic (ECL), 1184–1185
Mask-programmable, read-only memory (ROM), 1242–1243
Mask programming, 1243
Mass-storage memory, 1214
Master-slave configuration, 1213, 1214
Maximally flat response, 875, 1264
Maximum switching frequency, 1081
Mean transit time, 156
Medium-scale integrated (MSI), circuit package, 1087
Memory, 1203
Memory access time, memory chip, 1217
Memory cell, memory chip, 1215

Memory-chip organization, 1215–1217, 1246**S**
Memory-chip timing, 1217
Memory circuit
  clocked set/reset (SR) flip-flop, 1211, 1212
  column-address decoder, 1237, 1246**S**
  D flip-flop circuit, 1212–1214
  dynamic memory cell, 1225–1227
  erasable programmable ROM (EPROM), 1243–1245, 1246**S**
  flip-flop, 1206–1214, 1246**S**, 1246–1247**P**
  latch, 1204–1206, 1246**S**, 1246–1247**P**
  mask-programmable read-only memory (ROM), 1242–1243
  memory-chip organization, 1215–1217
  memory-chip timing, 1217
  MOS ROM, 1240–1242
  programmable ROMs, 1243–1245
  pulse-generation circuits, 1238–1240
  random-access memory (RAM) cells, 1217–1227, 1246**S**, 1248–1249**P**
  read-only memory (ROM), 1240–1243, 1246**S**, 1250–1251**P**
  read operation of static memory (SRAM), 1218–1222
  row-address decoder, 1235–1237, 1246**S**, 1249–1250**P**
  semiconductor memories, 1214–1217, 1246**S**, 1247–1248**P**
  sense amplifier, 1227–1235, 1246**S**, 1249–1250**P**
  set/reset (SR) flip-flop, 1206–1207, 1246**S**, 1246–1247**P**
  SR flip-flop implementation in CMOS, 1207–1211
  SRAM cell, 1218–1225
  write operation of SRAM, 1222–1225
Memory cycle time, 1217
Memory element, bistable circuit, 1358
Metallization, IC fabrication, **A6**
Metastable state, 1356
Meter conversion factors, **H2**
Microcomputer, microelectronic circuit, 5
Microelectronics, integrated-circuit (IC) technology, 5–6
Microprocessor, microelectronic circuit, 5
Midband
  frequency response, 322, 461–462, 687
  gain of CE amplifier vs. frequency, 688
Miller compensation, 886–889
Miller effect, 714, 730, 785**S**
Miller integrator, 83, 84, 85, 108**S**, 118–119**P**
Miller multiplication, 730
Miller multiplier, 714
Miller's theorem
  analysis using, 732–735
  high-frequency response, 727–731, 792**P**
Minority carrier, 354
Minority-carrier charge storage, 158
Minority carrier lifetime, 156, 158
Minority charge, 130
Mirror pole and zero, 767
Mixed-mode, circuit design, 14
Mixed-signal, circuit design, 14
Mixed-signal circuits, CMOS op amp, 986
Mixer, 806
Mobility and diffusion constant, 138, 157
Model
  741 op-amp circuit, 1028–1029
  body effect, 324–325
  cascaded amplifiers, 24–26
  circuit, 21
  constant-voltage-drop, 181–182
  determining resistance R_i and R_o, 27
  diode forward characteristic, 179–189, 221–224**P**
  ideal diode, 183, 215**S**
  relationships between amplifier, 27
  small-signal, for diode, 184–187
  small-signal, of 741 op-amp circuit, 1023–1025
  unilateral, 28–30
  voltage amplifiers, 22–23
  zener diode, 190–191
Monolithic circuit, 125, 158**S**
Monostable multivibrator, 1336, 1367–1369, 1386**S**, 1392**P**
  553 IC, 1370–1372
Monostable multivibrator circuit, 1239–1240
Moore's law, 330**P**, 1122
MOS (metal oxide semiconductor). *See* also Dynamic MOS logic circuit
  active-loaded MOS amplifier, 765–769
  cascode, 507–512, 553**S**
  cascode MOS mirror, 538, 553**S**
  current-steering circuit, 530–532
  differential pair, 588–598
  double-diffused (DMOS) transistor, 962–963, 967**S**
  power transistors, 962–966, 967**S**, 973**P**
  read-only memory (ROM), 1240–1242
  resistively loaded MOS amplifier, 760–765
  Wilson MOS mirror, 542–543, 553**S**
MOS cascode amplifier, high frequency response, 750–755, 785**S**, 794–795**P**
MOS differential pair, 599–612, 667–672**P**
  active-loaded, 637–638, 765–769
  basic configuration, 588
  cascode differential amplifier, 604–605
  CMRR (common-mode rejection ratio), 605–612
  common-mode gain, 605–612
  differential amplifier with current-source loads, 603
  differential gain, 599–601
  differential gain of active-loaded, 638–641
  differential half-circuit, 601–602
  differential vs. single-ended output, 612
  g_m mismatch on CMRR, 608–610
  input offset voltage, 629–631
  large-signal operation, 594–598
  operation with common-mode input voltage, 589–590
  operation with differential input voltage, 593–594
  resistively loaded, 760–765
  small-signal operation, 599–612
MOSFET (metal oxide semiconductor field-effect transistor)
  amplifier frequency response, 322–323
  applying, in amplifier design, 268–276, 337–339**P**
  basic, amplifier configuration, 291–306, 341–343**P**
  basic MOSFET current source, 527–530
  biasing, for linear amplification, 269–270
  biasing in, amplifier circuits, 306–314, 343–345**P**
  bias point Q, 275, 276
  body effect, 323–325, 347**P**
  breakdown and input protection, 325–326
  characterizing amplifiers, 293–294, 306
  circuits at dc, 258–267, 334–337**P**
  circuit symbol, 247–248
  common-drain (CD) amplifier, 293, 302–305
  common-gate (CG) amplifier, 292, 300–302, 318, 320
  common-source (CS) amplifier, 292, 294–297, 316–318, 319
  comparison to BJT, 554–569, 583–585**P**, 965
  complementary MOS (CMOS), 246
  constant-current source, 312–313
  creating channel for current flow, 234–236
  CS amplifier with source resistance, 297–300
  current-voltage characteristics, 247–258, 331–334**P**
  dc bias point, 276–277
  depletion-type, 326–327, 328**S**, 347**P**
  device structure, 232–234, 329–330**P**
  discrete-circuit, amplifiers, 314–323, 345–347**P**
  drain-to-gate feedback resistor, 311–312
  finite output resistance in saturation, 253–256
  fixing gate-to-source voltage V_{GS}, 307
  gate voltage V_G, 308–311
  high-frequency model, 701–706, 784–785**S**, 788**P**
  i_D-v_{DS} characteristics, 248–250
  i_D-v_{GS} characteristic, 250–253
  insulated-gate FET (IGFET), 234
  internal capacitance, 701–706, 785**S**, 788**P**
  model, 1129
  operation, 234–246, 329–330**P**
  p-channel, 244–246, 256–258
  separating dc analysis and signal analysis, 279, 280
  signal current in drain terminal, 277–279
  small-signal equivalent-circuit model, 280–281
  small-signal operation and models, 276–291, 337–341**P**
  small-signal voltage gain, 270–273
  source follower, 293, 302–305, 321–322
  square-law MOSFET model, 569
  structure of power MOSFET, 962–963, 967**S**
  subthreshold region, 246
  temperature, 325
  T equivalent-circuit model, 287–290
  three-terminal device, 231–232, 351–352
  transconductance g_m, 282–286
  unity-gain frequency, 703–705
  unmatched, in CMOS inverter, 1094–1095
  values of MOSFET parameters, 554–555
  velocity saturation, 326
  V-groove, 963
  VLSI process, **A9–A10**
  voltage amplifier, 268
  voltage gain, 279
  voltage transfer characteristic (VTC), 268–269
  voltage v_{DS} application, 236–239
  voltage v_{DS} increase, 239–241
  voltage v_{DS} reaching V_{OV}, 242–244
  VTC by graphical analysis, 274–275
  zero gate voltage, 234
MOSFET model, **B5–B9**
  dimension and gate-capacitance parameters, **B7–B9**
  diode parameters, **B6–B7**
MOSFET transconductance parameter, 238
Most significant bit (MSB), 13
Multiple tuned circuit, amplifier with, 1318–1321
Multisim examples. *See also* PSpice examples
  class B bipolar output stage, **B112–B118**
  CMOS CS amplifier, **B88–B92**
  CMOS inverter, **B123–B127**
  CE amplifier with emitter resistance, **B85–B88**
  CS amplifier, **B75–B83**
  dependence of β on bias current, **B83–B84**
  folded-cascode amplifier, **B92–B95**
  frequency response of discrete CS amplifier, **B100–B103**
  two-stage CMOS op amp, **B118–B123**, **B95–B100**
  two-stage CMOS op amp with series-shunt feedback, **B107–B112**
Multistage amplifier, 651–665, 666**S**, 682–685**P**
  bipolar op amp, 657–665, 783–784
  frequency response, 779–784, 799**P**, 801**P**
  two-stage CMOS op amp, 651–657, 780–783
Multistage differential BJT amplifier, PSpice amplifier, **B33–B40**
Multivibrator. *See also* Astable multivibrator; Bistable multivibrator; Monostable multivibrator
  circuit building block, 1336
Multivibrator circuit, 1239–1240

N

n-channel, MOSFET, 232–233, 234–235, 247–248, 328**S**
n type, doped semiconductor, 129
n-type silicon, **A2**
n well, CMOS, 246
n-well process, **A7**
NAND gate
  pseudo-NMOS type, 1150
  two-input, of BiCMOS inverter, 1193, 1194
NAND gate, two-input, 1114–1115
Narrow-band approximation, 1324
Narrow-band property, 1315
Natural devices, 1159
Natural modes, **F2**, 1260
  resonator, 1279–1280
Near rail-to-rail output swing, BJT op amp, 1033, 1045–1049
Negative feedback
  bandwidth extension, 810–811
  degenerative, 803
  gain desensitivity, 890
  interference reduction, 811–812
  inverting configuration, 58
  properties, 809–814, 890**S**, 891–893**P**
  reduction in nonlinear distortion, 813–814
Negative-feedback loop, 1008
Network parameter. *See* Two-port network parameter
Network theorem, **D1–D5**, **D5–D6P**
  Norton's theorem, **D1**, **D2**
  source-absorption theorem, **D3**
  Thévenin's theorem, **D1**, **D2**
Neutralizing, circuits, 1320
NMOS transistor, 234–235
  switch for PTL circuit, 1154–1156
  values, 554
Nodes, 1122
Noise margin
  digital logic inverter, 1064–1065, 1133
  emitter-coupled logic (ECL), 1183
  high-input, 1064
  low-input, 1064
Nondestructive, read operation, 1219
Nonideal characteristics, differential amplifier, 629–635, 677–678**P**
Nonideal operation, dynamic logic circuit, 1170–1173
Noninverting amplifier performance, PSpice example, **B13–B15**
Noninverting configuration
  analysis of circuit, 68
  closed-loop gain, 67–68
  finite open-loop gain, 69
  input resistance, 69
  op amp, 67–71, 107**S**, 113–115**P**
  output resistance, 69
  voltage follower, 69–71
Noninverting input terminal, 55, 56, 107**S**
Noninverting transfer characteristic, bistable circuit, 1359
Nonlinear-amplification method, sine-wave shaping, 1377
Nonlinear amplitude control, sinusoidal oscillator, 1339
Nonlinear distortion, amplifier, 15
Nonlinear distortion reduction, negative feedback, 813–814
Nonlinear macromodel, op-amp, **B3–B4**
Nonlinear oscillators, 1336
Nonlinear waveform-shaping circuit, 1374–1377, 1386**S**, 1392–1394**P**
  breakpoint method, 1375–1377
  nonlinear-amplification method, 1377
NOR gate, pseudo-NMOS type, 1150
NOR gate, two-input, 1113, 1114
Norton form, 6, 41**S**
Norton's equivalent, source, 7, 8, 45**P**, 864
Norton's theorem, **D1**, **D2**, 6
NOR transfer curve, emitter-coupled logic (ECL), 1183–1184
Notch (N) circuit, design data, 1291, 1292
Notch filter, 1275, 1277
Notch frequency, 1275
Notch function, realization, 1281, 1282–1284
Not-programmed state, 1244
npn transistor
  741 op-amp circuit, 1005
  base current, 356–357
  BJT, 353, 361
  BJT op amp, 1033
  collector current, 356
  current flow, 354–356
  emitter current, 357–358
  equivalent-circuit model, 358–359
  operation in active mode, 353–361, 465**S**
  parameter values, 556–557
  recapitulation, 358–359
Nyquist criterion, 870
Nyquist plot, stability, 869–870

O

Off current, 1130
Off resistance, inverter, 1067
Offset current, bipolar differential amplifier, 634–635
Offset voltage (V_{os}), 89–92, 107**S**
  inverting integrator operation, 95–97, 107**S**
Ohmic contacts, 214
Ohm's law, 42**P**
  output voltage, 66
One-shot multivibrator circuit, 1239–1240
One-transistor cell, 1225, 1246**S**
"On" resistance, inverter, 1067
Op amp (operational amplifier), 3
  bandwidth, 97–102
  bipolar, 657–665, 666**S**
  circuit performance, 97–102
  closed-loop gain, 59–61, 67–68
  common-mode input signal, 57–58
  dc imperfections, 88–97
  difference amplifiers, 71–80, 115–118**P**
  differential input signal, 57–58
  differentiators, 80, 85, 87–88
  finite open-loop gain, 61–62, 69, 97–102
  folded-cascode CMOS op amp, 991–1001, 1050**S**, 1052–1053**P**
  frequency response of bipolar, 783–784
  frequency response of two-stage CMOS, 780–783
  function and characteristics of ideal, 55–56
  ideal, 54–58
  input bias current (I_B), 93–95, 107**S**
  input offset currents (I_{os}), 93–95, 107**S**
  input resistance, 62–65, 69
  integrated-circuit (IC), 53–54
  integrators, 80–88
  inverting configuration, 58–67, 109–113**P**
  inverting integrator operation, 95–97
  large-signal operation, 102–107, 123**P**
  noninverting configuration, 67–71, 113–115**P**
  offset voltage, 89–92
  output resistance, 62, 65, 69
  power, 960, 961
  terminals of ideal, 54–55
  two-stage CMOS, 651–657, 666**S**
  two-stage CMOS op amp, 976–991, 1050**S**, 1051–1052**P**
  voltage follower, 69–71
  weighted-summer circuit, 65–67
Op-amp (operational-amplifier) circuit. *See also* 741 op-amp circuit; BJT op amp (operational amplifier); Folded-cascode CMOS op amp; Two-stage CMOS op amp
  741, 1002–1005, 1050**S**, 1053**P**
  bias design of BJT, 1033–1035
  BJT, 1031–1049, 1050**S**, 1056–1057**P**
  DC analysis of 741, 1006–1013, 1050**S**, 1053–1054**P**
  design of input stage to rail-to-rail V_{ICM}, 1035–1038
  folded-cascode CMOS, 991–1001, 1050**S**, 1052–1053**P**
  frequency response of 741, 1027–1028, 1050**S**, 1055–1056**S**
  gain of 741, 1026–1027, 1050**S**, 1055–1056**S**
  output-stage design for near rail-to-rail output swing, 1045–1049
  slew rate of 741, 1029–1030, 1050**S**, 1055–1056**S**
  small-signal analysis of 741, 1013–1026, 1050**S**, 1054–1055**P**
  two-stage CMOS, 976–991, 1050**S**, 1051–1052**P**
Op-amp model, SPICE, **B1–B4**
Op amp-RC oscillator circuit, 1342–1349, 1386**S**, 1387–1389**P**
  active-filter-tuned oscillator, 1347–1349
  phase-shift oscillator, 1344–1346
  quadrature oscillator, 1346–1347
  Wien-bridge oscillator, 1342–1344
Op amp-RC resonator, second-order active filter, 1286–1288, 1327**S**
Open-circuit (equilibrium), *pn* junction, 145–147
Open-circuit overall voltage gain, 1023
Open-circuit time constants, 724
  3-dB frequency, 724–727, 785**S**
  analysis using, 735–737
Open-circuit transresistance, 26
Open-circuit voltage gain, 22–23, 26, 425, 561
  amplifier, 294
Open-loop gain, 56, 805
  finite, 61–62, 69, 97–102, 122–123**P**
  frequency dependence of, 97–99, 107–108**S**
Open-loop transfer function, 868
Operating point, graphical analysis, 180
Operational transconductance amplifier (OTA), 995
Operation region, pseudo-NMOS inverter, 1147, 1148
Operation speed, emitter-coupled logic (ECL), 1185–1186
Optoelectronic, 214
Optoisolator, 215
Order of the network, **F2**
OR function, CMOS logic circuit, 1115–1116
OR transfer curve, emitter-coupled logic (ECL), 1181–1182
Oscillation criterion, 1337–1338
Oscillator, 869. *See* also Sinusoidal oscillator
  active-filter-tuned, 1347–1349
  crystal, 1353–1355, 1386**S**, 1389–1390**P**
  feedback loop, 1336–1337
  LC-tuned, 1349–1352, 1386**S**, 1389–1390**P**
  phase-shift, 1344–1346, 1386**S**
  quadrature, 1346–1347
  Wien-bridge, 1342–1344, 1386**S**
Output current limits, 102, 103–104

Output dc offset voltage, 629
Output resistance, 373
  741 op-amp circuit, 1020–1021
  class AB output stage, 926–927
  CMOS class AB output stage, 937–939
  current-source load, 499–500
  emitter-degenerated CE amplifier, 524–525
  inverter, 1133
  MOSFET and BJT, 558, 561–562
  op amp, 62–65, 69
  R_o, 22
  source-degenerated CS amplifier, 517–518
Output resistance (R_o), B3, 640–641
Output short-circuit protection, 741 op amp, 1026
Output sinusoid (V_o), 30
Output stage
  741 op-amp circuit, 1005, 1022–1025
  biasing class AB circuit, 929–933, 969–970P
  class A, 913–918, 967S, 967–968P
  class AB, 924–928, 967S, 969P
  class B, 918–924, 967S, 968–969P
  classification, 912–913
  CMOS class AB, 933–943, 967S, 970P
  design of BJT op amp, 1045–1049
  variations on class AB configuration, 950–955, 971–973P
Output-stage bias, 741 op-amp circuit, 1011–1012
Output swing
  folded-cascode CMOS op amp, 993–994
  near rail-to-rail, of BJT op amp, 1033, 1045–1049
  two-stage CMOS op-amp, 977–978
Output voltage decay, dynamic logic circuit, 1170–1171
Output voltage limit, 741 op-amp circuit, 1022–1023
Output voltage range, folded-cascode CMOS op amp, 1000–1001
Output voltage saturation, 102, 103–104
Overall voltage gain, common-source amplifier, 296
Overdriven, input stage, 1029
Overdrive voltage, 235
Overdrive voltage (V_{ov}), 258, 328S
Overlap capacitance, MOSFET, 702
Oxidation, IC fabrication, A2–A3
Oxide capacitance (C_{ox}), 236

P
p-base resistor, A12–A13
p-channel, MOSFET, 244–246, 256–258
p-channel MOS (PMOS), 258, 328S
p-type, doped semiconductor, 129
p-type silicon, A2
p-well process, A7
Packaging, IC fabrication, A6
Pair
  bipolar differential, with active load, 644–650
  BJT differential pair, 612–628, 672–676P
  conjugate, F2
  MOS differential pair, 599–612, 667–672P
  transistor, 546–551, 553S, 582–583P
Parameter
  741 op amp circuit, 1005
  BJT IC (integrated circuit), 556–557, 1033
  body-effect, 324
  CD (common-drain) amplifier, 303–305
  CE (common-emitter) amplifier, 427–428, 446
  CMOS device, 554–555
  CS (common-source) amplifier, 295–296, 306
  emitter follower, 439–441
  gate-capacitance, for MOFSET model, B7–B9
  MOSFET, 554–555
  MOSFET diode, B6–B7
  MOSFET transconductance, 238
  PMOS, 554
  process transconductance, 238
  source follower, 303–305, 306
  two-port network, C1-C7
  values of power transistors, 950
Passband, filter, 1257
Passband ripple, 1258
Passing signals, 1257
Passive LC filter, 1256
Passive limiters, 207
Passive sensitivities, 1308
Pass-transistor logic (PTL), 1153
Pass-transistor logic circuit, 1152–1166, 1195S, 1197–1199P
  CMOS transmission gates as switches, 1159–1164
  complementary pass-transistor logic (CPL), 1165
  design requirement, 1153–1154
  equivalent resistance of transmission gate, 1161–1164
  examples, 1164–1166
  NMOS transistors as switches, 1154–1156
  restoring value of V_{OH} to V_{DD}, 1158–1159
PD ("pull-down") switch, 1068
PD device, 1091
PDN (pull-down network), CMOS logic circuit, 1110–1113, 1115
Peak detector, 205
Peak inverse voltage (PIV), 196
Peak rectifier, 200–205
  buffered, 1385–1386
  precision, 1385
Performance, BJT op amp, 1031–1033
Periodic square wave, frequency spectrum, 10
Phase margin
  closed-loop response, 880–881
  stability using Bode plots, 879–880
  two-stage CMOS op amp, 982–984
Phase response
  amplifier, 31, 35
  angle ø, 30, 31
  frequency response of STC networks, 34
Phase-shift oscillator, 1344–1346, 1386S
Photodiode, 214
Photolithography, IC fabrication, A3–A4
Photonic, 214
Physical frequencies, F1
Physical frequency, transfer function T, 32
Piecewise linear, diode, 166
Pierce oscillator, 1354, 1355
Pinched-base resistor, A12–A13
Pinched-off channel, MOSFET, 242, 249
PMOS parameters, 554
pn junction
  applied voltage, 145–154, 159S, 161P
  capacitive effects, 154–157, 159S, 161–162P
  current-voltage relationship, 147–152
  depletion of junction capacitance, 154–155
  depletion region, 139–140, 159S
  description of junction operation, 145–147
  diffusion capacitance, 155–157
  diffusion current I_D, 139, 159S
  drift current I_S and equilibrium, 140–141, 159S
  junction built-in voltage, 141, 159S
  open-circuit terminals, 138–145, 159S, 160P
  operation with open-circuit terminals, 139–143
  physical structure, 138, 139, 159S
  reverse breakdown, 152–154
  width of and charge stored in depletion region, 141–145, 159S
pn junction diode, VLSI process, A11
pnp transistor
  741 op-amp circuit, 1005
  BJT, 353
  BJT op amp, 1033
  lateral *pnp*, 556
  operation in active mode, 364–365
  small-signal models, 412
Pole
  amplifier, 870–879, 907–908P
  amplifiers with three or more, 877–879
  amplifier with single-, response, 872–873
  amplifier with two-, response, 873–877
  feedback amplifier, 872
  s-domain analysis, F2
  splitting, 886–889, 890S
  stability and, location, 871–872
Pole frequency, F2, 874, 1274
  inspection, 693
  STC networks, 35
Pole Q, 1274
Pole Q factor, 874
Pole quality factor, 1274
Pole splitting, 886–889, 890S
Poly Si (polycrystalline silicon), A5–A6
Positive feedback, 657
  inverting configuration, 58
  regenerative, 803
  sense amplifier with, 1228–1230
Positive-feedback loop, 1336
Power amplifier, 15, 17–19
  bridge-amplifier configuration, 960–962
  fixed-gain IC (integrated circuit), 956–959
  IC, 955–962, 967S, 973P
  op amps, 960, 961
Power-balance equation, amplifier, 18
Power BJT, 943–950, 970–971P
  BJT safe operating area, 949–950
  heat sink, 946–949
  junction temperature, 944
  parameter values of power transistors, 950
  power dissipation vs. temperature, 944–945
  thermal resistance, 944
  transistor case, 946–949
Power-conversion efficiency
  class A output stage, 917–918
  class B output stage, 920–921
Power-delay product (PDP), digital logic inverter, 1084–1085
Power-derating curve, 945
Power dissipation
  class A output stage, 915–916
  class B output stage, 921–922
  digital logic inverter, 1078–1080
  dynamic, of CMOS inverter, 1109–1110
  emitter-coupled logic (ECL), 1186–1187
  power BJT, 944–945
Power efficiency, 18
Power gain of amplifier (A_p), 16–17
Power MOSFET
  characteristics of, 963, 964
  class AB output stage, 965–966
  comparison to BJTs, 965
  DMOS (double-diffused), 962
  structure, 962–963
  temperature effects, 964–965
Power supply, PSpice example, B18–B22
Power-supply hum, 812
Power-supply rejection ratio (PSRR), two-stage CMOS op amp, 986–987
Power transformer, 195
Power transistor, parameter values, 950
Power transistors, 911
Preamplifier, 15, 812
Precharge phase, 1167
Precharging, read operation, 1218
Precision half-wave rectifier, 206–207
Precision rectifier circuit, 1378–1386, 1386S, 1394–1395P
  alternative circuit, 1379–1380
  buffered precision peak detector, 1385–1386
  measuring AC voltage, 1380–1382
  precision bridge rectifier for instrumentation, 1384
  precision clamping circuit, 1386
  precision full-wave rectifier, 1382–1384
  precision half-wave rectifier, 1378–1379
  precision peak rectifier, 1385
  "superdiode," 1378–1379, 1385
Primary winding, 195
Processes, VLSI, A6–A14
Process transconductance parameter, 238
Programmable ROM (PROM), 1240, 1243–1245
Propagation delay
  CMOS inverter, 1099–1104, 1133
  digital logic inverter, 1080–1084
  fan-in and fan-out, 1121
Pseudo-NMOS logic circuit, 1144–1152, 1195S, 1196–1197P
  design, 1149–1150
  dynamic operation, 1149
  gate circuits, 1150
  inverter, 1144–1145
  static characteristic, 1145–1146
  voltage-transfer characteristic (VTC) derivation, 1146–1149
PSpice examples. *See also* Multisim examples
  active-filter-tuned circuit, B77–B79
  CE amplifier with emitter resistance, B27–B30
  characteristics of 741 op amp, B15–B18
  class B BJT output stage, B50–B55
  CMOS CS amplifier, B29, B30–B33
  CS amplifier, B23–B25
  dependence of BJT β on bias current, B26–B27
  design of dc power supply, B18–B22
  fifth-order Chebyshev filter, B69–B71
  folded-cascode amplifier, B43–B46
  frequency response of CMOS CS and folded-cascode amplifier, B40–B43
  loop gain of feedback amplifier, B46–B50
  multistage differential BJT amplifier, B33–B40
  operation of CMOS inverter, B60–B63
  performance of noninverting amplifier, B13–B15
  static and dynamic operation of ECL gate, B64–B69
  two-integrator-loop filter, B71–B74
  two-stage CMOS op amp, B55–B60
  Wien-bridge oscillator, B75–B77
PU (pull-up) device, 1091
PU switch, 1068
PU resistor, 1068
Pull-down (PD) device, 1091
Pull-down (PD) switch, 1068
Pull-down network (PDN), CMOS logic circuit, 1110–1113, 1115
Pulse generation circuit
  monostable multivibrator circuit, 1239–1240
  ring oscillator, 1238–1239
Pulse response, STC circuit, E13–E15
Pulsewidth modulation, 211
PUN (pull-up network), CMOS logic circuit, 1110–1113, 1115
Punch-through, MOSFET, 326
Push-pull manner, 622, 919

Q
Quadrature oscillator, 1346–1347, 1386S
Quantization error, 13
Quantized signal amplitude, 12
Quiescent point, 186, 270, 398

R
Radio frequency choke, 1318
Rail-to-rail input common-mode range, BJT op amp, 1032–1033
Rail-to-rail input operation, folded-cascode CMOS op amp, 999–1000
Rail-to-rail output swing, output stage design for near, 1045–1049
RAM (random-access memory), 1214, 1246S
RAM (random-access memory) cells, 1217–1227, 1246S, 1248–1249P
  dynamic memory cell (DRAM), 1217, 1225–1227
  read operation, 1218–1222
  static memory (SRAM) cell, 1218, 1225, 1246S
  write operation, 1222–1225
Random offset, 654
Rapid analysis, diode, 181
Rated output voltage, 102
Rate of closure, stability, 883
RC ladder network, 1163, 1164
Reactive ion etching (RIE), A3–A4
Read-only memory (ROM), 1215, 1246S
  erasable programmable ROM (EPROM), 1240, 1243–1245
  mask-programmable, 1242–1243
  MOS ROM, 1240–1242
  programmable ROM (PROM), 1243–1245
Read operation
  memory chip, 1215
  static memory (SRAM) cell, 1218–1222
Read/write memory, 1215
Recapitulation, *npn* transistor in active mode, 358–359
Recombination, 127–128
Recombination process, electrons, 355–356
Rectifier. *See* also Precision rectifier circuit
  diode, 167–168
Rectifier circuit, 194–207, 215S, 225–227P
  bridge, 199–200
  filter capacitor, 200–205
  full-wave, 197–199, 215–216S
  half-wave, 195–197, 215S
  peak rectifier, 200–205
  precision half-wave, 206–207
  superdiode, 206–207
Reference bias current, 741 op-amp circuit, 1007
Reference current, 526
Refresh process, 1204
Regenerative feedback, positive, 803
Regions, operation of pseudo-NMOS inverter, 1147, 1148
Regular notch (N), design data, 1291, 1292
Resistance, determining R_i and R_o, 27
Resistance-reflection rule, 433
Resistance R_{sig}, CS amplifier with low, 742–745
Resistance values, standard, H1–H2
Resistively loaded MOS amplifier, 760–765
Resistivity, ρ, 133, 157
Resistor
  combining, 42P
  p-base and pinched-base, A12–A13
  VLSI process, A10
Resonator circuit, design data, 1287, 1292
Resonator natural modes, 1279–1280
Reverse bias, *pn* junction, 145–147
Reverse biased diode, 166
Reverse-bias region, junction diode, 178
Reverse breakdown, *pn* junction, 152–154
Reverse breakdown region, zener diode, 189–194, 224–225P
R_i
  determining, 27
  input resistance, 22
Ringing, 1186
Ring oscillator, 1238–1239
Ripple, 195, 216S
Ripple bandwidth, 1259
Ripple voltage, 203
Rise and fall times, inverter, 1083
R_L, load resistance, 6–7
R_o
  determining, 27
  output resistance, 22
ROM. *See* Read-only memory (ROM)
Root-locus diagram, two-pole response, 873–874
Row-address decoder, 1235–1237, 1246S
Row decoder, memory chip, 1215
R_s, source resistance, 6

S
s-domain analysis, F1–F6, F6–F7P
  Bode plots, F3–F6
  first-order functions, F2–F3
  poles, F2
  zeros, F2
Safe operating area, BJT, 949–950
Sallen-and-Key circuits, 1305, 1306
Sampling process, 12
Saturation
  amplifier, 19, 20
  finite output resistance, 253–256
Saturation current, junction diode, 175, 178
Saturation current, I_S, 150, 158, 356
Saturation mode
  BJT, 352, 353
  BJT operation, 362–363, 465S
  operation of BJT, 379
Saturation region, MOSFET, 242–243, 248, 249, 258, 328S
Saturation resistance, 374–376
Saturation voltage, 374–376
Scale current, 356
  junction, 150
  junction diode, 175
Scaling. *See* Technology scaling
Schmitt trigger, 1358
Schottky-barrier diode (SBD), 213–214, 1043
Secondary winding, 195
Second breakdown, BJT safe operating area, 949, 950
Second-generation current convoyer, 905P
Second-order active filter. *See* also Filter
  all-pass circuit, 1289, 1292, 1293
  Antoniou inductance-simulation circuit, 1285–1286
  circuit implementation, 1295–1297
  design for circuits, 1292–1293
  inductor replacement, 1285–1293, 1328S, 1331P
  KHN biquad, 1295
  op-amp-RC resonator, 1286–1288
  realization of types, 1288–1289
  Tow–Thomas biquad, 1297–1298, 1328S
  two-integrator-loop biquad, 1293–1295
  two-integrator-loop topology, 1293–1299, 1328S, 1331P
Second-order filter function, 1271, 1274–1274, 1276–1278
Second-order LCR resonator, 1279–1285, 1327S, 1330–1331P
  all-pass function, 1281, 1284
  bandpass function, 1281, 1282
  high-pass function, 1281, 1282
  low-pass function, 1280, 1281, 1282
  notch function, 1281, 1282–1284
  resonator natural modes, 1279–1280
  transmission zeros, 1280, 1281
Second stage, 741 op-amp circuit, 1004–1005, 1019–1021

Second-stage bias, 741 op-amp circuit, 1011
Selected memory chip, 1215
Select gate, 1244
Selectivity factor, 1257
Semiconductor
  capacitive effects in *pn* junction, 154–157, 161–162**P**
  current flow in, 132–138, 159–160**P**
  diffusion current, 135–137
  doped, 129–132, 159**P**
  drift current, 132–133
  Einstein relationship, 138
  important equations, 157–158
  integrated circuit, 125
  intrinsic, 126–129, 159**P**
  monolithic circuit, 125
  pn junction with applied voltage, 145–154, 161**P**
  pn junction with open-circuit terminals, 138–145, 160**P**
  relationship between diffusion and mobility, 138, 157
Semiconductor memory, 1214–1217, 1246**S**, 1247–1248**P**
  main memory, 1214
  mass-storage, 1214
  memory-chip organization, 1215–1217
  random-access memory (RAM), 1214
  read-only memory, 1215
  read/write, 1215
Sense amplifier, 1227–1235, 1246**S**, 1249–1250**P**
  alternative, 1233–1235
  differential operation in dynamic RAMs, 1231–1232
  memory chip, 1216
  operation, 1230
  positive feedback, 1228–1230
  precharging, 1233
Sensitivity, 1307–1309, 1328**S**, 1332**P**
Sequential circuit, 1203
Series-series feedback
  ideal transconductance amplifier, 834–836
  practical transconductance amplifier, 836, 837
  topology, 819–820, 864
  transconductance amplifier, 834–846, 899–901**P**
Series-shunt feedback, 814, 815, 816, 864
  ideal voltage amplifier, 823–825
  Multisim examples, **B107–B112**
  practical voltage amplifier, 825–827
Set/reset (SR) flip-flop, 1206–1207
  CMOS implementation of, 1207–1211
  CMOS implementation of clocked, 1211, 1212
Shallow trench isolation (STI), **A7**
Sheet resistance, 1141**P**
Short-base diode, 161**P**
Short-channel, velocity saturation, 1124
Short-channel effects, square-law MOSFET model, 569
Short-circuit current gain β, 26, 28, 29
Short-circuit protection, 916
  741 op-amp circuit, 1004
  class AB output stage, 954, 955
Short-circuit transconductance, 26
Shunt regulator, zener diode, 191–193
Shunt-series feedback, 817, 864
  current amplifier, 855–863, 903–906**P**
  ideal, 855–856
  practical, 856–858
Shunt-shunt feedback
  topology, 821–822, 864
  transresistance amplifier, 846–855, 901–903**P**
SiGe BiCMOS process, **A13**, **A14**
Signal, 45**P**
  amplification, 14–15
  amplifier, 15
  analog and digital, 11–14
  frequency spectrum of, 9–11, 45**P**
  load, 6
  Norton form, 6, 7–8
  processing, 6
  separating, and dc quantities, 409–410
  source, 6–8
  Thévenin form, 6, 7–8
  time-varying quantity, 8
Signal current, MOSFET drain terminal, 277–279, 328**S**
Signal generators and waveform-shaping circuits
  astable multivibrator, 1363–1367, 1386**S**, 1391**P**
  bistable multivibrator, 1355–1362, 1386**S**, 1390–1391**P**
  crystal oscillator, 1353–1355, 1386**S**, 1389–1390**P**
  integrated-circuit (IC) timer, 1369–1374, 1386**S**, 1392**P**
  LC-tuned oscillator, 1349–1352, 1386**S**, 1389–1390**P**
  monostable multivibrator, 1367–1369, 1386**S**, 1392**P**
  nonlinear waveform-shaping circuit, 1374–1377, 1386**S**, 1392–1394**P**
  op amp-RC oscillator circuit, 1342–1349, 1386**S**, 1387–1389**P**
  precision rectifier circuit, 1378–1386, 1386**S**, 1394–1395**P**
  sinusoidal oscillators, 1336–1341, 1386**S**, 1387**P**
Signal ground
  common-emitter amplifier, 455
  common-source amplifier, 316
Signal-to-interference ratio, 811
Signal transmission, emitter-coupled logic (ECL), 1185–1186
Signal waveform, class A output stage, 915
Silicon area, digital logic inverter, 1085–1086
Silicon chip, circuit component, 5
Silicon dioxide, oxidation, **A2**
Silicon wafer, IC fabrication, **A2**
Simulation. *See* Multisim examples; PSpice examples; SPICE simulation
Sine-wave shaper, 1375
Sine-wave signal
  frequency, 11, 41**S**
  voltage, 9
Sine-wave voltage signal, $v_s(t)$, 9
Single-amplifier biquadratic active filter. *See also* Filter
  generation of equivalent feedback loops, 1303–1307
  injecting input signal, 1302–1303
  Sallen-and-Key circuits, 1305
  synthesis of feedback loop, 1299–1302
Single-amplifier biquads (SABs), 1299, 1328**S**
Single-ended conversion, differential to, 636
Single-ended outputs, 600
Single-flow diagram, feedback structure, 804
Single limiter, 208
Single operational amplifier, difference amplifier, 72–75
Single-pole model, 99
Single-pole response, amplifier, 872–873
Single-supply operation, class B output stage, 924
Single-time-constant (STC) networks, 33–35, 41**S**
Single-time-constant circuit, **E16–E17P**
  classification, **E4–E6**
  evaluating time constant τ, **E1–E4**
  frequency response of high-pass (HP), **E8–E10**
  frequency response of low-pass (LP), **E6–E8**
  high-pass (HP), **E4**, **E5**
  low-pass (LP), **E4**, **E5**
  pulse response of HP, **E14–E15**
  pulse response of LP, **E13–E14**
  rapid evaluation of τ, **E1–E4**
  step response of HP, **E11–E12**
  step response of LP, **E10–E11**
Single-tuned amplifier, 1315–1316
Sinusoidal oscillator, 1336–1341, 1386**S**, 1387**P**
  feedback loop, 1336–1337
  limiter circuit for amplitude control, 1339–1341
  nonlinear amplitude control, 1339
  oscillation criterion, 1337–1338
Sinusoidal signal, 30–31, 41**S**
Six-transistor, 1218, 1246**S**
Sizing
  CMOS inverter, 1107–1109, 1132**S**
  transistor, of CMOS gate circuit, 1117–1120
Slew rate (SR)
  741 op-amp circuit, 1029–1031, 1055–1056**P**
  folded-cascode CMOS op amp, 997
  large-signal operation, 104–105, 106, 107, 108**S**
  two-stage CMOS op amp, 984–986
Small-scale integrated (SSI), circuit package, 1087
Small-signal analysis, circuit diagram, 419–420
Small-signal approximation, 185, 404
Small-signal condition, MOSFET, 278
Small-signal diffusion capacitance, BJT, 707
Small-signal emitter–degeneration resistance, B27
Small-signal equivalent-circuit model, 280–281, 290, 328**S**, 412
Small-signal gain, 741 op-amp circuit, 1026–1027
Small-signal model
  741 op-amp circuit, 1023–1025
  BJT as amplifier, 403–422, 423, 465**S**, 477–481**P**
  diode, 184–187
  Early effect, 420–421
  MOSFET, 280–281, 328**S**
Small-signal operation
  BJT as amplifier, 403–422, 465**S**, 477–481**P**
  BJT differential pair, 618–624
  MOS differential pair, 599–612
Small-signal voltage gain, 270–273, 328**S**, 399–400
Soft limiting, 208, 209
Solar cell, 214
Source
  n^+, of MOSFET, 232–233
  wideband amplification by, 770–773
Source-degenerated CS amplifier, output resistance, 517–518
Source-degeneration resistance, 299
Source diffusion, MOSFET, 701
Source follower
  characteristic parameters, 303–305, 306
  discrete-circuit MOS, 321–322
  high-frequency response, 756–758, 785**S**, 795–796**P**
  MOSFET, 293, 302–305, 328**S**, 341–343**P**
Source resistance, common-source amplifier with, 297–300, 318, 319
Space-charge region, 139
Specification, filter, 1257–1260, 1327**S**
Speed of operation, emitter-coupled logic (ECL), 1185–1186
SPICE device models
  BJT model, **B9–B12**
  diode model, **B4–B5**
  MOSFET models, **B5–B9**
  Multisim examples, **B75–B127**
  op-amp model, **B1–B4**

  PSpice examples, **B13–B79**
  zener diode model, **B5**
SPICE simulation, 785**P**, 1051**P**, 1196**P**, 1246**P**, 1328**P**, 1387**P**. *See also* Multisim examples; PSpice examples
  BJT circuit, 378, 466**P**, 471**P**, 473**P**, 483**P**, 484**P**, 486**P**
  CMOS logic circuit, 1134**P**, 1137**P**
  diodes, 197, 216**P**, 223**P**, 225**P**
  feedback, 890**P**, 895**P**, 901**P**, 906**P**, 909**P**
  IC (integrated circuit) amplifier, 569**P**, 574**P**, 577**P**, 580**P**
  low-frequency of common-source amplifier, 689
  MOS differential pair, 667**P**, 671**P**
  MOSFET, 298, 329**P**, 336**P**, 340**P**, 344**P**, 345**P**
Splitting, pole, 886–889, 890**S**
Square-law model, **B5**
Square-law MOSFET model, 569
Square wave signal, frequency spectrum, 10
Stability
  Bode plots for investigating, 881–883
  pole location, 871–872
Stability problem
  feedback, 868–870, 890**S**, 907**P**
  Nyquist plot, 869–870
  transfer function of feedback amplifier, 868–869
Stable circuit, **F2**
Stacked-gate cell, 1244
Stagger tuning, tuned amplifier, 1323–1327, 1328**S**
Standard cells, 1089
Standardized pulse, monostable multivibrator, 1367–1369, 1386**S**, 1392**P**
Standard resistance values, **H1–H2**
Static power dissipation, 1078
Static random-access memory (SRAM) cell, 1217, 1218–1225, 1246**S**
  read operation, 1218–1222
  write operation, 1222–1225
Static sequential circuit, 1204
Step response, STC circuits, **E10–E12**
Stopband, filter, 1257
Stopping signals, 1257
Structure
  CMOS logic circuit, 1110–1113
  general feedback, 804–809, 890–891**P**
Subthreshold conduction, 1129–1130
Subthreshold region
  MOS transistor, 246
  operation, 497
Superdiode, 206–207
  precision rectifier, 1378–1379, 1385
Superposition principle, difference amplifier, 73–74
Sustained oscillations, 1338
Sustaining voltage, 463
Switch
  CMOS transmission gates as, in PTL circuit, 1159–1164
  NMOS transistors as, in PTL circuit, 1154–1156
Switched-capacitor filter, 1256, 1310–1315, 1328**S**, 1332**P**
  practical circuits, 1312–1315
  principle, 1310–1311
Symbol
  amplifier circuit, 15
  total instantaneous current, 20–21
Symbol convention, 20–21, 365–367
Synthesis, CMOS logic circuit, 1117
Synchronous tuning, tuned amplifier, 1321–1323
Systematic input offset voltage, bipolar differential pair, 648–650
Systematic offset, **B37**, 654
Systematic output dc outset voltage, CMOS op-amp circuit, 977

T

T model
  BJT, 411–412
  MOSFET, 287–290, 328S
  MOSFET and BJT, 558
Technology generation, 1122
Technology scaling, 1122–1131, 1139–1141**P**
  deep-submicron design, 1122–1131, 1139–1141**P**
  device and voltage scaling, 1123
  interconnect, 1130–1131
  scaling implications, 1123
  subthreshold conduction, 1129–1130
  velocity saturation, 1124–1129
  wiring, 1130–1131
Telescopic cascode, 520n.3
Temco, 194
Temperature
  BJT, 464, 465
  emitter-coupled logic (ECL), 1187
  MOSFET, 325
  MOS power circuits, 964–965
  zener diode, 194
Temperature coefficient (TC), 194
Terminal characteristics, junction diode, 173–179, 219–221**P**
Terminals, operational amplifier, 54–55, 107**S**
Thévenin-equivalent circuit, 43**P**
  second-stage, 1021
Thévenin form, 6, 41**S**
Thévenin representation, emitter-follower output, 442–443
Thévenin's equivalent, source, 7, 8, 45**P**, 864
Thévenin's theorem, **D1**, **D2**, 6
Thermal dissipation, BJT safe operating area, 950
Thermal resistance, power BJT, 944
Thermal runaway, 930, 949, 967**S**
Thermal shutdown, class AB output stage, 955, 956
Thermal voltage, 138
  junction diode, 175
Three-stage amplifier, cascade, 24–25
Three-terminal device
  BJT (bipolar junction transistor), 351–352
  MOSFET, 231–232
Threshold voltage, channel, 235
Time constant, τ, single-time-constant circuits, **E1–E4**
Topologies, basic feedback, 814–822, 864, 893–894**P**
Total harmonic distortion (THD), 911, 1377
Total instantaneous current, 20–21
Totem-pole configuration, 1191
Tow–Thomas biquad, second-order active filter, 1297–1298, 1328**S**
Transconductance amplifier, 27, 41**S**
  circuit model, 26, 47–49**P**
  feedback, 834–836, 864, 899–901**P**
  feedback topology, 819–820
  ideal, 834–836
  operational, 995
  practical, 836, 837
Transconductance g_m
  741 op-amp circuit, 1020
  BJT, 404–406
  body, 324–325
  determining, 638–640
  MOSFET, 278, 282–286
  MOSFET and BJT, 558, 561
Transconductance parameter
  MOSFET, 238
  process, 238
Transducer, 6
Transfer characteristic
  bistable circuit, 1356–1358
  bistable circuit with noninverting, 1359
  class A output stage, 913–915
  class B output stage, 919–920
  CMOS class AB output stage, 939–941
  linear amplifier, 16, 19, 20, 41**S**
Transfer function
  feedback amplifier, 868–869
  filter, 1256, 1260–1263, 1327**S**, 1329**P**
  frequency response of STC networks, 34
  $T(s)$, 32, 41**S**
Transfer-function poles, **F2**, 1260
Transfer-function zeros, **F2**, 1260
Transformer, tuned amplifier, 1318
Transistor
  graphical representation, 370, 371
  inactive, of BJT op amp, 1047–1049
Transistor breakdown, BJT, 463–464
Transistor case, power BJT, 946–949
Transistor pairing, 546–551, 553**S**, 584–585**P**
  CC–CE, 546–547
  CD–CE, 546–547
  CD–CS, 546–547
  Darlington configuration, 549, 550, 553**S**
Transistor sizing, CMOS gate circuit, 1117–1120
Transition band, 1257
Transition frequency, 564, 987
  BJT, 710
  MOSFET, 703–705
  MOSFET and BJT, 559
Transition region, 1064
Transmission
  filter, 1256–1257, 1327**S**, 1328–1329**P**
  frequency response of STC networks, 34
Transmission-gate logic, 1153
Transmission zeros, **F2**, 1260
  realization, 1280, 1281
Transresistance amplifier, 27, 41**S**
  circuit model, 26
  feedback, 846–855, 901–903**P**
  ideal, 846–848
  practical, 848–849
  topology, 821–822, 864
Tree decoder, 1237
Triangular waveform, astable circuit, 1366–1367
Trigger, bistable circuit, 1358
Trigger signal, 1358
Triode region, MOSFET, 243, 248, 249, 258, 328**S**
Tuned amplifier, 40, 1315–1327, 1328**S**, 1332–1333**P**
  cascode, 1321
  CC–CB cascade, 1321
  inductor losses, 1317–1318
  multiple tuned circuits, 1318–1321
  principle, 1315–1317
  stagger-tuning, 1323–1327, 1328**S**
  synchronous tuning, 1321–1323
  transformers, 1318
Turned on, diode, 166
Twin-well CMOS process, **A7–A9**
Two-input NAND gate, 1114–1115
  BiCMOS gate, 1193, 1194
Two-input NOR gate, 1113, 1114
Two-integrator-loop biquad, second-order active filter, 1293–1295
Two-integrator-loop filter, PSpice example, **B71–B74**
Two-pole response, amplifier, 873–877
Two-port network, **C7P**
  characterization of linear, **C1–C7**
  equivalent-circuit, **C5–C6**
  g parameters, **C5**
  h parameters, **C4–C5**

Two-port network *(continued)*
y parameters, C2–C3
z parameters, C3–C4
Two-power supply, classical bias arrangement, 450–451
Two-stage CMOS op amp, 651–657, 666**S**, 976–991, 1050**S**, 1051–1052**P**
circuit, 977
common-mode rejection ratio (CMRR), 981
configuration, 651, 976
design trade-offs, 987–988
frequency response, 780–783, 981–984
input common-mode range, 977–978
Multisim example, B118–B123, B95–B100
Multisim examples, B107–B112
output swing, 977–978
phase margin, 982–984
power-supply rejection ratio (PSRR), 986–987
PSpice example, B55–B60
simplified equivalent circuit, 982
slew rate, 984–986
transition frequency, 987
voltage gain, 652, 978–980

U

Unconditionally stable, single-pole amplifier, 872
Uncovered, charge, 139
Unilateral, amplifier circuit, 294, 427–428
Unilateral model, 28–30
Unit prefixes, H1–H2
Unity-gain amplifier, 69–70
Unity-gain bandwidth, 98, 107–108**S**, 709, 985–986, 1030–1031
Unity-gain frequency, 565, B3
MOSFET, 703–705

V

Varactors, 214
V_{BE} multiplier, biasing class AB circuit, 931–932, 967**S**, 969–970**P**
Velocity saturation, 963
deep-submicron process, 1124–1129
MOSFET, 326
Vertical, *npn* transistor, 556
Very-large-scale integration (VLSI), 1078
V-groove MOSFET, 963
Virtual ground, 59, 600
Virtual short circuit, 59
VLSI (very-large-scale-integrated circuits)
BiCMOS process, A12
capacitors, A10–A11
chemical vapor deposition, A5–A6
circuit design, 1087
diffusion, A4–A5
etching, A4
fabrication steps, A2–A6
fabrication technology, A1–A17
integrated devices, A9
ion implantation, A5
lateral *pnp* transistor, A12
metallization, A6
MOSFETs, A9–A10
oxidation, A2–A3
packaging, A6
p-base and pinched-base resistors, A12–A13
photolithography, A3–A4
pn function diodes, A11
resistors, A10
SiGe BiCMOS process, A13, A14
silicon wafers, A2
twin-well CMOS process, A7–A9
VLSI layout, A14–A16
VLSI processes, A6–A14
v_o, output voltage, 7
Voltage, sine-wave signal, 9
Voltage amplifier, 15, 41**S**
BJT, 396
circuit model, 22–23, 26, 47**P**
feedback topology, 814–816, 864
ideal case, 823–825
MOSFET, 268
practical case, 825–827
series-shunt feedback, 823–833, 894–899**P**
Voltage buffer
emitter follower, 438–439
source-drain amplifier, 302–303
Voltage-controlled switch, inverter, 1066–1067
Voltage divider, 42–43**P**
Voltage doubler, 212–213
Voltage follower, noninverting configuration, 69–71
Voltage gain, 279
BJT, 408–409
common-emitter (CE) amplifier, 428–429
distribution in cascode amplifier, 514–517
emitter follower, 441–442
folded-cascode CMOS op amp, 994–996
small-signal, 399–400
two-stage CMOS op amp, 652, 978–980
Voltage gain of amplifier (A_v), 15–16, 17, 22
Voltage-mixing, current-sampling, topology, 819–820
Voltage-mixing, voltage-sampling, 814
Voltage regulator, diode forward drop, 187
Voltage scaling, device and, 1123
Voltage signal, $v_i(t)$, 9
Voltage transfer characteristic (VTC), 268–269, 397
CMOS class AB output stage, 939–941
CMOS inverter, 1092–1094, 1129, 1133
digital logic inverter, 1062–1064, 1066
emitter-coupled logic (ECL), 1180–1185
graphical analysis, 274–275, 401–402
logic inverter, 1065, 1066
pseudo-NMOS inverter, 1146–1149
regions of pseudo-NMOS inverter operation, 1147, 1148
Voltage v_{DS}
increasing, 239–241, 329–330**P**
MOSFET, 236–239

W

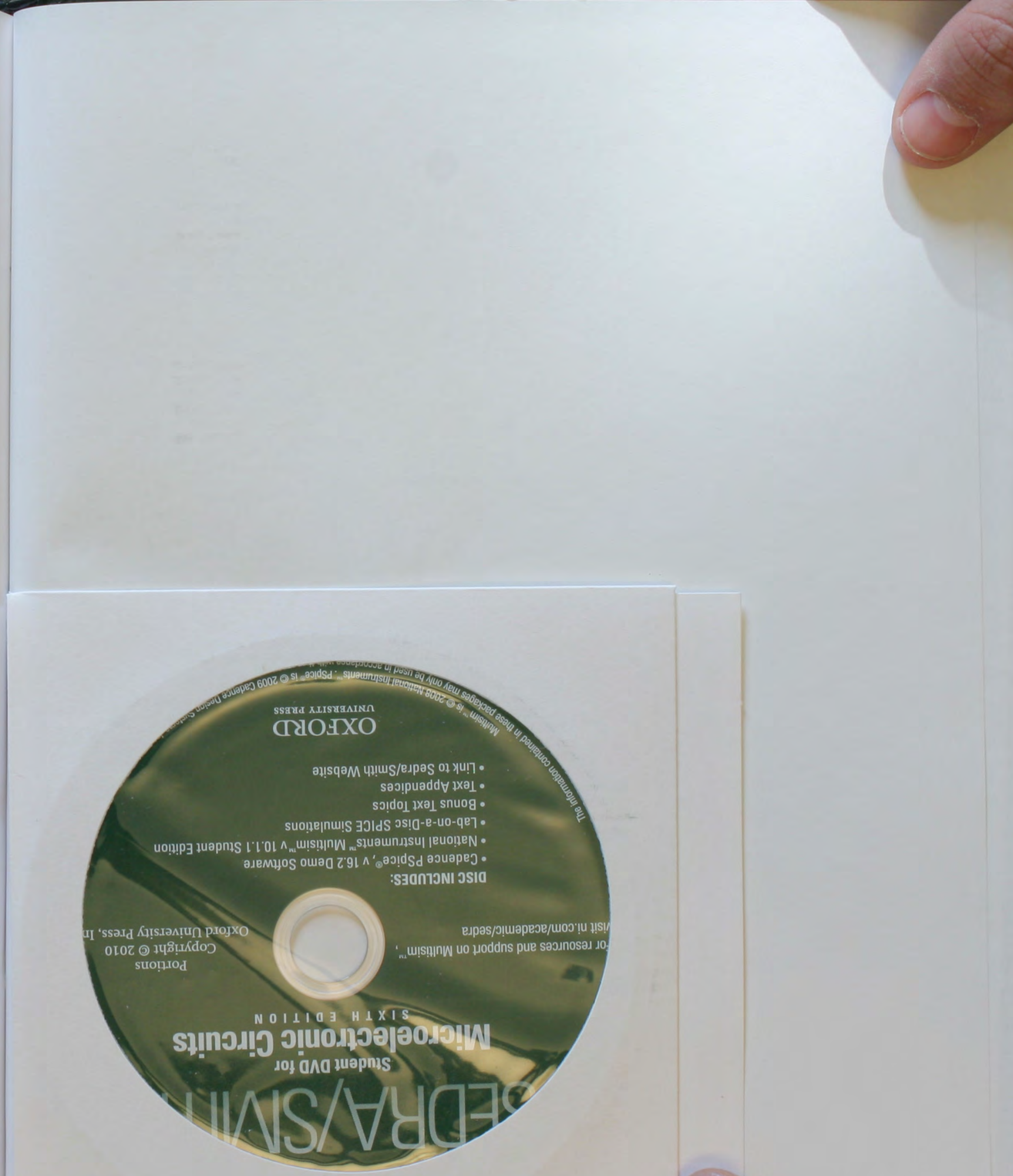
Waveform, frequency spectrum, 11
Waveform shaping, 1375
Waveform-shaping circuit. *See also* Signal generators and waveform-shaping circuits
nonlinear, 1374–1377, 1386**S**, 1392–1394**P**
Weak avalanche, MOSFET, 325
Weighted-summer circuit, inverting configuration, 65–67
Wet etching, A4
Wet oxidation, A2
Wideband amplifier
CC–CB configuration, 777–779
CC–CE configuration, 773–777
CD–CE configuration, 773
CD–CG configuration, 777–779
CD–CS configuration, 773
configurations, 770–779, 785**S**, 796–799**P**, 800**P**
source and emitter degeneration, 770–773
Wide-swing current mirror, folded-cascode CMOS op amp, 1000–1001
Widlar current source, 543–546, 553**S**
Width of depletion region, 141–145, 157
Wien-bridge oscillator, 1342–1344, 1386**S**
PSpice example, B75–B77
Wilson current mirror, 539–541, 553**S**
Wilson MOS mirror, 542–543, 553**S**
Wired-OR capability, emitter-coupled logic (ECL), 1190
Wiring, technology scaling, 1130–1131
Wiring capacitance $C\omega$, 1105
Word line, memory chip, 1215
Write operation
memory chip, 1216
static random-access memory (SRAM), 1222–1225

X

XOR function, CMOS logic circuit, 1115–1116

Z

Zener diode
modeling, 190–191
reverse breakdown region, 189–194, 215**S**, 224–225**P**
shunt regulator, 191–193
specifying, 190–191
temperature, 194
Zener diode model, B5
Zener effect, *pn* junction breakdown, 153
Zero
mirror pole and, 767
s-domain analysis, F2
Zero gate voltage, diode, 234, 329–330**P**



Today's Technologies. Tomorrow's Engineers.

The best-selling microelectronics textbook worldwide continues its standard of excellence and innovation built on the solid pedagogical foundation that Adel S. Sedra and Kenneth C. Smith have shared with more than one million students to date. All material in the sixth edition of *Microelectronic Circuits* has been thoroughly updated to reflect changes in technology. These technological changes have shaped the book's organization and topical coverage, making it the most current resource available for tomorrow's engineers learning how to analyze and design electronic circuits.

ADDITIONAL SUPPORT

- **Lab-on-a-Disc in-text DVD** contains complete simulations with activities, investigations, and directions for examples in the chapters and study problems from the ends of chapters, simulated in Multisim™ and PSpice®. Also includes student versions of PSpice® and Multisim™ so you can simulate your own activities and designs.
- **Bonus text topics** including JFETs, TTL, GaAs circuits, and Bode plots are also contained on disc.
- **Companion websites** www.sedrasmith.org and www.oup.com/us/sedrasmith feature PowerPoint-based figures from the text, device datasheets, and links to industry and academic sites.

ABOUT THE AUTHORS

Adel S. Sedra is Dean of the Faculty of Engineering at the University of Waterloo and former Vice President and Provost of the University of Toronto.

Kenneth C. (KC) Smith is Professor in Electrical and Computer Engineering, Computer Science, Industrial and Mechanical Engineering, and Information Studies at the University of Toronto.

FEATURES

- **Design problems for the real world:** Includes design problems in the end-of-chapter homework problems and real-world examples in the chapters. Sedra and Smith concentrate on developing your design sensibility, so you understand the "trade-offs" and "what-ifs" inherent in engineering design.
- **Extensive SPICE simulation:** Uses both National Instruments™ Multisim™ software and Cadence PSpice® software, providing a full lab experience for students using SPICE. Also includes a new Appendix on Design and Simulation using SPICE.
- **Flexible quick-start on op amps:** Op amps are covered in Chapter 2, so that you can encounter a real device right away, and start lab experiments.
- **Parallel treatment of MOSFETs and BJTs:** The chapters on BJTs and MOSFETs are exactly parallel, so whichever you read first, you can then speed through the second topic by concentrating only on the differences between the two transistors.
- **Abundant examples and study problems:** Examples, exercises, and end-of-chapter study problems—more than half of which are new or revised—help you learn.
- **Streamlined and Signposted:** Shorter, more modular chapters are easier to study. Visual cues and icons make the book easier to navigate. Explanations to the reader of why to read sections—and how multiple techniques might be used—are much more prominent. A new icon clearly marks topics that can be skipped on a first reading, while you are grasping the basics, or that look ahead to advanced industrial applications. Other icons indicate key equations, and which problems and examples are good candidates for SPICE simulation.
- **Semiconductor primer in a separate chapter:** If you have not taken a prior course in Semiconductor Device Physics, Chapter 3 concisely covers the basics necessary to study Microelectronics. (Students who have had a devices course will also find this a handy refresher.)

Cover Design: Dan Niver

Cover Photograph: PMC-Sierra. NASDAQ:PMCS

OXFORD
UNIVERSITY PRESS
www.oup.com/us/he

ISBN 978-0-19-532303-0