GOMACTech-2020

Chip Scan: 3D x-ray imaging of CMOS circuits

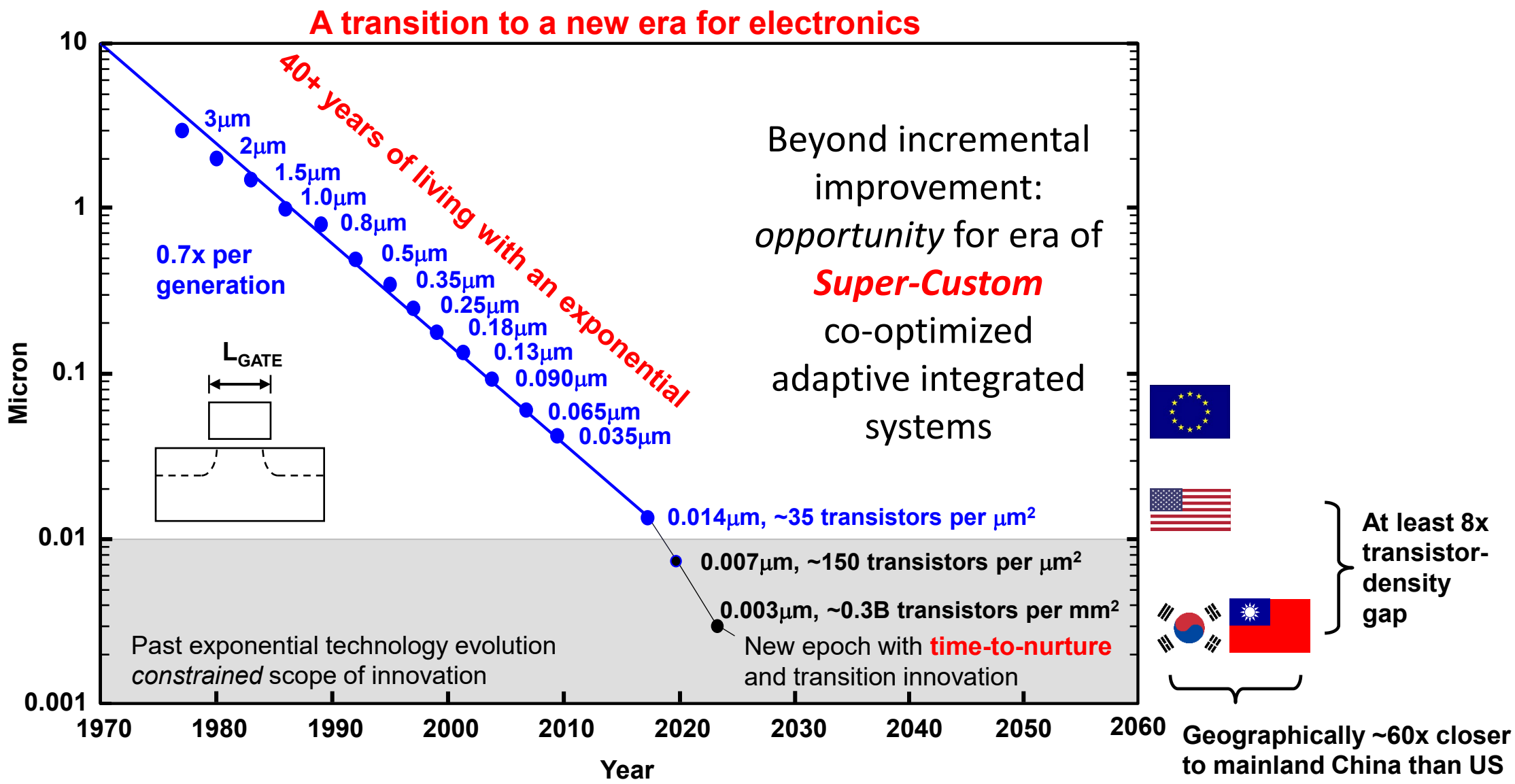
Session 29: Imaging (Paper No. 29.2)

Wednesday, March 18 2020, 3:30-5:10 PM

Tony Levi

University of Southern California

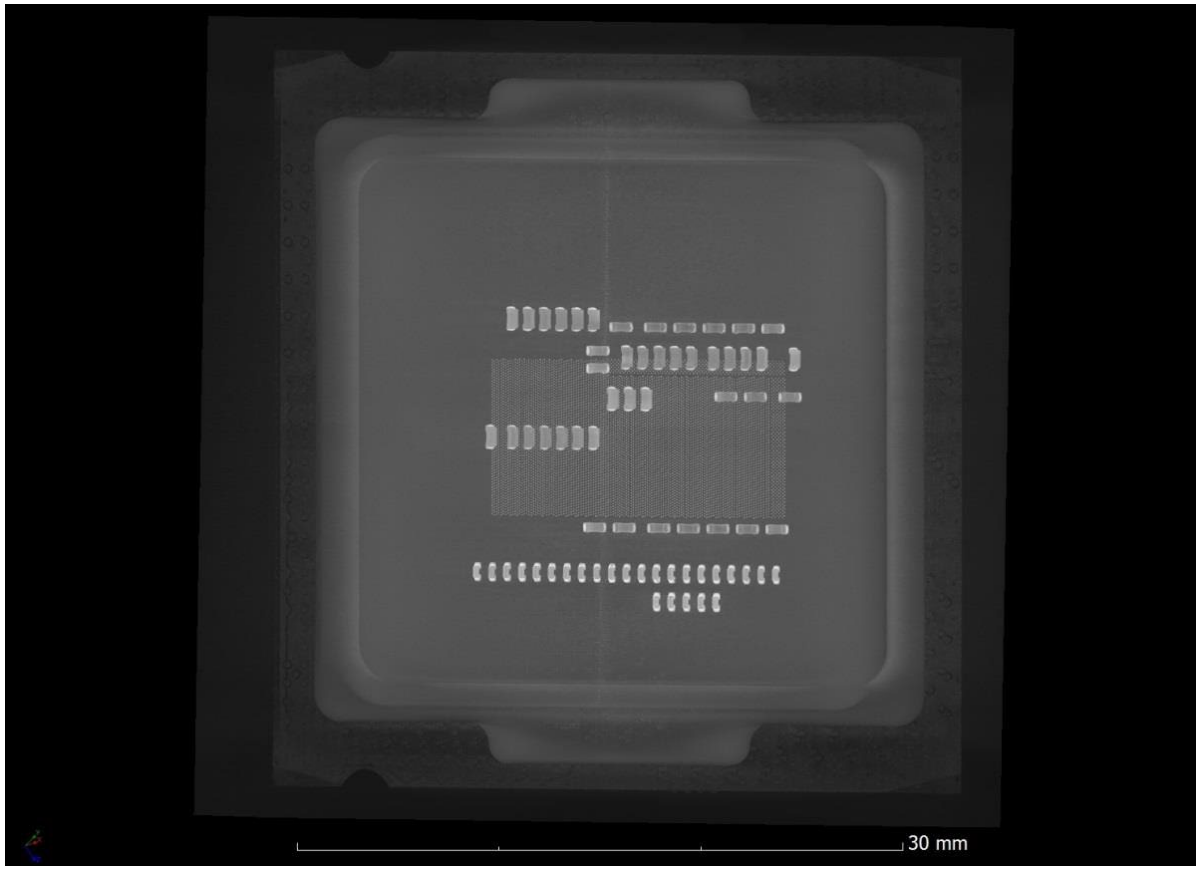
System challenges after transistor scaling flat-lines



Conventional package-level x-ray computed tomography 3D image reconstruction of Intel G3260 microprocessor

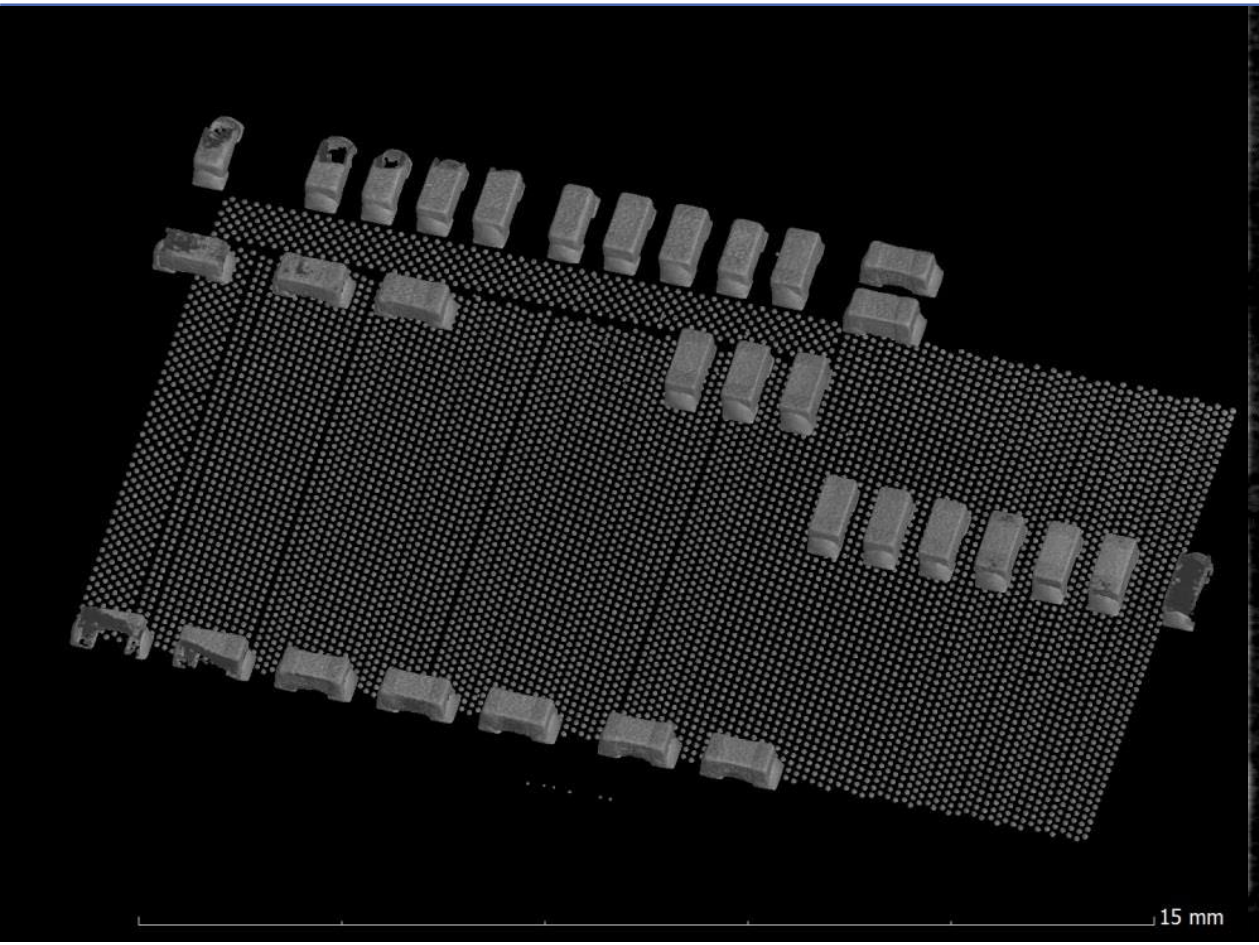
Can you trust what's inside … ?

How can you be sure it is:
Functional and trusted, has no kill-circuits, not counterfeit or maliciously defective?
Manufactured to within specifications at a known foundry?



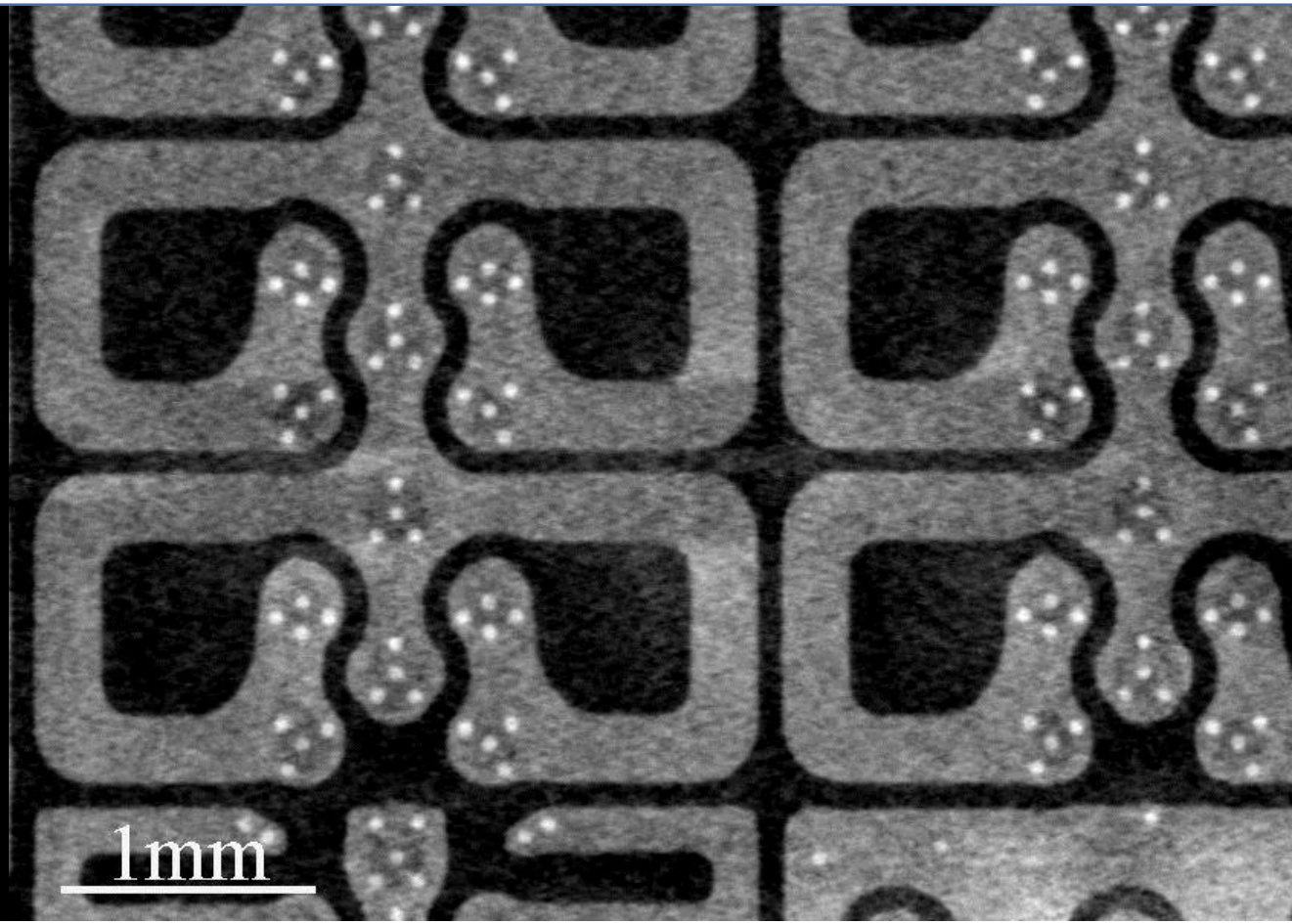
3D volume rendering (18 μm^3 voxels) of flip-chip area, Intel G3260 microprocessor ID 0402
2016 PSI report

Conventional package-level x-ray computed tomography 3D image reconstruction of Intel G3260 processor



15 mm

3D volume rendering (6 μm^3 voxels) of Intel G3260 processor flip-chip area



2D slice image (6 μm^2 pixels) of processor showing in-package copper layers

The “Chip Scan” challenge: efficient 3D x-ray imaging of CMOS circuits *at nm scale* (~1/1000 smaller than package-level)

A non-destructive 3D x-ray imaging project with USC, GF and PSI/ETH-Zurich using information-driven 3D tomographic reconstruction that could be used to enable *certified TRUST* that integrated circuits are manufactured defect-free, at a known foundry, and to customer design.

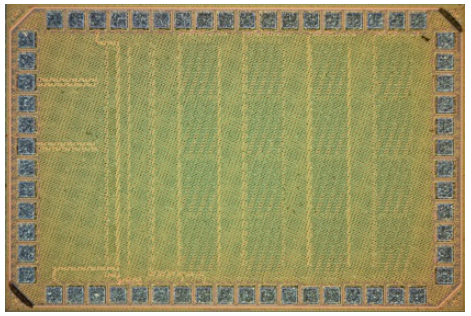
Current state-of-art is large-area laminographic 3D x-ray chip scan with zoom capability.

Contributors: Mirko Holler, Michal Odstrcil, Manuel Guizar-Sicairos, Maxime Lebugle, Elisabeth Müller, Simone Finizio, Gemma Tinti, Oliver Bunk, Jörg Raabe, Joshua Zusman, Walter Unglaub, A. F. J. Levi, Gabriel Aeppli

Publication: Holler et al., *Nature Electronics* **2** 464 (2019)

Chip Scan: 3D x-ray imaging of CMOS circuits at nm-scale

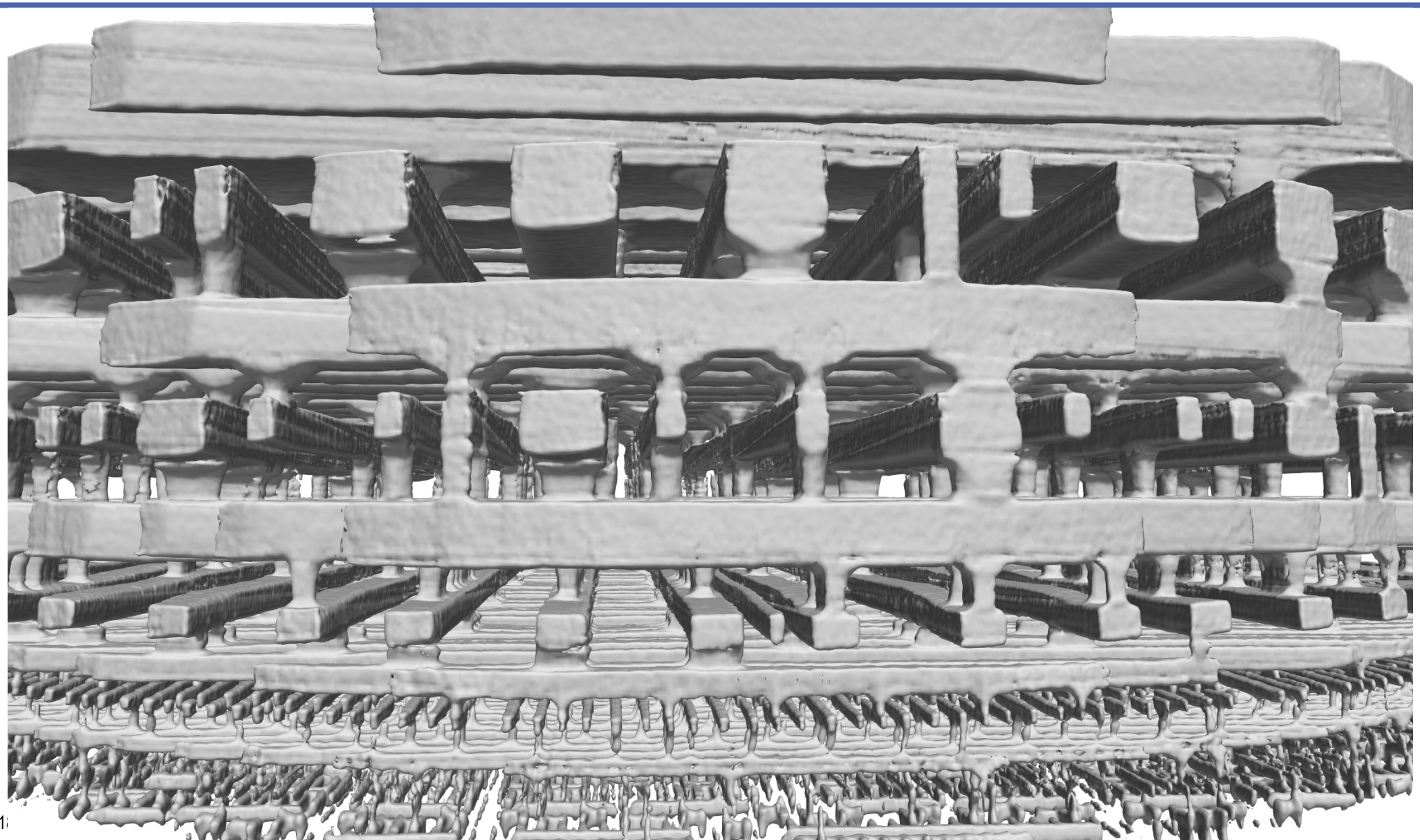
- **Objective is to rapidly find out if you can trust "*what's inside*"**
- **How can you be sure it is:**
  - Functional and trusted, has no kill-circuits, not counterfeit or maliciously defective?
  - Manufactured to within specifications at a known foundry?



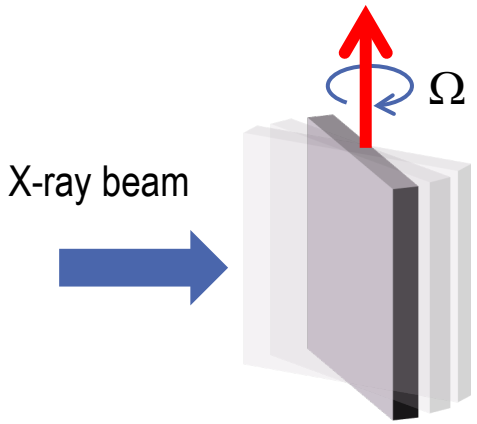
USC-designed digitizing matrix-multiplier chip for ML manufactured by Global Foundries in 2017 in 14nm FinFET CMOS technology

- **Non-destructive** lensless coherent x-ray diffraction 3D-imaging of CMOS integrated circuits with nanometer resolution:
  - **Big data**: >PB/cm^2, **Complexity**: many transistors and interconnects at high resolution, >1B/cm^2, **Algorithms**: regularized inverse problem with ML to optimize data acquisition
  - Establishes *feasibility* of future physical chip-to-schematic and design of manufacturing masks in a few days
- **Comment** (AFJL opinion in 2016): *If* the technology proves-in as anticipated then new era of "opensource hardware" is inevitable
  - Nowhere to hide static hardware IP, ***even*** with **contemporary obfuscation, hardware access keys, protected memory, etc., of working chips**

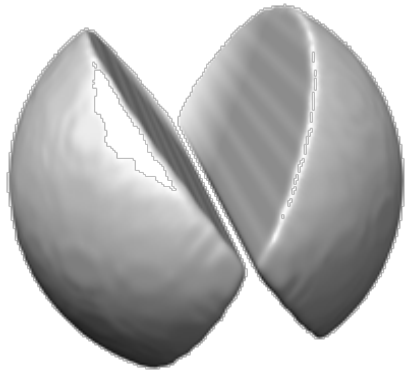
Chip Scan: 3D x-ray image of Intel Pentium G3260 processor manufactured in 22 nm FinFET technology



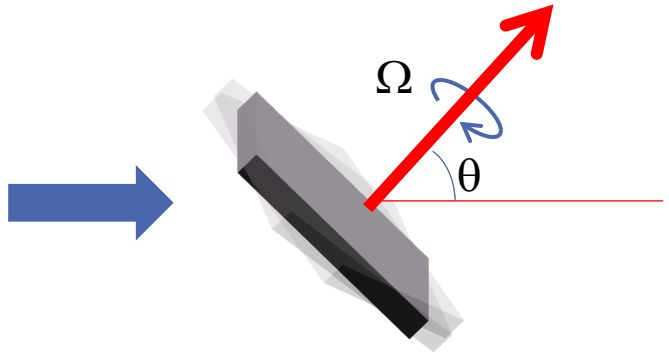
Sample geometry for large-area chip scan: The challenge of missing information with limited-angle x-ray tomography and laminography



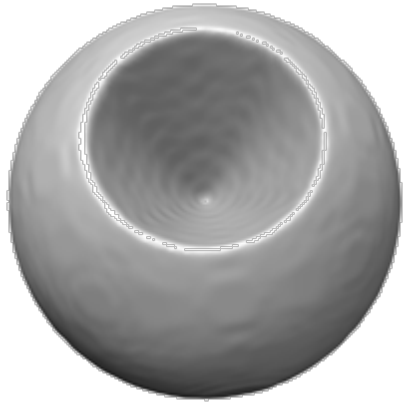
Limited-angle tomography at normal incidence (θ=90°) and limited rotation W about chip-plane



Missing *wedge* in 3D diffraction data



Laminography at angle θ and rotation Ω about chip-normal



Missing *cone* in 3D diffraction data

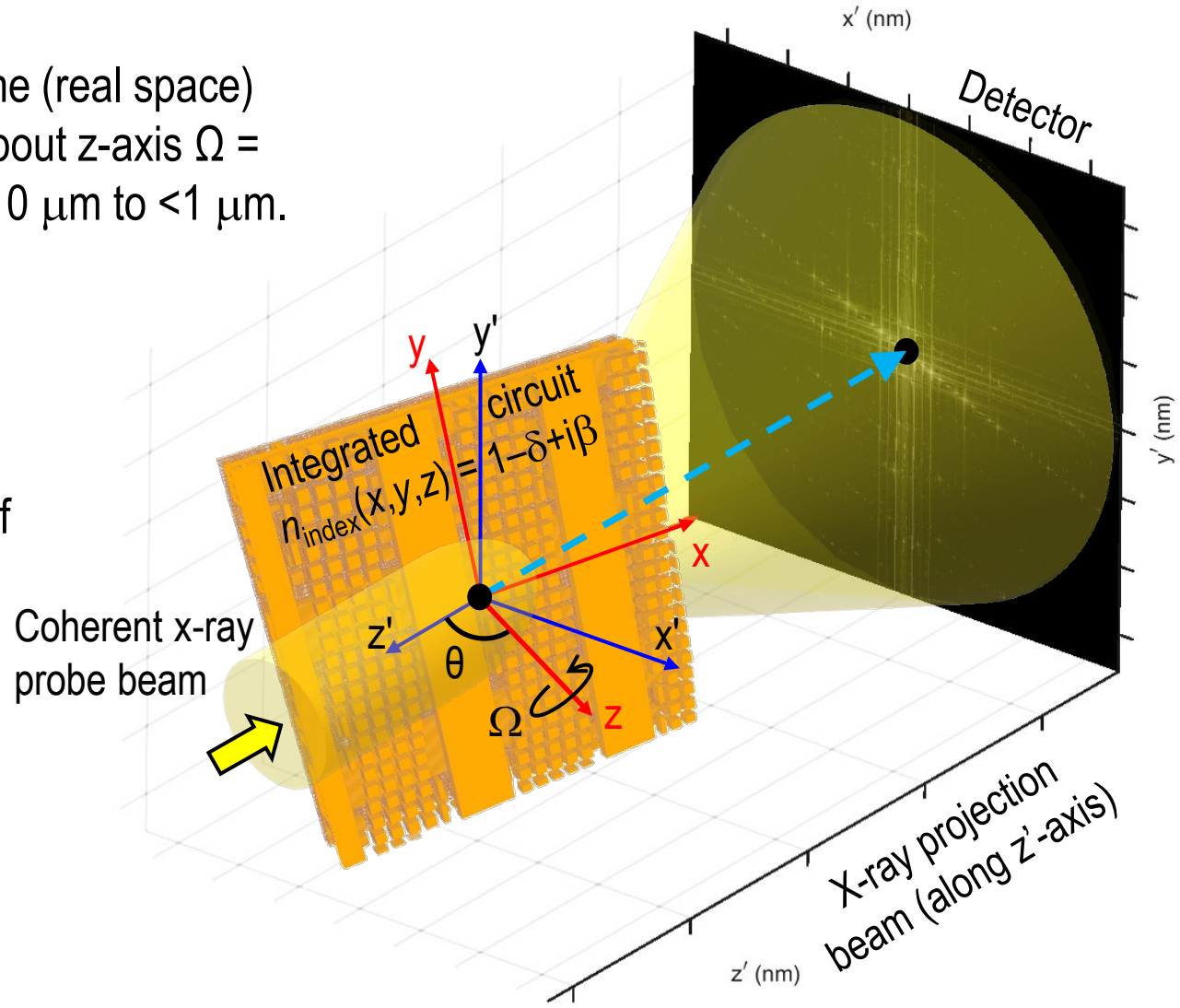
- Tomography at normal incidence suffers from reconstruction artifacts due to the missing wedge of diffraction data (missing information)
- The laminography geometry is suitable for flat samples such as ICs and the missing cone is less data lossy than the missing wedge of diffraction data in standard tomography

Sample geometry for large-area chip scan

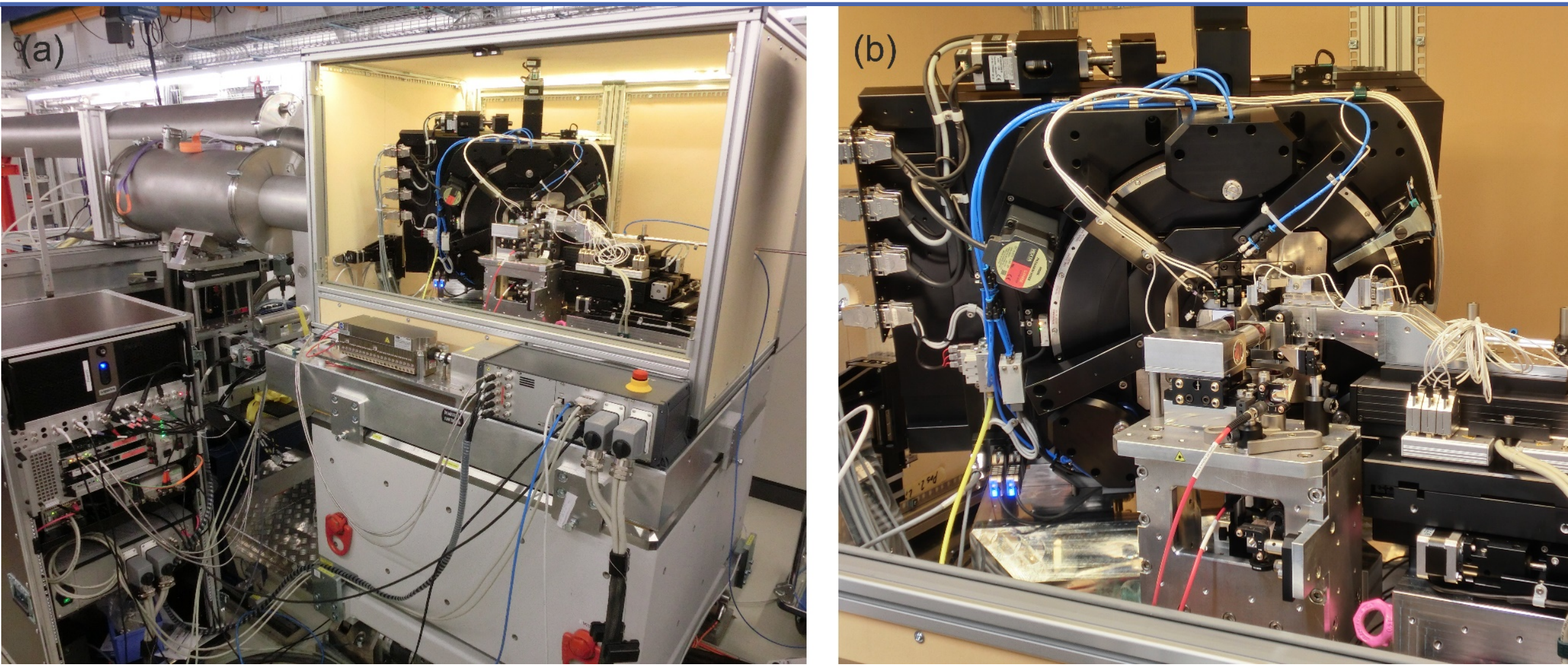
Laminography geometry: probe-beam reference frame (real space) (Tilt angle from chip-plane normal θ = 61°, rotation about z-axis Ω = 0°:1°:359°). Probe-beam diameter selectable from >10 μm to <1 μm. Integrated circuit is ~7.3 m from detector plane.

The 2D Fourier transform $P(k_u,k_v)$ of a projection through the sample corresponds to a cross-section of the 3D Fourier transform $M(k_x,k_y,k_z) = FT\{n_{index}(x,y,z)\}$.

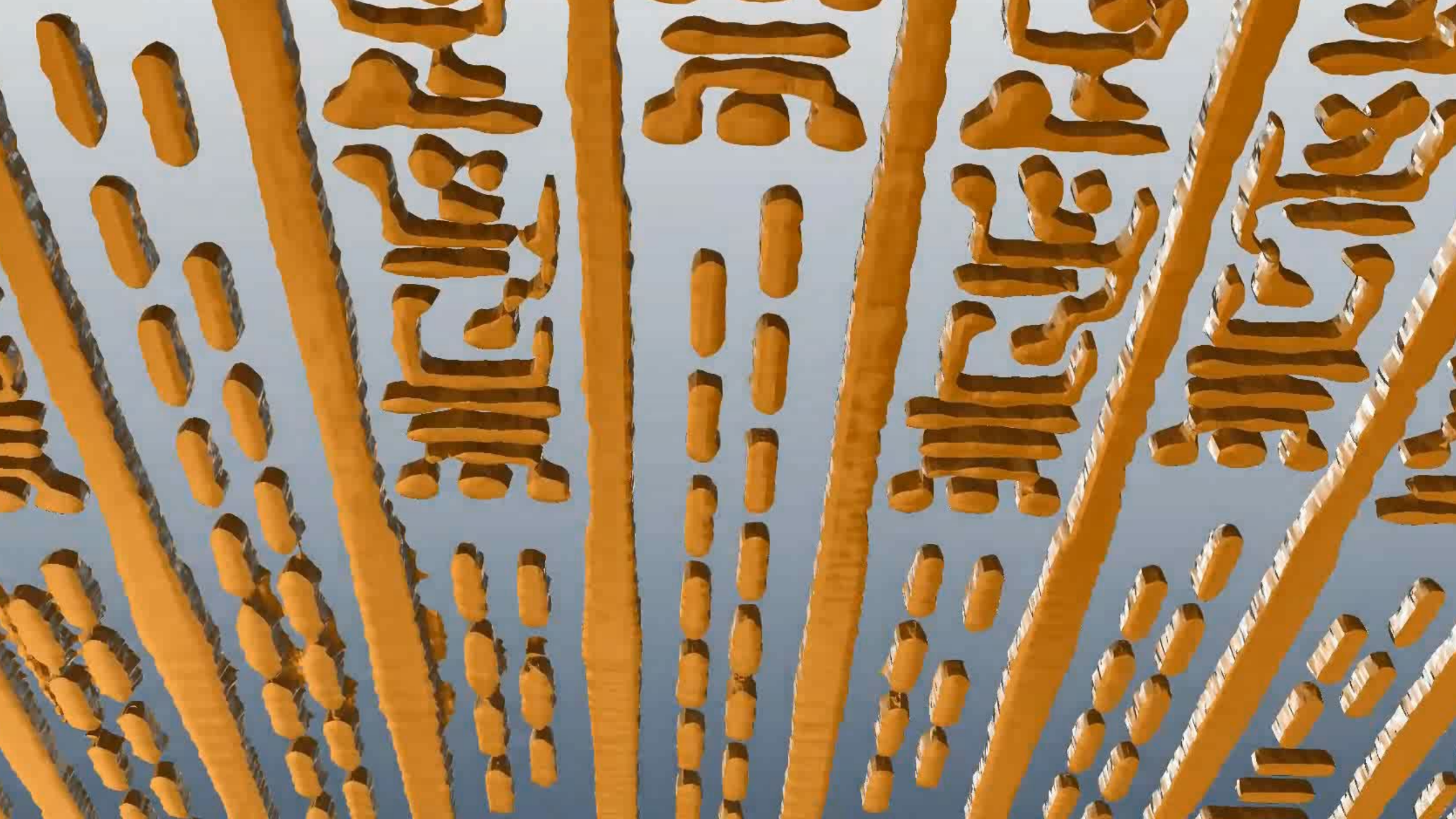
The vectors k_u and k_v span a Cartesian coordinate system on this plane.



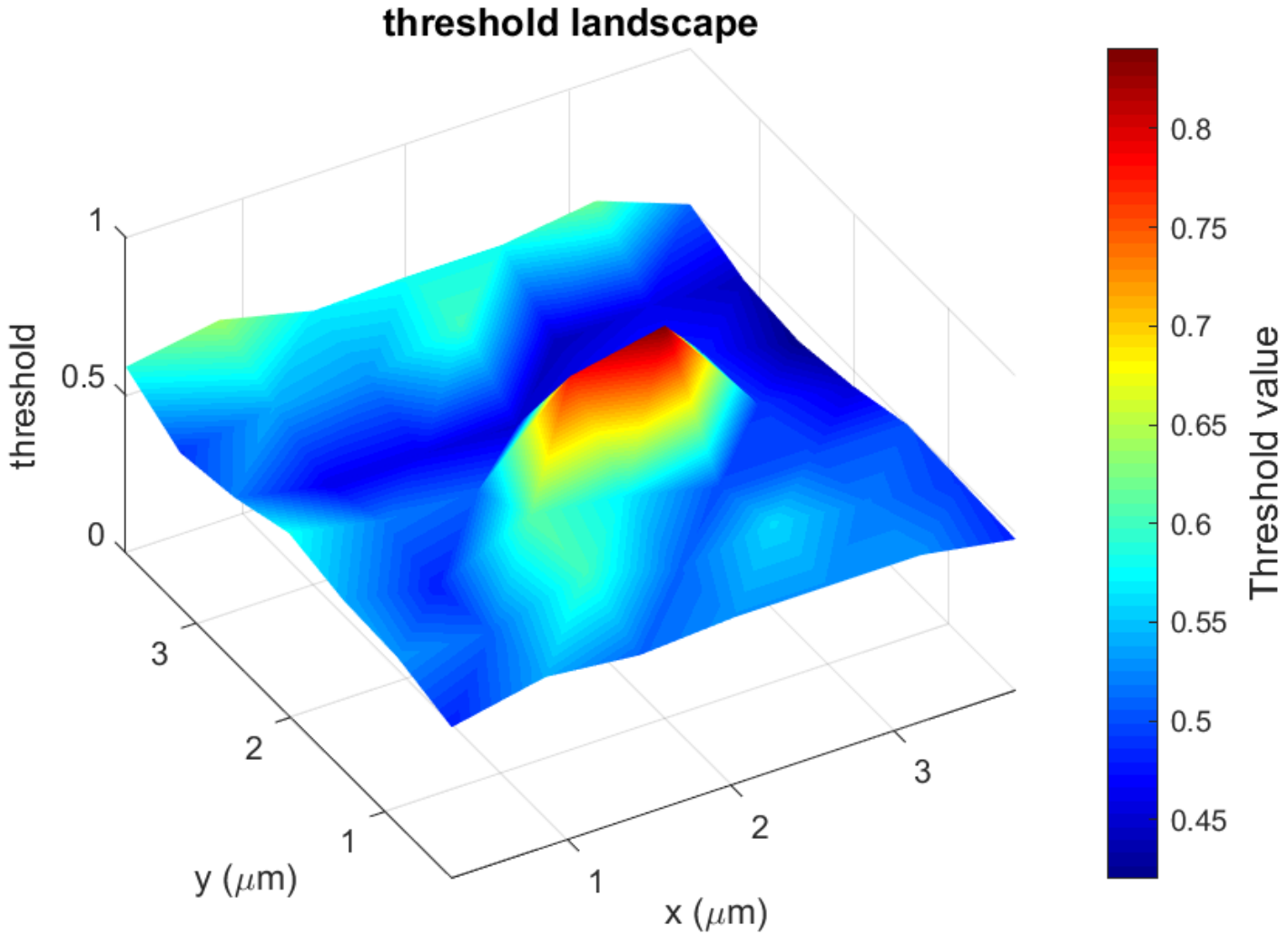
3D x-ray chip-scan microscope (2018 beta-version, now at ANL)

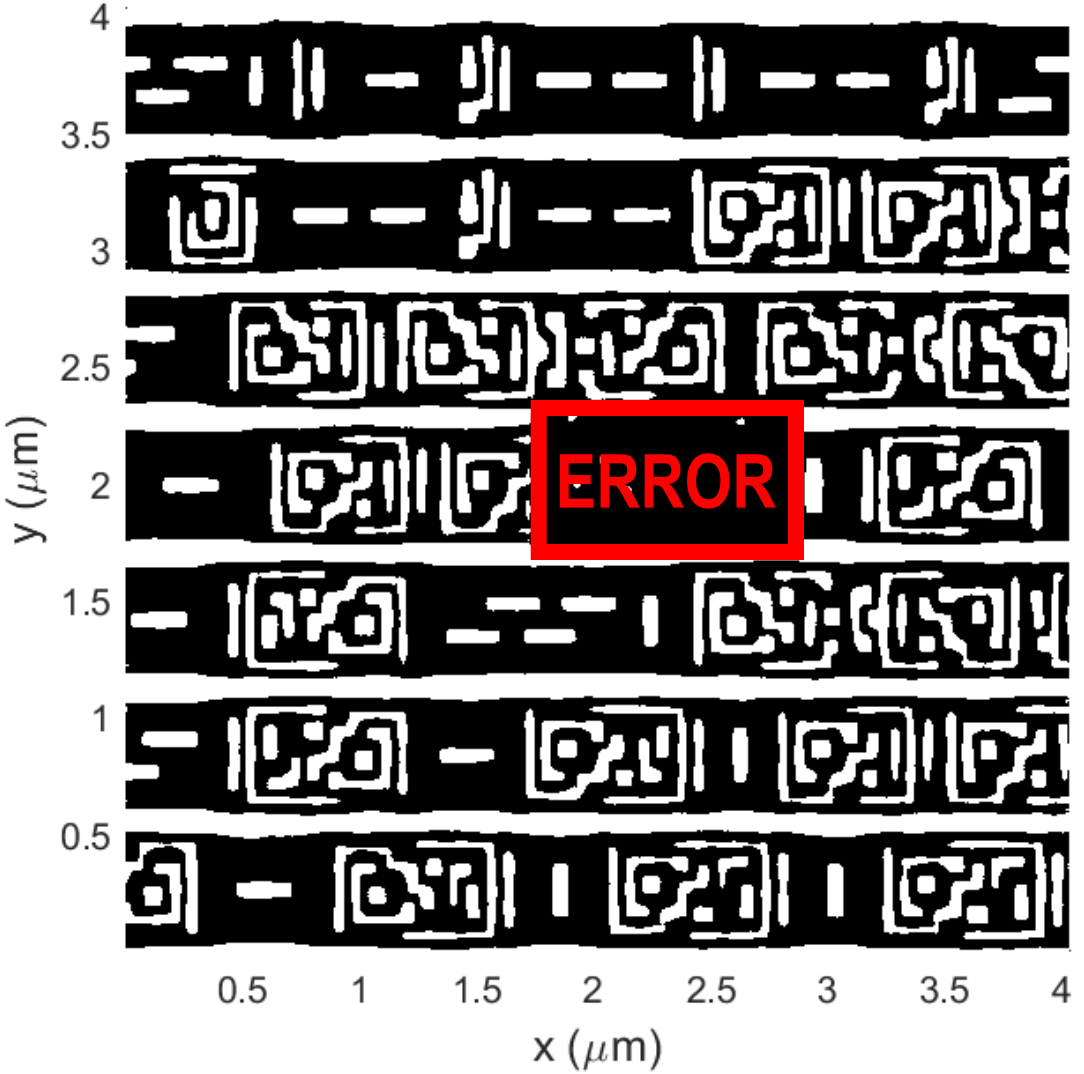


Laminography microscope at SLS cSAXS beamline with enclosure doors removed. (a) Overview with flight tube and control rack. (b) Stage detail



Machine-detection of error in M1 manufacture versus design





The challenge of reducing scan-time and increasing resolution

Reported scan-time and resolution is limited by beam-flux:
Example: 40 μm diameter 3800x3800x600=8.7x10^9 voxels (13 nm)^3 with resolution <19 nm in **60 hours**

Increasing flux:
100x increase in brilliance with 4th generation synchrotron source
10x increase in spectral bandwidth
10x increase in efficiency replacing Fresnel zone plate with Kirkpatrick-Baez mirror

For example: a 10^4 increase in flux enables 2 nm resolution for same volume and time, **or** 1 mm^2 chip area at 50 nm resolution in 30 hours

Further significant reduction in scan-time and/or increase in resolution using:
Next-generation microscope and new geometry
Use of prior or machine-learned information and new algorithms

summary

Chip-scan of large-area (> 1 cm^2) integrated CMOS electronics circuits using coherent x-ray laminography microscope with zoom for 3D reconstruction, virtual delayering, and metrology

Additional summary information: Holler et al., *Nature Electronics* **2** 464 (2019)

Next-generation chip-scan in a day
Zoom to deep sub-10nm resolution
A path to certified *TRUST* that integrated circuits are manufactured defect-free and to customer design.

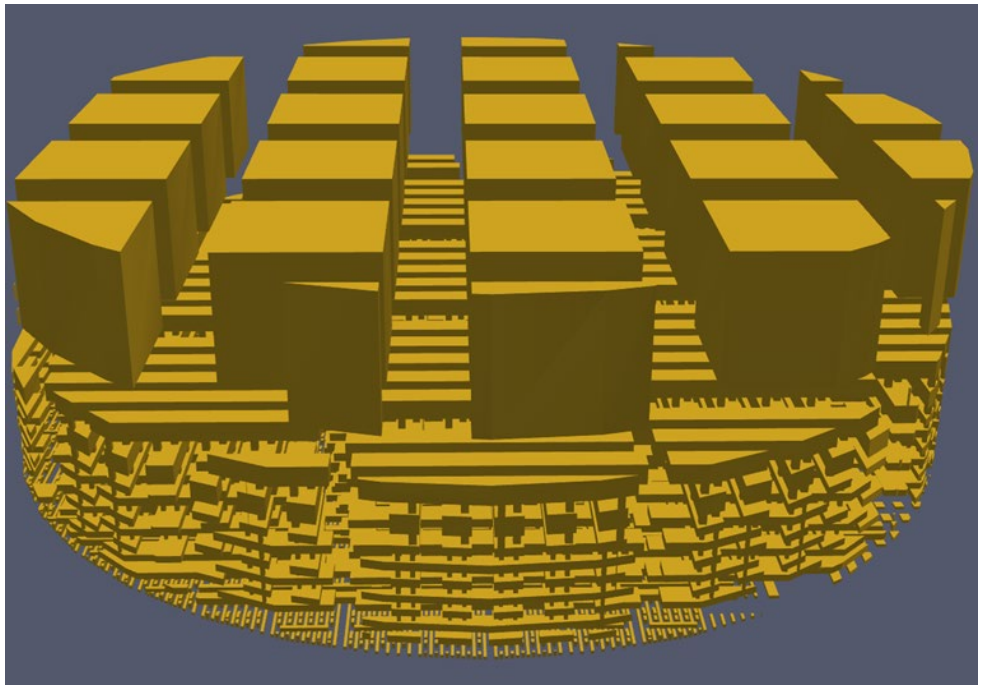
Chip Scan: 3D x-ray imaging of CMOS circuits

Enables *certified*

TRUST

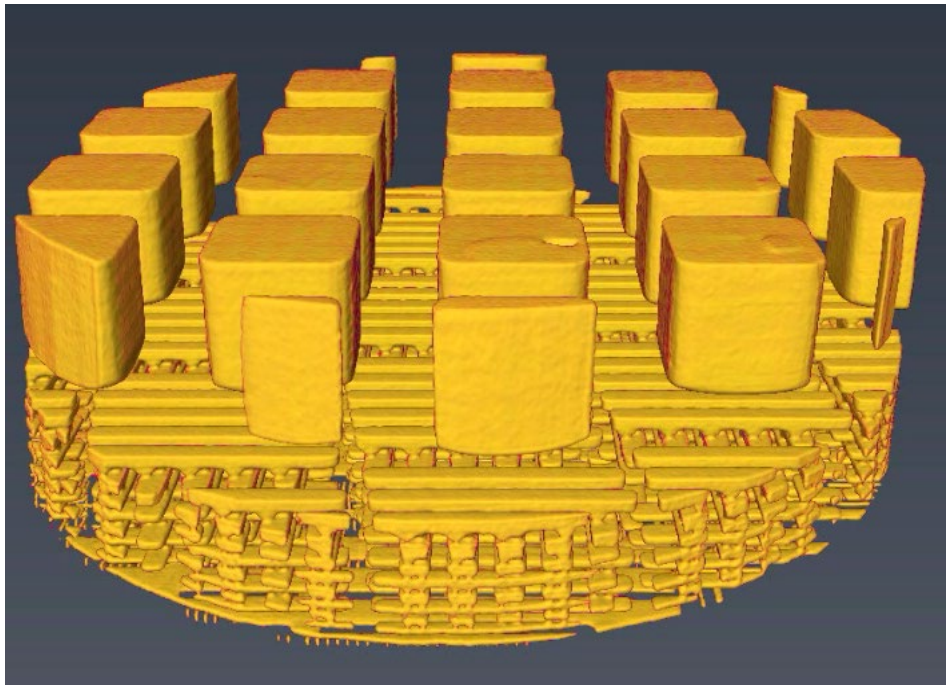
that integrated circuits are manufactured defect-free and to customer design

GF CMOS Design



3D nano-scale CMOS ***design***

GF CMOS Measured x-ray image (2016)



3D nano-scale CMOS ***manufacture***

END

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