Unleash Innovation

TSMC Packaging Technologies for Chiplets and 3D

Dr. Douglas Yu

R&D Vice President
TSMC Distinguished Fellow

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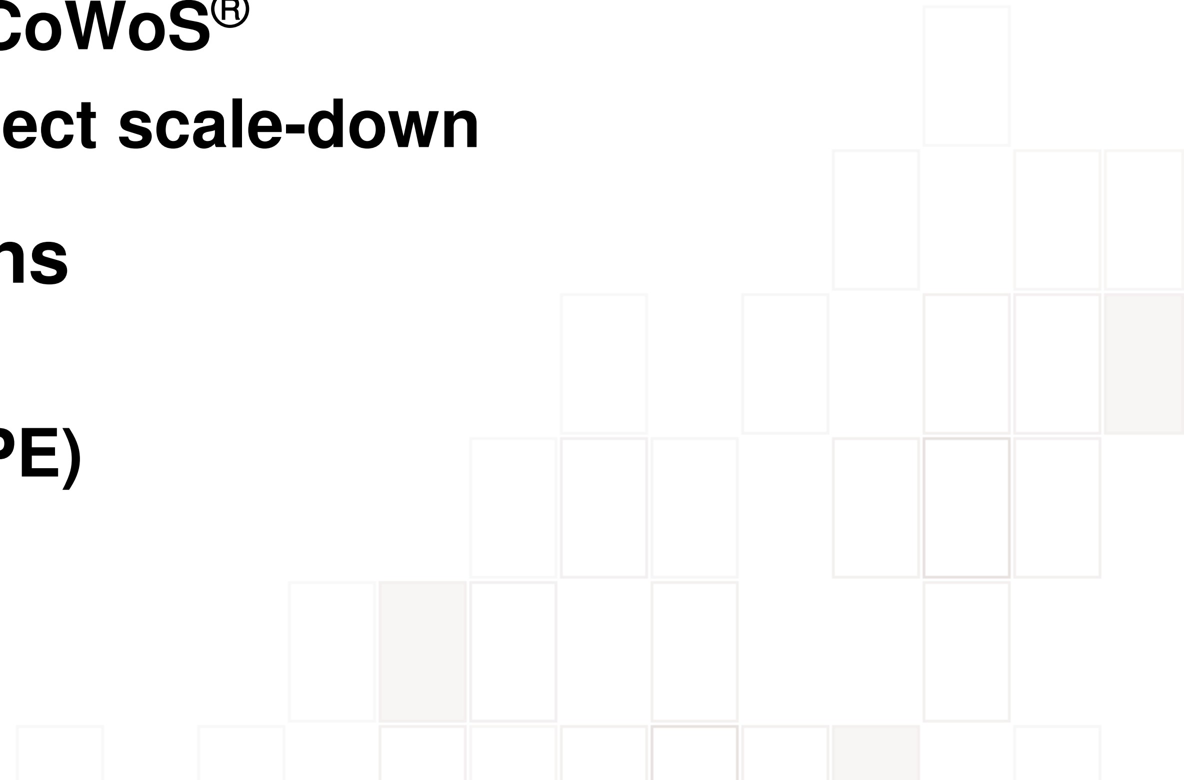
Outline

- Introduction
  - Industry Transition
- TSMC Packaging Technologies
  - 3DFabric™- SoIC™, InFO and CoWoS®
  - System scale-up and Interconnect scale-down
- New Heterogeneous Integrations
  - Advanced Thermal Solutions
  - Si Photonics Integration (COUPE)
- Summary



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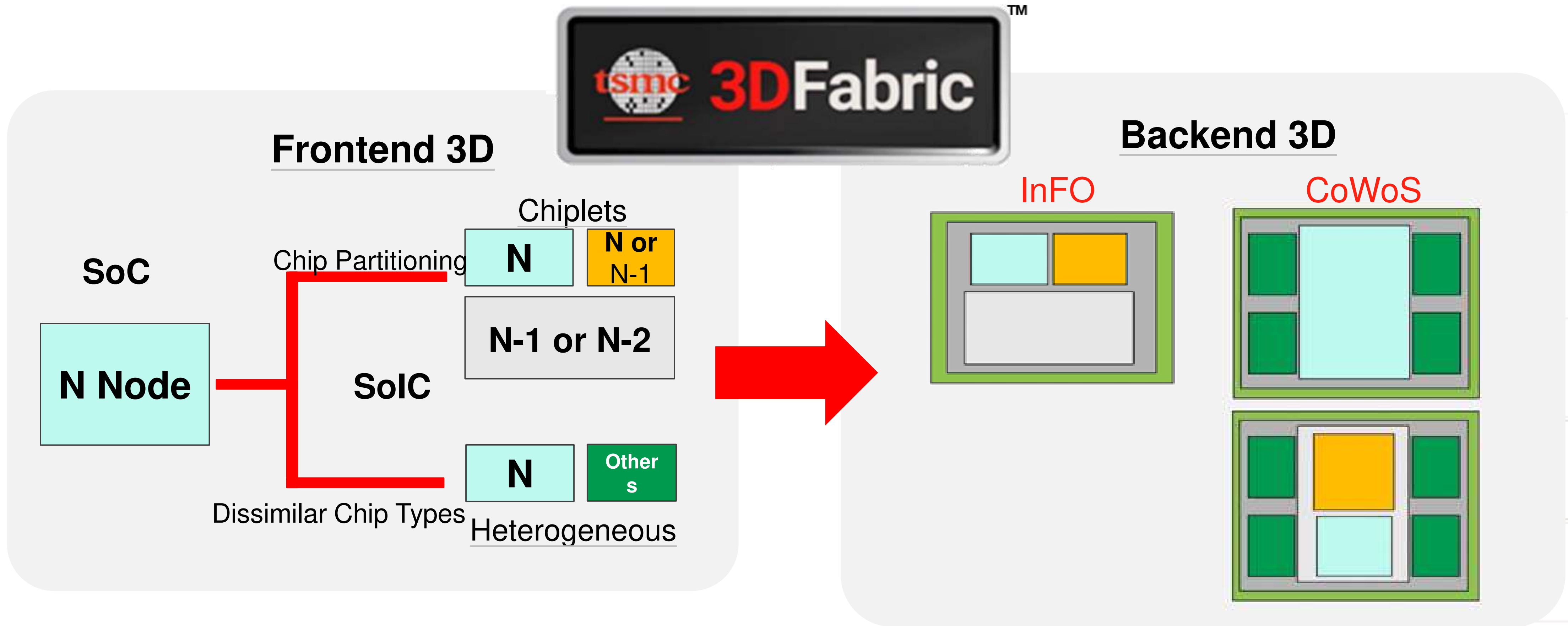
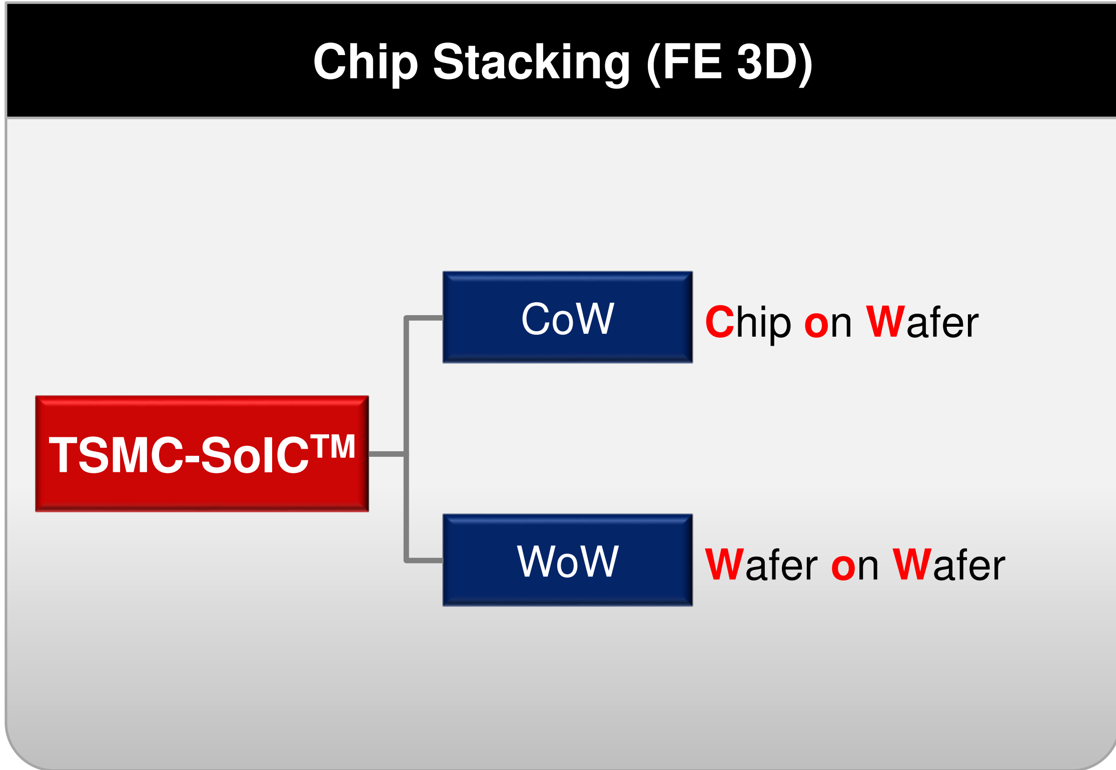
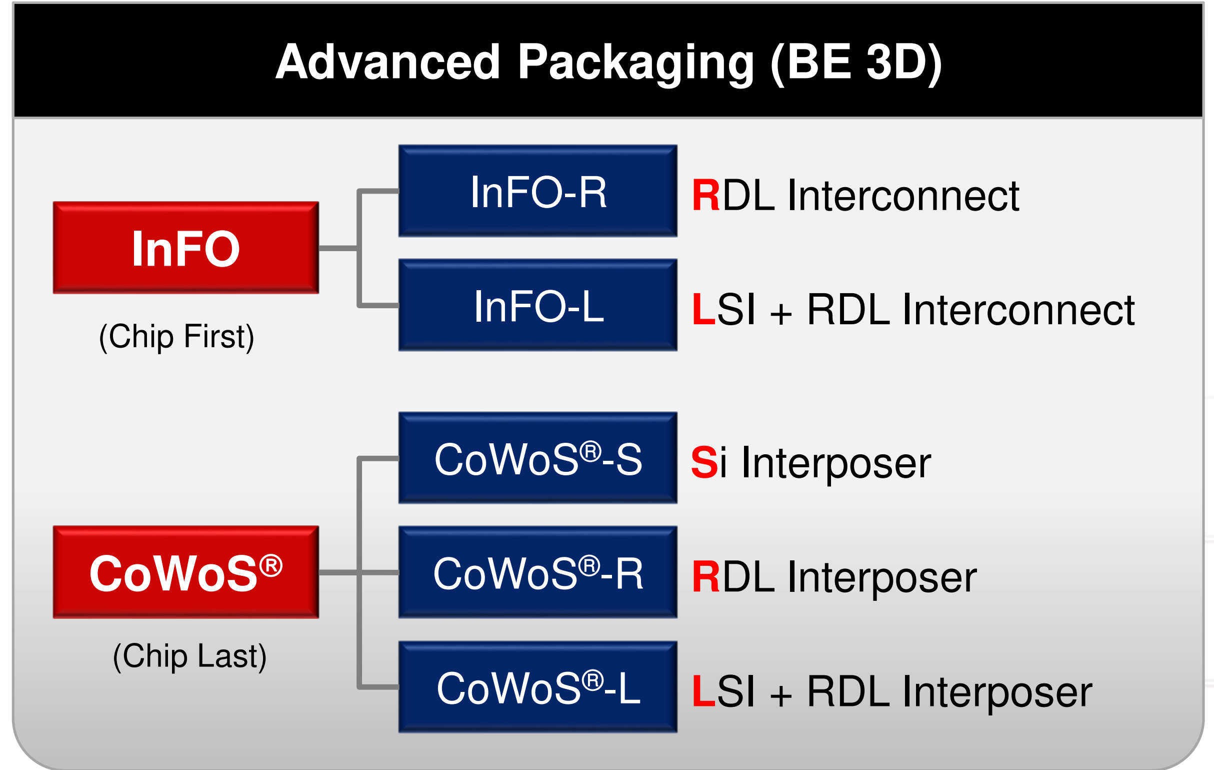
TSMC Integration Technologies

- Cost, Performance, Power, Form Factor
- Time to Market, Flexibility and Scalability



TSMC 3DFabric™





SoIC: System on Integrated Chips

InFO: Integrated Fan-Out
CoWoS: Chip on Wafer on Substrate
RDL: Redistribution Layer
LSI: Local Si Interconnect

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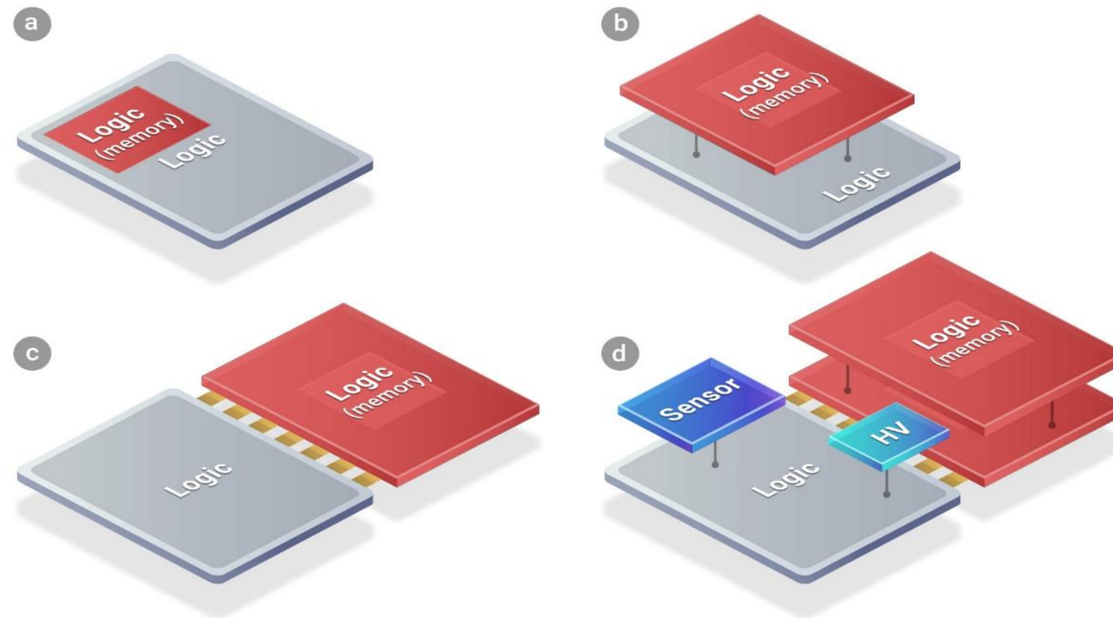
New Transition

- **Advanced foundry packaging technologies for chiplets and 3D can start a new era-**
- **Transition from CMOS to CSYS (Complementary Systems, SOCs and Chiplets integration) for More Moore's and More-than-Moore systems**



Ref: TSMC 3D Fabric

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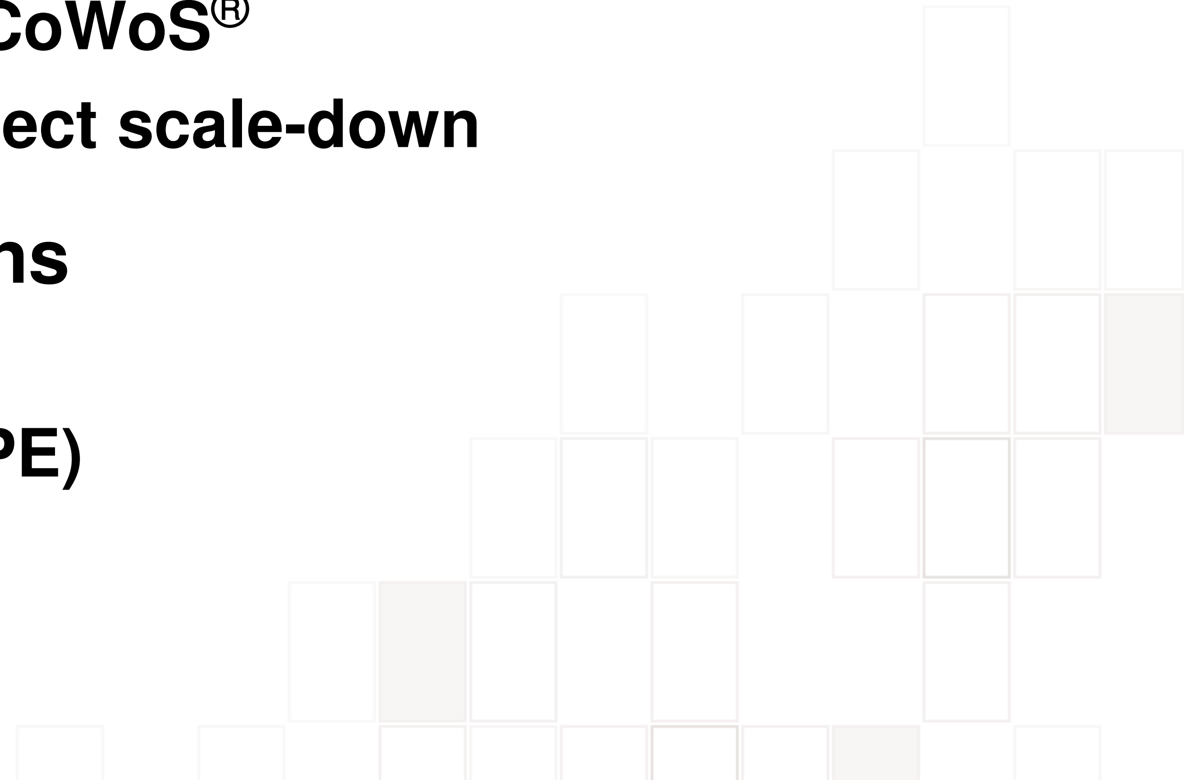

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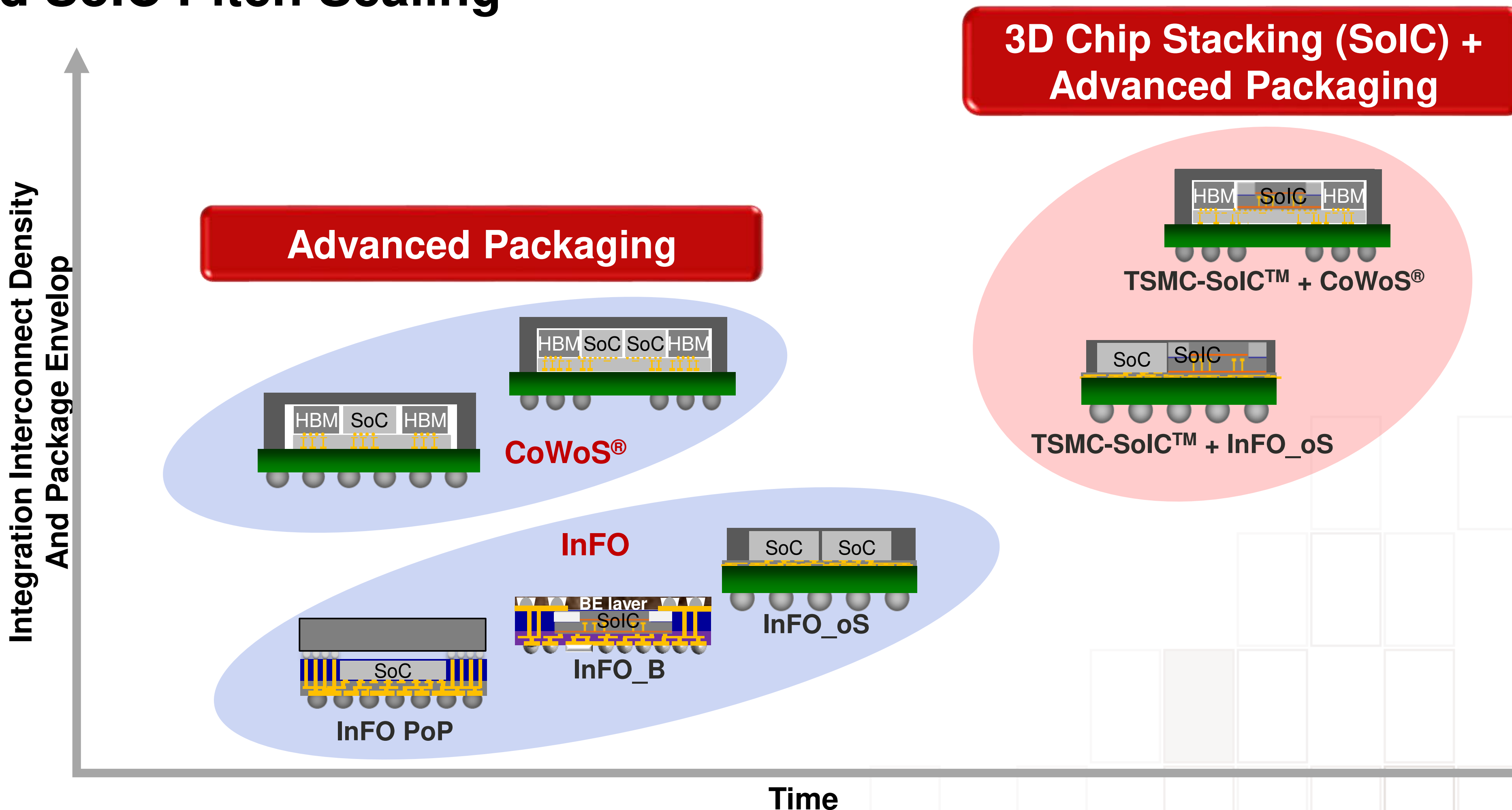
Integration Technologies

- 3DFabrics updates- additional structures, Packaging Envelop Increase and SoIC Pitch Scaling



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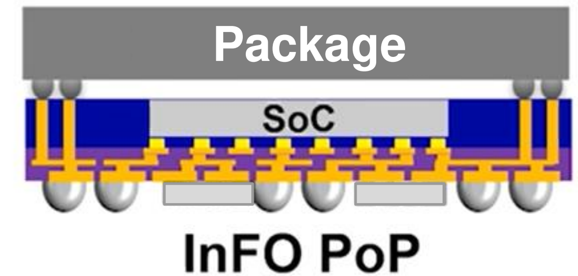
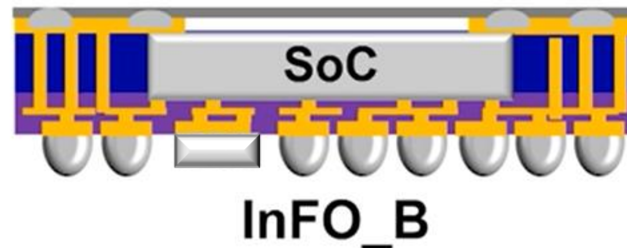
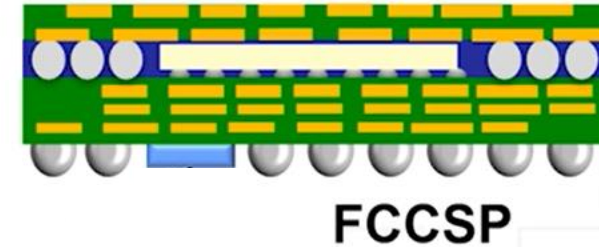
InFO_B (Bottom Only) for Mobile AP

- Leverages high-volume InFO PoP experience
- Enables LPDDR DRAM package stacking at CM (Contract Manufacturers)
- Enhances performance with InFO's lower parasitic (ACR/ACL) and TSMC's deep trench capacitor (DTC) technology







Attributes	Package Size 14x14mm	
CPU voltage droop reduction	1.06X	1X
Max. chip size, mm²	135	115
CPI sensitivity	Low	High
TIV/TMV pitch, µm	180	~270
Si thickness, µm	Up to 200	90

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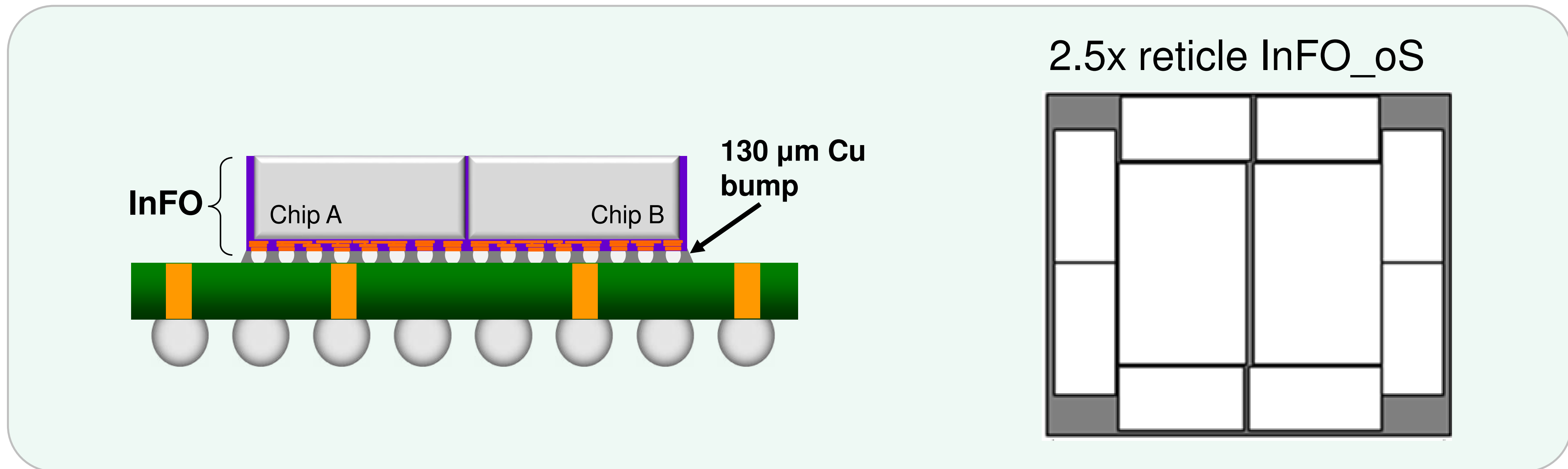
InFO-R/oS Update for HPC Chiplet Integration

- Offers Min. 2/2 μm 5x RDL layers with 130μm pitch Cu bump.
- 1.5x reticle InFO_oS in mass production since 2018, flexible floor plan
- Chiplet scheme 2 + 8, 2.5x Reticle (51x42mm), substrate 110mmSQ in '21



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InFO_oS Envelope Growth for HPC Applications

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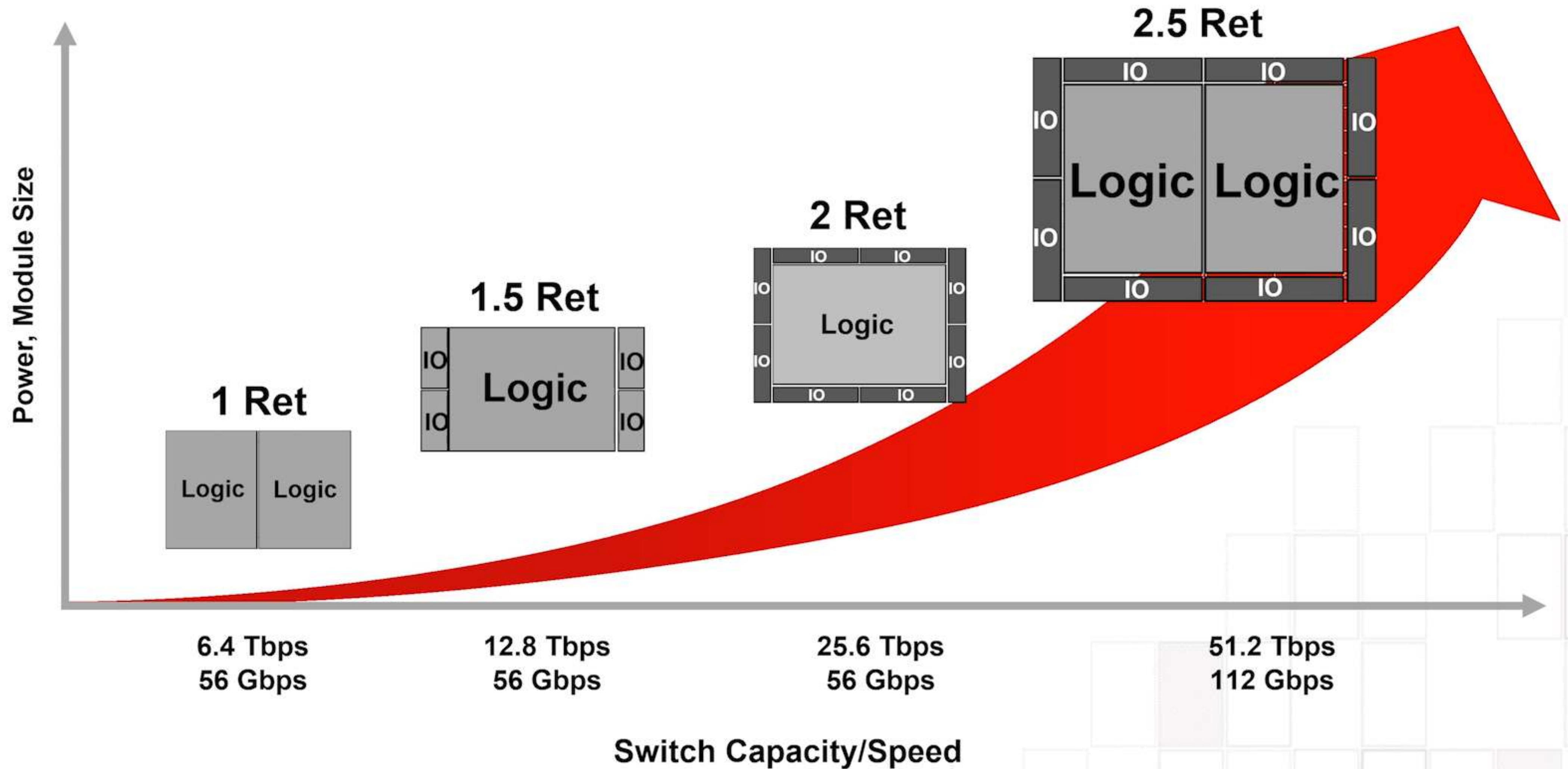

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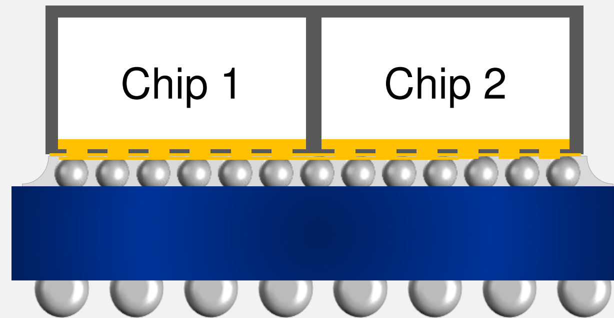
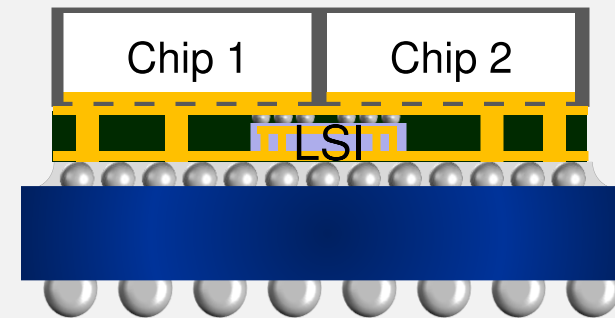
InFO-L/LSI for UH-Bandwidth Chiplet Integration

- **Integrating SoC chips with high-density Local Si Interconnect (LSI) and InFO technology**

	InFO_oS	InFO_LSI
		
I/O Pad pitch (μm)	40μm	25μm
RDL L/S (μm)	2/2 (3RDL)	0.4/0.4 (4Mz)
C4 Bump Pitch (μm)	130μm	90μm
InFO Size, Reticles	2X	1X

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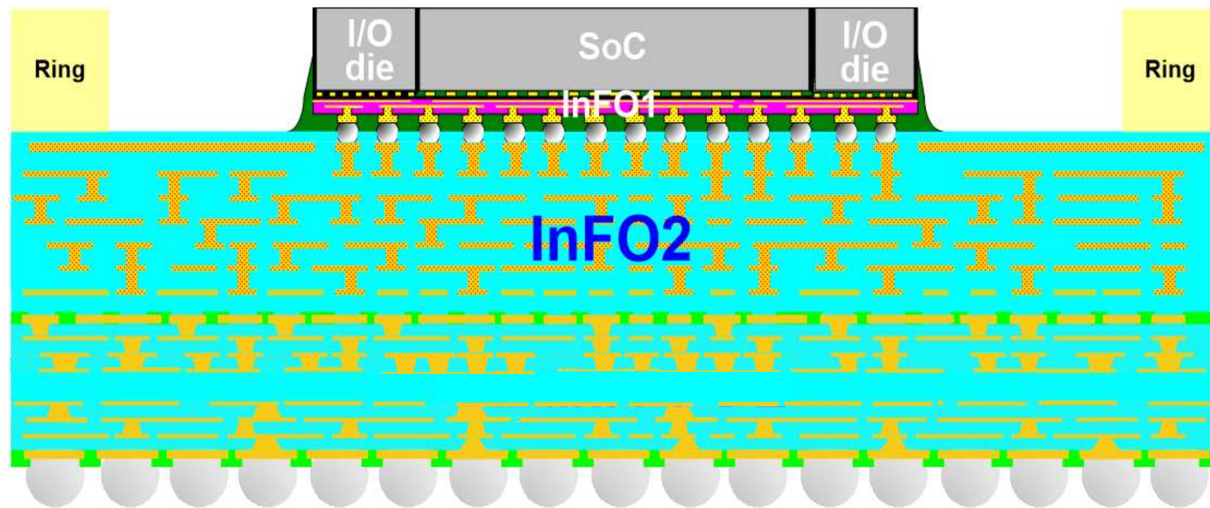
InFO for Ultra High Performance Compute Systems

- InFO_SoIS (System-on-Integrate Substrate)



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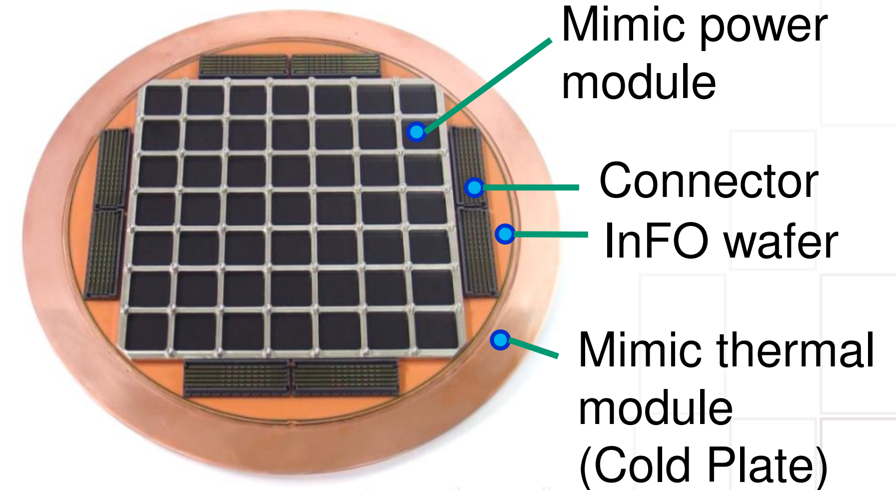
- InFO_SoW (System-on-Wafer)



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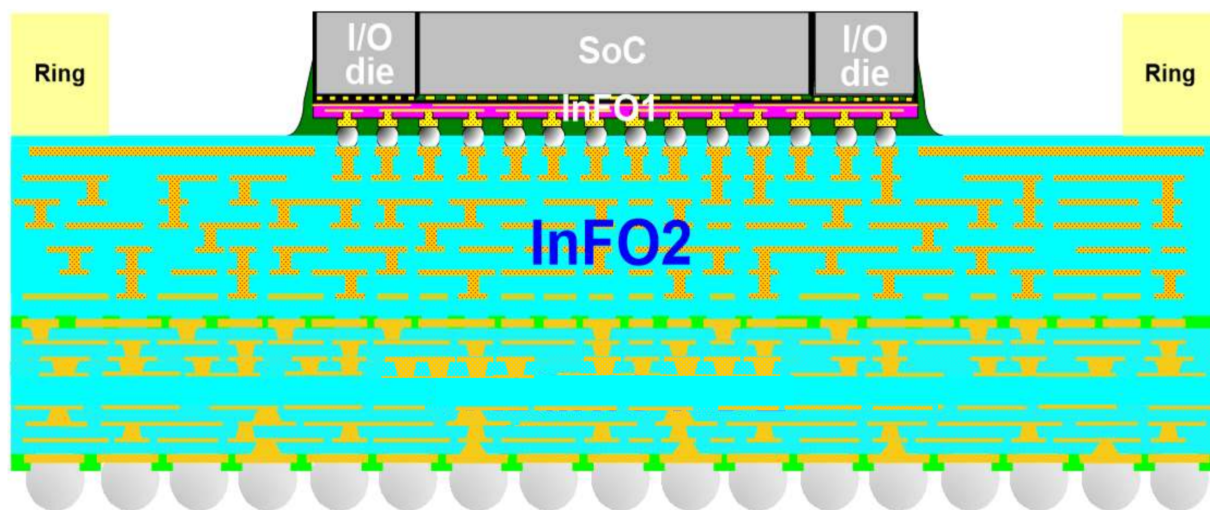
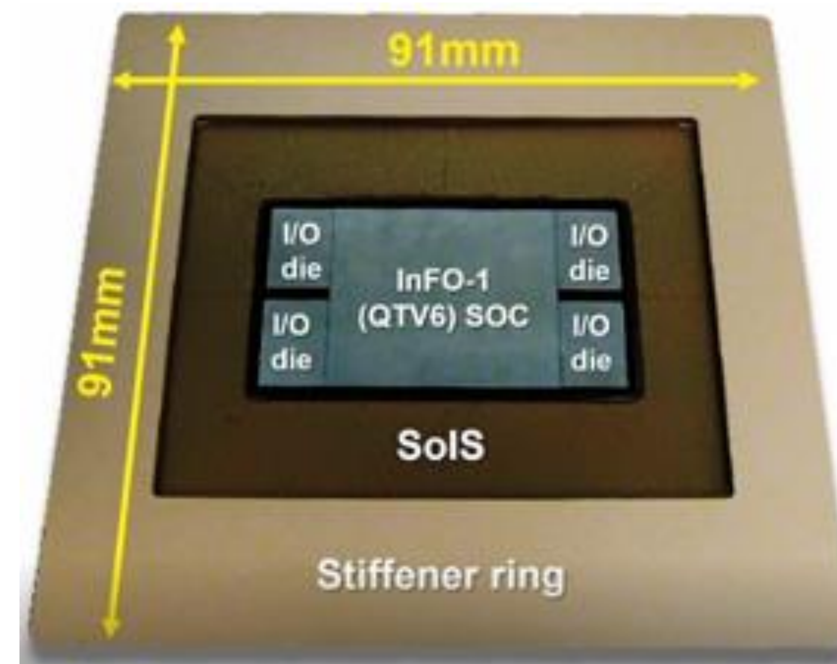
SoIS (System on Integrated Substrate)

- Leverage InFO to build organic substrate for FC/InFO/CoWoS stacking with KGDs- chip, passives, components, PKGs and supporting substrate
- Achieve high yield- > 95% (91mmSQ), 100% yield 110mmSQ





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SoIS Interconnect Performance

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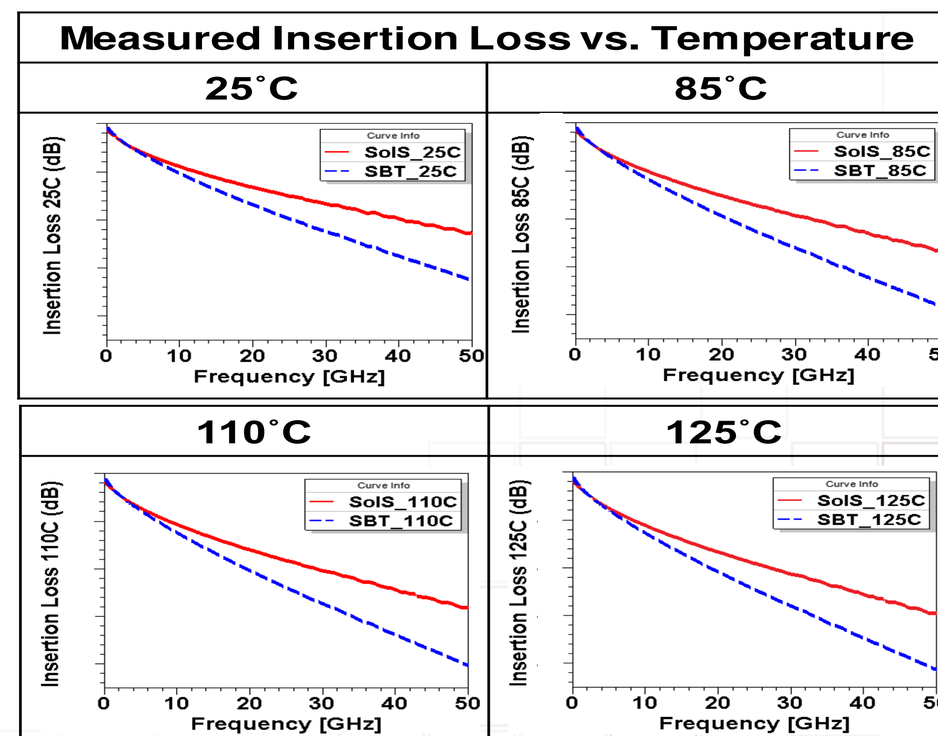
- SoIS exhibits ~25% and ~30% lower insertion loss than organic substrate over 25˚C to 125˚C at 28GHz and 50GHz, respectively.
- The varied temperature conditions (over 25˚C to 125˚C) will not impact the measured insertion loss.

Insertion Loss vs Temperature		Diff Impedance= 90Ω			
		25˚C	85˚C	110˚C	125˚C
Insertion Loss @ **28 GHz**	**SoIS**	~ 0.75x	~ 0.75x	~ 0.75x	~ 0.76x
	SBT (GL102)	1.0x	1.0x	1.0x	1.0x
Insertion Loss @ **50 GHz**	**SoIS**	~ 0.7x	~ 0.7x	~ 0.7x	~ 0.71x
	SBT (GL102)	1.0x	1.0x	1.0x	1.0x



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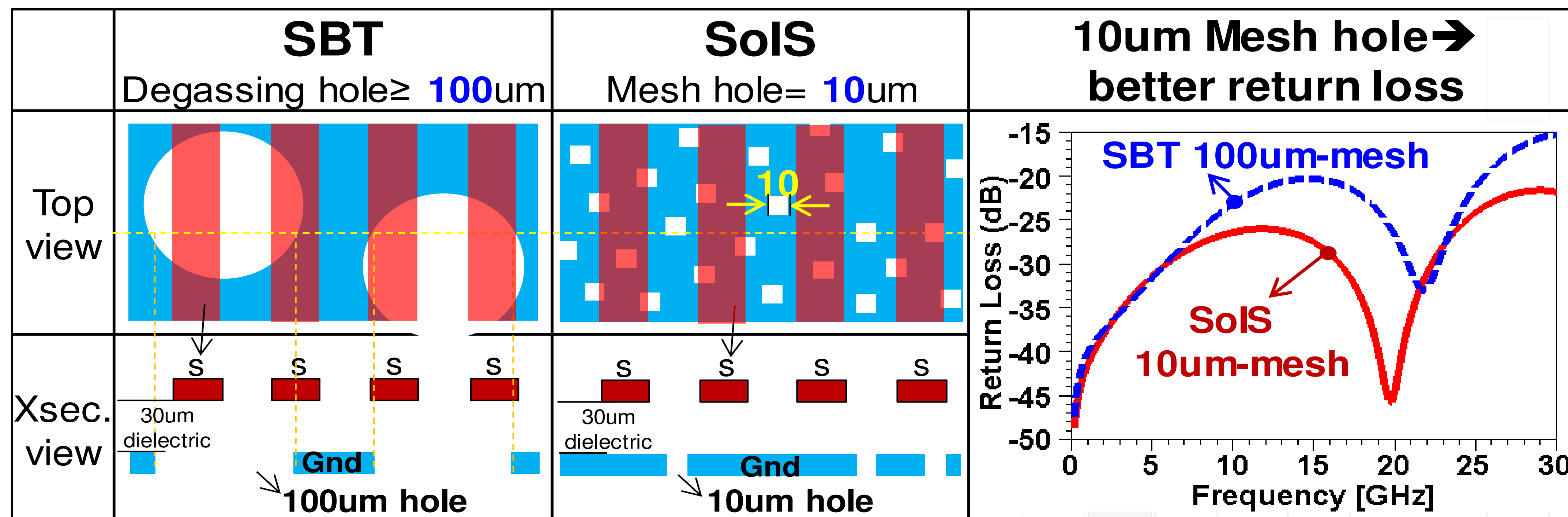
SoIS Design Rule & Power Performance

- High-density rouitng capability with finer line pitch (< 10um pitch) & via (25um CD) to gain more SerDes pairs and mitigate signal crosstalk.
- Samll mesh hole (10*10um) on P/G planes showed significantly better return loss (< - 45dB).



SoIS Reliability Evaluation

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- A 91mmSQ mechanical TV adopted to evaluate SoIS reliability
- Passed package-level reliability tests and microstructure sanity check after the reliability tests showing robustness.

Reliability	Test item	Result
Quick torture	MR6x (reflow 250°C)	Pass
CLR	MSL4a+TCG3000 (-40~125°C)	Pass
	MSL4a+uHAST 360hr (110°C/85%RH)	Pass
	HTS 1500hr (150°C)	Pass
BLR	TCJ 5000x (0~100°C)	Pass

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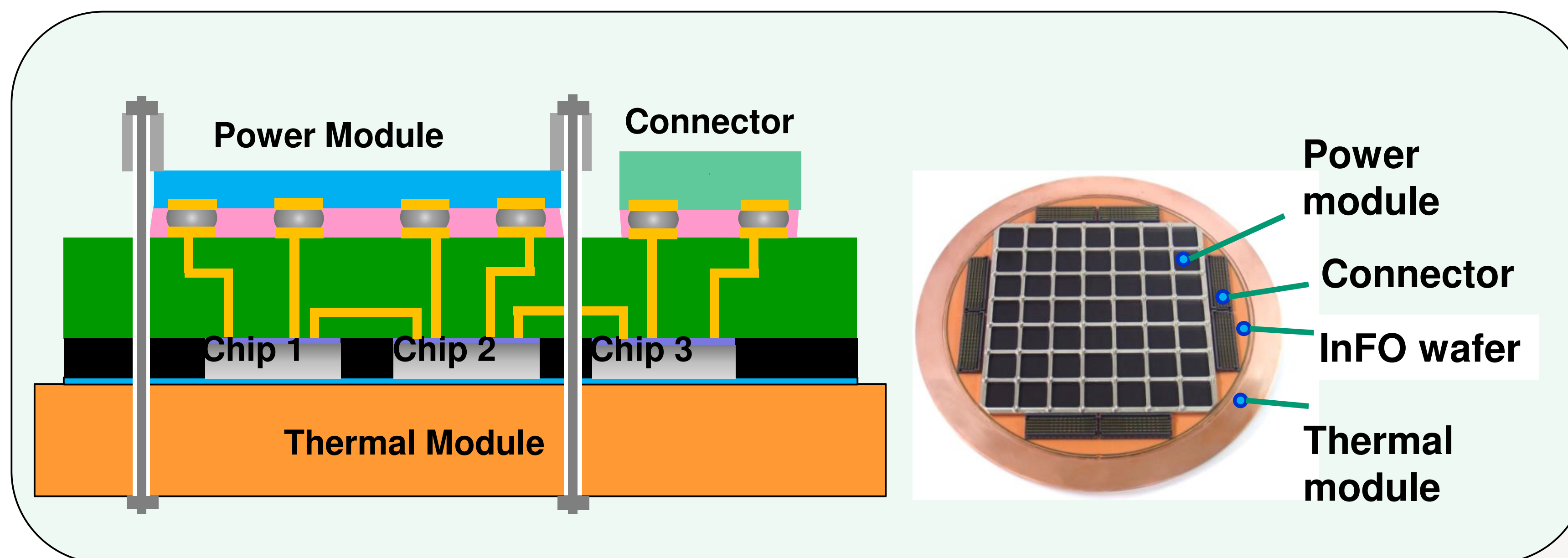
Key Advantages of InFO_SoW

- Full-wafer system integration with KGDs, compact size with integrated PWR supply and thermal modules.
- Leverage InFO technology for maturity, high bandwidth density. Low latency C2C communication and low PDN impedance.
- Heterogeneous integration of compute, IO, memory, passives chiplets, etc.



Wafer-Scale Engine by Cerebras systems

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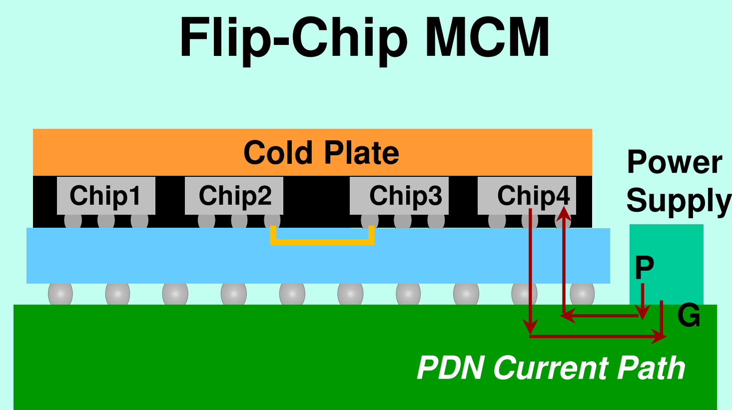
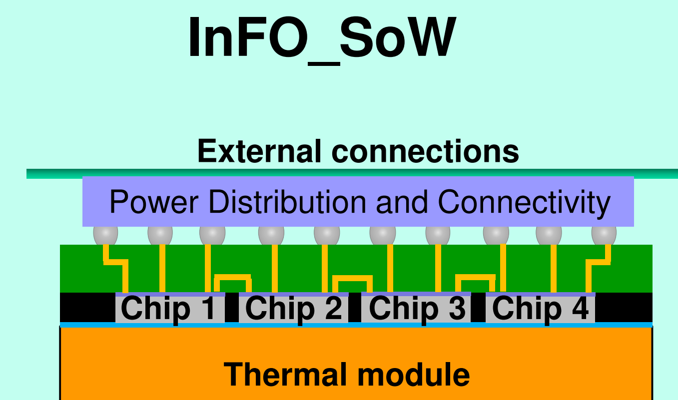
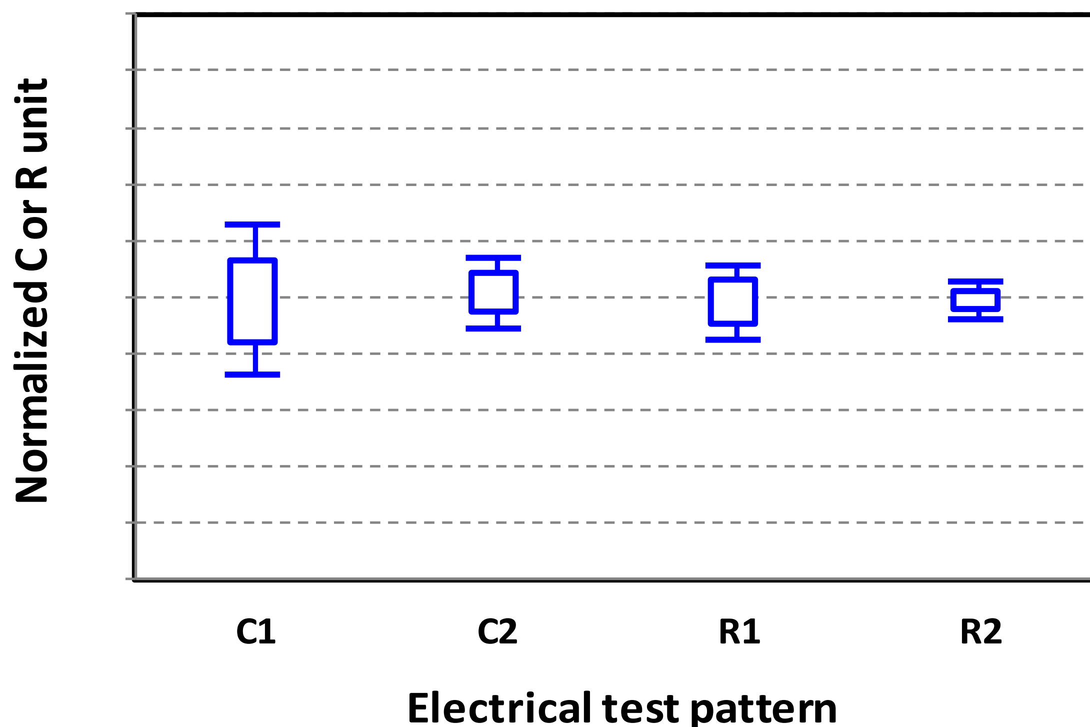
Benchmark MCM vs. InFO_SoW

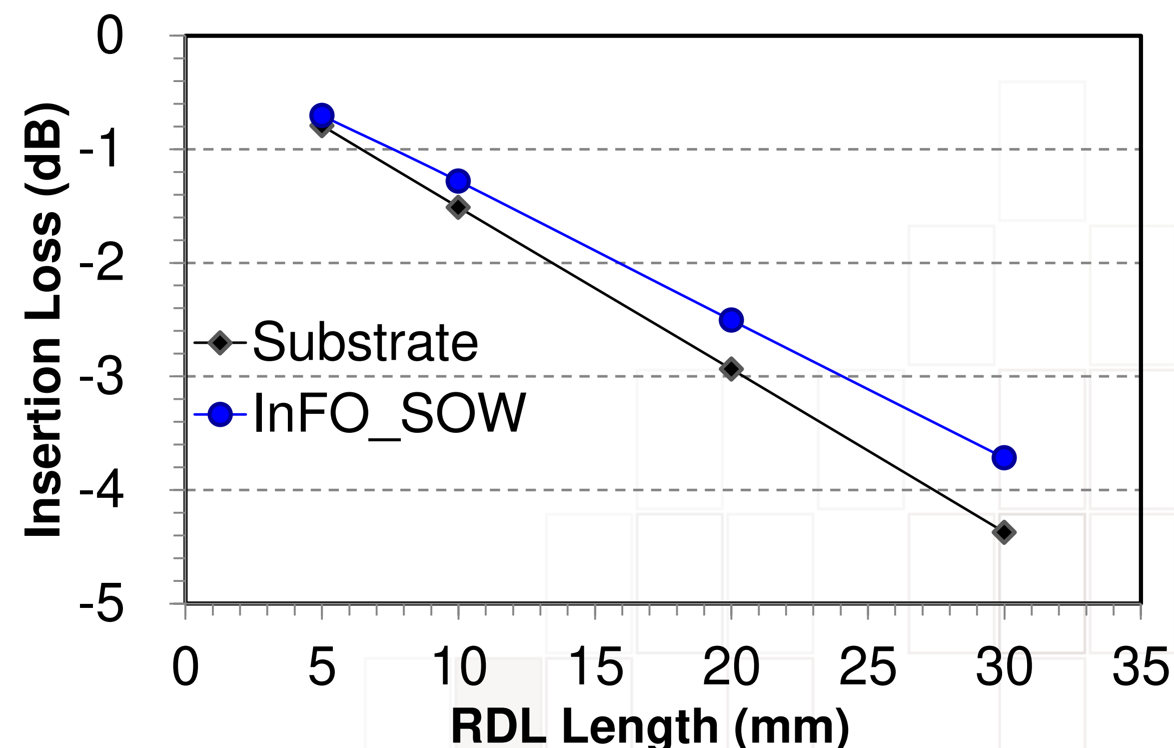
- Higher BW density (2x): Superior line density due to fine pitch RDL.
- Better power efficiency (0.03x PDN impedance): Simplified and low profile structure (without substrate or PCB).

Package Technology	Flip-Chip MCM	InFO_SoW
		
Line width / space (µm)	10 / 10	5 / 5
Line density	1x	2x
Bandwidth density	1x	**2x**
PDN impedance	1x	**0.03x**

Electrical Characterization

- Good process uniformity in R and C across the whole wafer.
- Higher quality Cu trace (vs. Substrate). 0.4/0.7 dB lower loss for RDL length 20/30mm at 28GHz, achieve 10/15% power saving, respectively.





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InFO_SoW Summary

- **Demonstrated industry-first full-wafer heterogeneous integration technology with good process control and high quality RDL across the whole wafer.**

Electrical Performance	**2x bandwidth density** & **97% lower PDN impedance** **15% power saving of the interconnects** (line length 30mm @28GHz)
Thermal Solution	**Scalable POC thermal solution: TDP 7000 W** (**power density 1.2 W/mm^2**) Maximal temp. <90°C
Process Robustness	**Verified** through **wafer-level quick torture** & **system level reliability tests** **CPI risk is relatively low** (<60% of qualified TV)

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CoWoS®-S Technology

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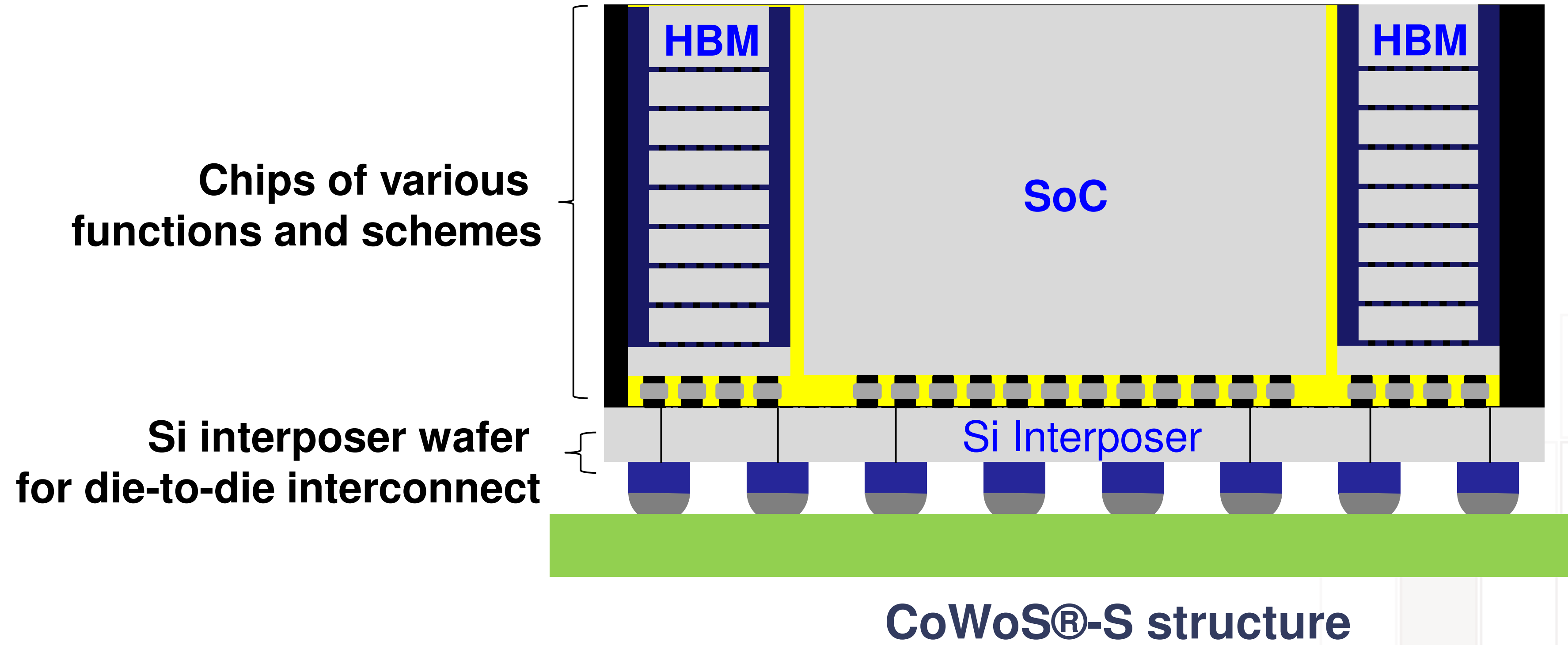
- Silicon interposer 2.5D system integration for advanced SoC and HBM.
- One decade of production with high yield and premium quality
- Continue to enrich the interposer features with extended envelope for HPC



CoWoS®-S structure

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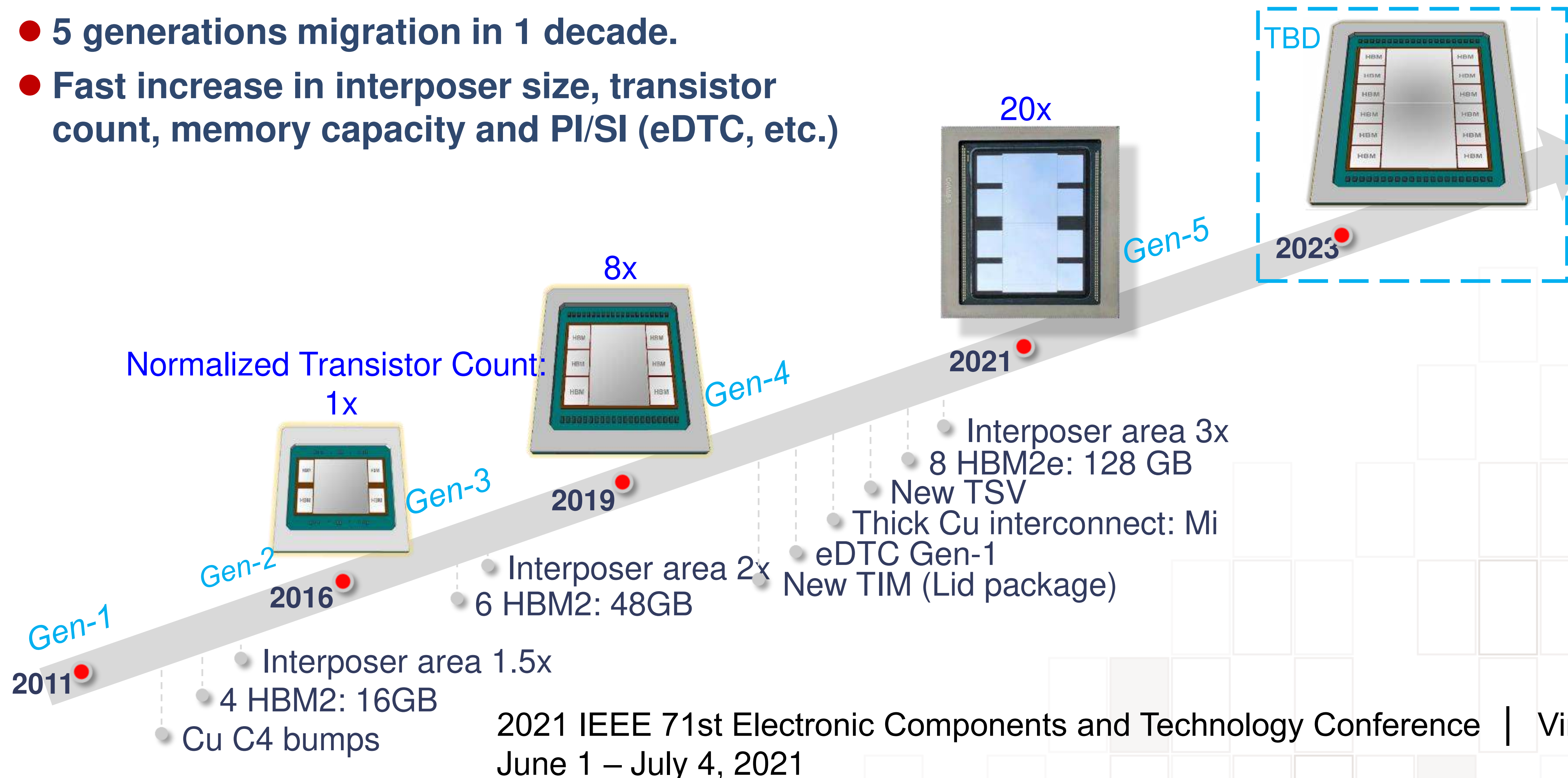
CoWoS®-S Rapid Progress

- 5 generations migration in 1 decade.
- Fast increase in interposer size, transistor count, memory capacity and PI/SI (eDTC, etc.)



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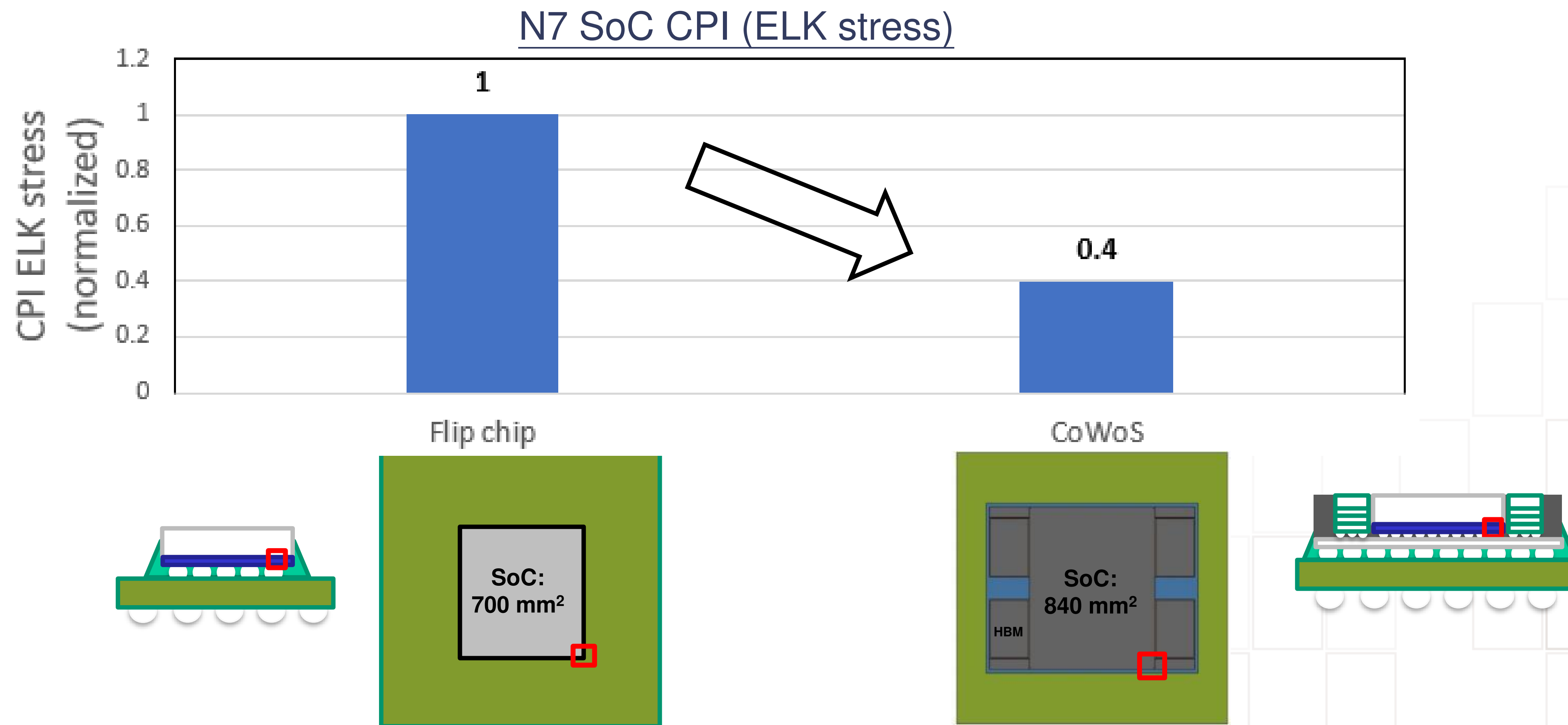
CoWoS®-S & Flip-chip CPI Comparison

- Leverage Cu/LK technology for high density interconnect
- Si interposer, a stress buffer between SoC and substrate, for reduced CPI



C.Y. Lu et al, IEEE 71st Electronic Components and Technology Conference June 1 – July 4, 2021

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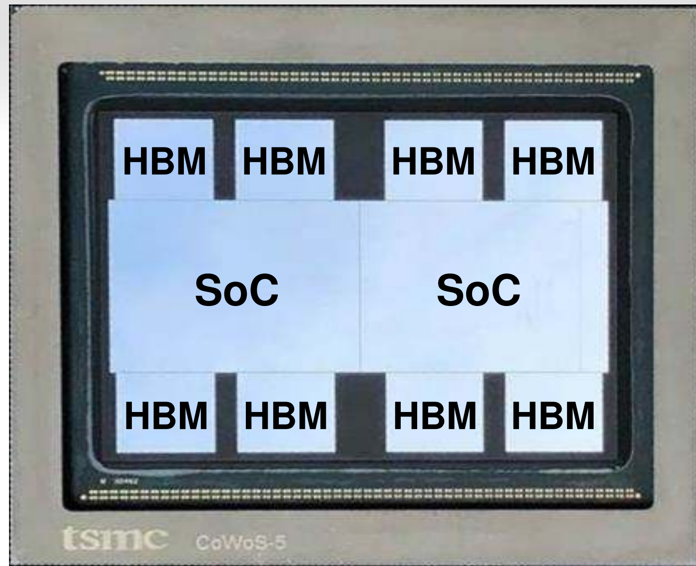
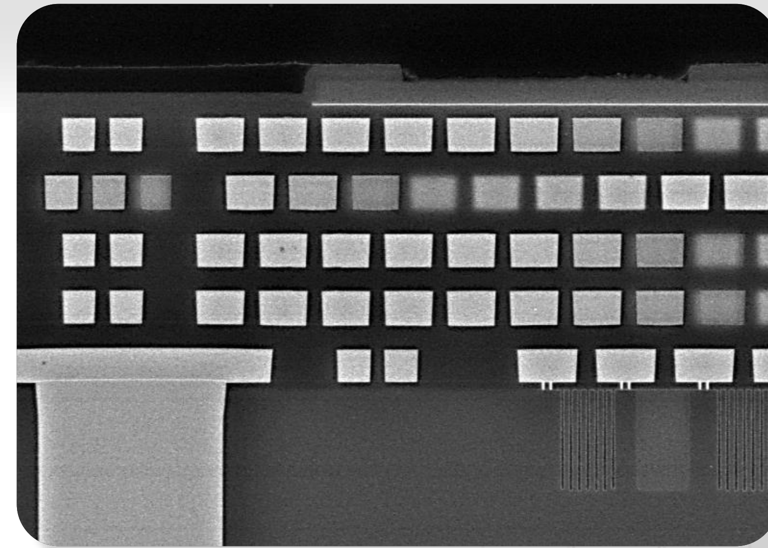
Leading CoWoS® Solutions for HPC

- Qualify 3-reticle Si interposer with thicker metal (5Mi), eDTC* and HBM2E in 2021 to further push for HPC.



CoWoS-S with 3-reticle Si interposer



Si Interposer with 5Mi and eDTC

*eDTC: Embedded Deep Trench Capacitor

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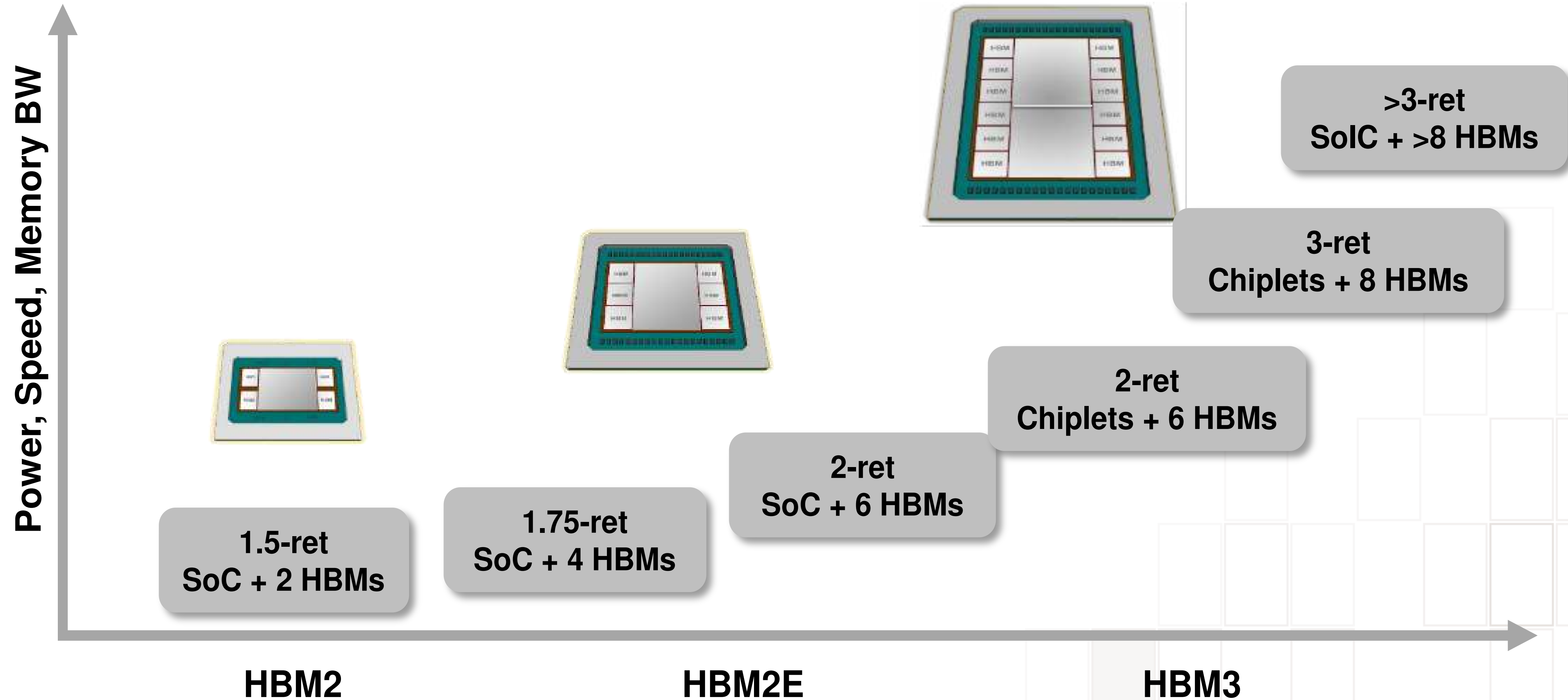
Chiplets Integration Reduces System Cost/function



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CoWoS®-S STAR (STandard ARchitecture)

- Shorten design cycle time and faster time to market
- 100% success rate for STAR adopters in 2020.
- More flexible design options in 2021. Adoption rate to grow 4x in 2021

	STAR 1.0 (HBM2)			STAR 2.0 (HBM2E)		
Floor Plan	ASIC, HBM	ASIC, HBM	SoC, HBM	ASIC, HBM	ASIC, HBM	SoC, HBM
Ret. Size	≤ 2X reticles	≤ 1.5X reticles	≤ 1.3X reticles	≤ 2X reticles	≤ 1.5X reticles	≤ 1.3X reticles
Status	Released	Released	Released	Released	Released	Released

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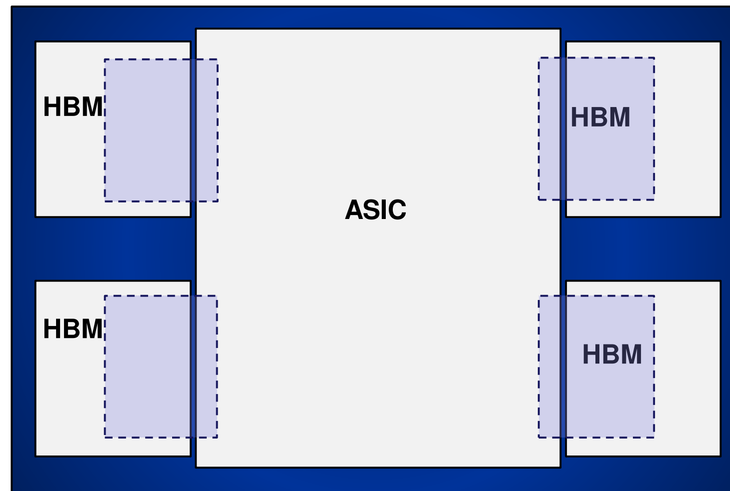
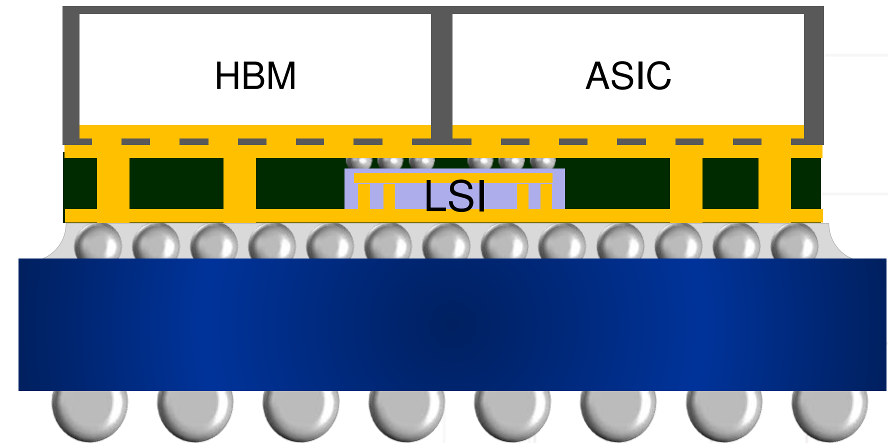
CoWoS®-L For Heterogeneous Integration

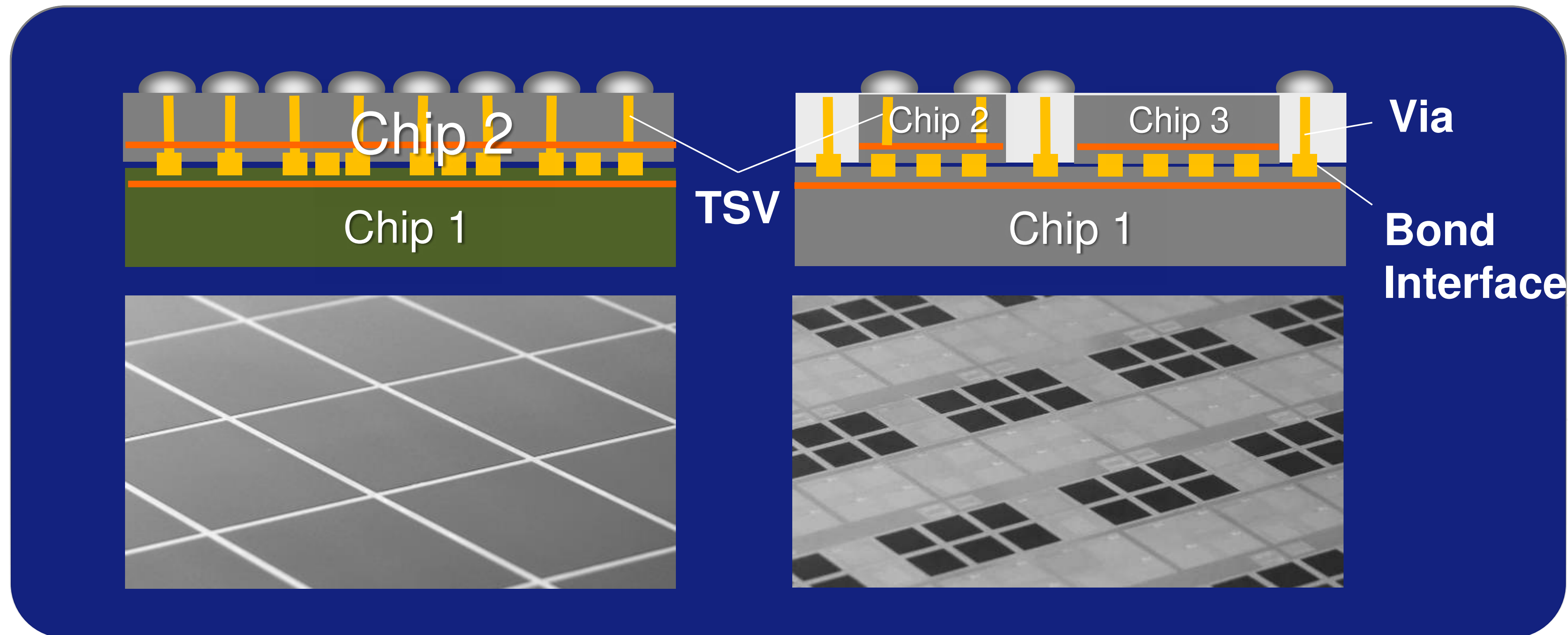
- Leverage InFO and CoWoS to integrate Si bridge, passives and RDL to best optimize CT, yield learning, system performance and EoS, etc.
- TSV in LSI (Local Si Interconnect), active & passive chip integration optional for better performance, power integrity, and design flexibility





3D Chip Stacking- SoIC^{TM}

- CoW development: N7-on-N7 CoW and N5-on-N5, KGDs
- WoW Development: Logic-on-DTC (Deep Trench Capacitor). Demonstrated power droop reduction



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SoIC Development Direction

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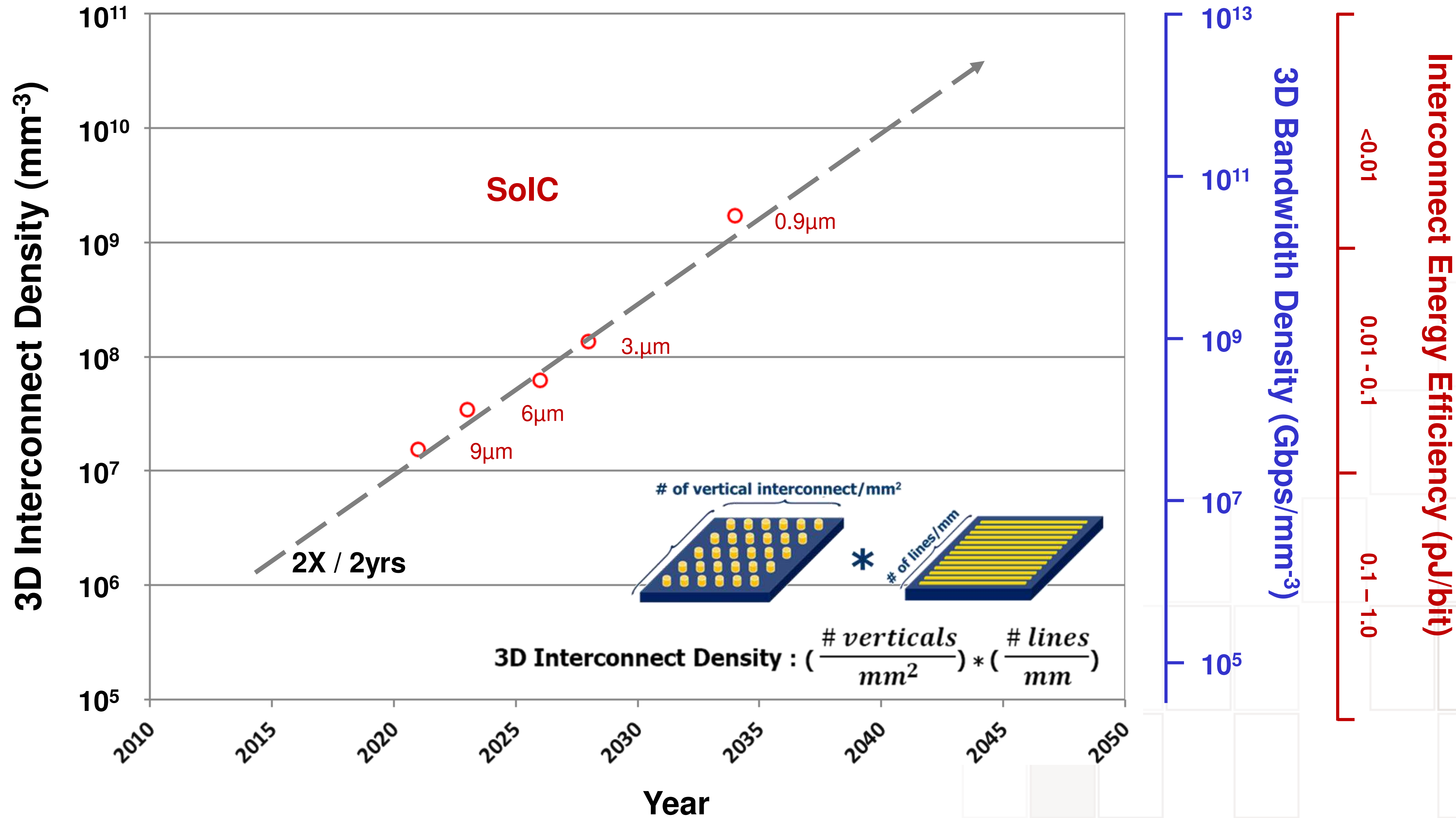
Inter-chip Interconnect Scaling Roadmap



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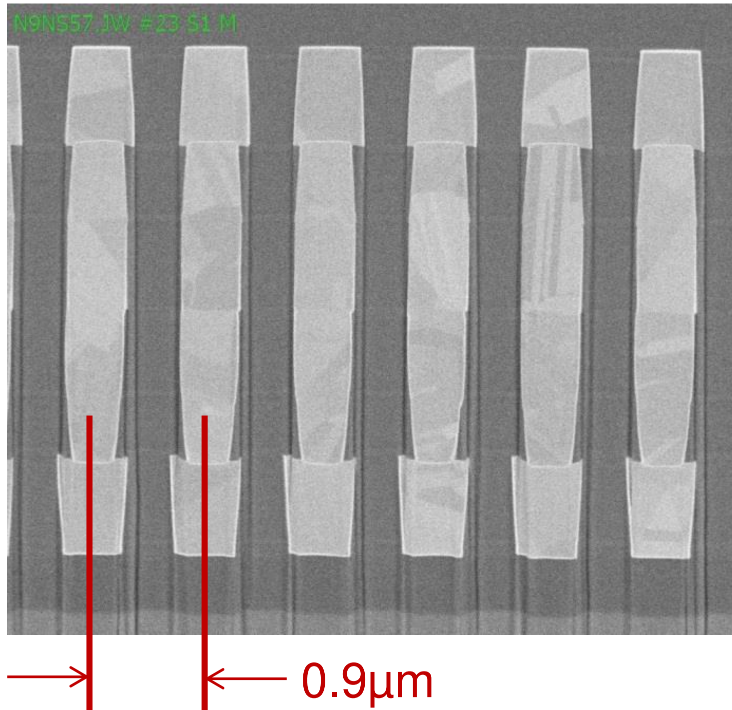
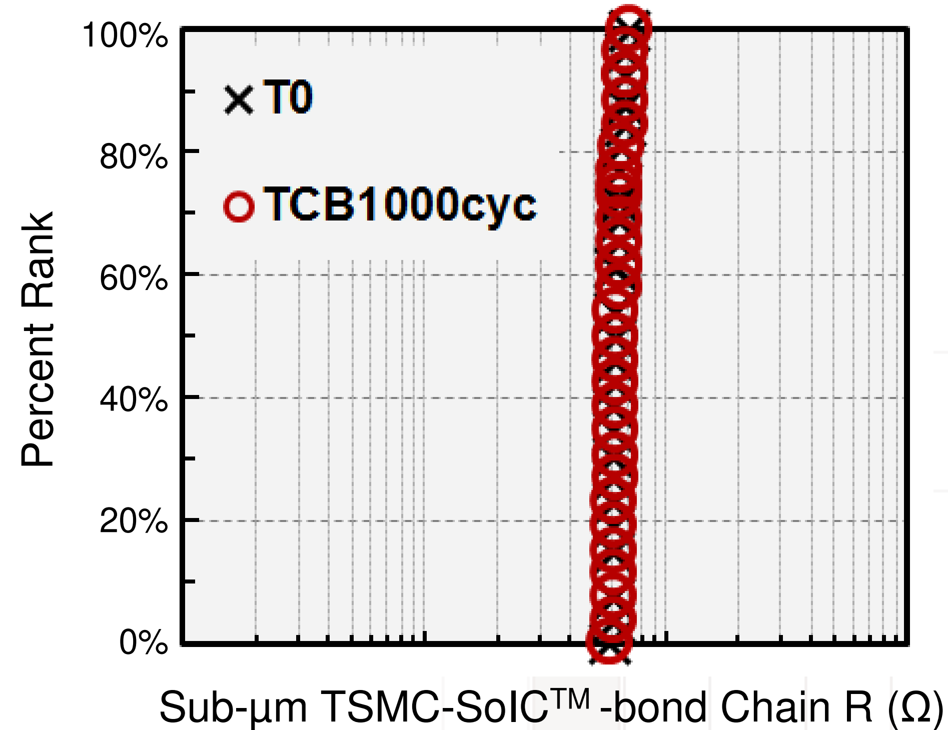
Sub-μm CoW Interconnect Feasibility

- 0.9μm bond pitch stacking
- Highly reliable after TCB 1000 cycle
- Enable direct integration of SoIC/bonding and SoC/BEOL interconnect





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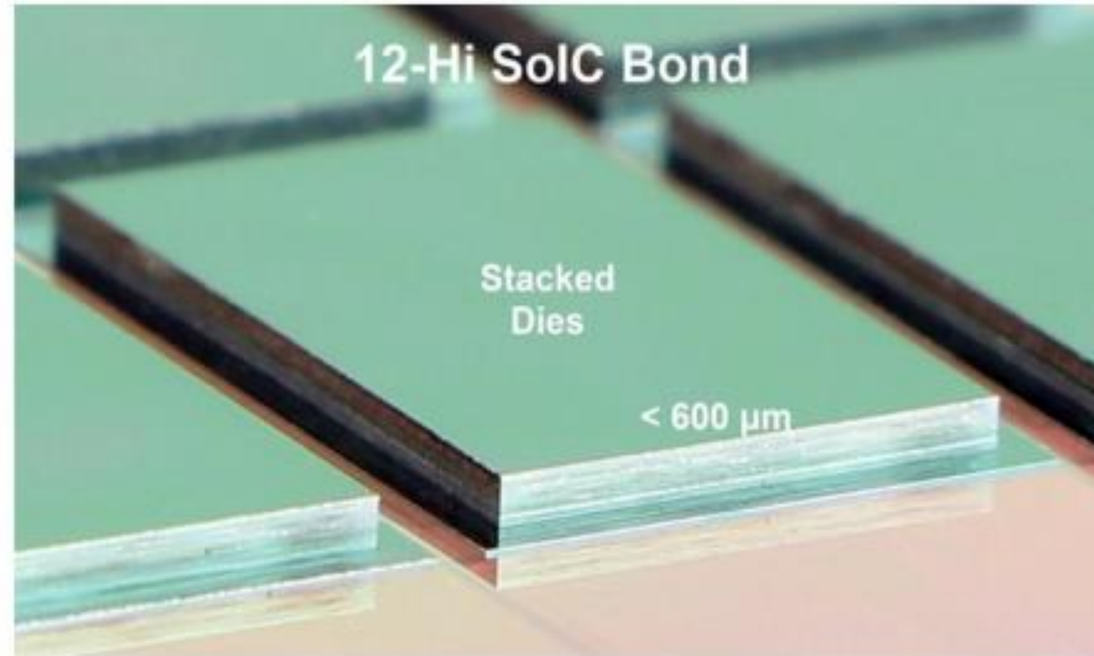
SoIC "Envelop Growth"

- **Bigger SoIC can be achieved with either more/larger units (2D) or more layers (3D) to integrate more memory capacity and/or higher functions.**
- **Thermal wall need to be addressed to remove heat accumulated in 3D stacking.**



Ref: IEEE Trans on Electron Devices, vol. 67, no. 12, 2020

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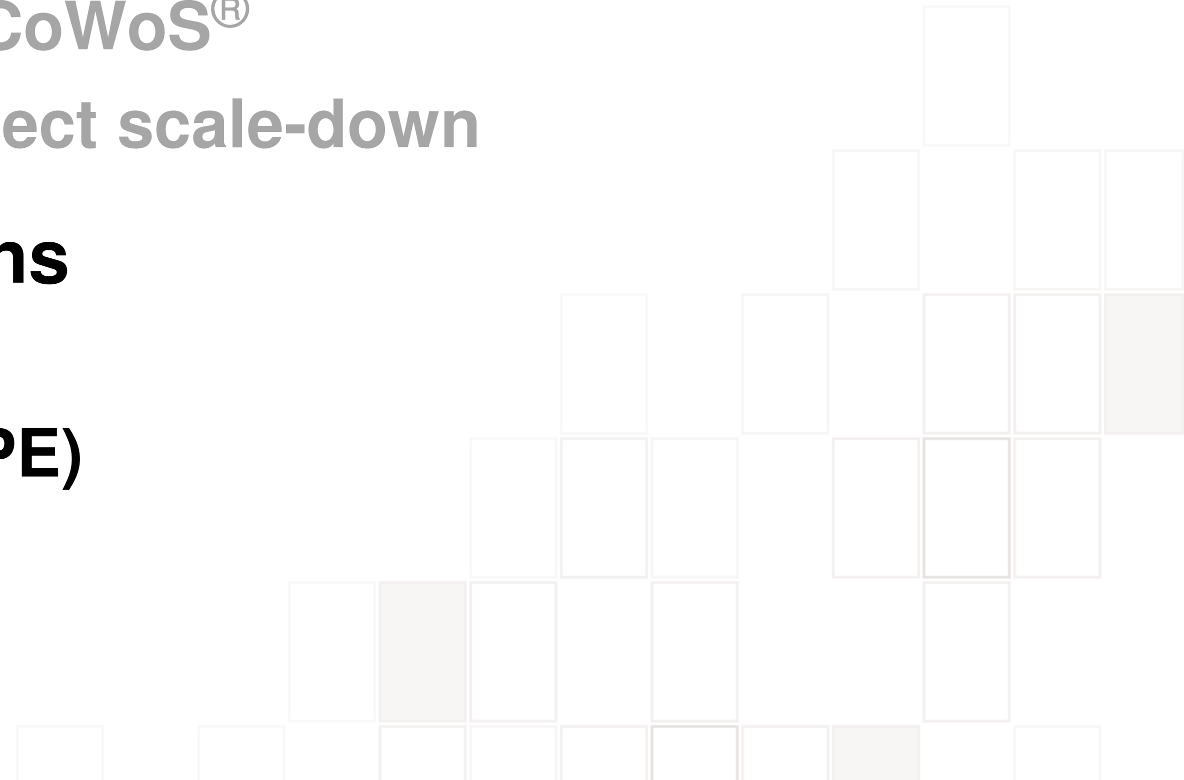

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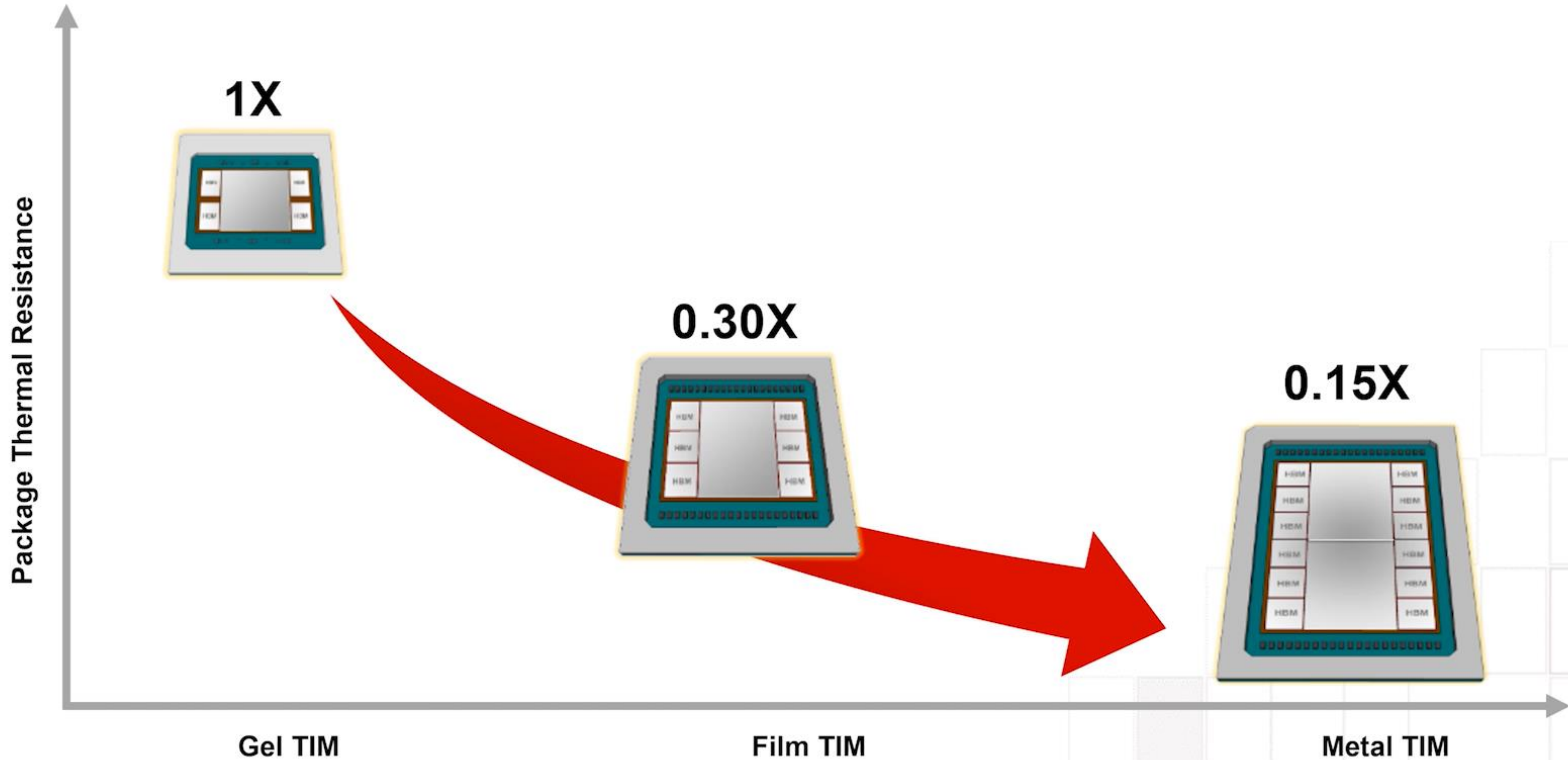
Thermal Solution Enhancement



TIM: Thermal Interface Material

Integrated Si Micro-Cooler (ISMC) for Ultra-HPC

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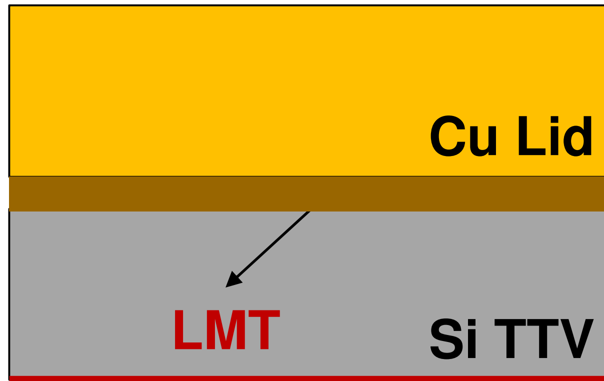
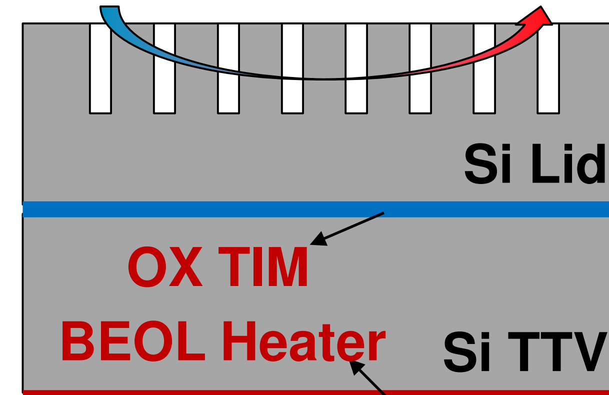
- Thin SiOx bonding interface (OX TIM) by fusion bonding Si lid and Si chips
- Low interface TR, even though K_{SiOx} at low single digit W/m·K

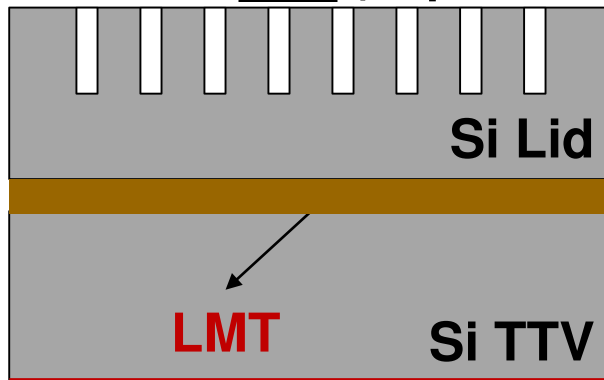
Cu Lid with LMT (Liquid Metal TIM)



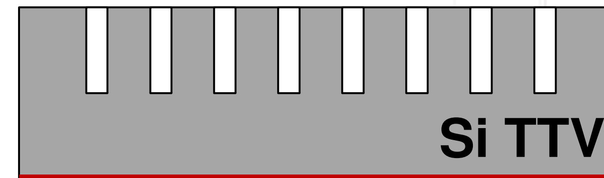
Si Lid with OX TIM



Si Lid with LMT (Liquid Metal TIM)



DWC (Direct Water Cooling)



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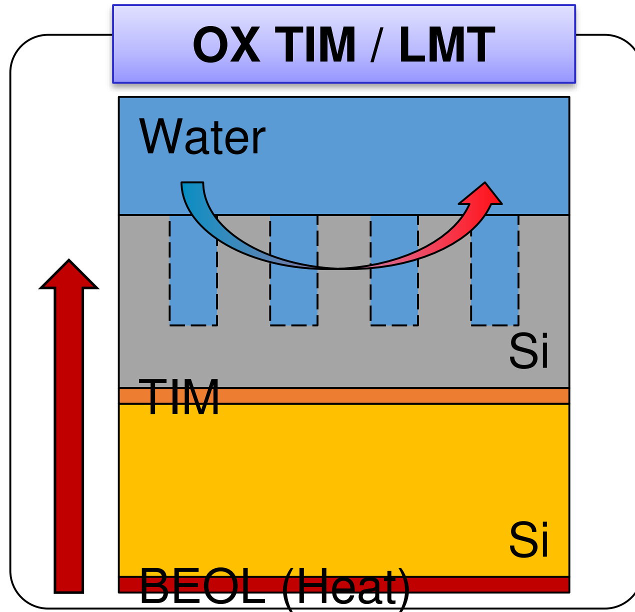
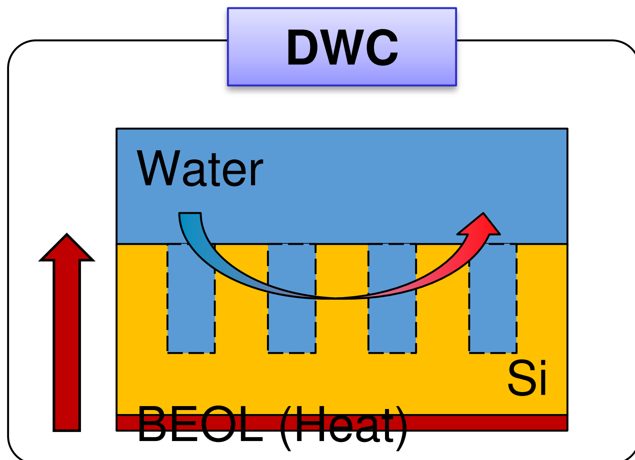
Cooling Performance Benchmark





	LMT (2LPM)	LMT (5.8LPM)	OX TIM (2LPM)	OX TIM (5.8LPM)	DWC (2LPM)	DWC (5.8LPM)
Total TR	31	22	28.5	19.5	22	13
Si/Water	20	11	20	11	20	11
Bulk Si in lid	2	2	2	2		
TIM	4	4	1.5	1.5		
Bulk Si	5	5	5	5	2	2

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ISMC Summary

- Leverage 3DFabric to develop new Ox TIM to replace LMT, achieved TR~2 K·mm^2/W, 50% reduction from LMT.
- Demonstrated fusion bond Si lid (OX TIM) provides kW level heat dissipation solution for large chip size (>500mm^2).
- Further improvement on the thermal performance obtained from DWC scheme. Mechanical strength of the new structures and their reliability will be studied.

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The Need for SiPh

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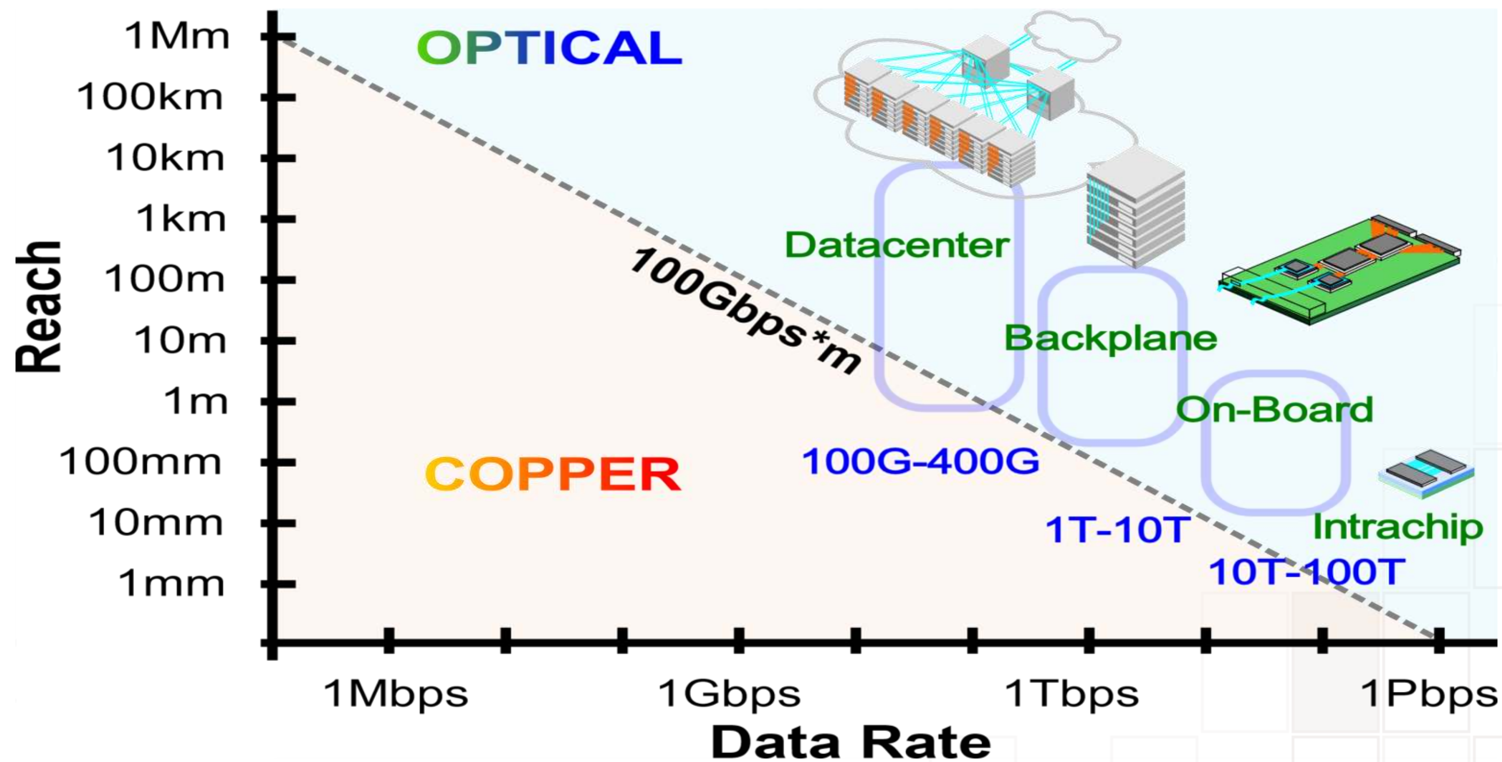
- The explosive growth of internet traffic has driven data centers to turn to Silicon photonics (SiPh) for its high speed and low power consumption.
- Compact Universal Photonic Engine is proposed to address the need for wide range applications on performance/power and volume/cost.



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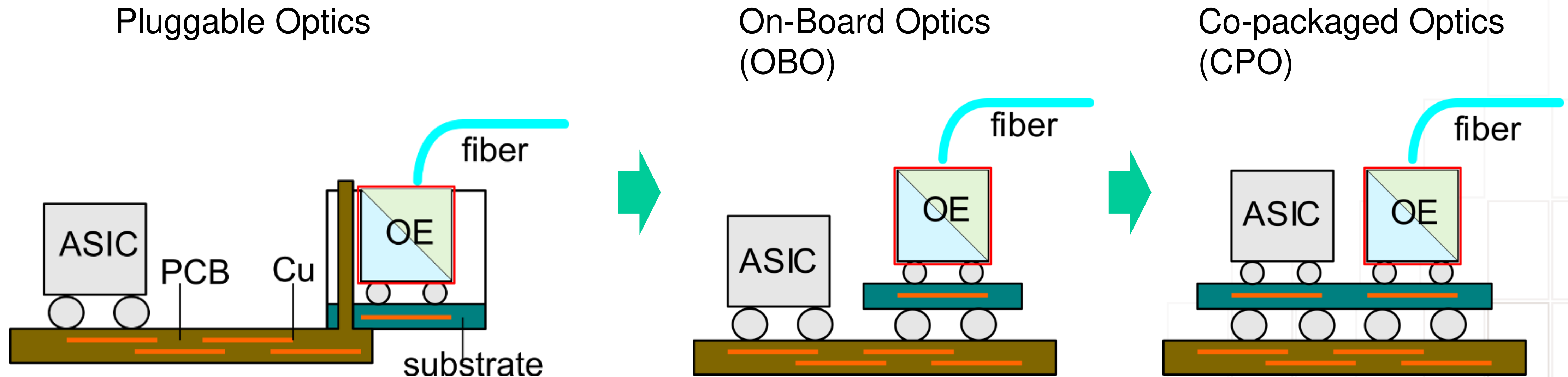
Evolution of SiPh Package

- Evolution of the SiPh package: from Pluggable Optics, On-Board Optics (OBO), to Co-Packaged Optics (CPO).
- Drive to closer proximity between key components for bandwidth, power efficiency and even cost (eg. super-large size substrate)



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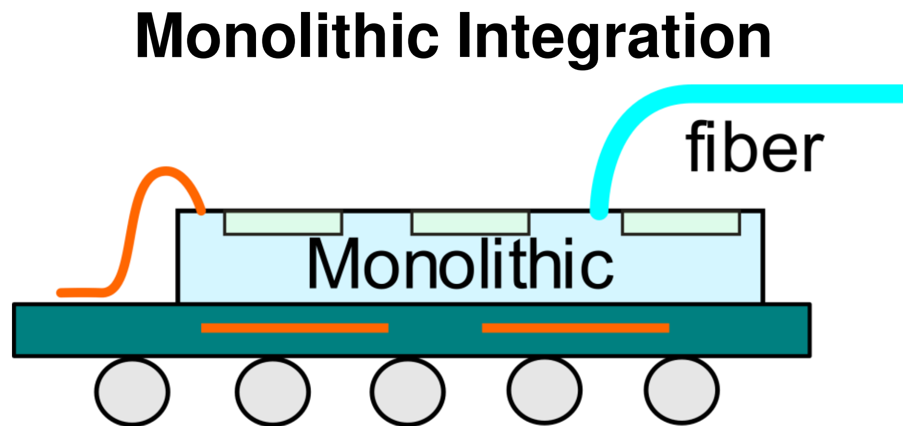
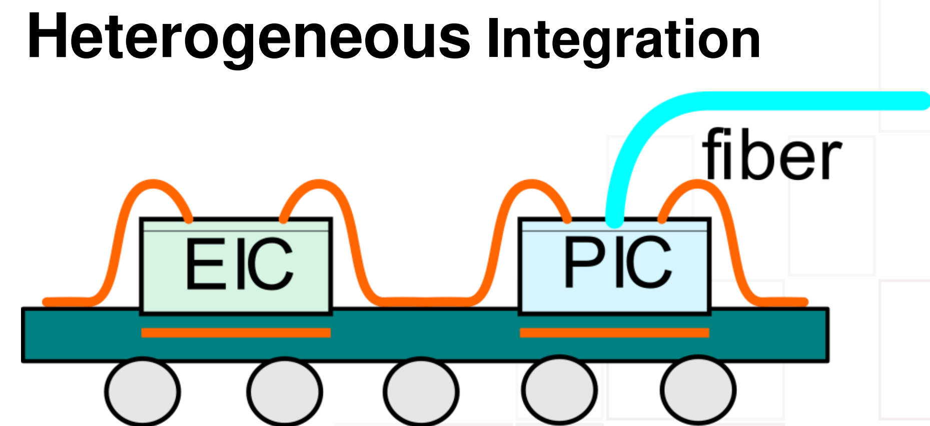
Photonic Engine Integration Schemes

- High data rate and power efficiency could be achieved by monolithic integration.
- Technology node disparity between EIC and PIC is the main economic challenge for monolithic integration.
- COUPE, being a heterogeneous integration technology, is designed to minimize electrical coupling loss.





Electrical Interface (1/2)- Parasitics and PDN Impedance

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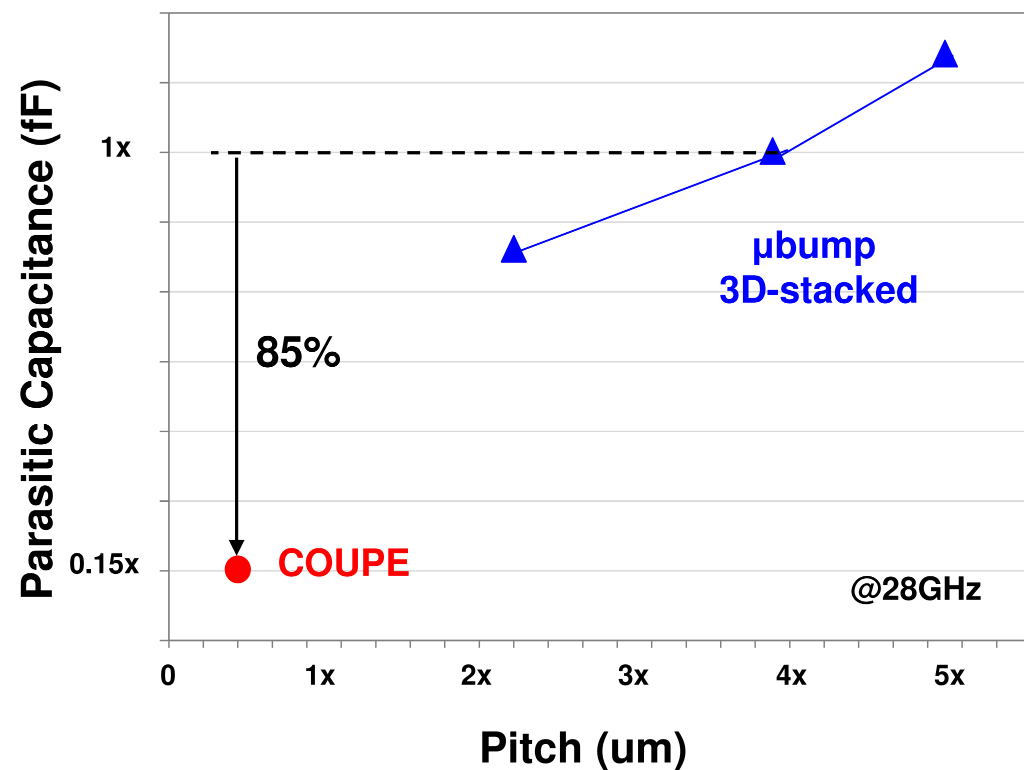
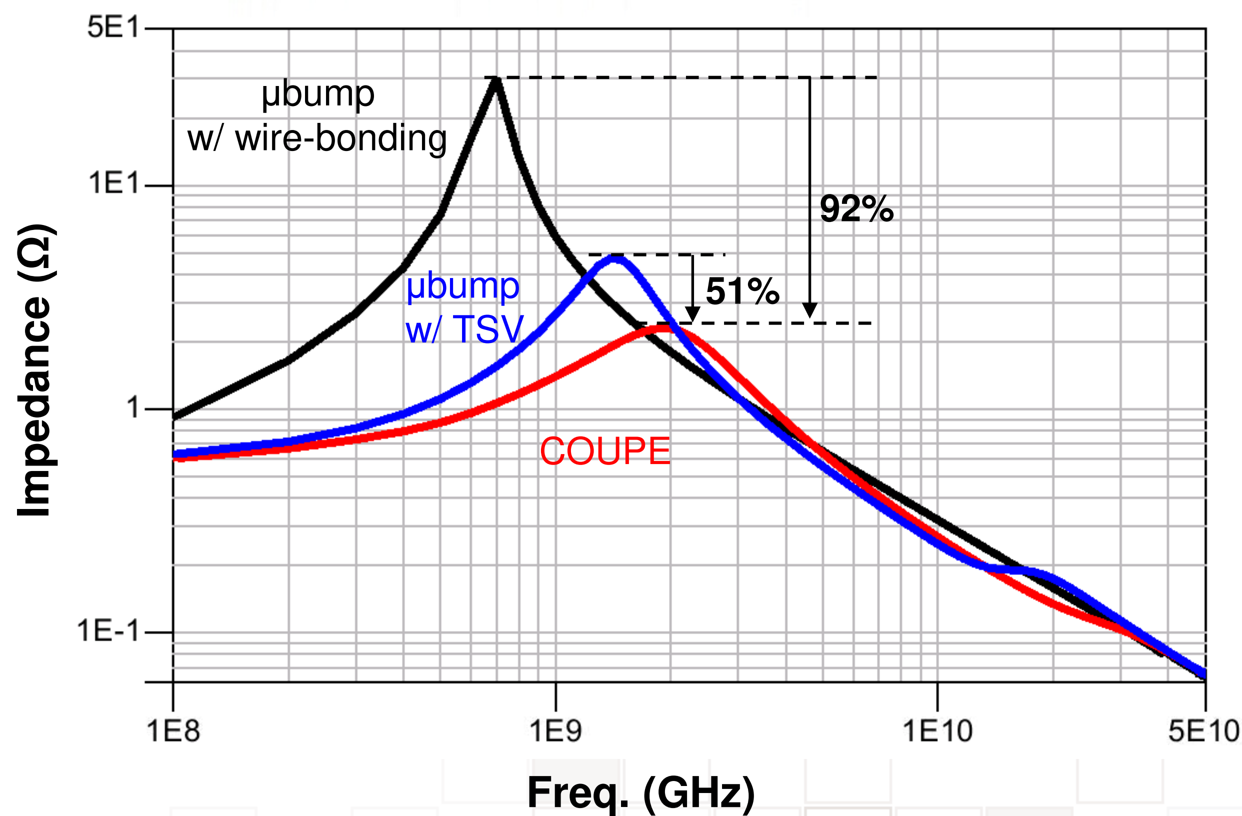
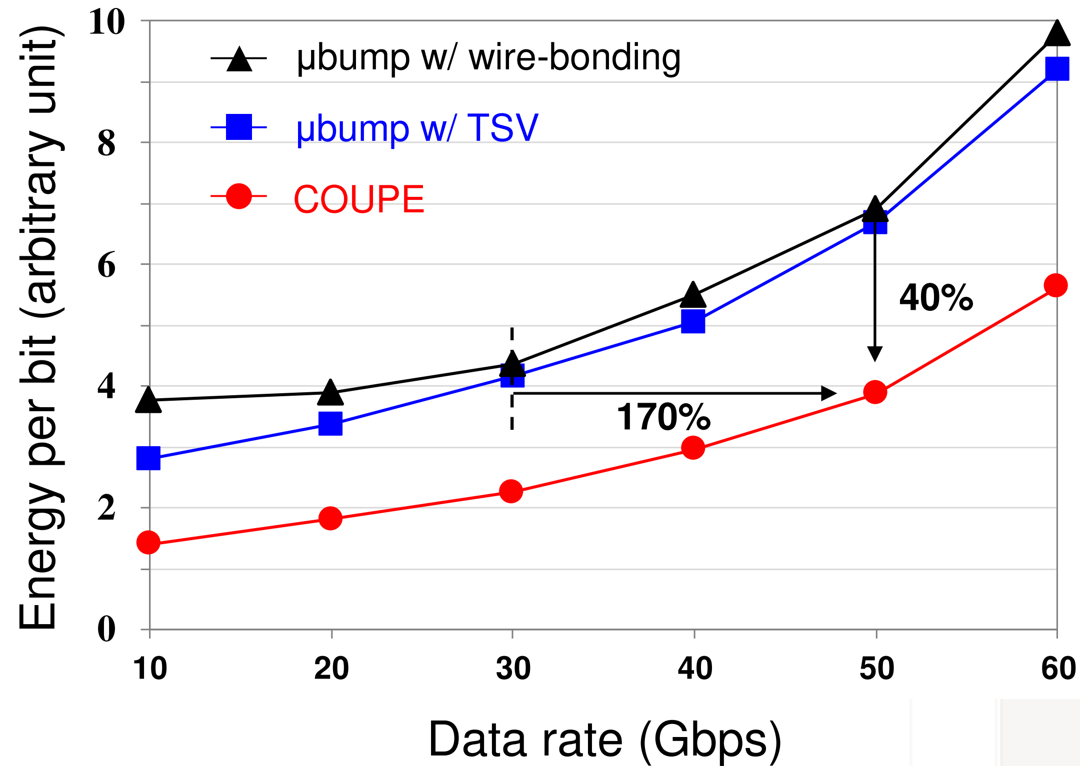
- COUPE has low parasitics at EIC-PIC Electrical Interface, 85% lower capacitance compared with uBump
- 51% reduction in PDN impedance comparing with uBump w/ TSV; and 92% reduction of uBump w/ wire-bonding.





Electrical Interface (2/2)- Power Consumption

- **Power Consumption Comparison with uBump-based PE:**
  - **COUPE has 40% lower power consumption at the same speed.**
  - **COUPE can reach 170% speed gain with the same power.**



Photonics Engine's TX Power Consumption

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Optical Interface (1/2): Overview

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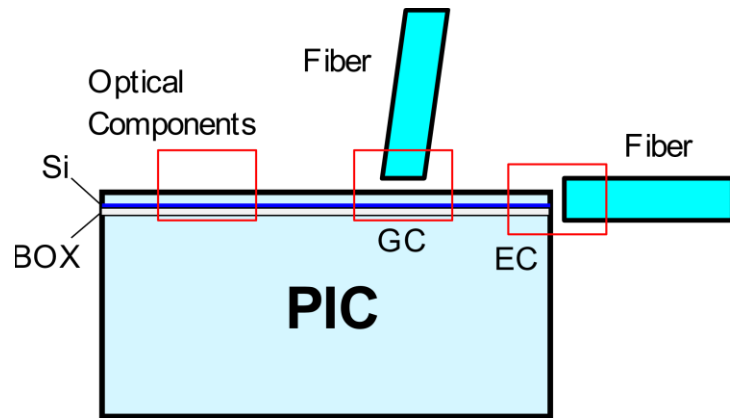
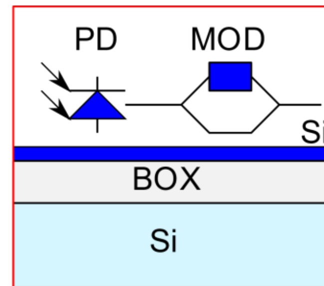
Light can be coupled either vertically (GC) or horizontally (EC):

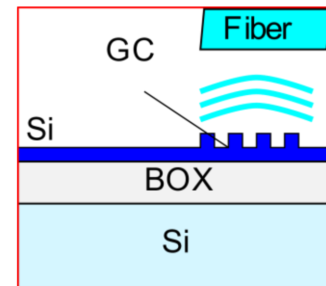
- GC, as a surface coupler, requires cleanliness and integrity of the optical path from grating surface all the way to the fiber core.
- For EC, care must be taken to prevent the expanded optical mode from overlapping with the bulk silicon underneath SSC.



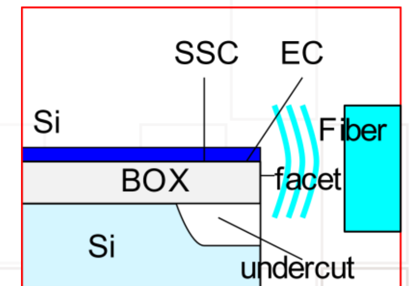
PIC is based on SOI wafer



(A) Optical Components



(B) Grating Coupler



(C) Edge Coupler

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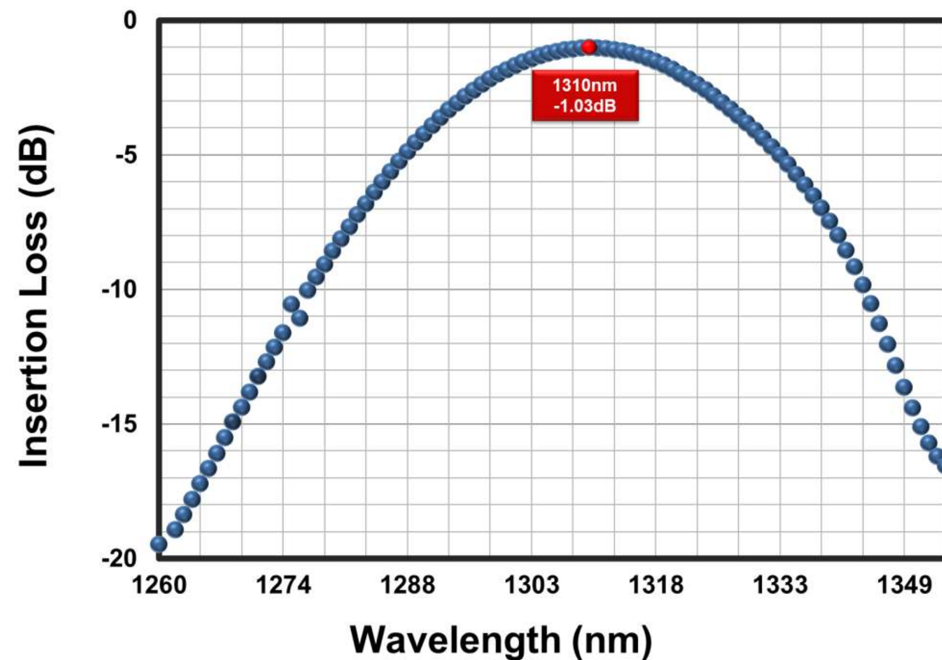
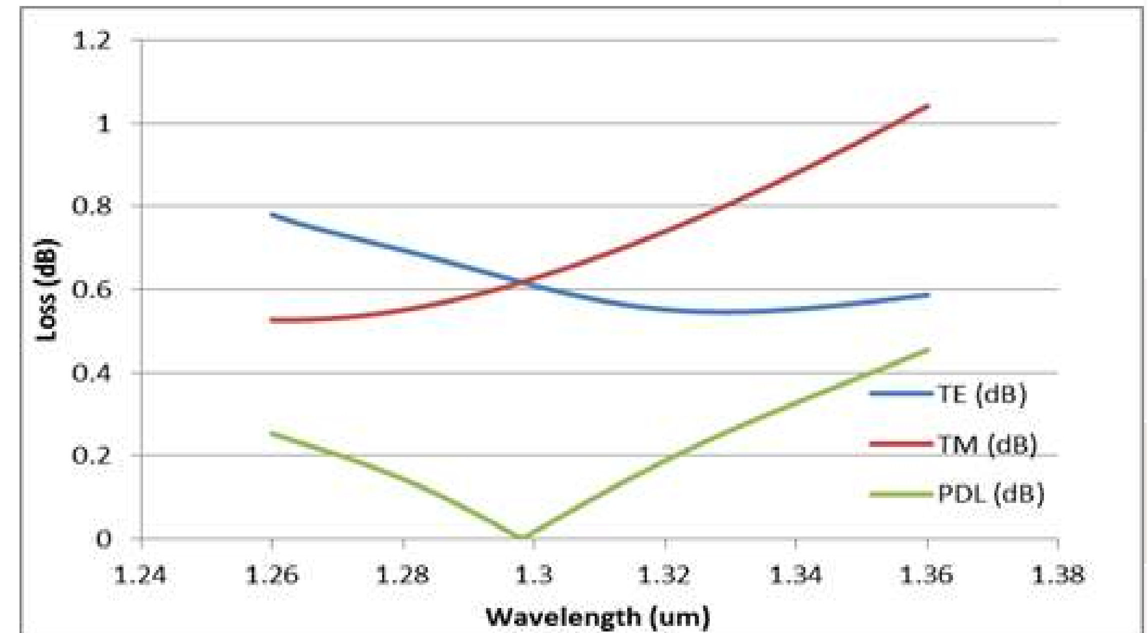
Optical Interface (2/2): GC and EC with COUPE

- GC is designed with optical path intrinsically sealed with dielectrics all the way to the fiber attachment unit, achieving IL (1D apodized GC) -1.03dB @1310nm for TE
- EC avoids optical loss due to beam overlapped with underneath Si, achieving IL -0.6dB @1310nm for TE&TM modes
- With COUPE, GC and EC can built with essentially the same structure.



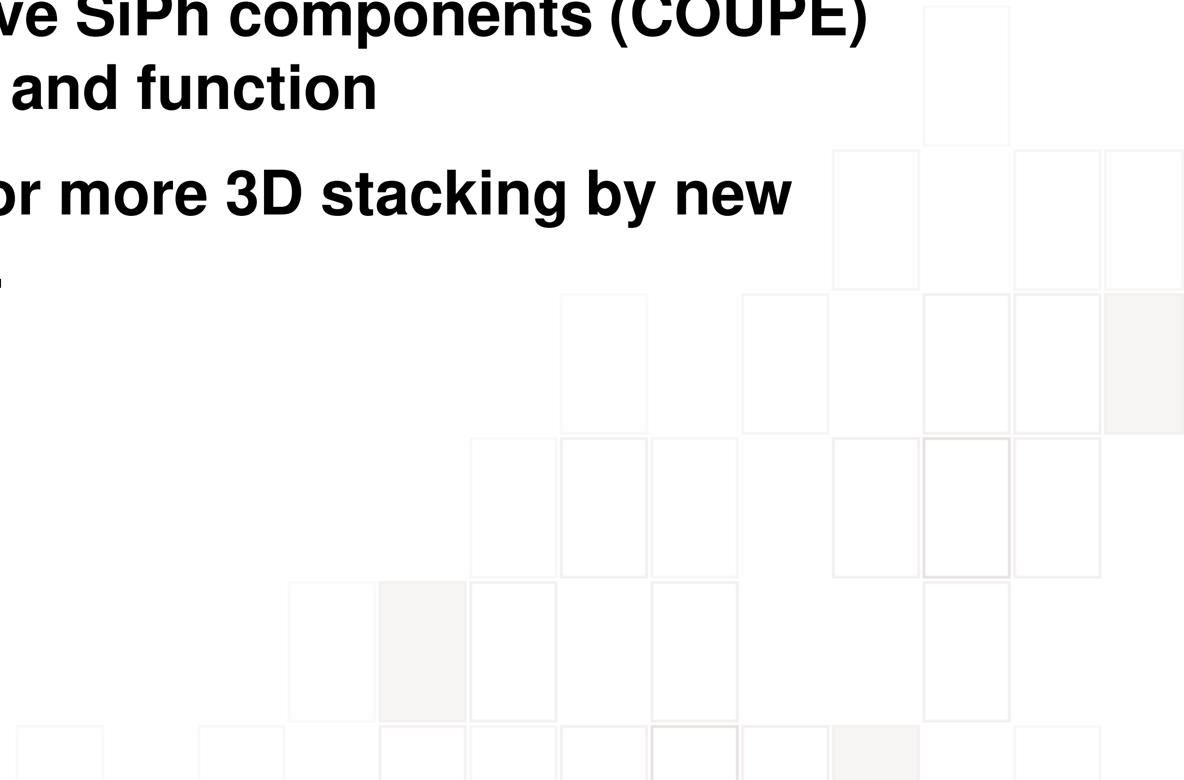
Grating Coupler Insertion Loss



Edge Coupler Insertion Loss

Summary

- TSMC 3DFabric™ technology platform continues packaging envelop scale-up, and 3D stacking interconnect density scale-down to drive energy efficient performance.
- Leverage 3DFabric to integrate innovative SiPh components (COUPE) to further enhance system performance and function
- Thermal wall could also be addressed for more 3D stacking by new micro-cooling systems- ISMC and DWC.



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Thanks for Your Attention.