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Semiconductor Reliability Handbook

Handbook

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Renesas Technology
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Section 1 Quality Assurance

1.1 Renesas' Approach to Quality Assurance

Renesas Technology Corp. has integrated reliability/quality assurance techniques and know-how that the semiconductor divisions of our mother companies Hitachi Ltd, and Mitsubishi Electric Corporation have acquired over many years in the semiconductor business and has built a quality assurance system that complies with ISO 9001-2000 and ISO/TS16949. Based on the concept of building in reliability from the design stage backed up by reliability engineering, Renesas provides a comprehensive quality assurance/management program that covers all product stages from planning to after-sales servicing.

Renesas' focus is on ensuring and improving quality and reliability. To achieve our goal, we enforce quality control at three levels: design, production, and finished product. Quality first: This is how every Renesas employee strives to satisfy customers.

1.2 Quality Assurance System for Semiconductor Devices

Figure 1.1 outlines our quality assurance system, which embraces the life cycle of a product from development and design to mass production to shipment and field use.

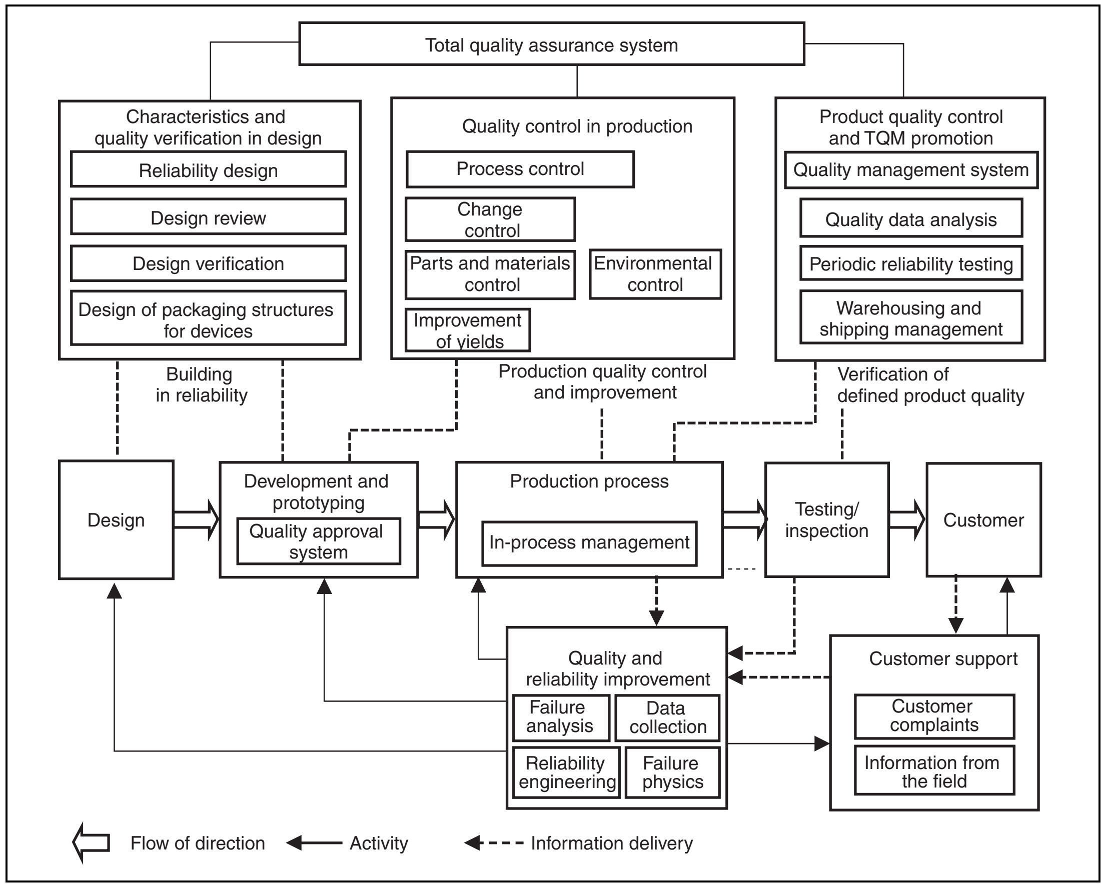

Figure 1.1 Renesas Quality Assurance System for Semiconductor Devices

Quality control in the design stage builds the specifications and quality of the product. It focuses on optimization and review of structures, materials, circuit design, packaging, and production processes. For each product type, prototypes are fabricated to verify characteristics and reliability before mass production begins.

Quality control in the production stage builds quality during the production process. It is used to manage the quality of manufacturing equipment, jigs and tools, air and water cleanliness, gases, and manufacturing conditions, and finished product. We have established EDP (Electronic Data Processing) management of quality control information as an integral part of the Renesas total quality control system.

Quality control in the finished product stage has two aspects. The first is in-house testing and inspection by device, by lot, or of samples to determine if products have met the prescribed functionality and reliability. The second is customer support by which we accept returned products and provide quality control information.

The quality control information is collected in the development and design, production, shipping, and field use stages, and is fed back to each stage to improve quality.

Figure 1.2 shows a flowchart of the quality assurance program.

Our quality control system was built based on the ISO 9001 and ISO/TS 16949 standards.

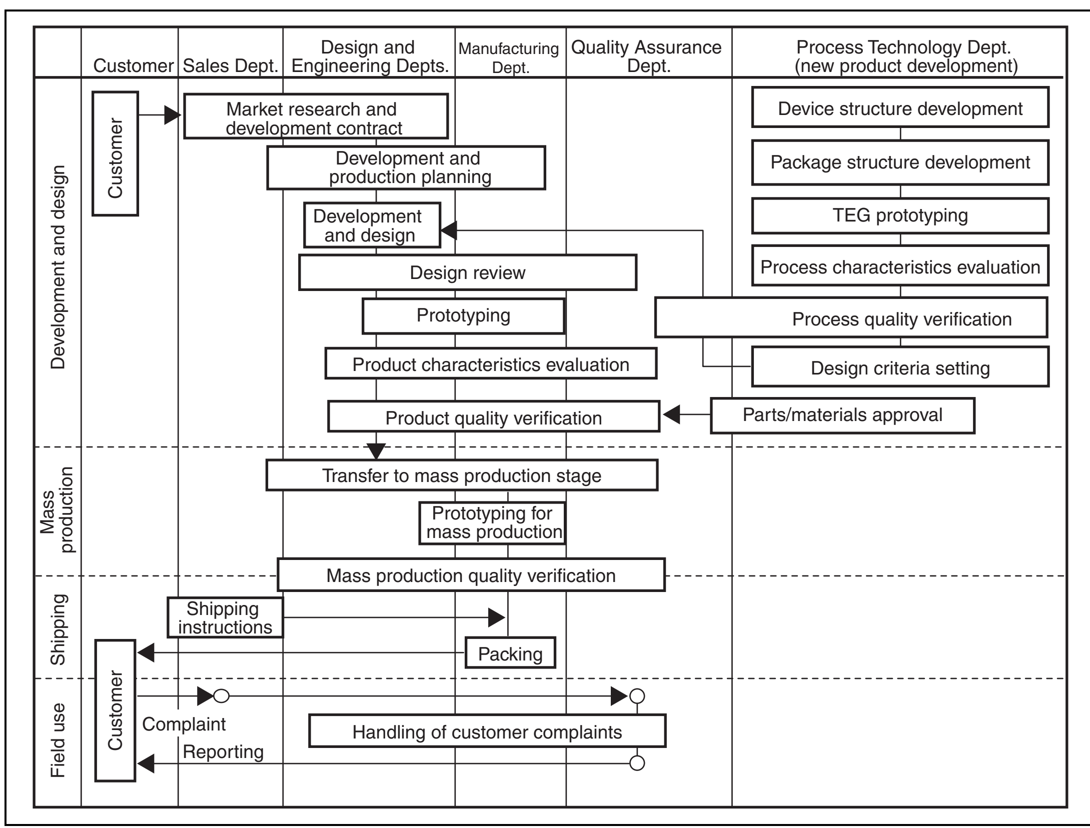

Figure 1.2 Quality Assurance Program Flowchart

Not only have Renesas products been manufactured with high reliability and then improved for higher reliability by the quality assurance system illustrated in figure 1.2, but they also they have been specified from the product development stage for an appropriate degree of reliability based on the classification in table 1.1.

Table 1.1 Quality Levels

Quality Level	Description	Typical Product Applications
High reliability	High-quality products	Vehicles (drive-train systems) and general traffic systems
Industry	Industrial applications	Vehicles (accessories) and industrial factory automation
Consumer	General-use products (including products subject to PPM (parts per million) control and custom-made products)	PCs, home appliances, and mobile phones
Custom	Products with individual specifications (products not fitting into any of the levels above and set with different standards)	Video games, mobile phones, and applications requiring ultra high reliability*

Note: * Designed under a separate contract

1.3 Quality Assurance at Development Stage

We use the following procedure to ensure the target quality and reliability in product development. Using the demand estimate based on market research, we plan development considering the required levels of quality, functionality, reliability and production issues. Then new theories, technology and ideas are adopted for design and development. For this purpose, we have defined three development levels.

Level I: Developing products with new design rules, materials, and process technology

Level II: Modifying the design of mass-produced products, or partially modifying processes, packages, materials, and equipment

Level III: Using the current processes and packages or those of similar or slightly modified quality levels

Fault tree analysis (FTA), failure mode and effects analysis (FMEA), or and/or other methods are used to review the design and then prototype is fabricated. Then the prototype undergoes a qualification test that checks whether their electrical characteristics, maximum ratings, and reliability meet the quality target.

When the prototype passes the reliability test, a pre-production meeting is held to check for any problems related to design, production, and quality. If no problems are found, the prototype goes to the pre-production stage. Each development level has a specific quality check and approval flow. The steps for Level I, for example, are usually performed as follows.

To help ensure the desired quality and reliability, quality certification, which is based on reliability design, is conducted at each stage of device design trials and mass production.

The concepts are:

1. Use an objective viewpoint of the customers' stand point.
2. Incorporate examples of past failures and field use information.
3. Certify design modifications and operation alterations.
4. Certify parts, materials, and processes using stringent criteria.
5. Investigate the process capability and causes of deviation and verify the control points during mass production.
   The process of certification is divided into four steps:
   a. Certification of Parts and Materials
   b. Characteristics Approval
   c. Certification of Design Quality
   d. Mass Production Quality Certification

Design verification for parts and materials is performed during the Certification of Parts and Materials. Product design verification is covered in Characteristics Approval. Design validation is through Certification of Design Quality. Finally the product quality level on the mass production line is checked through Mass Production Quality Certification.

At the pre-production stage, initial period management is carried out to check the quality of manufactured products. Initial period management applies for a limited time after production start, during which an increased quantity of information is collected. Immediate corrective actions are then taken for any failures detected and the results are checked. Also at this stage, we prepare standard forms for mass production and train workers. In addition, we set up materials/and parts supply systems and provide equipment and tools required for production. The new device is now ready to enter the mass production stage.

1.4 Quality Assurance at Mass Production Stage

At the mass production stage, the device is put into continuous production based on the production plan. The Manufacturing Department controls the materials, parts, production process, environment and equipment conditions. They also perform in-process inspections, final inspection and quality assurance test on both semi-manufactured and manufactured products to check quality levels.

Building in quality at this stage is very important for manufacturing high quality products economically. To do this, the Manufacturing/Engineering Department provides operating instructions and defines control items for critical production conditions. Operation proceeds in accordance with the instructions. Check sheets are used to control manufacturing conditions that affect the quality and some specific product/process data is controlled to maintain or improve quality level.

Periodical inspections and accuracy adjustments are performed for early detection of abnormalities and for establishing/monitoring preventive maintenance schedules.

The in-process quality control performs Statistical Process Control (SPC) with completed products production and measurement values. The quality control information is fed back to earlier processes to improve quality levels.

To build in quality, statistical techniques are used at each stage. In particular, in the mass production stage, management diagrams are applied to critical work steps to monitor whether process dispersion is within the acceptable range. In this SPC, the process capability indexes (Cp and Cpk) are checked to reduce any further process dispersion.

The process capability indexes, which are defined below, are used to obtain the stability of the process with respect to the process specifications from the process data and the specified control values for a specified period. The Cp value (agreement between the specified center value and the average of the process data) and the Cpk value (disagreement between the specified center value and the average of the process data) are periodically acquired and used to reduce the process dispersion.

$$\mathrm{Cp} = \frac{(\text{Specified upper limit - Specified lower limit})}{6\sigma}$$

$$\mathrm{Cpk} = \frac{|\text{Specified limit close to the average - Average}|}{3\sigma}$$

At the final inspection, all products undergo electrical characteristic testing. Screening is performed to reject defective marginal products. The resulting data is used for improving quality.

Samples of the completed products that have passed the final inspection are subjected to quality assurance tests to check whether they meet the customer's requirements. The quality assurance test consists of a lot-by-lot test and a periodical test. The lot-by-lot test judges whether a lot should be accepted or rejected. It includes visual, electrical characteristics, thermal and mechanical environment, and maximum rating tests. The periodical test checks reliability by sampling at a regular interval. It includes electrical characteristics, thermal, mechanical, and operating life tests. The test results are immediately fed back to relevant departments to improve quality. They are also used to estimate the reliability in field use.

The quality information from the purchasing of materials and parts for production, inspection, shipping, and field use is controlled using the quality management system.

The information is sent to the host computer where it is analyzed using statistical quality control methods. The result of analysis is fed back to the Manufacturing/Engineering Departments and other departments to maintain and improve quality levels and increased yields.

If a failure occurs during the production process or in the product itself, a failure information sheet is issued. Then relevant departments investigate the cause of failure and take corrective actions. Figure 1.3 is a flowchart of a corrective action.

When the design, materials and parts, production methods, equipment, and such can be changed, prototype is made to check for quality levels and evaluate the reliability. If no problem is detected, the change will be implemented after the customer gives their approval.

Quality control audits are performed by key members regularly of all departments such as Design and Engineering, Quality Assurance Department, Manufacturing, Sales, and Administration, Supplies regularly. They enable problems to be identified and corrected. They also increase awareness of quality control at the departmental level. The result is a more comprehensive quality control system.

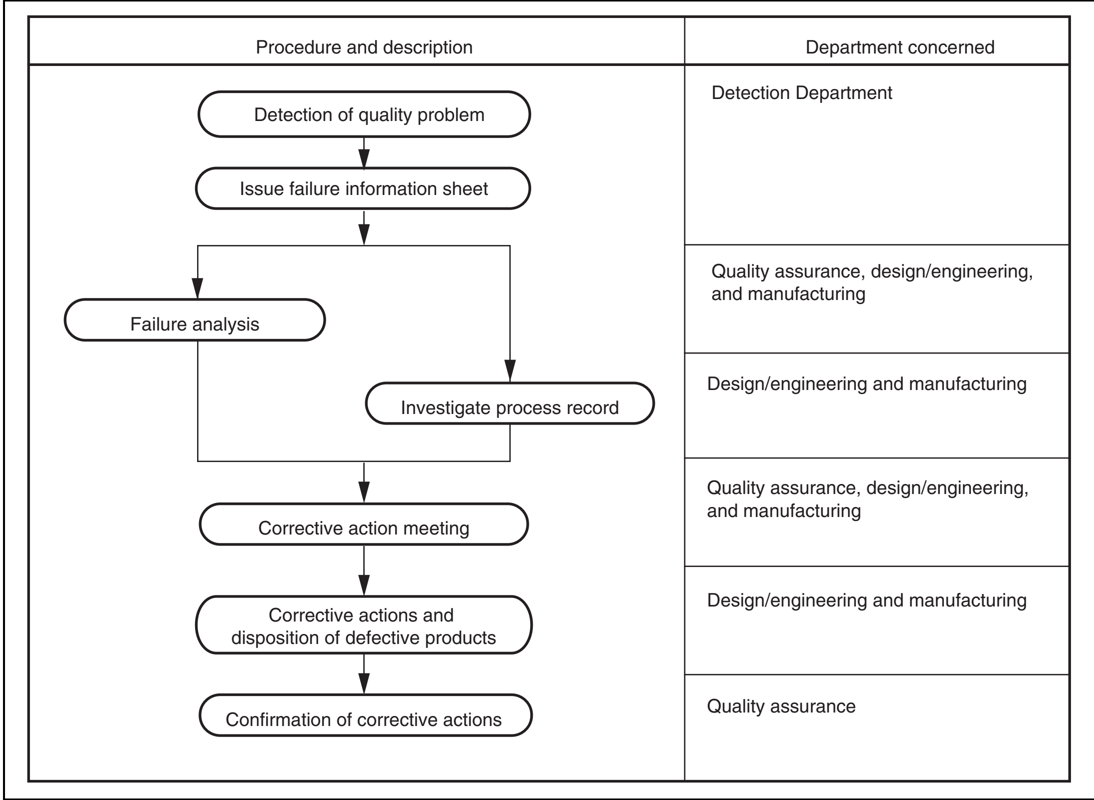

Figure 1.3 Flowchart of a Corrective Action

RENESAS

1.5 Change Control

We have adjusted and continue to optimize our manufacturing equipment and processes for stability against external factors. To minimize the risks from changes we have set up and are operating the change management system shown in figure 1.4. This system manages not only changes involving manufacturing equipment, manufacturing conditions, and manufacturing sites, but also changes at the detail level. If a change could affect either product quality or characteristics, we will inform our customers and make the change only after receiving their approval.

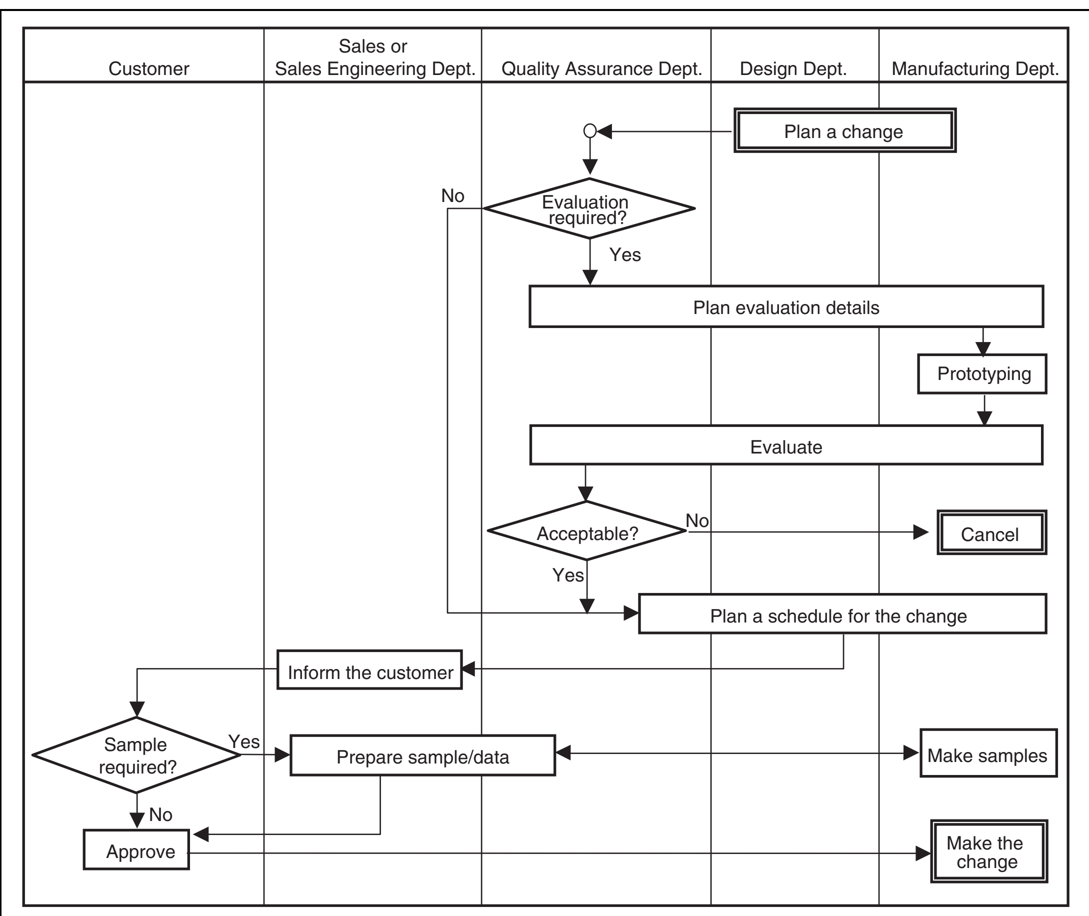

Figure 1.4 Semiconductor Device Change Management System

1.6 Product Identification and Traceability

Dates of manufacture are indicated on all Renesas products so that the manufacturing history can be confirmed and products can be identified. Also, manufacturing lot codes are given to the products so that the manufacturing history can be traced. A representation of a Renesas manufacturing lot code is given below. However, please note that restrictions on package dimensions and/or other factors may lead to some codes being omitted or displayed in different ways.

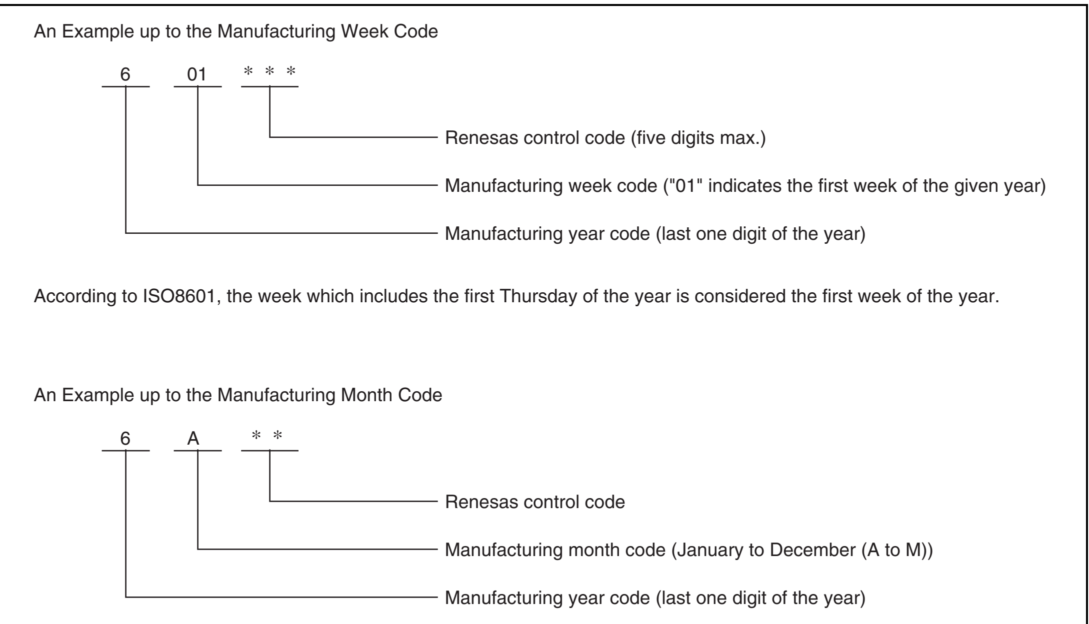

Figure 1.5 Examples up to the Manufacturing Week/Month Codes

Lot Traceability Management System

Renesas Technology has configured and been facilitating the system illustrated below; this allows the speedy and steady tracing of lot records as required.

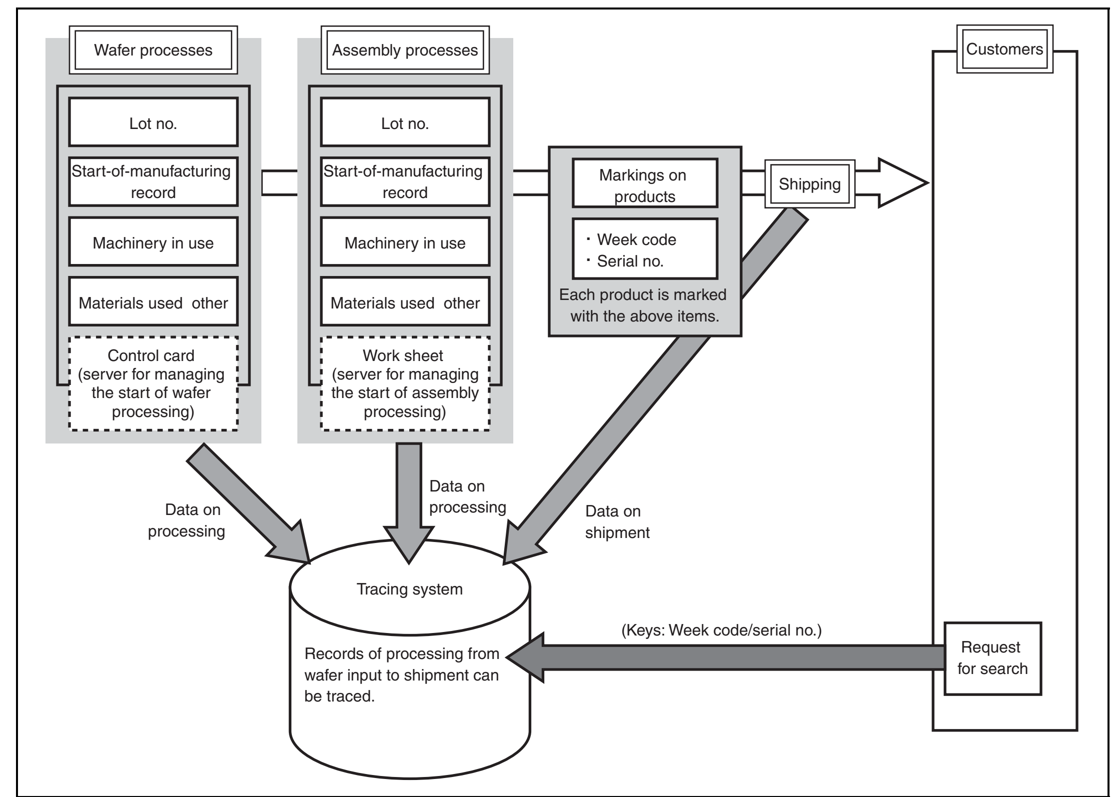

Figure 1.6 Lot Traceability Management System

1.7 Failure After Shipping and Corrective Actions

When a failure is found at the acceptance inspection, assembly, or in field use at the customer, the Quality Assurance Department plays the major role in identifying the cause of failure and implementing corrective actions. Based on the analysis request issued by the Sales Department, the Quality Assurance Department investigates the failure and analyzes it using various testing equipment and analysis methods.

Based on the analysis result, Design and Engineering, Manufacturing, and other related departments hold a meeting. Then corrective action is taken as required, and a report is issued to the customer. Figure 1.7 shows the flowchart of returned product control.

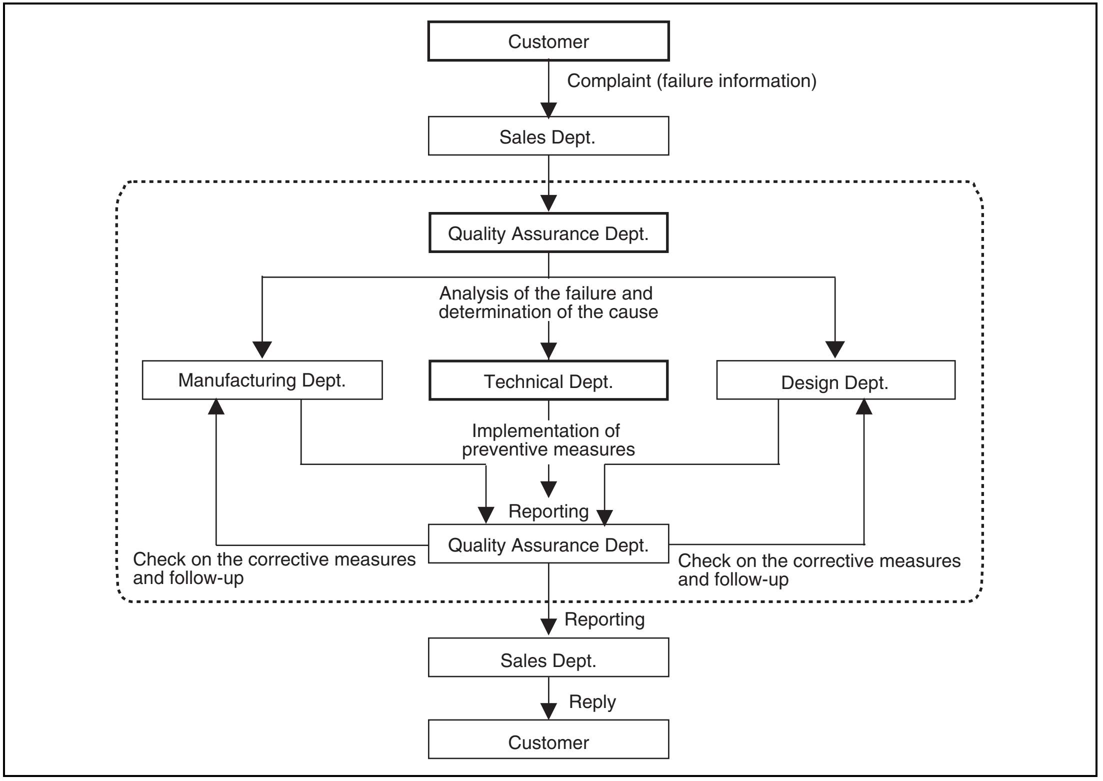

Figure 1.7 Flowchart of Complaint Handling and Corrective Measures

1.8 Quality Assurance for Materials And Parts

As the performance, degree of integration, and assembly density of semiconductor devices increase, the requirements for the purity of materials and precision of parts become severer. Semiconductor chips are manufactured from various materials (e.g. silicon wafers, compound semiconductor wafers, target materials, photo-resists, process chemicals, gases, and D.I. water) and assembly/packaging materials and parts (e.g. leadframes, metal wires, die bonding materials, substrates, and resins). Each material or part requires the highest levels of specifications and quality.

When developing a new semiconductor device, Renesas compiles purchase specifications and drawings for each material and part, then purchases them from specialty suppliers. We assure and improve the quality of material and parts by:

- Careful selection of materials and parts, and joint development with specialty suppliers to meet purchase specifications
- Quality audits of suppliers' factories, and approval of suppliers and factories
- Qualification tests and evaluation of each material or part type
- Acceptance inspection or conclusion of a ship to stock agreement with suppliers
- Prevention of degradation caused by storage and handling of materials and parts
- Collection of quality data for materials and parts, and control of abnormalities
- Change control for materials and parts
- Regular quality assurance surveys on suppliers, and quality meetings with them

Figure 1.8 shows the relationship between these activities.

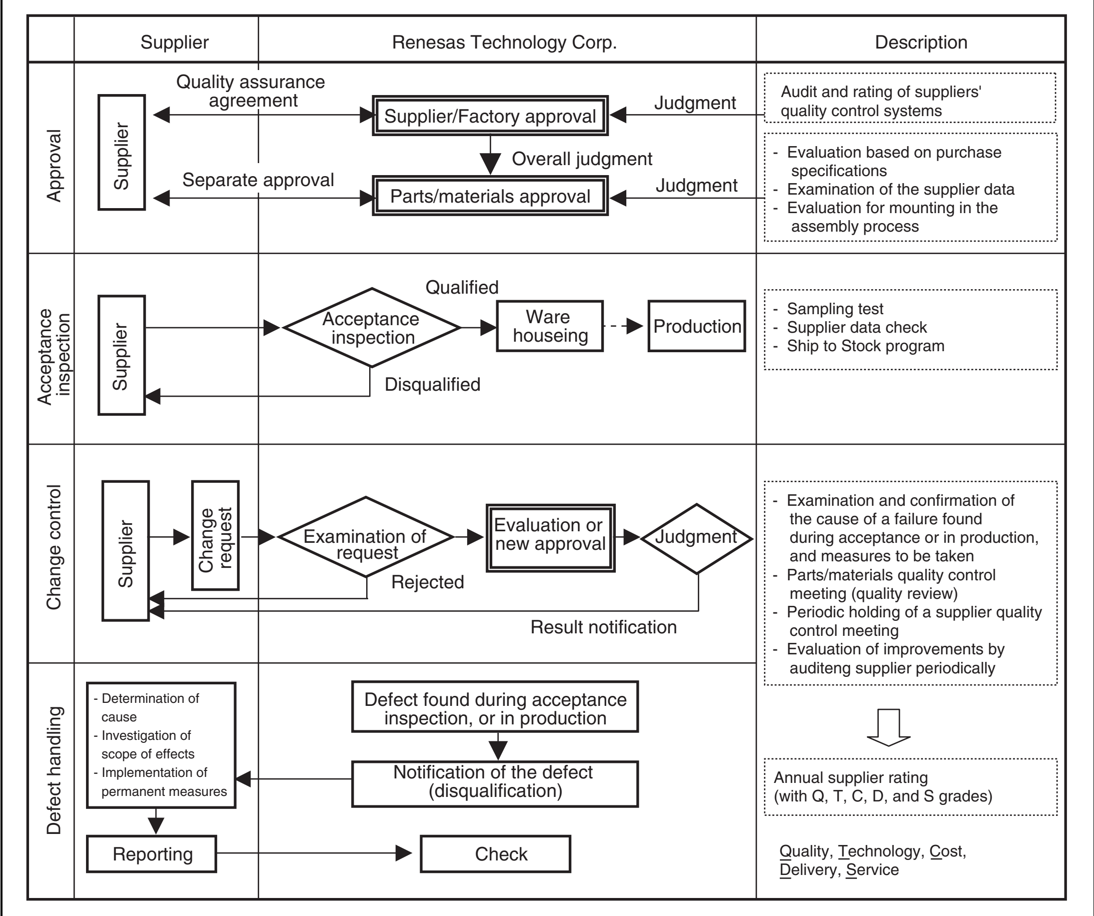

Figure 1.8 Quality Assurance Flowchart for Parts and Materials

RENESAS

1.9 Environmentally-Friendly Design

Based on ISO14001, Renesas Technology has built the Environmental Management System (EMS) and contributed to the environmental safety as a whole. Please see Environmental/RoHS Activity on the following Renesas Web site for details.

http://eu.renesas.com/fmwk.jsp?cnt=/env_category_landing.jsp&fp=/support/environmental_activity/&site=i

Semiconductor production processes use a lot of energy and chemicals and discharge a considerable amount of waste. The resulting impact on the environment from semiconductor production is not small.

In Europe, demand has been growing to reduce the environmental impact of products by, for example, strengthening the regulations on the chemical materials contained in electrical and electronic products. Against this background, our customers and society in general have increased their demands for products less harmful to the environment by, among other things, a reduction in the amount of chemicals contained in semiconductors and electronic parts.

To meet such demands, we commit to continuously: (1) reduce environmental stress in production by conserving energy and reducing wastes (eco-factory), (2) reduce the environmental impact of products (eco-products), and (3) strengthen our environmental management system and build an environmentally aware business foundation from which to educate employees about the environment (eco-management). Figure 1.9 shows our basic approach to developing and providing environment-friendly products.

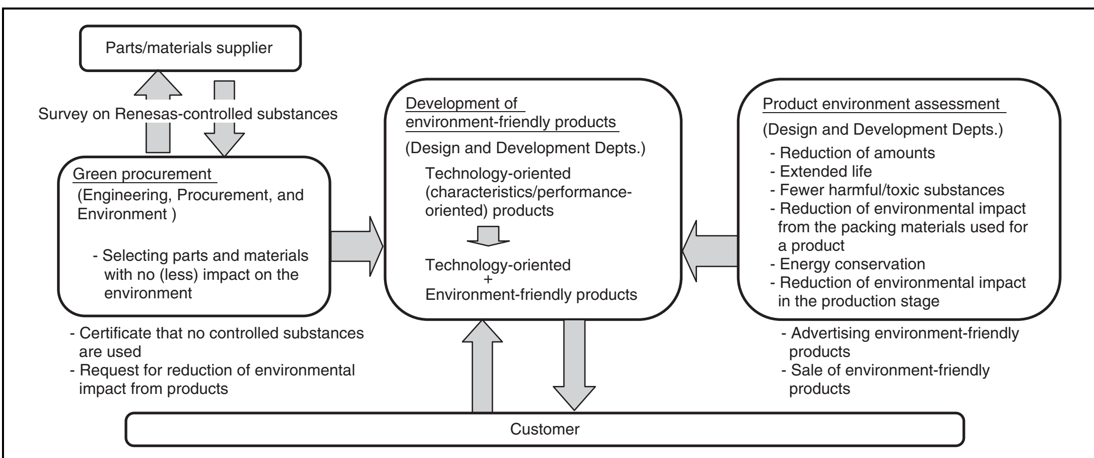

Figure 1.9 Development and Procurement of Environment-Friendly Products

1.9.1 Expansion of Green Procurement

Green procurement is an activity for controlling the chemical and toxic substances contained in products supplied to customers by managing them at the root of supply chains. More precisely, green procurement is a procedure for investigating the levels of chemical substances contained in purchased parts and materials and for examining our suppliers' environmental management systems. Figure 1.10 shows the green procurement flowchart.

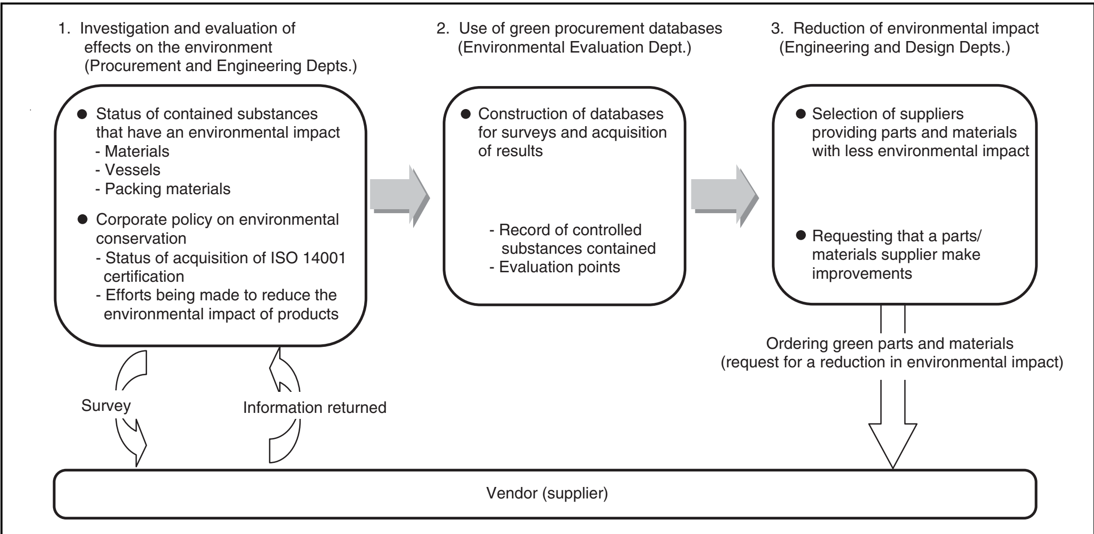

Figure 1.10 Green Procurement Flowchart

1.9.2 Reduction of Environmental Impact in the New Product Development Stage (Product Environment Assessment)

The product environmental assessment is a technique designed to provide a preliminary evaluation of the environmental aspects requiring consideration over the life cycle of a product. Included in the assessment at the time of development are the processing of materials, production, distribution, use, and collection and disposal. Specifically, the assessment is a way to understand how much improvement has been made regarding environmental impact by comparing the environmental impact of a new product with that of the previous-generation product. Figure 1.11 shows the items covered by the assessment.

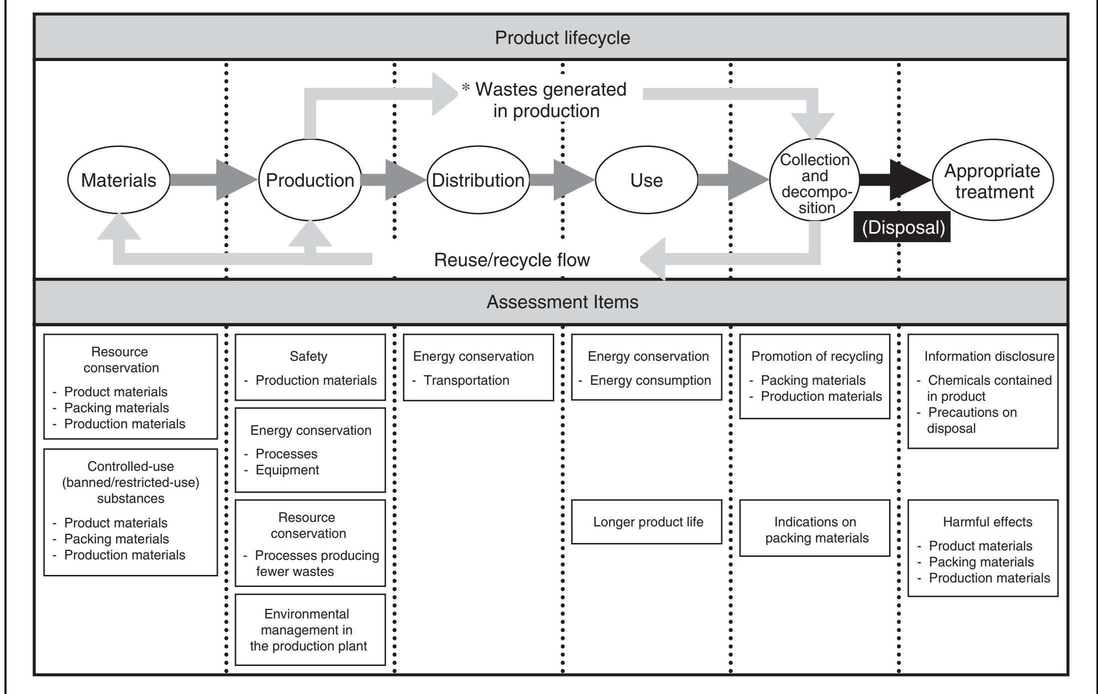

Figure 1.11 Product Assessment Items (Considerations Related to the Environment)

1.9.3 Management of Chemical Substances

For about 1000 types (classes) of chemical substances that might be contained in semiconductor products or used in production, we have defined specific management categories and have been managing the amounts of each substance consumed and transferred. In our chemical substance management system, about 200 types (classes) of chemical substances are classified as banned substances, about 160 types (classes) are classified as substances to be reduced, and about 560 types (classes) are classified as controlled substances. Of these types, all banned substances were abolished by the end of 2005. In the green procurement activities described above, the chemical substances that are to be managed have also been surveyed.

Renesas regards the chemical substances contained in its products as a critical quality concern, and is organizing a quality assurance system to address this concern.

Section 2 Reliability

This section describes the properties of semiconductor devices from the reliability perspective, and the criteria to express reliability quantitatively. Following are accounts of models of electronic parts failures and an account of "acceleration coefficients" computation methods. The last part of this section describes the statistical methods used for reliability analysis.

2.1 Failure rate function

The reliability of semiconductor devices is represented by the failure rate curve (called the "bathtub curve"), which is illustrated in figure 2.1. The curve can be divided into the three following regions: (1) initial failures, which occur within a relatively short time after a device starts to be used, (2) random failures, which occur over a long period of time, and (3) wear-out failures, which increase as the device nears the end of its life.

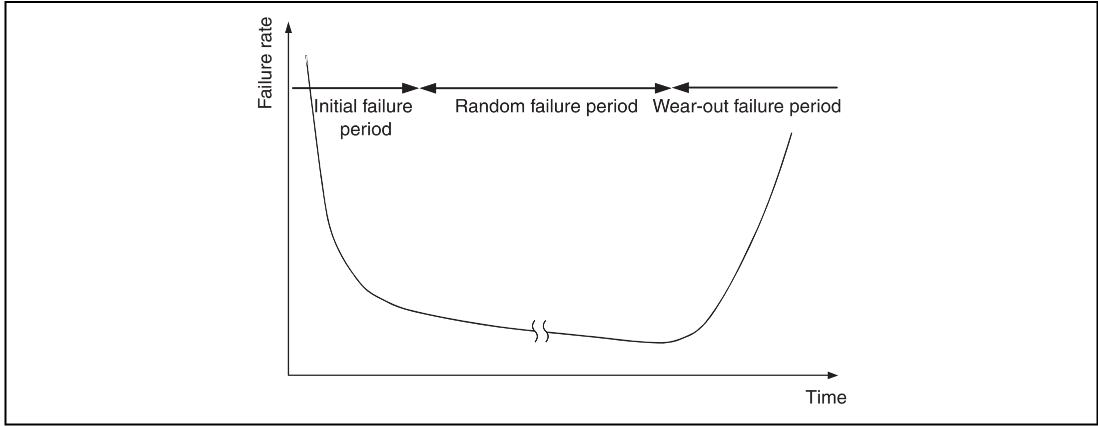

Figure 2.1 Failure Rate Curve (Bathtub Curve)

"Initial failures" are considered to occur when a latent defect is formed, for example, during the device production process and then becomes manifest under the stress of operation. For example, a defect can be formed by having tiny particles in a chip in the production process, resulting in a device failure later. The failure rate tends to decrease with time because only devices having latent defects will fail, and these devices are gradually removed.

"Random failures" occur once devices having latent defects have already failed and been removed. In this period, the remaining high-quality devices operate stably. The failures that occur during this period can usually be attributed to randomly occurring excessive stress, such as power surges,

and software errors. This group also includes devices susceptible to remains of initial failures (long-life failures).

"Wear-out failures" occur due to the aging of devices from wear and fatigue. The failure rate tends to increase rapidly in this period. Semiconductor devices are therefore designed so that wear-out failures will not occur during their guaranteed lifetime.

Accordingly, for the production of highly reliable semiconductor devices, it is important to reduce the initial failure rate to ensure the long life, or durability against wear-out failures.

To reduce the initial failure rate and thereby improve reliability, Renesas has implemented advanced quality controls and quality improvement activities as well as screening procedures, including electrical characteristics testing and burn-in tests. Furthermore, to provide the necessary product durability for the service life of products, the company has been building in reliability starting with the design and development stages. In addition, it carries out reliability design, design review, and other activities to ensure reliability, and also conducts reliability testing.

2.2 Dependencies of failure rate function

As shown in figure 2.2, the ideas discussed in the previous subsection can be illustrated if they are expressed in terms of the changes that occur with device failures. In figure 2.2, individual semiconductors are represented as sets (circles). At the start of device operation, there may be semiconductors with latent defects included in the set. These will fail under operating stress, and as they fail, they are removed from the set based on the definition of the failure rate. The initial failure period can therefore be defined as the period during which devices having latent defects fail. The failure rate can be defined as a decreasing function, since the number of devices having latent defects decreases as they are removed.

In the next several years, devices with latent defects are removed and the reliability goes up. Although there are no more failures resulting from latent defects in this period, semiconductors can still fail due to some excessive external stress. This period is considered as the period of random failures, and the failure rate accordingly becomes random (the failure rate is constant).

Finally, the basic device structure wears out due to stress over a period of several tens of years, and devices fail due to their age. All semiconductors have approximately the same lifetime, which means that the failure rate can be represented as an increasing function. As this discussion should make clear, initial failures and wear-out failures have different causes, even though they appear to be the same. A means of illustrating the causes of failure is the bathtub curve, shown in figure 2.3.

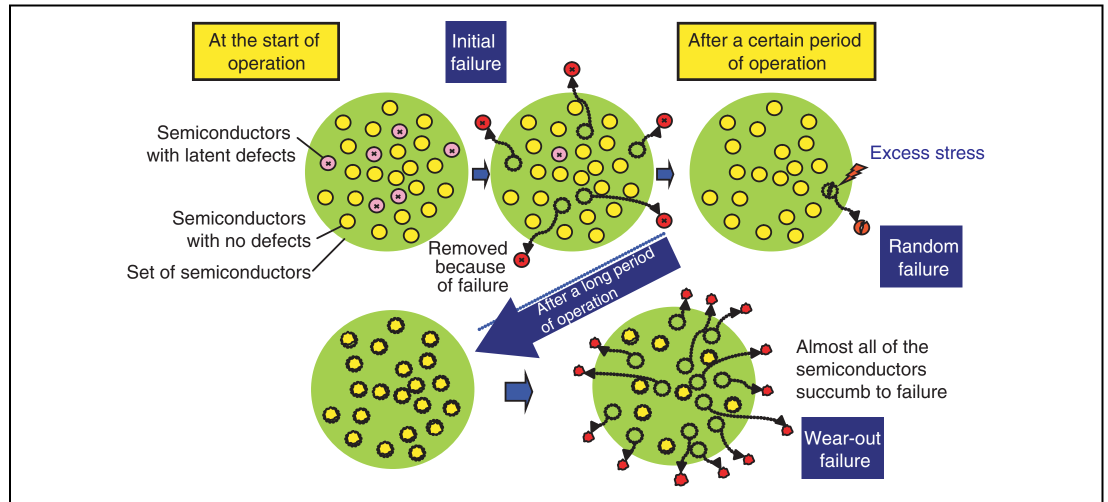

Figure 2.2 Image Showing Changes in the Semiconductor Failure Rate Results in a Bathtub Curve

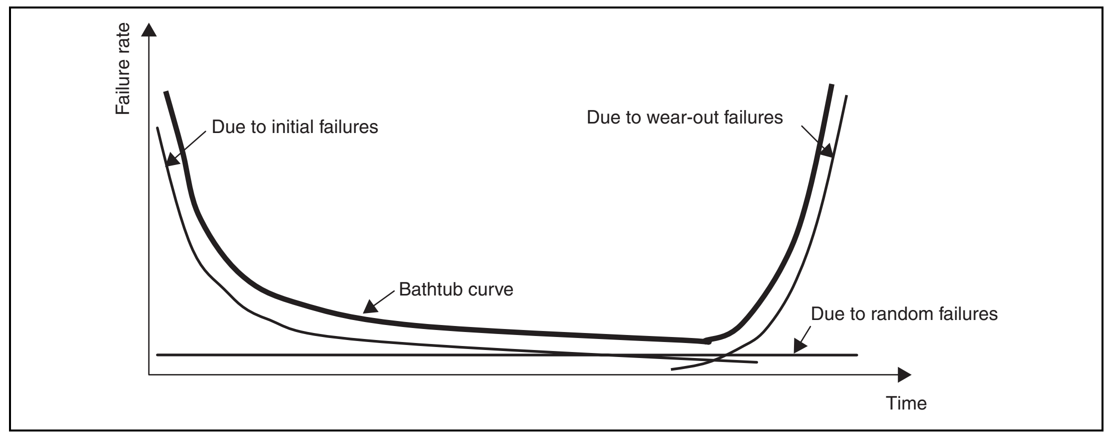

Figure 2.3 Factors Creating the Bathtub Curve

2.2.1 Initial Failures

In the production process, semiconductor devices probabilistically contain defects due to the presence of tiny particles, as well as variations in manufacturing equipment and variations in dimensions. This fact is known as the initial defect density. Products with the desired characteristics and reliability in the classification and inspection processes are classified and obtained within the range of variations and distinguished between good and bad ones. The rate of good products obtained is called as the yield. Products with a higher yield have a lower defect density, while products with a lower yield have a higher defect density. Generally, the period of initial failures is defined as the first six months to one year of a product life cycle. To reduce the failure rate in this period, semiconductor manufacturers are attempting to improve quality by introducing a screening process that can include stress, burn-in, and other types of tests. Since the failure rate in the initial failure period decreases with time, once the products with defects are screened out, only the products with low failure probability are left (See figure 2.2), which allows manufactures to bring high-quality products to the market. However, because the screening process itself entails a trade-off between quality and cost, it is desirable to set screening conditions by considering the usage of products and the quality requirements. Screening is nevertheless an after-the-fact measure for products that have already been manufactured. If you take such measures as reducing the defect rate initially incorporated in the production stage and designing a layout that helps to prevent defects, you can achieve stable quality from a reduction of initial defects as well as obtaining a higher yield (more efficient production). Note that, in the initial failure period, the Weibull distribution has a shape parameter (m) smaller than 1.

2.2.2 Random Failures

Failures resulting from production defects will attenuate with time. Even though initial failures are screened out, products having minor defects will still remain. Strictly speaking, therefore, the region of random failures can be considered to be an extension to the region of attenuation-type initial failures.

The mode in which the failure rate is constant (exponential function) in the true sense covers soft errors, electrical noise, electrostatic discharge, and other problems. All of these problems will occur at random under the stress of external factors. Accordingly, the magnitude of durability can be determined from the specifications used in the design stage. Note that, in the random failure period, the Weibull distribution has a shape parameter (m) approximately equal to 1. The failure rate function therefore approximates an exponential distribution.

2.2.3 Wear-out Failures

Semiconductors fail when they reach the limits of their basic durability. This period is called the region of wear-out failures, and indicates the life of different failure modes of semiconductors, such as HC, EM, and TDDB. Generally, in the design stage semiconductors are designed to last for dozens to hundreds of years against wear-out in the actual working environment, and in the process development stage they are further refined for higher quality and reliability. In the wear-out failure period, where it is necessary to monitor the life span, the Weibull distribution has a shape parameter (m) larger than 1.

2.3 Screening

Generally, semiconductor devices have a high initial failure rate immediately after they are manufactured. Thereafter, the failure rate begins to decrease. Given the above reliability considerations, Renesas sets reliability goals (initial failure rate (ppm/year or FIT)) based on the customer's quality needs and intended use of the product. Devices whose failure rate exceeds the set values undergo screening so that the target values can be achieved.

Initial failures can be screened by high voltage stress tests at wafer probing or by burn-in tests under high voltage and temperature on the finished products. A combination of screening and methods for improving yield in the production process is required to improve initial quality.

Because it is important to identify the failure rate of the target device in advance, screening conditions are usually set as follows. First, when a new process or product is developed, burn-in tests are repeated for a period ranging from several hours to several tens of hours on TEGs or on products numbering from several thousands to several tens of thousands. Next, the obtained results are plotted on Weibull probability paper for each failure mode. The initial failure rate can then be identified and the conditions set. The reliability target for initial failures is defined either by the annual average failure rate measured under practical operating conditions after product shipment or by the cumulative failure rate. The burn-in acceleration (temperature and voltage) needs to be determined to compare the transition of failure rate obtained from the burn-in saturation test and the reliability target.

Because acceleration differs depending on the failure mode, defects by analyzing products that become faulty during the assessment of burn-in repetitions must also be categorized. The failures that usually occur are likely to be poor functioning and leak problems resulting from gate oxide film leaks and metallic particles. The voltage acceleration parameter (β), which is the electric field (voltage) intensity coefficient (cm/MV), is determined from the electric-field-dependent data obtained from the single MOS transistor and TEG assessment. When the activation energy (Ea) known for each category of the failure mode is used, the acceleration rate from the equation can be calculated.

$$AF_V = \exp(Ea \mid kT) \times 10^{(-\beta \cdot Vox)}$$

In many cases, burn-in repetition assessment is performed during the development of a new process.

One of its advantages is that the failure rate in new products can be calculated from the same process by normalizing the chip area, gate count, transistor density, and other factors. Another advantage is that data flexibility is high, since, for example, it is relatively easy to provide feedback for the development of next-generation products.

The voltage and temperature conditions can be set by considering usage conditions and the reliability target regarding the acceleration conditions in burn-in tests.

For voltage conditions, set an assessment voltage that is equal to, or smaller than, the breakdown voltage for MOS dielectric films or joints and perform TDDB assessment under at least three voltage conditions with a target minimum value of +1 MV/cm against $V_{cc\ max}$, an operating voltage Plot the result on Weibull probability paper to be able to read the time for the breakdown voltage at the target failure rate value. There is also a method by which you can determine the electric field (voltage) strength coefficient (gradient: β) by examining the correlation between the electric field (voltage) and each of the obtained values for the breakdown time.

For temperature conditions, the activation energy by examining the dependence of oxide-film breakdown on the ambient (junction) temperature can be determined. Generally, the activation energy of TDDB is considered to be from 0.5 to 0.8 eV. Variations in this activation energy are related to the dependence on the operating voltage (electric field). When the voltage (electric field) is small, the energy tends to be large and vice versa.

Based on the values of voltage (β) and temperature dependence (Ea), burn-in tests should be conducted, and the burn-in time conditions that provide optimum quality should be determined. Recent advances in development of AC/DC stress tests in the earlier stages of process have allowed to reduce and sometimes made obsolete the burn-in of finished products.

2.4 Forecasting Lifetime

If screening is conducted for a certain length of time (t_0) before product shipment, the lifetime of the product (its life measured since t_0 which is the origin) can be forecasted by the probability density function (PDF) f(t0;t) where t0 is the screening time (see figure 2.4):

$$f(t_0 : t) = \frac{f(t_0 + t)}{R(t_0)} \qquad (2\text{-}1)$$

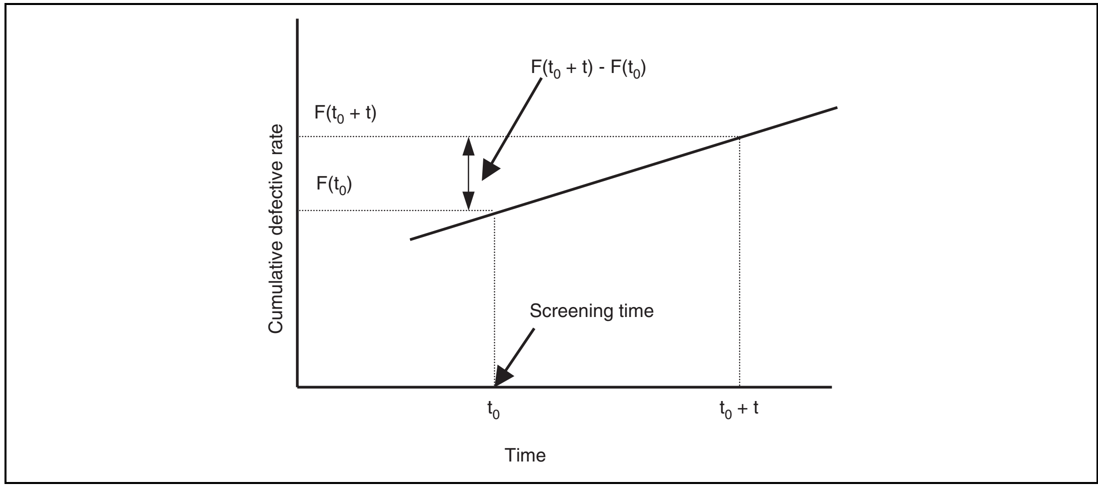

Figure 2.4 Estimating Device Lifetime

Here, R (t_0) indicates the accumulated reliability function available until time (t_0).

If the probability density function f (t_0) indicates the Weibull distribution, the following equation can be used:

$$f(t_0) = \frac{m t_0^{m-1}}{\eta^m} e^{-\frac{t^m}{\eta}} \qquad (2\text{-}2)$$

When Equation (2-2) is substituted into Equation (2-1), the probability density function becomes:

$$f(t_0 : t) = \frac{m(t_0 + t)^{m-1}}{\eta^m} \bullet \exp\left(-\frac{(t_0 + t)^m - t_0{}^m}{\eta^m}\right) \qquad (2\text{-}3)$$

Therefore, the rate of accumulated failures (t: t_0) available after screening becomes:

$$F(t_0 : t) = 1 - \exp\left(-\frac{(t_0 + t)^m - t_0{}^m}{\eta^m}\right) \qquad (2\text{-}4)$$

Equation (2-4) therefore makes it possible to estimate the product lifetime.

A note of warning, however, is necessary. Excessive screening will result in MOS destruction or consume some of the product's life. Accordingly, you must set screening conditions that are appropriate in consideration of the product's life.

2.5 Properties of Semiconductor Reliability

Reliability of semiconductor devices can be summarized as follows:

1. Semiconductor devices (figure 2.5) have a configuration, which is fundamentally very sensitive to impurities and particles, and the stability status of the surface state is extremely important. Consequently, to manufacture these devices it is necessary to manage many processes while completely controlling the level of impurities and particles. Furthermore, the quality of the finished product depends upon the complex relationship of each interacting substance in the semiconductor, including chip material, metallization and package.
2. The problems of thin films and micro-processes must be fully understood as they apply to metallization and bonding. It is also necessary to analyze surface phenomena from the aspect of thin films.

3. Due to the rapid advances in technology, many new products are developed using new processes and materials, and there is a high demand for product development in a short time period. Consequently, it is not possible to refer to the reliability achievements of existing devices.
4. In greed, semiconductor products are manufactured in high in volume. In addition, repair of finished semiconductor products is impractical. Therefore incorporation of reliability at the design stage and reduction of variation in the production stage have become essential.
5. Reliability of semiconductor devices may depend on assembly, use, and environmental conditions. Stress factors effecting device reliability include voltage, current density, temperature, humidity, gas, dust, contamination, mechanical stress, vibration, shock, radiation, and intensity of electrical and magnetic fields.

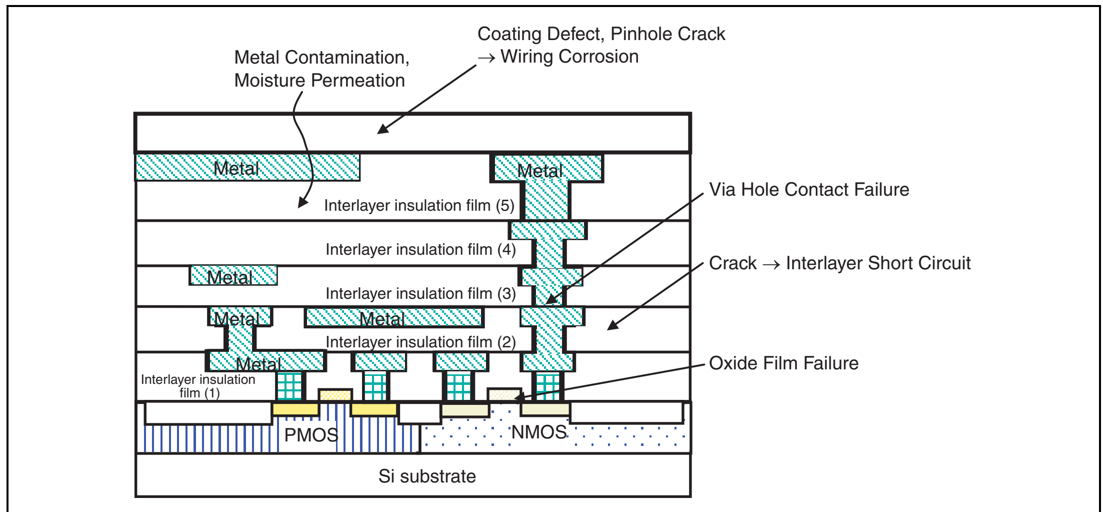

Figure 2.5 Semiconductor Device Cross-Section

In recent years high-level functions, systemization, and large scale integration have advanced rapidly, therefore ensuring reliability has become extremely important. Reliability is usually expressed as the "Failure Rate."

Generally, the failure rate of electronic parts and devices, including semiconductor devices, follow the 'bathtub' curve as shown in figure 2.1. The manner in which failures occur can be divided into three periods, i. e.–an initial failure period, a random failure period and a wearout failure period.

Failures during the "initial failure period" most commonly result from deficiencies in production. During this period the failure rate falls with time and finally becomes stable. The "random failure period" is the useful lifetime of semiconductor devices and the failure rate in this period is generally constant. The "wearout failure period" (aging period) is a period of concentrated incidence of failures of specific defects coinciding with the end of the component life. The semiconductor component will not exhibit wearout failures in its predefined lifetime if environmental stresses in the field use do not exceed those of the intended application profile.

Almost all semiconductor devices with latent defects, which may fail in the initial failure period, can be screened out by using a testing method such as a burn-in test.

2.6 Reliability Criteria

Reliability is defined by JIS Z 8115 "Reliability Terms" as;

"The features that enable the accomplishment of specified functions of an item under given conditions for a specific period of time." In this definition, reliability includes the concept of time. Therefore, the concept of reliability has to be differentiated from the concept of initial product quality which does not include the time parameter. But in practice reliability is often expressed as the fraction defective irrespective of time during this "initial failure period."

2.6.1 Initial Failure Period Criteria

In the initial failure period, measurement of defect rate or failure rate against the total number of tested components, irrespective of the time parameter, is generally expressed by (%) or ppm. Where ppm is the abbreviation for "parts per million," 1 ppm means one defective component out of 1,000,000 semiconductor devices. Therefore, if the fraction defective is 100 ppm then there are 100 defective components out of 1,000,0000 or 1 component out of 10,000.

2.6.2 Random Failure Period Criteria

In the random failure period it is necessary to consider the time parameter. The following criteria are used:

- Reliability Function
- Unreliability Function
- Probability Density Function
- Conditional Failure Rate Function (Failure Rate Function)

These criteria are related. In particular the unit of FIT (Failure in Time) is widely used.

(1) Reliability Function and Unreliability Function

The Reliability Function is the proportion of components (devices, parts and elements) which continue to perform their designed functions and remain stable after time (*t*). This can be expressed by the equation:

$$R(t) = (n - c(t))/n \qquad (2\text{-}5)$$

where $R(t)$ = Reliability function

n = The total number of tested components

$c(t)$ = The total number of failures up to time (t)

On the other hand, the complement of the Reliability Function is the Unreliability Function.

The Unreliability Function, alternatively known as the Cumulative Failure Distribution Function, is defined as the Distribution Function when the failure time is considered as the probability Function. That is the total number of failures (the cumulative number of failures) which cease to perform their designed functions after any particular device, part, or component is being used for a period of time expressed as (*t*).

This can be expressed by the equation:

$$F(t) = c(t) / n \qquad (2\text{-}6)$$

where $F(t)$ = Unreliability Function

n = The total number of tested components

$c(t)$ = The number of failures to develop up to time (t)

In addition, the following relation is true:

$$R(t) + F(t) = 1 \qquad (2\text{-}7)$$

Further, as shown in figure 2.6, the reliability function $R(t)$ is a monotonically decreasing function and the unreliability function $F(t)$ is a monotonically increasing function.

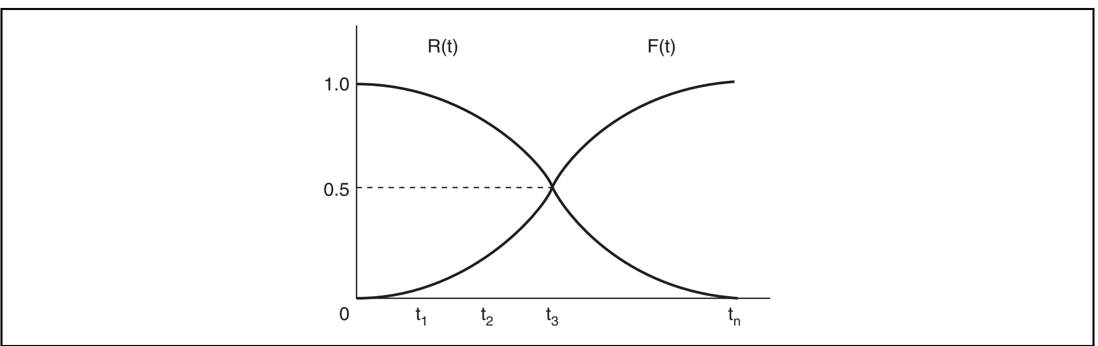

Figure 2.6 Example of *R*(*t*) and *F*(*t*)

(2) Probability Density Function

The Probability Density Function (of failures) is defined as the probability of failure of any particular device or component after being used for a period of time (t). From this definition probability density function can be expressed by the equation:

$$f(t) \equiv dF(t)/\mathrm{d}t = -dR(t)/\mathrm{d}t \qquad (2\text{-}8)$$

As can be seen from the above equation, the Reliability Function $R(t)$ and the Unreliability Function $F(t)$ can be calculated by taking the integral of the Probability Density Function, as below:

$$F(t) = \int_0^t f(t)dt \qquad (2\text{-}9)$$

$$R(t) = 1 - F(t) = 1 - \int_0^t f(t)dt = \int_t^\infty f(t)dt \qquad (2\text{-}10)$$

Figure 2.7 shows a schematic of $f(t)$, $R(t)$, $F(t)$.

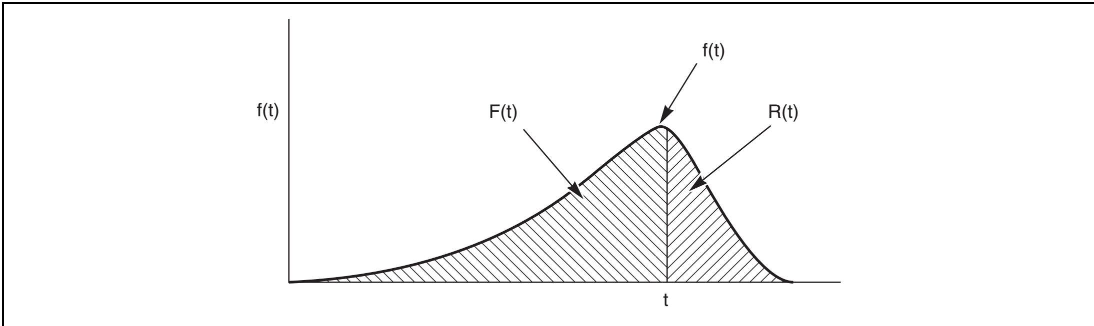

Figure 2.7 Schematic of $f(t)$, $R(t)$, $F(t)$

(3) Failure Rate Function

The Failure Rate Function (also known as "hazard function") is defined as the rate of failures, that occur per time (t) given below, out of all sample performing normally until the time (t) passes after particular device, part, or component is being used. The Failure Rate Function, $\lambda(t)$, is given by

$$\lambda(t) = f(t) / R(t) \qquad (2\text{-}11)$$

Each information that f(t),R(t), or $\lambda(t)$ possesses is equivalent. Using previously described information and by developing equations (2-8), (2-9), (2-10) and (2-11), we can calculate $R(t)$ and $f(t)$ and $\lambda(t)$.

The Failure Rate Function is also known as the Momentary Failure Rate. This is often used to express reliability of semiconductor devices and other components. Momentary Failure Rate is theoretically very accurate, but in practice it is impractical to calculate failure rate at a point of time in a short period. Therefore, one time period of 1000 hours, one month or one year, is selected and the Average Failure Rate is used.

$$\text{Average failure rate} \equiv \text{Total failures in the period} / \text{Total operating time in the period}$$

The values of average failure rates are expressed in unit of % per 1000 hours or ppm/1000 hours. The more common term Failure in Time (FIT) is widely used as a unit to express the failure rate:

$$1 \text{ FIT} = 1 \times 10^{-9} \text{ 1/h} = 1\text{ppm/1000h}$$

$$\text{Number of failures} / (\text{actual number of devices tested} \times \text{actual operation time})$$

However, if the failure rate is 100 FIT the probability of a failure developing is 1 in 10^7 of operating hours, but this does not mean that the life of an individual component is 10^7 operating hours.

It is important to understand that the total operating hours (= actual number of devices tested × actual operation time) are not obtained by focusing on one single component.

(4) Cumulative Hazard Function

The Reliability Function $R(t)$ and Failure Rate Function $\lambda(t)$ can be determined by expanding (2-11) from equation (2-8) to produce the following relation shown in equation (2-12).

$$R(t) = \exp\left[-\int_0^t \lambda(t)dt\right] \qquad (2\text{-}12)$$

Further if the cumulative hazard function $H(t)$ is defined by the expression (2-14), then

$$H(t) = \int_0^t \lambda(t)dt \qquad (2\text{-}13)$$

where $\lambda(t)$ expresses a Weibull distribution, the following relation applies.

$$R(t) = e^{-(\frac{t}{\eta})^m}$$

Therefore,

$$H(t) = (\frac{t}{\eta})^m \qquad (2\text{-}14)$$

Further

$$R(t) = \exp\,[-H(t)] \qquad (2\text{-}15)$$

This relation will be applied later to hazard analysis.

(5) Criteria to Express Lifetime

Like the failure rate, "Time to Failure" is widely used. Time to Failure is defined as the time until failure develops in components (devices, parts, and elements) from when they commence to be used.

Generally semiconductor devices cannot be repaired, maintained and reused once a component fails. Therefore, they can be referred to as non-repairable (non-maintainable) products. The average time for non-repairable components (devices, parts, elements) to fail is defined as the Mean Time to Failure (MTTF) and can be expressed by the equation:

$$MTTF = \int_0^t tf(t)dt \qquad (2\text{-}16)$$

or as the exponential distribution,

where $f(t) = \lambda \exp(-\lambda t)$

$R(t) = \exp(-\lambda t)$

$\lambda(t) = \lambda$ (constant)

then from equation (2-16) MTTF can be expressed as

$$\mathrm{MTTF} = \int_0^\infty t\lambda e^{-\lambda t} dt = 1/\lambda \qquad (2\text{-}17)$$

becoming the reciprocal of the failure rate.

References:

[1] Hiroshi Shiomi: "Introduction to Failure Physics," JUSE Press, 1982

[2] Hiroshi Shiomi: "Introduction to Reliability Engineering," Revision 3, Maruzen, 1995

[3] Hisashi Mine, Hajime Kawai: "Fundamental Mathematics of Reliability and Integrity," JUSE Press, 1984

[4] Shozo Shimada: "Reliability and Lifetime Tests," JUSE Press, 1964

Section 3 Reliability Testing and Reliability Prediction

3.1 What Is Reliability Testing

Reliability testing is a series of laboratory tests carried out under known stress conditions to evaluate the life span of a device or system.

Reliability tests are performed to ensure that semiconductor devices maintain the performance and functions throughout their life. These reliability tests aim to simulate and accelerate the stresses that the semiconductor device may encounter during all phases of its life, including mounting, aging, field installation and operation. The typical stress conditions are defined in the testing procedure described later in this document.

Reliability tests are performed at various stages of design and manufacture. The purpose and contents differ in each stage. When testing semiconductor devices, (1) the subject and purpose of each test, (2) the test conditions, and (3) the judgement based on test results must be considered. Table 3.1 shows the subject, purposes, and contents of some reliability tests carried out at our laboratories.

Table 3.1 Examples of Reliability Testing Conducted When New Products are Developed

Phase	Purpose	Name	Contents
Development of semiconductor products	To verify that the design reliability goals and the customer's reliability requirements are satisfied	Quality approval for product developed	The following and other tests are carried out as required: 1. Standard tests 2. Accelerated tests 3. Marginal tests 4. Structural analysis
Development or change of materials and processes	To verify that the materials and processes used for the product under development satisfy the design reliability goals and the customer's reliability requirements To understand the quality factors and limits that are affected by materials and processes	Quality approval for wafer process/package developed or changed	TEGs or products are used to perform acceleration tests and other analyses as required with attention paid to the characteristics and changes of materials and processes.
Pilot run before mass production	To verify that the production quality is at the specified level	Quality approval for mass production	This category covers reliability tests for examining the initial fluctuation of parameters that require special attention, as well as fluctuations and stability in the initial stage of mass production.

3.2 Reliability Test Methods

Reliability tests are performed under known stress conditions. A number of standards have been established including Japan Electronics and Information Technology Industries Association (JEITA) standards, U.S. Military (MIL) standards, International Electrotechnical Commission (IEC) standards, and Japan Industrial Standards (JIS). The testing procedures and conditions differ slightly from one another, their purpose is the same. Tables 3.2 to 3.4 list the test items, purposes, and conditions defined in the EIAJ ED-4701 "Environmental and Endurance Test Methods for Semiconductor Devices."

The test period including the number of cycles and repetitions, and test conditions are determined in the same manner as the number of samples, by the quality level of design and the quality level required by the customer. However, mounting conditions, operating periods, as well as the acceleration of tests are considered to select the most effective and cost-efficient conditions. Reliability tests must be reproducible. It is preferable to select a standardized testing method. For this reason, tests are carried out according to international or national test standards.

The definition of a device failure is important in planning reliability tests. It is necessary to clarify the characteristics of the device being tested and set failure criteria. This failure criteria must be used in determining whether or not any variations in the device characteristics before and after the test is in an allowable range.

The reliability of a device is usually determined by its design and manufacturing process. Therefore, a reliability test is conducted by taking samples from a population within the range that the factors of design and manufacturing process are the same. The sampling standard for semiconductor devices is determined by both the products reliability goal and the customer's reliability requirements to achieve the required level of lot tolerance percent defective (LTPD). The reliability tests for materials and processes are performed with the number of samples determined independently.

For newly developed processes and packages, however, there are cases in which the existing processes or packages cannot be accelerated within the maximum product rating or in which new failures cannot be detected within a short period of time. In these cases, it is important to perform reliability testing based on the failure mechanism by means of Test Element Groups (TEGs). To ensure reliability during product design, we conduct testing according to the failure mechanism in the same process as the products, clarify the acceleration performance for temperature, electric field, and other factors, and reflect this in the design rules used in designing the product.

Table 3.2 Test Categories and Conditions for Environmental Tests of Semiconductor Devices (Mechanical Tests)

<table>
<tr><th>Test Category</th><th>JEITA Standard Number</th><th>Purpose</th><th>Conditions</th><th>Related Standards</th></tr>
<tr><td>Shock</td><td>EIAJ ED-4701/400
Test method 404</td><td>To evaluate the structural and mechanical resistance to any shock the device can experience by careless handling and during transportation</td><td><table><tr><th>Con-dition</th><th>Maximum Acceleration (G)</th><th>Pulse Width (ms)</th><th>Direction and Number of Times</th></tr><tr><td>A</td><td>100</td><td>6</td><td rowspan="4">X1, (X2)
Y1, Y2
Z1, (Z2)
3 times in each direction</td></tr><tr><td>B</td><td>500</td><td>1</td></tr><tr><td>C</td><td>1000</td><td>0.5</td></tr><tr><td>D</td><td>1500</td><td>0.5</td></tr></table>Shock waveform: half-wave sine wave</td><td>IEC 68-2-27,
MIL-STD-883D
2002.3,
MIL-STD-750C
2016.2,
MIL-STD-202F
205E, 207A,
213B</td></tr>
<tr><td>Acceleration
(Steady state)</td><td>EIAJ ED-4701/400
Test method 405</td><td>To evaluate the resistance to steady state acceleration</td><td><table><tr><th>Condition</th><th>Acceleration (G)</th></tr><tr><td>A</td><td>5,000</td></tr><tr><td>B</td><td>10,000</td></tr><tr><td>C</td><td>20,000</td></tr><tr><td>D</td><td>30,000</td></tr></table>1minute each for X1, X2, Y1, Y2, Z1, and Z2 directions
(Condition 'D' is not applied for gold wire bonding devices)</td><td>IEC 68-2-7,
MIL-STD-883D
2001.2,
MIL-STD-750C
2006,
MIL-STD-202F
201A, 212A</td></tr>
<tr><td>Solderability</td><td>EIAJ ED-4701/300
Test method 303</td><td>To evaluate the solderability of leads</td><td>Leads immersed after aging<table><tr><th>Con-dition</th><th>Solder Temperature (°C)</th><th>Immersion Time (s)</th><th>Remarks</th></tr><tr><td>A</td><td>235 ± 5</td><td>5 ± 0.5</td><td>Simulating wave solder</td></tr><tr><td>B</td><td>215 ± 5</td><td>10 ± 0.5</td><td>Simulating reflow solder</td></tr></table>Using rosin-type flux
Leads are immersed up to 1 mm to 1.5 mm from the package main body.</td><td>IEC 68-2-20,
MIL-STD-883D
2003.7, 2022.2
MIL-STD-750C
2026.4,
MIL-STD-202F
208E</td></tr>
<tr><td>Resistance to soldering heat</td><td>EIAJ ED-4701/300
Test method 302
(Other than SMD)</td><td>To evaluate the resistance to the heat during soldering operation</td><td><table><tr><th>Con-dition</th><th>Solder Temperature (°C)</th><th>Immersion Time (s)</th><th>Remarks</th></tr><tr><td>A</td><td>260 ± 5</td><td>10 ± 1</td><td rowspan="2">Flux Immeresion (rosin-type)</td></tr><tr><td>B</td><td>350 ± 10</td><td>3.5 ± 0.5</td></tr></table></td><td>IEC 68-2-20,
MIL-STD-202F
210A</td></tr>
</table>

Test Category	JEITA Standard Number	Purpose	Conditions	Related Standards
Resistance to soldering heat	EIAJ ED-4701/300 Test method 301 (SMD)	To evaluate the resistance to the heat during soldering operation	Heating after humidification treatment (see below)	IEC 68-2-20, MIL-STD-202F 210A

Heating after humidification treatment

Humidification treatment condition examples

Simulating storage in moistureproof packing	85°C, 30%, 168h	
Simulating storage after opening packing	30°C, 70%, 168h	
Simulating non-moistureproof packing	A	85°C, 65%, 168 h
	B	85°C, 85%, 168 h

Heating treatment conditions

(I) Infrared ray reflow and air-reflow (lead-free solder)

Preheat: 160 to 90°C, 80 to 140s

Peak temperature (Tp) (Tolerance: +5/-0°C)

Thickness (mm)	Volume (mm^3)		
	< 350	**350 - 2,000**	**> 2,000**
< 1.6	260	260	260
1.6 – 2.5	260	250	245
> 2.5	250	245	245

Condition	Time (s) of (Tp - 5°C) or more
A	10 + 6/–0
B	20 + 6/–0

(II) Vapor phase reflow

Con-dition	Solder Temperature (°C)	Heating Time (s)	Remarks
II-A	$210 \pm^{10}_{0}$	40 ± 4	Preheat: 150°C, 90s

(III) Wave solder bath

Con-dition	Solder Temperature (°C)	Heating Time (s)	Remarks
III-A	260 ± 5	5 ± 1	Simulating single
III-B	260 ± 5	10 ± 1	Simulating double

(IV) Solder bath

Con-dition	Solder Temperature (°C)	Heating Time (s)	Remarks
IV -A	350 ± 10	3.5 ± 0.5	Flux immersion

The leads are immersed vertically up to the flat or effective soldering area.

Table 3.3 Test Categories and Conditions for Environmental Tests of Semiconductor Devices (Weather Resistance Tests)

<table>
<tr><th>Test Category</th><th>JEITA Standard Number</th><th>Purpose</th><th>Conditions</th><th>Related Standards</th></tr>
<tr><td>Soldering heat stress series test</td><td>EIAJ ED-4701/100
Test method 104</td><td>To evaluate the durability against temperature and humidity cycles a plastic mold SMD can experience during storage and mounting</td><td>The series test is performed before specified tests.

Same as
EIAJ ED-4701/300, Test method 301 (Resistance to soldering heat)</td><td>JESD22-A112,
JESD22-A113</td></tr>
<tr><td>High-temperature storage</td><td>EIAJ ED-4701/200
Test method 201</td><td>To evaluate the resistance to prolonged high temperature storage.</td><td>The device is stored in the following conditions unless other wise specified.
• Tstg max (maximum rated storage temperature)
• 1,000 h</td><td>IEC 68-2-2,
MIL-STD-750C 1031.4,
MIL-STD-883D 1008.2</td></tr>
<tr><td>Low-temperature storage</td><td>EIAJ ED-4701/200
Test method 202</td><td>To evaluate the resistance to low-temperature storage</td><td>The device is stored in the following conditions unless other wise specified.
• Tstg min (minimum rated storage temperature)
• 1,000 h</td><td>IEC 68-2-1</td></tr>
<tr><td>High-temperature high-humidity storage</td><td>EIAJ ED-4701/100
Test method 103</td><td>To evaluate the resistance to high-temperature and humidity storage and operation</td><td><table><tr><th>Test condition</th><th>Ta (°C)</th><th>RH (%)</th></tr><tr><td>A</td><td>40 ± 2</td><td>90 ± 5</td></tr><tr><td>B</td><td>60 ± 2</td><td>90 ± 5</td></tr><tr><td>C</td><td>85 ± 2</td><td>85 ± 5</td></tr></table>1,000h (unless otherwise specified)</td><td>IEC 68-2-3,
MIL-STD-202F 103B</td></tr>
<tr><td>High-temperature high-humidity bias
(THB)</td><td>EIAJ ED-4701/100
Test method 102</td><td>To evaluate the corrosive resistance (of mainly wiring) to high-temperature and humidity storage and operation</td><td><table><tr><th>Condition symbol</th><th>Temperature (°C)</th><th>Humidity (%)</th><th>Time (h)</th></tr><tr><td>A</td><td>40</td><td>90</td><td>1000</td></tr><tr><td>B</td><td>60</td><td>90</td><td>1000</td></tr><tr><td>C</td><td>85</td><td>85</td><td>1000</td></tr></table>Power supply: Continuous, or intermittent (with a specified cycle) for high power dissipation devices
For SMDs, Moisture soaking and soldering heat stress series test (test method B-101) is performed as a preconditioning.</td><td></td></tr>
</table>

Note: Shaded conditions are usually applied.

<table>
<thead>
<tr><th>Test Category</th><th>JEITA Standard Number</th><th>Purpose</th><th>Conditions</th><th>Related Standards</th></tr>
</thead>
<tbody>
<tr>
<td>Unsaturated pressurized vapor</td>
<td>EIAJ ED-4701/100
Test method 102</td>
<td>To evaluate with acceleration the resistance to storage and use in high-temperature and humidity</td>
<td>Unsaturated pressure inside chamber
<table>
<tr><th>Con-dition</th><th>Tempe-rature</th><th>Relative Humidity</th><th>Vapor Pressure (Pa)</th></tr>
<tr><td>A</td><td>110°C</td><td>85%</td><td>1.2×10^5</td></tr>
<tr><td>B</td><td>120°C</td><td>85%</td><td>1.7×10^5</td></tr>
<tr><td>C</td><td>130°C</td><td>85%</td><td>2.3×10^5</td></tr>
</table>
For SMDs, moisture soaking and soldering heat stress series test (test method 104) is performed as a preconditioning.</td>
<td></td>
</tr>
<tr>
<td>Temperature cycle</td>
<td>EIAJ ED-4701/100
Test method 105</td>
<td>To evaluate the resistance to sudden changes in temperature the device can experience during storage, transportation, or in use.</td>
<td>For SMDs, Test method 104 is performed as a preconditioning.
Maximum storage temperature (Tstg max)
Normal temperature (T_N)
Minimum storage temperature (Tstg min)
t t Step a b c d Cycle1
t: The longer one out of 5minutes, or 10% of either step a or step c.
<table>
<tr><th>Step</th><th>Temperature</th><th>Time</th></tr>
<tr><td>a</td><td>Minimum storage temperature (Tstg min)</td><td>Select a condition from the table below</td></tr>
<tr><td>b</td><td>Normal temperature 5 to 35°C (T_N)</td><td></td></tr>
<tr><td>c</td><td>Maximum storage temperature (Tstg max)</td><td></td></tr>
<tr><td>d</td><td>Normal temperature 5 to 35°C (T_N)</td><td></td></tr>
</table>
Dwell time of temperature cycle
<table>
<tr><th rowspan="2">Mass of the sample (m) g</th><th>Step b</th><th>Step a</th></tr>
<tr><th>Step d</th><th>Step c</th></tr>
<tr><td>m ≤ 15
15 < m ≤ 150
150 < m ≤ 1500</td><td>5 minutes or shorter</td><td>10 minutes or longer</td></tr>
<tr><td>1500 < m</td><td colspan="2">Specified in the individual specifications</td></tr>
</table>
Tstg min and Tstg max are defined by the individual specifications. 10 cycles are performed for evaluating.</td>
<td>IEC 68-2-14,
MIL-STD-883D 1010.7,
MIL-STD-750C 1051.2,
MIL-STD-202F 102A</td>
</tr>
</tbody>
</table>

Note: Shaded conditions are usually applied.

Table 3.4 Test Categories and Conditions for Environmental Tests of Semiconductor Devices (Other Tests)

Test Category	JEITA Standard Number	Purpose	Conditions	Related Standards
Human body model electrostatic discharge. (HBM/ESD)	EIAJ ED-4701/300 Test method 304	To evaluate the resistance to static electricity that can be generated in handling	R_1, R_2 =1.5 kΩ, S_1, V, C = 100 pF, Test sample V: Specified DC voltage (both polarities) Ta: 25°C Times applied: 3 Terminals applied to: All terminals except the reference one (MM/ESD: Reference test) C = 200 pF R2 = 0 Ω Times applied: 1	MIL-STD-883C 3015.6, JESD22-A114
Charged device model electrostatic discharge. (CDM/ESD)	EIAJ ED-4701/300 Test method 305	To evaluate the resistance to electrostatic discharges in a charging model that simulates the handling before the device is mounted	Test circuit (a) Discharging with a switch Metal discharge bar, Electrode, Switch s, Sample device, Terminal, Insulating sheet, Metal plate (b) Discharging by contact Metal discharge bar, Sample device, Front end, Terminal, Insulating sheet, Metal plate Test voltage: Specified (both polarities) in the individual specification (Recommended: 500 V) Ta: 25°C Terminals applied: 1 Lead applied to: All terminals	

Test Category	JEITA Standard Number	Purpose	Conditions	Related Standards
Latch-up	EIAJ ED-4701/300 Test method 306	To evaluate the resistance of a CMOS device to electric noise	Method 1: Pulse current application Current: Specified trigger pulse current (both polarities) Ta = 25°C Times applied: 1 Circuit (for positive polarity) Method 2: Supply overvoltage Voltage: Specified trigger pulse Ta = 25°C Times applied: 1 Circuit	JESD 17

3.3 Accelerated Lifetime Test Methods

The reliability of semiconductors varies greatly with environmental factors such as ambient temperature, humidity, voltage and current.

The accelerated lifetime test is a method to estimate the failure rate of a component during actual use. The test focuses on the specific stresses of the environment in which the component is used and observations are made of the failures using the conditions of these stresses as parameters. This method is widely used in the adoption of new processes and the development of new products.

Following is an explanation of failure models, which form the basis for accelerated lifetime models, and statistical analysis methods.

3.3.1 Fundamental Failure Model

(1) Reaction Theory Model

The reaction theory model is the most commonly used failure model for accelerated lifetime tests of semiconductor devices. Generally, deterioration and destruction of substances are due to changes at the atomic and molecular level. The mechanisms of such changes include diffusion, oxidation, adsorption, dislocation (displacement), electrolysis, and development of corrosion cracks. The progression of these changes promotes deterioration of material and parts, then surpasses a certain threshold and finally leads to failure. This is called the reaction theory model. At one point in the process, from normal conditions to deteriorated conditions, there is an energy threshold. The energy needed to surpass this threshold must be drawn from the environment. This threshold energy is called the activation energy. Figure 3.1 shows a schematic of the energy condition before and after the reaction.

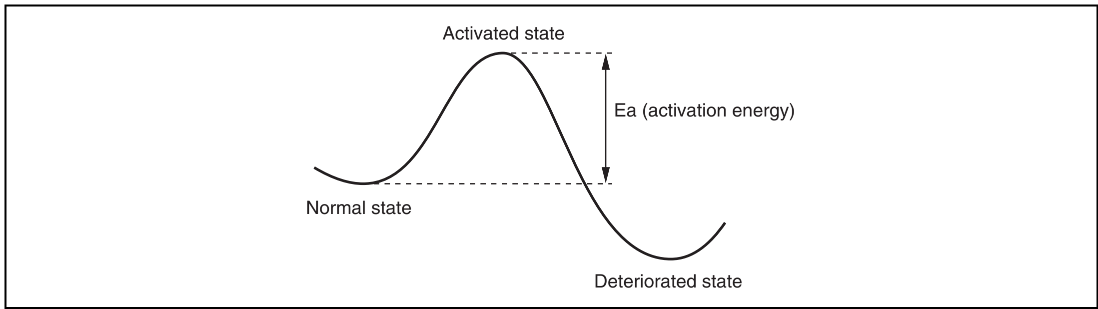

Figure 3.1 Activation Energy

The dependence of reaction rates on temperature was discovered by Arrhenius and the Arrhenius Equation is widely used.

If the reaction rate is K, then this equation can be expressed as

$K = \Lambda \exp(-Ea/kT)$

where Λ: Reaction rate constant

Ea: Activation Energy (eV)

k: Boltzmann Constant [8.617×10^{-5} (eV/K)]

T: Absolute Temperature (K)

If the time to failure is L, then

$L = A \exp(Ea/kT)$

and by taking the logarithm gives the equation

$\ln L = A + Ea/kT$

This equation shows the logarithm of lifetime (L) plotted against the reciprocal of temperature is linear, and the gradient of the straight line produced represents the activation energy. Then, based on this, the acceleration coefficient between two given temperatures can be derived.

For example, if L_1 and L_2 represent the lifetimes at T_1 and T_2 respectively, then

$$\ln (L_1/L_2) = 1/k\ (1/T_1 - 1/T_2)\ Ea$$

This equation provides an acceleration standard to determine the activation energy of a reaction. Figure 3.2 shows a schematic of this model.

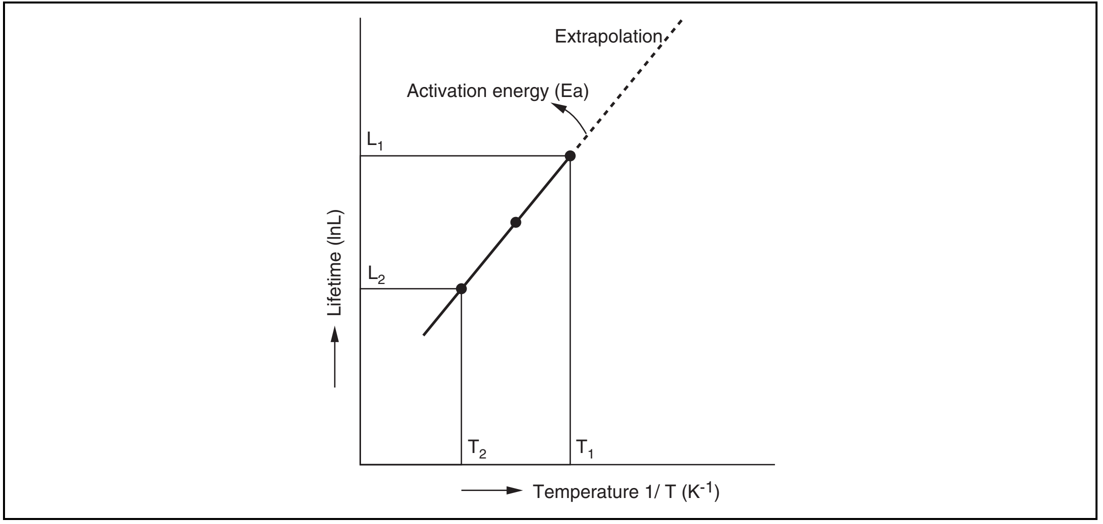

Figure 3.2 Graph of the Arrhenius Model

(2) Eyring Model

While the Arrhenius model emphasizes the dependency of reactions on temperature, the Eyring model is commonly used for demonstrating the dependency of reactions on stress factors other than temperature, such as mechanical stress, humidity and voltage.

The standard equation for the Eyring model is as follows

$$K = a(kT/h) \bullet \exp(-Ea/kT) \bullet S^{\alpha}$$

where a, α: Constants

h: Planck Constant

S: Stress Factors other than Temperature

T: Absolute Temperature

If the temperature range T is small, then this equation can be approximated as

$$K = \Lambda \exp(-Ea/kT) \bullet S^{\alpha}$$

Further, if we focus on stress factors other than temperature then lifetime (L) is proportional to 1/K and then taking the logarithm gives the equation

$$\ln L = A - \alpha \ln S$$

where A: Constant

The Eyring equation is often applied when conducting accelerated stress tests.
For example consider heat fatigue of plastics. If the stress is represented by alternating reaction stress S and lifetime by a repeated lifetime N then the repeated lifetimes N_1 and N_2 for the alternating reaction stresses S_1 and S_2 can be expressed by the equation:

$$\ln(N_1/N_2) = -\alpha \ln(S_1/S_2)$$

Further in the example of temperature cycle tests by substituting the change in temperature ΔT for stress and let N be the number of temperature cycles to failure, then the above equation can be expressed as

$$\ln(N_1/N_2) = -\alpha \ln(\Delta T_1/\Delta T_2)$$

Figure 3.3 shows a graph of the Eyring Model.

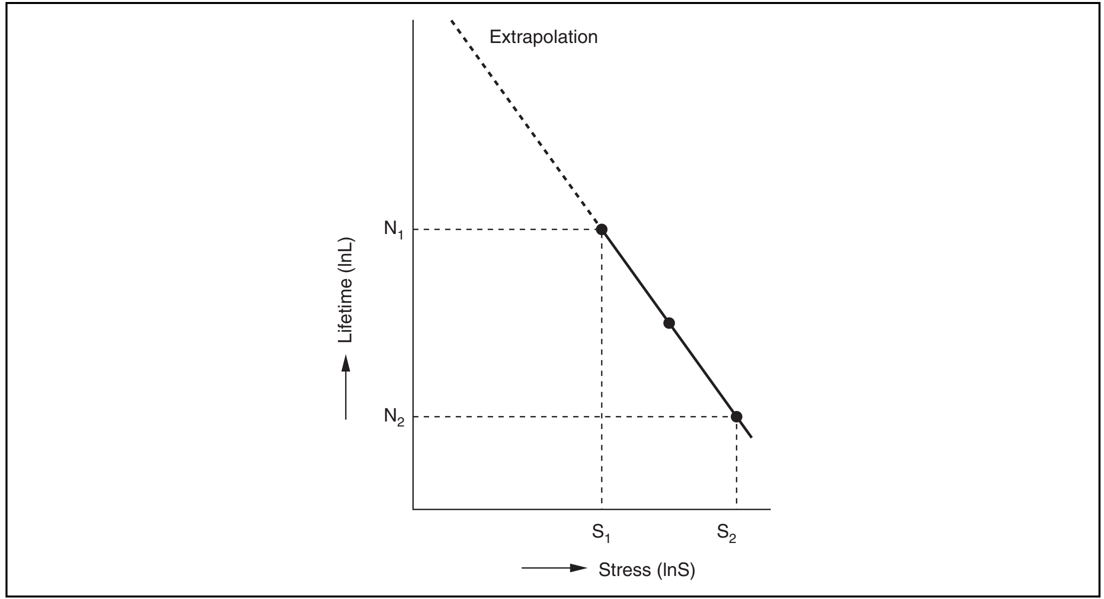

Figure 3.3 Schematic of the Eyring Model

(3) Stress Strength Model

As shown in figure 3.4, this model, after previously ensuring a safe margin between material strength and stress, demonstrates failure when material strength due to deterioration over time falls to below stress.

As shown by stress strength distribution, failure includes an element of probability.

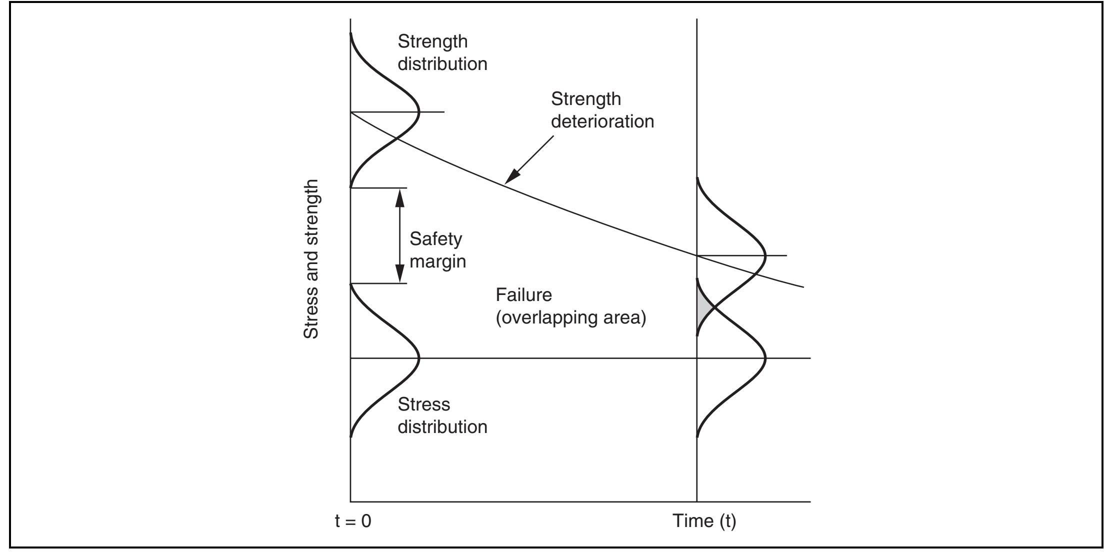

Figure 3.4 Stress Strength Model

3.3.2 Method of Accelerated Life Testing

(1) Means of Acceleration

Accelerated lifetime tests are conducted under stress conditions more severe than actual conditions of use (fundamental conditions). They are methods of physically and chemically inducing the failure mechanisms to assess, in a short time, device lifetime and failure rates under actual conditions of use.

The means of acceleration are:

- Increase the degree of stressors (e.g. temperature, voltage)
- Increase the frequency of the applied stress.
- Use tighter failure criteria.
- Use test vehicles/structures specific to the failure mode

(2) Applied Stress Method

Examples of how stress is applied in accelerated lifetime tests are constant stress, and step stress methods. The constant stress method is a lifetime test where stress, such as temperature or voltage, is held constant and the degree of deterioration of properties and time to failure lifetime distribution are evaluated. In the step stress method, contrary to the constant stress method, the time is kept constant and the stress is increased in steps and the level of stress causing failure is observed. This relation is shown in figure 3.5. In the figure, the continuously increasing stress test can be consider as a step stress test where the constant time is extremely short.

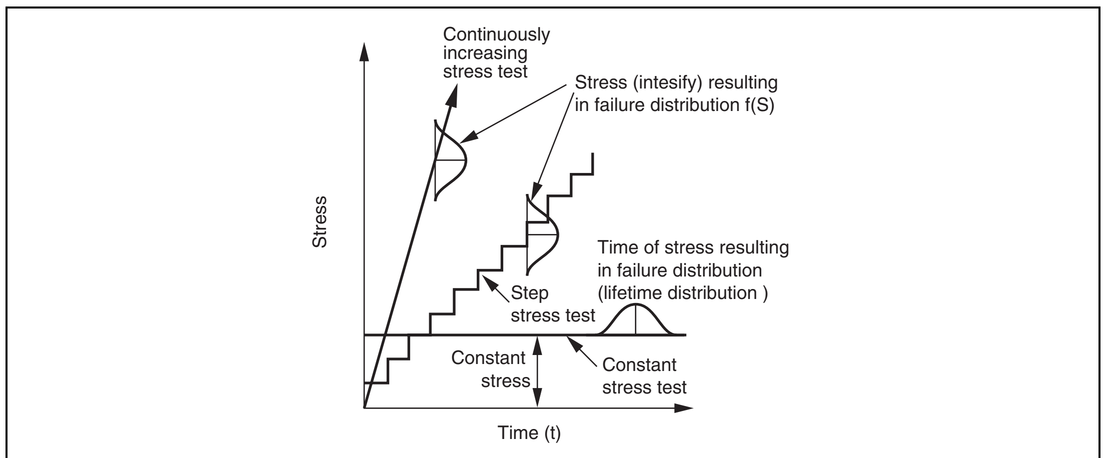

Figure 3.5 The Outline of Each Stress Tests

The constant stress method determines the lifetime distribution for a given stress and the step stress method determines the distribution of stress resulting in failure when time is constant. Assuming the failure mechanism does not change, the results obtained from these two methods can be expected to fall on the same straight line in a graph of the Arrhenius model or the Eyring model.

Representative examples of tests using the constant stress method, the step stress method, and the cyclic stress method, a variation of the constant stress method, are shown in table 3.5.

Table 3.5 Distribution of Representative Accelerated Lifetime Tests

Applied Stress Method	Purpose	Accelerated Test	Main Stressor	Failure Mechanism
Constant stress method	Investigation of the effects of constant stress on a device	High-temperature storage test	Temperature	Junction degradation, impurities deposit, ohmic contact, inter-metallic chemical compounds
		Operating lifetime test	Temperature Voltage Current	Surface contamination, junction degradation, mobile ions, EMD
		High temperature high-humidity storage	Temperature Humidity	Corrosion, surface contamination, pinhole
		High temperature high-humidity bias	Temperature Humidity Voltage	Corrosion, surface contamination, junction degradation, mobile Ions
Cyclic stress method	Investigation of the effects of repeated stress	Temperature cycle	Temperature difference Duty cycle	Cracks, thermal fatigue, broken wires and metallization
		Power cycle	Temperature difference Duty cycle	Insufficient adhesive strength of ohmic contact
		Temperature-humidity cycle	Temperature difference Humidity difference	Corrosion, pinhole, surface contamination
Step stress method	Investigation of the stress limit that a device can withstand	Operating test	Temperature Voltage Current	Surface contamination, junction degradation, mobile ions, EMD
		High-temperature reverse bias	Temperature Voltage	Surface contamination, junction degradation, mobile ions, TDDB

3.3.3 Analysis of Test Results

(1) Weibull Probability Paper [1] [2]

(a) Purpose

Weibull probability paper is used 1) to determine if the life span or strength data obtained from the reliability test conforms to the Weibull distribution and 2) to obtain the parameter of the Weibull distribution from the chart. The data is plotted as pairs of test time t (or value of stress strength) and cumulative failure rate F(t).

(b) Format

Figure 3.6 illustrates the basic format of Weibull probability paper. As shown in the right hand margin, the vertical axis is scaled evenly with a space of lnln {1/(1 - F(t))}, and the horizontal axis in the upper margin is scaled evenly with ln t. The corresponding F(t) is scaled in the left hand margin and the t is scaled in the lower margin.

The main axis scaled with lnln {1/(1 - F(t))}=0 is hereafter referred to as X_0 and the main axis scaled with ln t = 0, as Y_0. The point where X_0=1 and Y_0=0 is indicated by "○". Typical Weibull probability paper also contains the nomographs μ/η, σ/η, and F(μ) corresponding to m. Figure 3.7 is an example of Weibull probability paper.

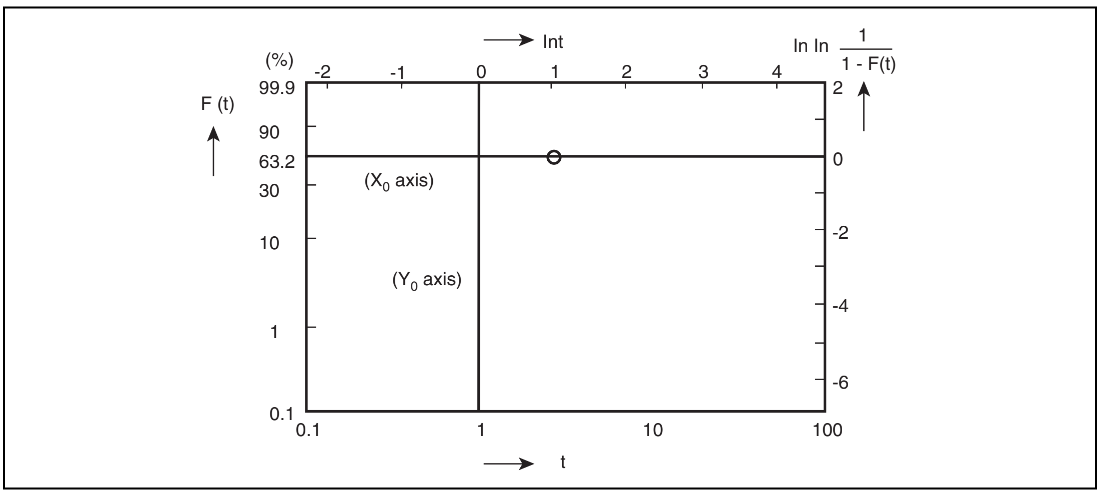

Figure 3.6 Basic Format of Weibull Probability Paper

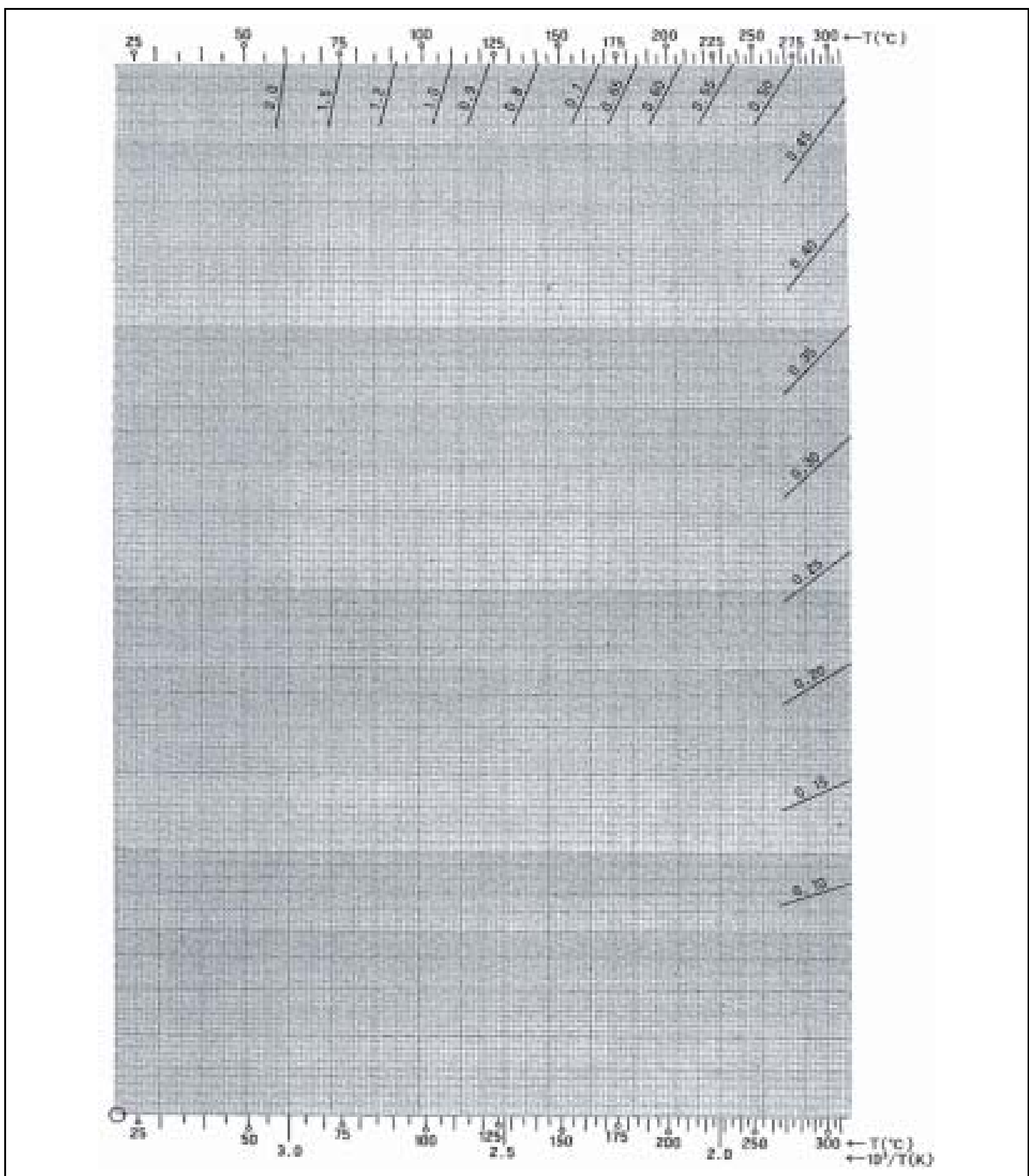

Figure 3.7 Chart for Determining Relationship between Activation Energy and Acceleration Factor

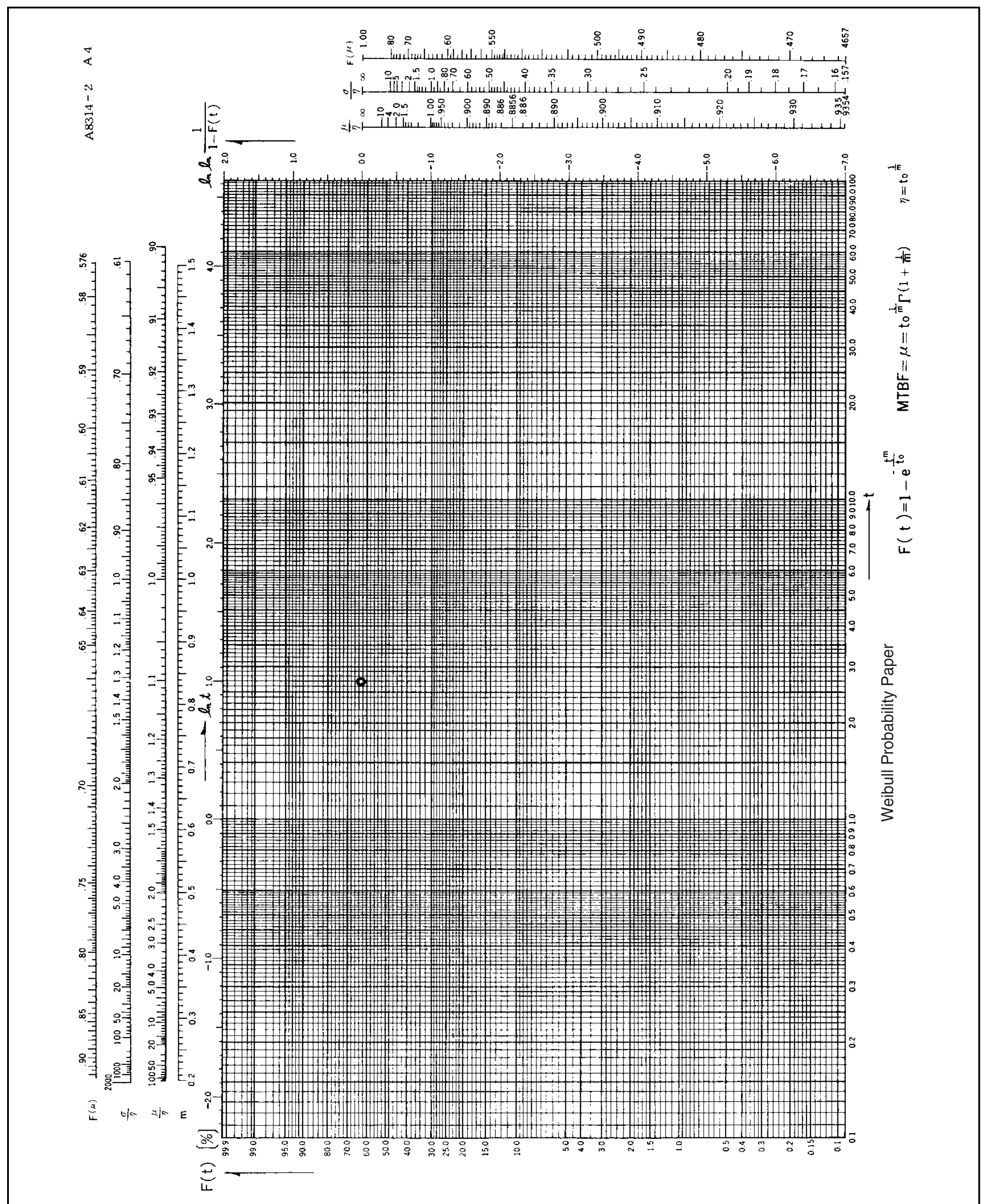

Figure 3.8 Example of Weibull Probability Paper

(c) Theory

The failure rate on the Weibull distribution is obtained from the Weibull failure distribution function using shape parameter m, scale parameter t_0, and characteristic life $\eta = t_0^{\frac{1}{m}}$ with position parameter $\gamma = 0$.

$$F(t) = 1 - e^{\frac{t^m}{t_c}} = 1 - e^{-(\frac{t}{\eta})^m} \qquad (3\text{-}1)$$

This is shown as a straight line on the Weibull probability plotting paper described in figure 3.8. The mean value μ, standard deviation σ, and failure distribution $F(\mu)$ of the Weibull distribution are expressed as follows,
using the gamma function $\Gamma(z) = \int_0^{\infty} e^{-t} \; t^{z-t} \; dt$

$$\mu = \eta \, \Gamma(1 + \frac{1}{m}) \qquad (3\text{-}2)$$

$$\sigma = \eta \sqrt{\Gamma(1 + \frac{2}{m}) - \Gamma^2(1 + \frac{1}{m})} \qquad (3\text{-}3)$$

$$F(\mu) = 1 - e^{\{1 \, (1 + \frac{1}{m})\}^m} \qquad (3\text{-}4)$$

μ/η, σ/η, and $F(\mu)$ are the Functions of m only and can constitute a nomograph corresponding to m.

(d) Usage

1. Plot the data on the Weibull probability paper

Obtain $F(t) = r / (n + 1)$ by the average ranking method where **n** is the total number of samples, t is the time when each sample fails, and r is the cumulative number of failure samples at t.

Plot the points on the Weibull probability paper and fit a straight line. To ensure that the points are entered correctly, the lower scale is multiplied by 10^{α} (where α is a positive or negative integer). When a curve can be fit, search for a proper γ and replace t with $(t - \gamma)$ for plotting so that a straight line fits.

2. Obtain parameters on the Weibull probability paper

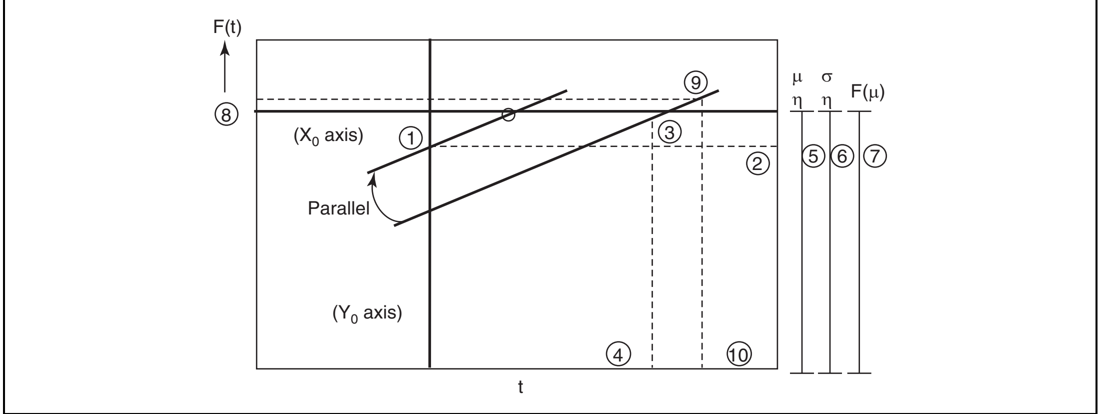

Figure 3.9 Procedure for Use of Weibull Probability

Next, obtain the gradient m of the straight line from the scales at the upper and right hand margins. To simplify the procedure, using the scale on the right hand margin, read the value of the point where the line that is parallel to the plot line goes through the point circled ("○") which crosses the Y_0 axis. Then invert the value to obtain m (① → ② as in figure 3.9).

η is read from the point that the plot line crosses the X_0 axis, using the scale at the lower margin (③ → ④). If the plot line is too low, the value can be recalculated by equation $\eta = e^{(\frac{1}{m} \cdot \ln t_0)}$ as the value of the point that crosses the Y_0 axis, read on the right hand scale, corresponds to the value $-\ln t_0$.

The values of μ and σ, which correspond to the value of m, are obtained by reading the values on the μ/η scale and σ/η scale and multiplying them η (② → ⑤, ⑥). The enlarged scale nomograph at the upper margin on the Weibull probability paper can also be used.

To obtain μ more simply, obtain F(μ) that corresponds to m from the F(μ) scale and use t as μ that corresponds to the plot line F(μ) (② → ⑦ → ⑧ → ⑨ → ⑩).

Where γ is used in (1), obtain μ corrected to (μ + γ) and η corrected to (η + γ).

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3. Interpretations of Weibull Plotting [3]

Figure 3.10 shows major interpretations of the obtained value m and the corresponding failure number including those of complex models.

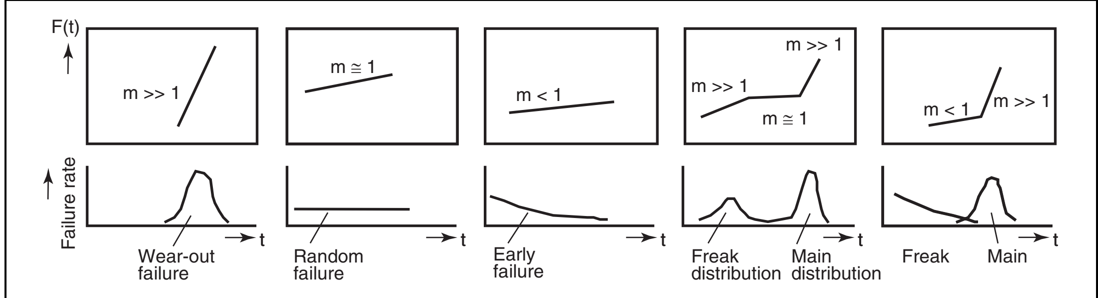

Figure 3.10 Example of Weibull Probability Results

(2) Cumulative Hazard Paper [1] [2]

(a) Purpose

When there are several failure modes in the reliability tests and when the distribution parameter must be checked for each failure mode, or when there are some suspended data, plotting on the Weibull probability plotting paper may require a complicated procedure. In this case plotting on the cumulative hazard paper is less complicated. The data is plotted as pairs of test time t (or stress intensify) and cumulative hazard H(t). Weibull type cumulative hazard paper is explained below.

(b) Format

Figure 3.11 illustrates the basic format of the Weibull type cumulative hazard paper.

Compared with the Weibull probability plotting paper in figure 3.7, the only difference is that the vertical axis is scaled with cumulative hazard function H(t). The example in figure 3.12 (made by the Union of Japanese Scientists and Engineers (JUSE)) shows the nomograph as having the μ/η, σ/η, and t^*/η scales, and no $F(\mu)$ scale. The F(t) scale on the left margin corresponds to H(t).

(c) Theory

When the cumulative hazard is $H(t) = \int_0^t h(t)\,dt$,

$$F(t) = 1 - e^{-\int_0^t h(t)\,dt} = 1 - e^{-H(t)} \qquad (3\text{-}5)$$

and if this is compared to the equation (3-5) indicating the Weibull distribution, then

$$1 - e^{-H(t)} = 1 - e^{(\frac{t}{\eta})^m}$$

Therefore, $H(t) = (\frac{t}{\eta})^m$

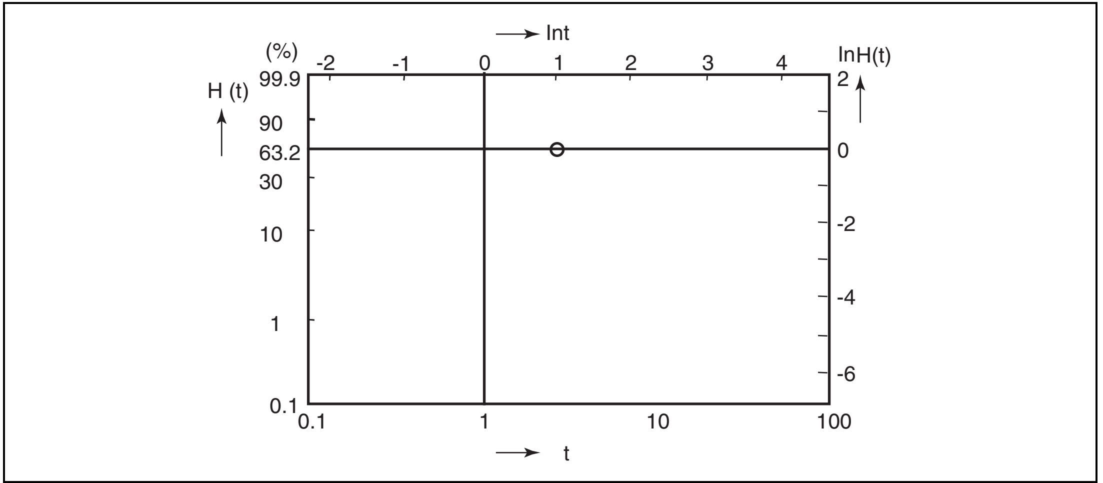

Figure 3.11 Basic Format of Weibull Type Cumulative Hazard Paper

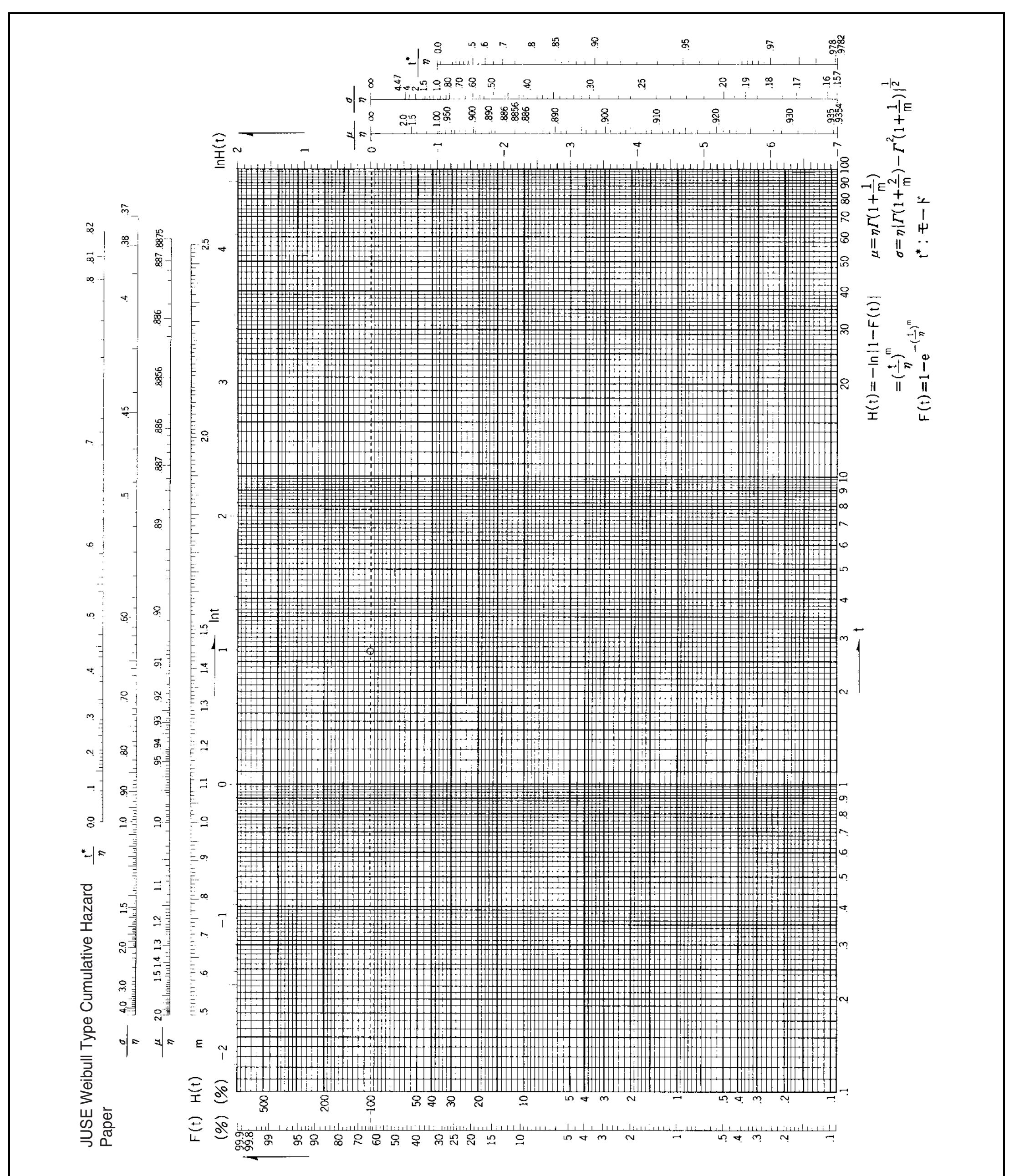

Figure 3.12 Example of Weibull Type Hazard Paper

From the logarithm of both sides, we have

$$\ln H(t) = m(\ln t - \ln \eta) \qquad (3\text{-}6)$$

When we let Y=ln H(t), X=lnt, and b=-ln η^m, (3-6) becomes an equation of the direct function with Y=mX+b, shown as a straight line on the Weibull type hazard paper described in figure 3.12.

For a reference, figure 3.13 shows an example of the relationship between cumulative failure rate F(t) obtained from equation (3-5) and cumulative hazard H(t). When t = η (characteristic lifetime), H(η) = 1 and F(η) = 0.632.

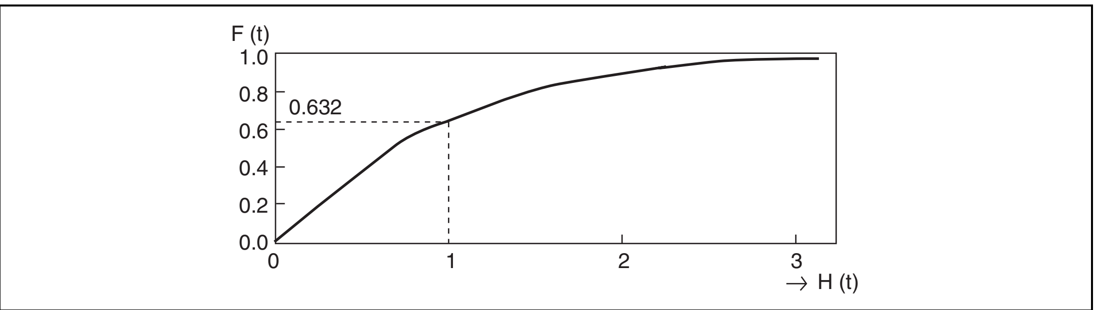

Figure 3.13 Relationship between F(t) and H(t)

(d) Usage

1. Prepare a work sheet

   Prepare a work sheet as shown in figure 3.14 to obtain the cumulative hazard value from the test data.

2. Fill in the work sheet

   Enter the observed failure time and censored time in ascending order into the ti column of the work sheet. Enter sequence i starting from 1 and enter the sample number and failure modes, displaying ti in the graph on the right hand margin. Then visually reconfirm the data in the graph. When entering the failure mode, mark censored data as C (censored).

3. Obtained cumulative hazard H(ti)

   Obtain the hazard value h(ti). Calculate the reverse sequence Ki = n – i + 1 from sequence j where total number of samples is n, and enter the value into the work sheet. Then obtain the hazard value h(ti) = 1/Ki × 100(%) and enter it in the chart.

   H(ti) is obtained by accumulating h(ti). If several must be analyzed, use Hj(ti) to that h(ti) corresponding to Mi and add one by one.

   An example is shown in figure 3.15.

Sample Number	Sequence	Reverse Sequence	Observed Value	Position Parameter Correction	Failure Mode	Hazard Value	Cumulative Hazard Value Hj (ti)		
	i	Ki = n - i + 1	ti Units (h)	—	Mj	h(ti) %	M_1 (A)	M_2 (B)	M_3 ( )
#4	1	10	200		A	10.0	10.00		
#7	2	9	300		B	11.11		11.11	
#5	3	8	300		A	12.50	22.50		
#9	4	7	800		C				
#2	5	6	800		A	16.67	39.17		
#8	6	5	800		C				
#1	7	4	900		B	25.00		36.11	
#3	8	3	1000		C				
#6	9	2	1600		B	50.00		86.11	
#10	10	1	2500		B	100.0		186.11	

Notes: C: Censored
Position parameter $\gamma = 0$

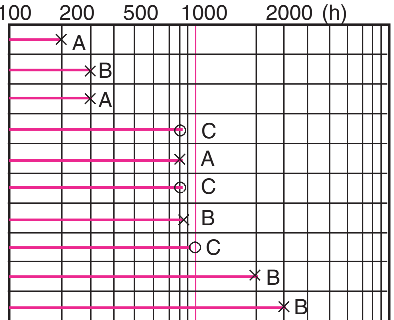

Figure 3.14 Fill-in Example of Work Sheet

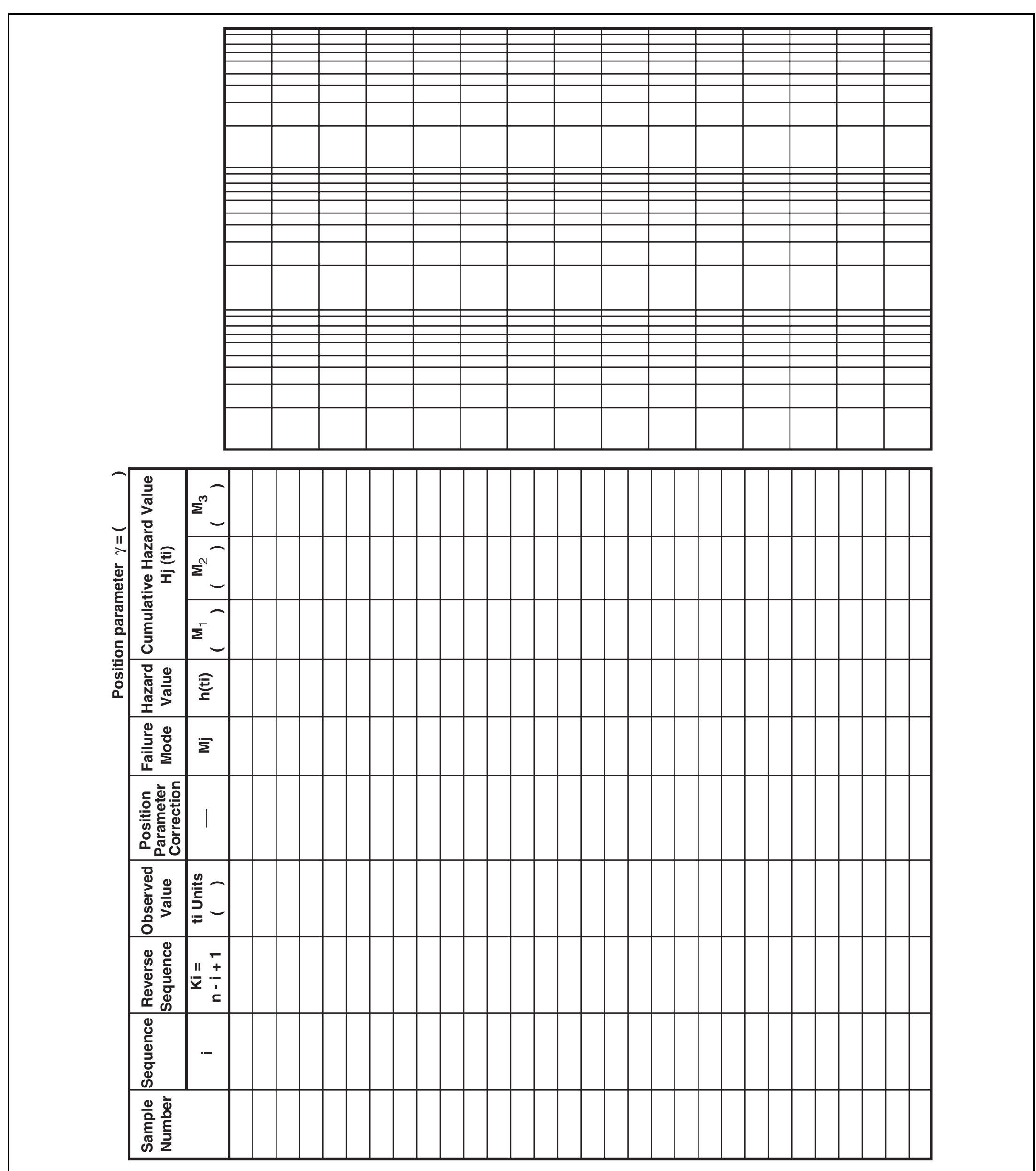

Figure 3.15 Example of Work Sheet Used for Data on Cumulative Hazard Paper

4. Plot data on the cumulative hazard paper

   Plot the point that is a pair of Hj(ti) and ti for each failure mode and try to fit a straight line. If a curve fits, search for proper γ and replace t with $(t-\gamma)$ so that a straight line fits.

   Then obtain m, η, μ, and σ as described in section 3.3.3 (2). The mode t* (most frequent value) can be obtained using the method shown in figure 3.12.

3.3.4 Procedure for Failure Rate Prediction With 60% Confidence Level [4] [5]

In some cases, it is required to make a rough estimate of failure rate from the reliability tests assuming m = 1. In such a case, a prediction can be made with a confidence level of 60% (hereafter abbreviated to 60% C.L.) to obtain a proper value that is neither too small nor too large.

The 60% C.L. is obtained as follows.

(1) Calculate the components hours

Let us assume a reliability test of Ti hours is performed on the same sample group with the number of samples ni and the number of failure samples is ri. The component hours for this group is niTi. If several groups exist for the same reliability test, ΣniTi is the total component hours. Ti is multiplied by the acceleration factor as necessary.

(2) Obtain the 60% C.L.

Obtain the failure rate by replacing ri (or total number of failure samples Σri) with J in figure 3.6 and using the following equation.

$$\text{60\% C.L. failure rate} = \frac{J}{\text{Total component hours}} \qquad (3\text{-}7)$$

The unit can be %/1,000 h, $\times 10^{-a}$/h, or FIT (1FIT = 1×10^{-9}/h).

Table 3.6 R-J Conversion for 60% C.L. Failure Rate

r	J	r	J	r	J	r	J
0	0.92	4	5.24	8	9.44	21 to 30	1.08
1	2.02	5	6.30	9	10.44	31 to 40	1.06
2	3.11	6	7.32	10	11.5	41 to 50	1.05
3	4.18	7	8.40	11 to 20	1.11	50 or greater	1.00

Notes: 1. For r over 11, use equation J = r × j.

2. The values in this table can also be obtained by inverse solution of Poisson distribution.

3.4 Reliability Prediction Based on the Failure Mechanism

The prediction of a failure rate for semiconductor devices when used in electronic systems is also important for system reliability and integrity design.
The reliability of semiconductor devices is considered using three major failure modes: initial failures, random failures, and wear-out failures. Of these, wear-out failures have a well-defined distribution, implying that you need only a small number of samples to recognize their distribution.

The failure mechanisms related to the wafer process will be explained in section 4. Typical examples such as TDDB, EM, HC, and NBTI are well-known.

Meanwhile, the trend in product development is toward increasingly shorter development periods, and the meeting of user requirements has become a critical task. In the design review (DR), which is conducted at the beginning of development, we use the Failure Mode and Effects Analysis (FMEA) method so that we build in quality in the development and design phases for new products both effectively and within the allotted time. To meet the requirements for the product use environment and for quality, we strive to identify reliability-related failure modes and mechanisms so that we can build in quality in the design phase. In the first DR phase, we plan on accelerated tests that conform to the failure modes and mechanisms. Prior to product development, we conduct the accelerated tests by means of TEGs and use the results to build in both quality and reliability and to create design manuals (design rules). This allows us to build in quality in the design phase.

A variety of typical failure mechanisms are illustrated in section 4. For information about how to test reliability based on these failure mechanisms, refer to the related standard of the Japan Electronics and Information Technology Industries Association (JEITA) (EIAJ ED-4704).

3.4.1 Example of Predicting the Initial Failure Rate (Initial Failures from Oxide Film Breakdown)

The typical initial failure mechanism, mainly for MOS devices, is the degradation of oxide films over time. The results of reliability testing based on this failure mechanism provide us with data about electric field and temperature acceleration. After converting the data to an actual time axis, we use the following method to predict reliability.

Based on screening data (V-stress, aging, etc.) in the production process, we make predictions from the calculations by assuming that the initial failures occurring after screening have a Weibull distribution. Renesas defines initial failures as the fraction defective (ppm/year) assumed as one year after a product is launched on the market.

A major characteristic of initial failures is that the shape parameter (m) is small. Identifying this with a test requires a large amount of data. Reliability prediction based on the Weibull distribution refers to the process of predicting the reliability of products on the market both from screening conditions (at the wafer and package levels) through burn-in and other tests and from the number of defectives produced under those conditions. For example, you can estimate the shape parameter (m) by plotting burn-in defectives in the Weibull distribution. You can also predict the market failure rate and set the aging time at an appropriate value by obtaining the scale parameter (η). The following is an example application using this method.

Let the screening time be "ta," the reliability measured at the time of screening be "R(ta)," and the time during which a product has been available in the marketplace be "t." Assuming that the reliability measured at the time (ta+t) is R(ta+t), the cumulative failure rate measured from "ta" to "ta+t" will be equal to "R(ta) - R(ta+t)," where the time "ta" is equivalent to the value converted to the actual working time. If R(ta) and F(ta) are the reliability function and unreliability function, respectively, immediately after screening and R'(ta), and F'(ta) are the reliability function and unreliability function, respectively, for the time with "ta" as the starting point, then

$$R(ta) = \exp\{- (ta/\eta)^m\} \quad (3\text{-}8)$$

$$F'(t) = 1-R'(t) \quad (3\text{-}9)$$

$$R'(t) = R\,(ta + t)/R\,(ta)$$

$$= \exp\,[-\{(ta + t)\,/\eta\}^m + (ta/\eta)^m\,] \quad (3\text{-}10)$$

substitute the shape parameter (m) and the reliability obtained from the result of screening into Equation (3-8) to calculate the scale parameter (η).

$$\eta = ta/\{-\ln R(ta)\}^{1/m}$$

Substitute the scale parameter (η). From this and the relation with Equation (3-9), you can obtain the F'(t) unreliability function from the time "ta" used as the starting point. This is the cumulative failure rate.

Cumulative fraction defective

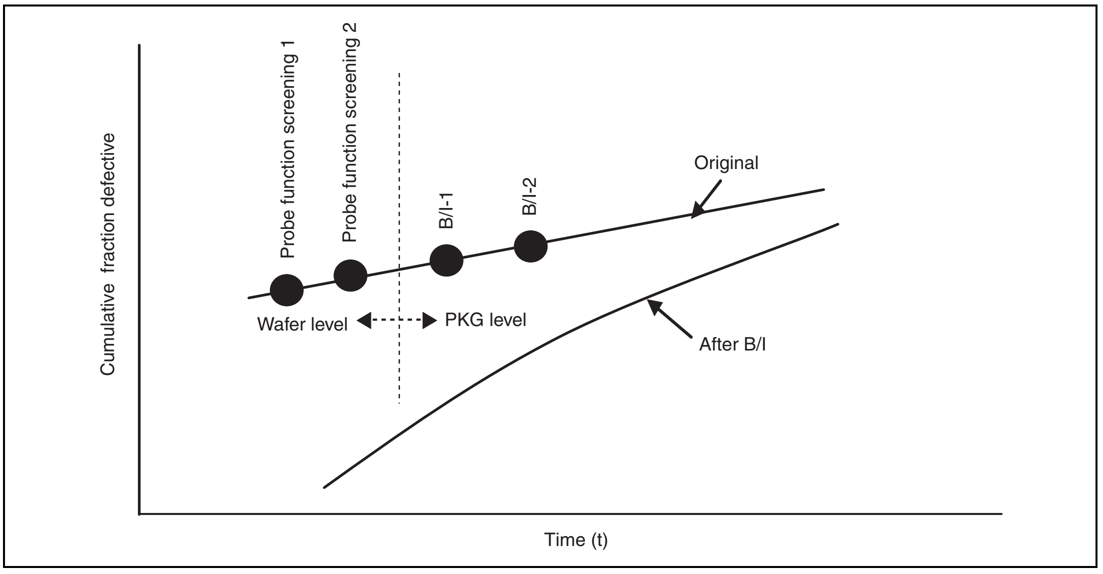

Figure 3.16 Life Prediction through Weibull Plotting

3.4.2 Example of Predicting the Random Failure Rate (Method of Estimating a Failure Rate at a 60% Reliability Level)

The internal quality certification conducted by Renesas during the development stage of semiconductor devices is an overall evaluation of quality and reliability, not just an evaluation of electrical properties and functionality. During reliability evaluation, we perform a variety of reliability tests involving such factors as operating lifetime, moisture resistance, thermal resistance, mechanical resistance, and environmental resistance, and assess pass or fail criteria for each product according to whether the product meets market requirements.
The reliability data we publish is mainly a compilation of the reliability test results we obtain from quality approval.

Note that the format of reliability data differs slightly according to device type. Table 3.7 shows an example of a specific microcontroller product (function: single-chip microcontroller, wafer process: 0.8 µm, CMOS, package: PLCC).

The reliability tests include a lifetime test (endurance test), environment test, and mechanical test. The lifetime test evaluates elements, patterned wires, and the oxide films formed on the chip, as well as the moisture resistance of the plastic packages. The environment test mainly evaluates resistance to the thermal stress exerted during use.

Test results are presented as the number of samples and the number of failures. You can check these results to see the failure rate for the product. For example, solderability in table 3.7 has a lot tolerance percent defective (LTPD) of 10% pass standard, and high-temperature unbiased storage has a lot tolerance failure rate (LTFR) of 10%/1000 h.

Furthermore, failure rates can be estimated using the test results in the reliability data. The examples given here use the methods described in JIS C5003, "General Test Procedures for Failure Rate in Electronic Components." Using the operation lifetime test results in table 3.7, you can determine failure rates as follows.

$$\frac{\text{Number of failures (r)} \times \text{Coefficient (a)}}{\text{Total test time (T)}} = \frac{0.92}{45 \times 1000}$$

$$= 20\ \%\ \text{(1/1000 hours)}$$

$$= 20 \times 10^{-5}\ \text{(1/hour)}$$

Assuming a reliability standard of 60%, the calculation uses a = 0.92 (corresponds to the 60% reliability standard), since the test resulted in no failures (r = 0).
The value calculated here is the failure rate obtained under accelerated test conditions. When obtaining the failure rate under actual working conditions, however, the above value must be

divided by the acceleration coefficient obtained from the test conditions and actual working conditions.

The accelerating factors in the accelerated test conditions include the temperature and voltage applied. Activation energy is the parameter used to express the degree of acceleration related to temperature. Although different values are used with different failure mechanisms, a typical value for each failure mechanism can be obtained (see section 4).

The above example of calculating a failure rate is based on microcontroller module design, layout, wafer process, and structure data, as well as data on components and materials.

For these standardized elements, we use the TEG (Test Element Group) and other means beforehand to evaluate and check quality and reliability. Because each product is composed of these standardized elements, quality and reliability are maintained at the same level. These are obtained from the data about individual products and there is a limit on the number of samples. Even if the value obtained by the total number of test items multiplied by the time is small, and the failure rate is zero, the estimate value will be relatively large. But the data obtained from other products also show that the actual failure rate is much smaller. This is because of the standardized designs.

Renesas believes that reliability design is very important to ensure semiconductor device quality and reliability. In reliability design, standardization of design is currently ongoing. Through standardization, quality and reliability can be maintained at the same standard even if device characteristics and functions differ. When considering the actual reliability of circuits, elements, and individual products, it is essential to consider the test results in conjunction with test results of other products that have the same fundamental design (products in the same product family), such as the wafer process and structure test results. Examples of standardization for wafer process design include CMOS 1.3 µm, 0.8 µm, 0.5 µm, 0.35 µm, and the structural design is standardized by the external configuration, such as DIP, QFP, and PLCC package designs. Items with the same standardized elements, including the wafer process and package, can be treated as a single product family.

The microcontroller in table 3.8 is manufactured with a CMOS 0.8-µm wafer process and uses a PLCC package. Table 3.8 shows individual products that use the same wafer process that is used for the microcontroller.

The failure rate (0.51%/1000 h = 5.1×10^{-6} (1/h), Ta = 125°C, reliability standard of 60%) calculated by adding the test data (not shown here) of these individual products is the estimated failure rate for the SH7034. For dedicated logic and microcontrollers, it is normal for many separate products with different characteristics and functions to be developed from the same wafer process and package type (in the same family). For memory products, by contrast, a single individual product line is usually developed from the same wafer process and package. Table 3.7 is inserted as an example of reliability test results. Note that the time of testing and the number of samples contained in the reliability data actually submitted to customers are different from those shown in table 3.7.

Table 3.7 Reliability Test Results for SH7034 (HD6437034A)

Classification	Test Item	Test Conditions	Results*
Lifetime test	High-temperature operation	Ta = 125°C, V_{CC} = 5.5 V, t = 1000 h	0/45
	High-temperature storage	Ta = 150°C, t = 1000 h	0/22
	Low-temperature storage	Ta = –55°C, t = 1000 h	0/22
	High-temperature/high-humidity storage	Ta = 65°C RH = 95%, t = 1000 h	0/77
	High temperature/high-humidity bias	Ta = 85°C, RH = 85%, V_{CC} = 5.0 V, t = 1000 h	0/22
Environment test	Temperature cycle	–55°C to 150°C, 200 cycles	0/45
	Thermal shock	0°C to 150°C, 15 cycles	0/22
	Solderability	230°C, 5 s, rosin type flux	0/22
	Solder heat resistivity	Infrared rays reflow 235°C, 10 s	0/22
	Pressure cooker (PCT)	Ta = 121°C, RH = 100%, t = 100 h	0/22
Mechanical test	Lead pull strength	2.5 N, 10 s, 1 time	0/22

Note: * Failure count/sample size.

Table 3.8 Products Using the Same Process as SH7034

Microcontroller Unit	SH7034A, SH7042/43,SH7050
Microcontroller Peripheral LSI	H8S/2244, H8S/2246, H8S/2655, HD6433048S, HD6473035, HD64411F

Next we will explain the general procedure for failure rate prediction of Renesas semiconductor devices, based on reliability test data.

(1) Failure Rate Prediction Based on Temperature Accelerated Tests

Temperature accelerated tests induce failures in a shorter period of time than occur under conditions of the actual working environment. In these tests thermal stress, the accelerating factor is applied to semiconductor devices to activate failure mechanisms (failure factors). In other words, thermal stress induces chemical and physical reactions and when exceeding a certain limit causes device failure to be accelerated. For example, destruction of junction, gate dielectric film and interlayer dielectric film, and breaks in metallization or contacts, develop as failure mechanisms. The reaction theory model discussed earlier can explain these kinds of phenomena.

High-temperature operation tests and high-temperature storage tests are representative of temperature acceleration test methods. The temperature acceleration factor is expressed by a unit of measurement called activation energy (Ea). This value varies according to the failure mechanism. If the Ea value is large, the temperature acceleration characteristic is large. If it is small, the temperature acceleration characteristic is also small. When predicting failure rate from reliability test results, Ea is considered indispensable.

The failure rate under conditions of actual use can be predicted from the high-temperature operating life test in table 3.7, SH7034 Reliability Test Results, (125°C, 5.5-V operating test), as explained below.

The conditions of actual use are

$$\text{Ta} = 40°\text{C}, \ V_{CC} = 5.0 \text{ V}$$

assuming $Tj = Ta$, calculated as follows. (Where Tj is the junction temperature.)

Generally activation energy (Ea) can be determined from the evaluations of the various thermal conditions, however from previously accumulated records, supposing

$$Ea = 0.80 \text{ eV}$$

then, the procedure for prediction of the failure rate for conditions of actual use is as follows.

First, calculate the acceleration factor (temperature acceleration coefficient γr) for conditions of the temperature accelerated test against conditions of actual use. The product of the temperature acceleration coefficient γr and the test time is equivalent to operating time under conditions of actual use. In other words, if temperature accelerated test time is $L(Tb)$, the operation time under conditions of actual use is $L(Ta)$, then

$$L(Ta) = \gamma r \times L(Tb)$$

From the Arrhenius model, the relation between $L(Ta)$ and $L(Tb)$ can be expressed by

$$L(Ta) = C \bullet e^{Ea/kTa},\ L(Tb) = C \bullet e^{Ea/kTb}$$

where

Ta: Temperature under Conditions of Actual Use (40°C)

Tb: Temperature under Accelerated Conditions (125°C)

Ea: Activation Energy (0.80 eV)

k: Boltzmann Constant (8.617×10^{-5} eV/K)

C: Constant

Therefore, the acceleration factor γr is

$$\gamma r = \frac{L\ (Ta)}{L\ (Tb)} = \frac{e^{Ea/kTa}}{e^{Ea/kTb}}$$

$$= [e^{\{0.80/8.617 \times 10^{-5}\ (273+40)\}}/[e^{\{0.80/8.617 \times 10^{-5}\ (273+125)\}}]$$

$$= 561.8$$

This shows that compared to conditions of actual use, the temperature accelerated test has an equivalent acceleration factor of approximately 560 times and time to failure is reduced by a factor of 560 times. Consequently, the operating time $L(Ta)$ under conditions of actual use is equivalent to

$$L(Ta) = 560 \times 1000\ \text{(h)}$$
$$= 560000\ \text{(h)}$$

Considering reliability test data of the SH7034 product family described in the previous section, the failure rate under the temperature accelerated test is calculated:

Failure rate = 5.1×10^{-6} (1/h)

The failure rate under conditions of actual uses is equivalent to the failure rate under the temperature accelerated test divided by the acceleration factor γr:

$$\text{Failure rate} = 5.1 \times 10^{-6}/560$$
$$= 9.1 \times 10^{-9}(1/h) \cong 9(FIT)$$

Therefore, 9(FIT) becomes the expected value for the SH7034.

If the temperature accelerated test is 1000 hours of continuous operation, this is equivalent to 560000 hours (roughly 64 years) of continuous operation under conditions of actual use. However, very few systems, equipment, or devices are used continuously for 560000 hours. If the stress during operation is larger than that while in standby, it is possible to estimate a value which is close to the failure rate under conditions of actual use by multiplying by the reduction factor.

In temperature accelerated tests, the higher the temperature within a certain range, the shorter the time to failure. However, for excessive temperatures, failures that would not occur in actual use, are sometimes induced (in other words, failure may be caused by a completely different failure mechanism than what will be found in actual use). Therefore certain precautions must be taken. Generally, 125°C is used operating life tests to minimize probability of inducing different failure mechanisms.

(2) Failure Rate Prediction Based on Temperature Cycle Tests

Temperature cycle tests use rapidly changing temperature as an acceleration factor. The alternating high and low temperatures generate stress in semiconductor devices. This stress can activate failure factors that subsequently induce failures in a shorter time when compared to failure under "actual use" conditions. In other words, the temperature cycles repeatedly cause heat related deformities such as warping in and between the various materials comprising the semiconductor devices. Consequently physical and mechanical reactions are induced which in turn lead to device failure. Furthermore, by exceeding certain limit, failures can rapidly occur.
As an example failures such as package cracks, wire breaks, and shorts can be induced.

Various high and low-temperature conditions are prescribed for temperature cycle tests; representative values are

–65°C to 150°C

–55°C to 150°C

–55°C to 125°C

–45°C to 125°C

0°C to 125°C

Temperature cycle failure acceleration characteristics are determined by the difference between the high and low temperature, the transition time from high to low and from low to high temperatures, and the time the specimens are held at high and low temperatures.

Stress S is proportional to temperature difference ΔT. Experience shows that the Eyring model forms between S and temperature cycle count N.

$$\ln N = \ln C + (-n) \cdot \ln \Delta T$$

C: Constant

n: Temperature Difference Factor

This shows that the full lifetime temperature cycle count N is inversely proportional to temperature difference ΔT raised to the power n, and is expressed as

$$N = C \times \Delta T^{-n}$$

The value of n differs with the failure mechanism; if the value n is large, the test condition acceleration characteristic is large; conversely, if the value n is small, the test condition acceleration characteristic is small. The value n is indispensable information for the prediction of failure rate from the temperature cycle test results.

The failure rate under conditions of actual use is predicted from the temperature cycle test results (temperature cycle –55°C to 150°C test) shown in table 3.7, SH7034 Reliability Test Results.

The temperature difference ΔTb under test conditions is

$$\Delta Tb = 150 - (-55) = 205$$

The temperature difference ΔTa under conditions of actual use is determined mainly from the difference in emission of heat (the degree of thermal radiation) from a device or system when the power supply is on and off. It is also essential to consider the temperature differences due to air conditioning being on and off in the room where the system is used, or the atmospheric temperature variations when the system is used outside.

Assume

$\Delta Ta = 40°C$

Also,

assume $n = 6$

Therefore, the acceleration coefficient $\gamma\sigma$ for test conditions to conditions of actual use can be calculated as

$$\gamma\sigma = \frac{Na}{Nb} = \frac{C \times \Delta Ta^{-n}}{C \times \Delta Tb^{-n}} = \frac{\Delta Ta^{-n}}{\Delta Tb^{-n}}$$

$$= \left(\frac{40}{205}\right)^{-6} = 18120$$

Consequently, the test conditions can shorten the full lifetime cycle count for actual use.

For the SH7034 example, the results are

–55°C to 150°C
200 cycles 0/45

The temperature cycle count for the actual working environment is

Cycle count = 200 × 18,120 = 3,624,000

If, in the actual working environment, 10 cycles of thermal stress are applied per day, the failure rate for a 60% confidence level can be predicted by

$$\text{Failure rate} = \frac{0.92}{45 \times (3{,}624{,}000/10) \times 24}$$

$$= 2.4 \times 10^{-9} \text{ (1/h)}$$
$$= 2.4 \text{ (FIT)}$$

Therefore, failure rate for the SH7043 can be predicted as approximately 3 FIT.

In temperature cycle accelerated testing, the higher or the lower the temperature within a certain range, the shorter the number of cycles to failure. When temperatures exceed a certain critical limit, failures that would not occur in actual operation are sometimes induced (failures due to completely different failure mechanisms), therefore precautions must be taken. Generally, the temperature range between the maximum and minimum of storage temperature can be applied.

(3) Failure Rate Prediction Based on Moisture Resistance Tests

In moisture resistance accelerated tests, humidity stress is applied as an acceleration factor. Device failure factors, such as destructive chemical and physical reactions are induced by humidity stress, and failure mode is accelerated by exceeding certain limits. These phenomena can be described using the Arrhenius model.

Representative of moisture resistance accelerated tests are high-temperature, high-humidity bias tests and high-temperature, high-humidity unbiased tests. Typical of conditions for the former are the 85°C-85% RH bias test, and HAST (Highly Accelerated Temperature and Humidity Stress Test) where the temperature is 100°C or greater and the pressure is 1 atmosphere gauge or greater. The latter are 65°C-95% RH unbiased test. The pressure cooker test (PCT) is also unbiased, where the temperature is 100°C or greater and the pressure is 1 atmosphere gauge or greater.
Moisture resistance acceleration factors are humidity, temperature, and voltage acceleration. Moisture resistance lifetime is expressed by the Arrhenius model for the temperature factor, in combination with humidity and voltage factors. This can be expressed by the equation:

$$L(Tb) = \mathrm{C} \cdot e^{Ea/kTb} \cdot (\mathrm{RH})^{-n} \cdot \mathrm{V}^{-\alpha}$$

where, generally

$L(Tb)$: Lifetime

C: Constant

RH: Relative Humidity

n: Relative Humidity Factor

V: Applied Voltage

α: Applied Voltage Factor

The Ea, n , and α are indispensable in the prediction of failure rate under conditions of actual use from moisture resistance test results. These values, of course, differ according to the failure mode. Using table 3.7, SH7034 Reliability Test Results as an example, following is an explanation of the procedure for predicting failure rate under conditions of actual use from results of high-temperature, high-humidity bias tests. Assuming conditions of actual uses are

Ta = 30°C, V_{CC} = 5.0 V, RH = 85%

The moisture resistance test conditions are

Ta = 85°C, V_{CC} = 5.0 V, RH = 85%

The test results are

1000 hours 0/22

Using this method, what follows is the procedure for predicting the failure rate under conditions of actual use. Because the test conditions for humidity and externally applied voltage are assumed to be the same as conditions of actual use, the relative humidity coefficient σ and voltage coefficient *n* do not need to be calculated. Consequently, only the temperature acceleration characteristic needs to be examined. Because a failure did not occur, the activation energy cannot be determined. However, from existing records the activation energy *Ea* is assumed to be

$Ea = 1.0$ eV

From the Arrhenius model, *L*(*Ta*) and *L*(*Tb*) are

$$L(Ta) = C \cdot e^{Ea/kTa}$$
$$L(Tb) = C \cdot e^{Ea/kTb}$$

where

Ta: Actual use temperature conditions (30°C)
Tb: Accelerated temperature conditions (85°C)
Ea: Activation energy (1.0 eV)
k: Boltzmann constant (8.617×10^{-5} eV/K)
C: Constant

Therefore, the test condition acceleration coefficient γ*H* is obtained

$$\gamma H = \frac{L\ (Ta)}{L\ (Tb)} = \frac{e^{Ea/kTa}}{e^{Ea/kTb}}$$
$$= \frac{e^{[1.0/\{8.617 \times 10^{-5}\ (273+30)\}]}}{e^{[1.0/\{8.617 \times 10^{-5}\ (273+85)\}]}}$$
$$= 359.6$$

This means that for temperature accelerated tests compared to conditions of actual use, failure occurs 359 times faster (time to failure is reduced by a factor of 359). Consequently, the operation time *L*(*Ta*) under conditions of actual uses is equivalent to

$$L(Ta) = 359 \times 1000\ (h)$$
$$= 359{,}000\ (h)$$

Therefore, the SH7034 failure rate can be predicted for conditions of actual use as

$$\text{Failure rate} = 0.92 / (22 \times 359{,}000)$$
$$= 1.2 \times 10^{-7} (1/h)$$
$$= 120 (FIT)$$

In moisture resistance accelerated tests, the higher the temperature and relative humidity within a certain range, the shorter the time to failure. However, when temperature and relative humidity exceed a certain limit, failures that would not occur in actual use are sometimes induced (failures due to completely different failure mechanisms), therefore precautions must be taken. In tests like the PCT, where relative humidity is close to 100%, with a temperature of 100°C or greater, failure mechanisms sometimes change. For this reason individual failure analysis is essential. Furthermore, the sample calculations shown here are examples of single (isolated) stress conditions, and with these calculations very long expectant lifetime values can be obtained. However, under conditions of actual use, it is necessary that other factors also be considered.

(4) Failure Rate Prediction by Aggregation of Failure Data

By collecting and analyzing failure data from actual application, it is possible to predict the failure rate, assuming failures will occur in the future. However, for many various reasons, complete collection of data is nearly impossible. Therefore, in this situation, one applicable method is the Hazard Function Analysis because, when collecting a series of data, any kind of hazard should be considered. The following is an example analysis using the Hazard Function.

- Example

When using an electronic device, failure resulted from a specific cause. From the data we obtain the shape parameter (m) and the scale parameter (η). The data currently obtained is similar to that shown in the table below. However, two of the same devices are mounted on a PCB and when one device fails, both are removed from the board.

Table 3.9 Failure Data

Time to Failure (*h*)	No. of Failures (*ri*)	Remarks
3600	0	Total 200 electronic devices
6000	1	2 samples taken
8640	2	4 samples taken
13140	5	10 samples taken
17520	10	20 samples taken
26280	17	

We can explain this using Weibull hazard probability paper. For details see (2) on section 3.3.3.

First, the Weibull probability paper has the following format.

Right Vertical Axis: $\ln \ln \{1/[R(t)]\} = \ln \ln \{1/[1 - F(t)]\} = m \ln t - m \ln \eta$
Top Horizontal Axis: $\ln (t)$
Left Vertical Axis: Unreliability Function $F(t)$ on a percentage (%) scale
Bottom Horizontal Axis: Time t

Therefore

Vertical Axis: $Y = \ln \ln \{1/[1 - F(t)]\}$
If Gradient: m
Horizontal Axis: $X = \ln (t)$
Intercept: $b = -m \ln \eta$
Then $Y = mX + b$
From the Cumulative Hazard Function expressed as $H(t) = (t/\eta)^m$
and taking the logarithm of both sides of the equation produces

$$\ln H(t) = m (\ln t - \ln \eta)$$

Next by plotting t and $H(t)$ on the Weibull probability paper which has log-log scales, both produce a linear relationship and thereby obtaining m and η. From this relationship m and η, the Weibull parameter can be derived easily using spreadsheet software. See (2) on section 3.3.3 for details of the analysis procedure. Using this procedure we can produce a Cumulative Hazard Table.

Table 3.10 Cumulative Hazard Table

Time to Failure (*h*)	*X*: ln (*t*)	No. of Failures	Hazard Value: (*hi*)	Cumulative Hazard Value: *H*(*t*)	*y*: ln *H*(*t*)
6000	8.7	1	0.005 (1/200)	0.005	–5.298
8640	9.06	2	0.010 (2/198)	0.015	–4.12
13140	9.48	5	0.026 (5/194)	0.041	–3.194
17520	9.77	10	0.054 (10/184)	0.095	–2.354
26280	10.18	17	0.104 (17/164)	0.199	–1.614

Figure 3.17 shows this cumulative hazard table plotted on Weibull probability paper. From this graph the respective values can be obtained.

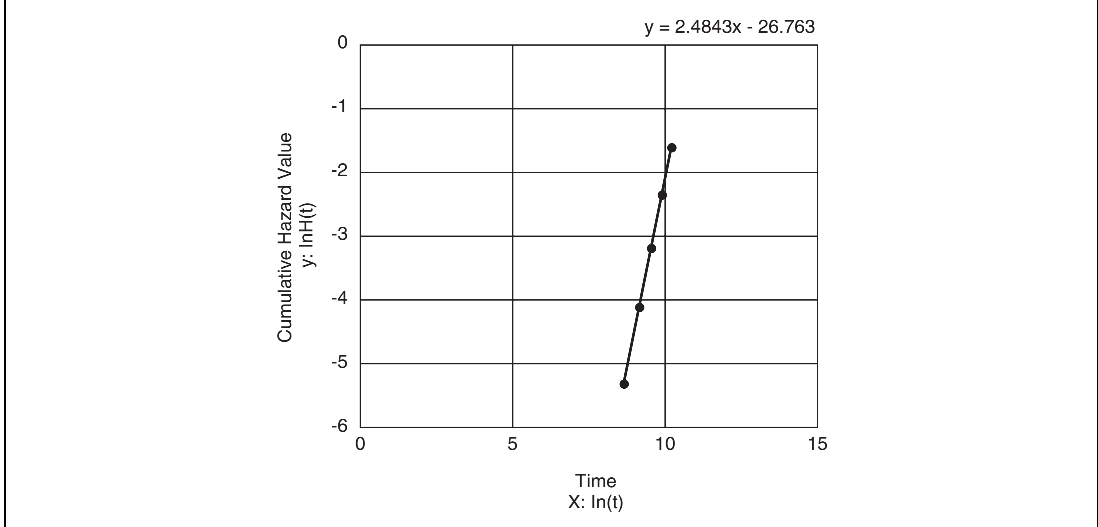

Figure 3.17 Lifetime Distribution from Weibull Cumulative Hazard Paper

From the relationship shown between the equations $y = 2.4843X - 26.763$ and $\ln H(t) = m(\ln t - \ln \eta)$, the following values can be determined:

Shape Parameter (m): 2.5

Scale Parameter (η): 47,700

3.4.3 Predicting Wear-Out Failures

Since the Weibull shape parameter (m) is larger than 1, rather than predicting the wear-out failure rate, it is more appropriate to predict the useful life of the product, which ends at the time wear out failures begin to occur. The products useful life is defined as the time until a certain number of cumulative failures occur, for wear-out failures occur. In Renesas terminology, the useful life is defined as the time when 0.1% of the cumulative failure rate is reached. Accordingly, the useful life (as defined here) of individual product is checked. In particular, for the known failure mechanisms, we identify the useful life at 0.1% of the cumulative failure rate during product design from environmental conditions under the actual operating state and by acceleration equations based on the failure mechanism. In the product approval testing phase, we also verify the useful life through the required number of samples in the Weibull distribution.

3.4.4 Future Product Life

If you conduct pre-shipment screening for a certain period of time (t), the product life as measured from the starting point (t_0) to its lifetime after (t_0) can be calculated in the following way. If you express the probability density function (PDF) available after the screening time (t_0) as $f(t_0{:}t)$, you obtain Equation (3-11). (See figure 3.18.)

$$f(t_0 : t) = \frac{f(t_0 + t)}{R(t_0)} \tag{3-11}$$

Note that $R(t_0)$ is the cumulative reliability function available until the time (t_0) is reached.

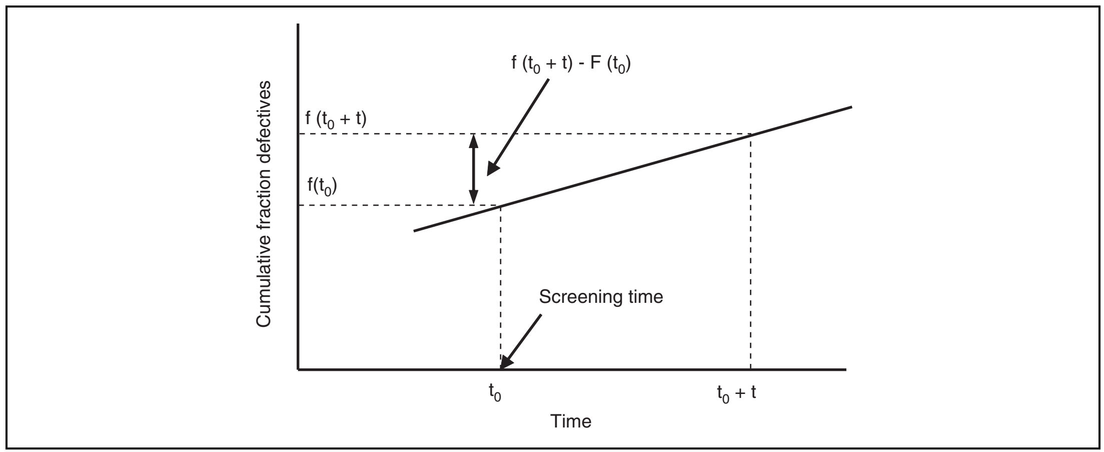

Figure 3.18 Future Product Life

If the probability density function, $f(t_0)$, has the Weibull distribution, the function can be expressed as

$$f(t_0) = \frac{m t_0^{m-1}}{\eta^m} e^{-\frac{t^m}{\eta^m}} \tag{3-12}$$

Substituting Equation (3-12) into Equation (3-11) gives the following probability density function:

$$f(t_0 : t) = \frac{m(t_0 + t)^{m-1}}{\eta^m} \bullet \exp\left(-\frac{(t_0 + t)^m - t_0^m}{\eta^m}\right) \tag{3-13}$$

The post-screening cumulative failure rate, $F(t: t_0)$, can therefore be expressed by Equation (3-14), from which you can estimate the future product life.

$$F(t_0 : t) = 1 - \exp\left(-\frac{(t_0 + t)^m - t_0^m}{\eta^m}\right) \tag{3-14}$$

References:

[1] JUSE Committee for Reliability Probability Paper: "Know-how in Using Probability Paper," Union of Japanese Scientists and Engineers (1981)

[2] Kimura: "How to Use Probability Plotting Paper," Ostrich Manufacturing Co. (1976)

[3] M. J. Howes and D. V. Morgan: "Reliability and Degradation (The Wiley Series in Solid State Devices and Circuits)," A Wiley-Inter Science Publication (1981)

[4] Koshikawa and Morimura: "Idea of a 60% Confidence Level and its Failure Rate Sampling Test Table," Publication of Inst. Electronics and Communication Engineers of Japan R69-20 (1970-2)

[5] JIS C 5003: "General Test Procedure of Failure Rate for Electronic Components," (1969)

[6] Hiroshi Shiomi: "Introduction to Reliability Engineering," (Revision 3) Maruzen Co., Ltd. (1995)

[7] Japan Electronics and Information Technology Industries Association (JEITA) Standard: " Failure Mechanism Driven Reliability Test Methods for LSIs," (EIAJ ED-4704) May 2005

Section 4 Failure Mechanisms

Reliability tests are designed to reproduce failures of a product which can occur in actual use. Understanding failure mechanisms from the results of reliability testing is extremely important to know the product is reliable in actual use. The effect of stresses (temperature, humidity, voltage, current etc.) on the occurrence of failures can be identified by understanding the failure mechanisms. The product reliability in actual use can be predicted from the results of the reliability tests, which are conducted under accelerated conditions. Reliability-affecting problems of the product can also be identified by clarifying the failure mechanisms. Such information is useful in improving the product design and manufacturing processes to enhance the product reliability and quality, as well as in determining precautions for use which must be made clear to the customers. Reliability testing also provides useful information for the manufacturer to screen products using an optimal method selected according to the identified failure mechanisms. Furthermore, in the event of a failure reported in the market, understanding of the failure mechanisms enables the manufacturer to take prompt and proper measures for correcting the design and/or manufacturing processes, so that the recurrence of the failure can be prevented.

This chapter introduces typical failure mechanisms of semiconductor devices that can be encountered in actual use.

4.1 Failure Classification

Statistical methods and methods for treating failure from a physical standpoint are used to analyze semiconductor device reliability. This approach is called the physics of failure. Its objective is to make failure mechanisms clear by understanding the physical characteristics of failure down to the atomic and molecular levels.

Semiconductor device failure modes are generally divided into open circuits, short circuits, degradation, and others. The relationship between these failure modes and their failure mechanisms is detailed in table 4.1.

Table 4.1 Failure Factors, Mechanisms, and Modes

Failure Factors		Failure Mechanisms	Failure Modes	Example
Diffusion Junction	Substrate Diffused junction Isolation	Crystal defect Impurity precipitation Photoresist mask misalignment Surface contamination	Decreased breakdown voltage Short circuit Increased leakage current	
Oxide film	Gate oxide film Field oxide film	Mobile ion Pinhole Interface state TDDB Hot carrier	Decreased breakdown voltage Short circuit Increased leakage current h_{FE} and/or Vth drift	Figure 4.1
Metallization	Interconnection Contact hole Via hole	Scratch or void damage Mechanical damage Non-ohmic contact Step coverage Weak adhesion strength Improper thickness Corrosion Electromigration Stress migration	Open circuit Short circuit Increased resistance	Figure 4.2
Passivation	Surface protection film Interlayer dielectric film	Pinhole or crack Thickness variation Contamination Surface inversion	Decreased breakdown voltage Short circuit Increased leakage current h_{FE} and/or Vth drift Noise deterioration	

Failure Factors		Failure Mechanisms	Failure Modes	Example
Die bonding	Chip-frame connection	Die detachment Die crack	Open circuit Short circuit Unstable/intermittent operation Increased thermal resistance	Figure 4.3
Wire bonding	Wire bonding connection Wire lead	Wire bonding deviation Off-center wire bonding Damage under wire bonding contact Disconnection Loose wire Contact between wires	Open circuit Short circuit Increased resistance	Figure 4.4 Figure 4.5
Sealing	Resin Sealing gas	Void No sealing Water penetration Peeling Surface contamination Insufficient airtightness Impure sealing gas Particles	Open circuit Short circuit Increased leakage current	Figures 4.6 and 4.7, Figure 4.8
Input/output pin	Static electricity Surge Over voltage Over current	Diffusion junction breakdown Oxide film damage Metallization defect/destruction	Open circuit Short circuit Increased leakage current	Figure 4.9
Others	Alpha particles High electric-field Noise	Electron-hole pair generation Surface inversion	Soft error Increased leakage current	

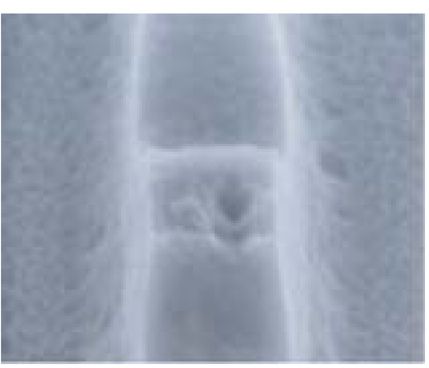

Figure 4.1 Gate Pinhole

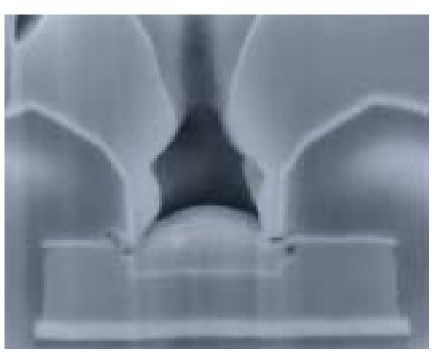

Figure 4.2 Al Wiring Coverage Disconnection

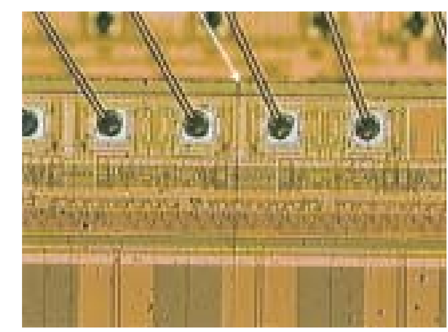

Figure 4.3 Crack

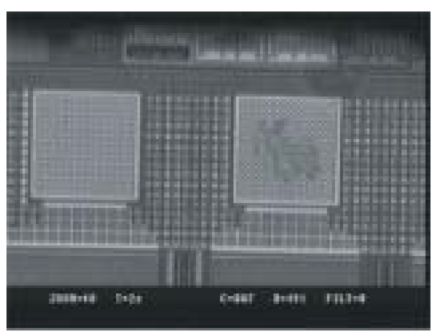

Figure 4.4 Damage under Bonding (Bottom View)

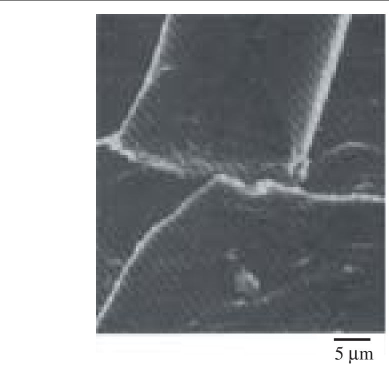

Figure 4.5 Damage on Wire Due to Ultrasonic Fatigue

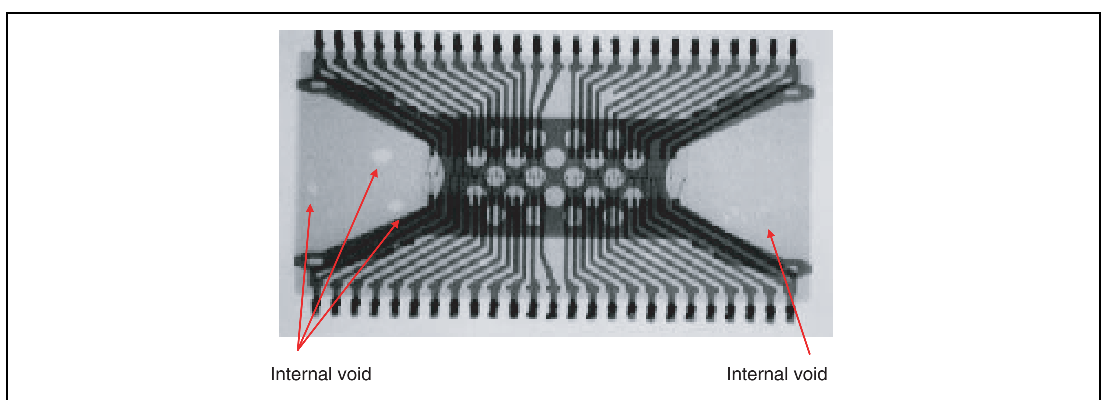

Figure 4.6 Internal Voids in Package

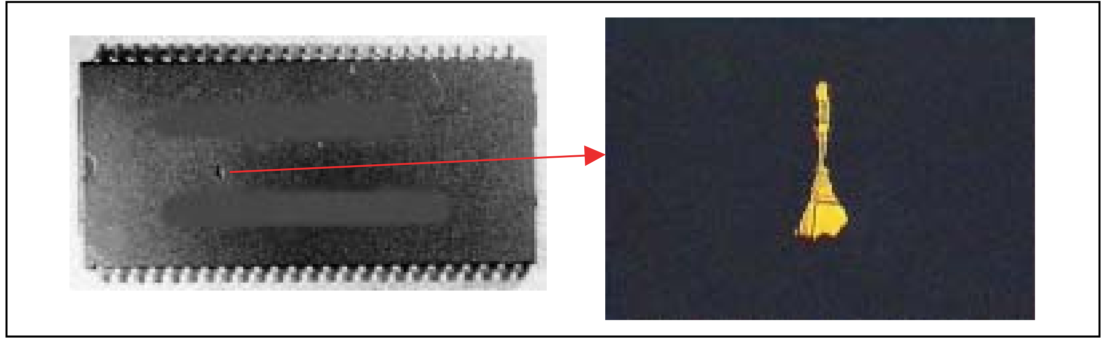

Figure 4.7 No Molding Resin Injected

Figure 4.8 Short Circuit Due to Conductive Particles in Package

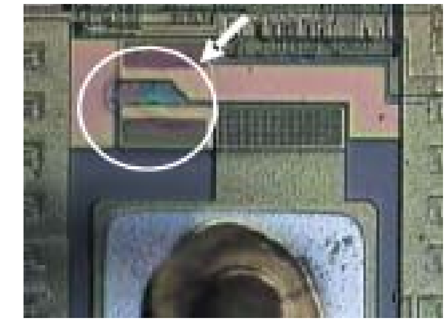

Figure 4.9 Terminal Breakdown Due to Overvoltage

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4.2 Failure Mechanisms related to the Wafer Process

As microfabrication technology continues to advance, the density of semiconductor devices increases. The scaling rule shown in table 4.2 has been used for microfabrication so far, but it tends to be unsuitable for scaling (lower supply voltage) from the standpoint of system requirements and the internal signal levels. As a result, the electric field of MOS FETs and the currents flowing in the wires become higher and the reliability of MOS devices takes on more importance than ever.

Table 4.2 Scaling Rule [1]

Parameter	Constant Electric Field Scaling Factor
Gate oxide film thickness	1/k
Gate length	1/k
Gate width	1/k
Junction depth	1/k
Impurity concentration	k
Voltage	1/k
Electric field	1
Current	1/k

Table 4.3 shows typical failure mechanisms related to the wafer process. The details of the respective failure mechanisms are described in the subsections that follow.

Table 4.3 Typical Failure Mechanisms related to the Wafer Process

Failure Mechanism	Activation Energy (eV)
Time-dependent dielectric breakdown (TDDB)	0.5 to 0.8
Hot carrier	—
NBTI	About 1
Al electromigration	0.6 to 1.0
Al stress migration	About 1
Soft error	—
Volatile failure of Nonvolatile memory	1 or more

4.2.1 Time Dependent Dielectric Breakdown [2] [3]

As the degree of integration increases, MOS gate oxide films become thinner. Supply voltages have also decreased, but the trend of miniaturization and improvement in performance resulted in higher electric fields across gate oxide films. Electric field intensity increases to about 4–5 MV/cm for sub-micron processes. Therefore, oxide film reliability becomes ever more important.

Good quality thermal oxide films have dielectric breakdown strength of 10 MV/cm or more. However, oxide film failure over time even in lower electric-field intensity (conditions of practical use) is a major cause of failure. Destruction occurring over time is called TDDB (time dependent dielectric breakdown). The time-dependent destruction of the oxide film (dielectric film) is one of major causes of failure.

(1) Failure Phenomena

Because stressing an actual product under accelerating conditions to evaluate its TDDB phenomena is difficult, a specially designed TEG (test element group) is used for this purpose.

Figures 4.10 and 4.11 show the results of a TDDB evaluation. The time-to-failure decreases with increased electric field or temperature.

Empirically, the following equation is often used as the TDDB failure model equation:

$$MTTF = A \times 10^{-\beta E} \times e^{Ea/(kT)} \quad (4\text{-}2\text{-}1)$$

where

MTTF: Mean time to failure (h)

A: Constant

Ea: Activation energy (eV)

E: Electric field intensity (MV/cm)

ß: Electric field intensity coefficient (cm/MV)

k: Boltzmann constant

T: Absolute temperature (°K)

For TDDB acceleration, it has been reported that, in reality, the less the electric field, the higher the activation energy (Ea), as shown in figure 4.12.[4] [5] Ea obtained at a high stress results in a difficult forecast for the market with equation (4-2-1). We are applying values obtained from TEG evaluations corresponding to the respective processes, and we have obtained 0.5 to 0.8 eV in evaluations in high electric fields for the activation energy, and 1 to 2 for the electric field intensity coefficient β (cm/MV).

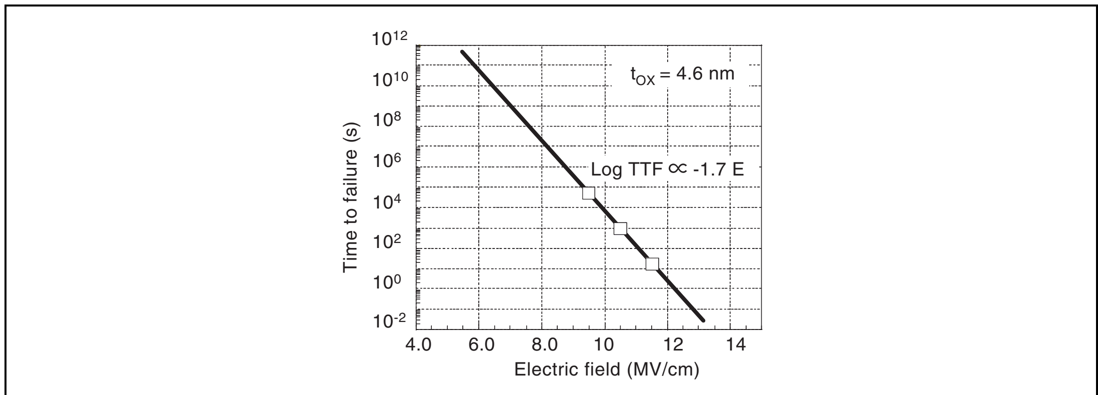

Figure 4.10 Electric Field Dependency of TDDB

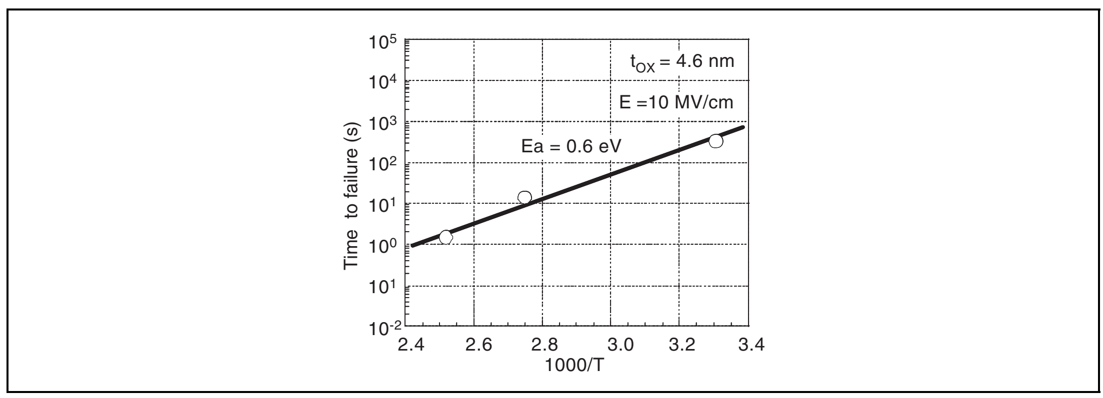

Figure 4.11 Temperature Dependency of TDDB

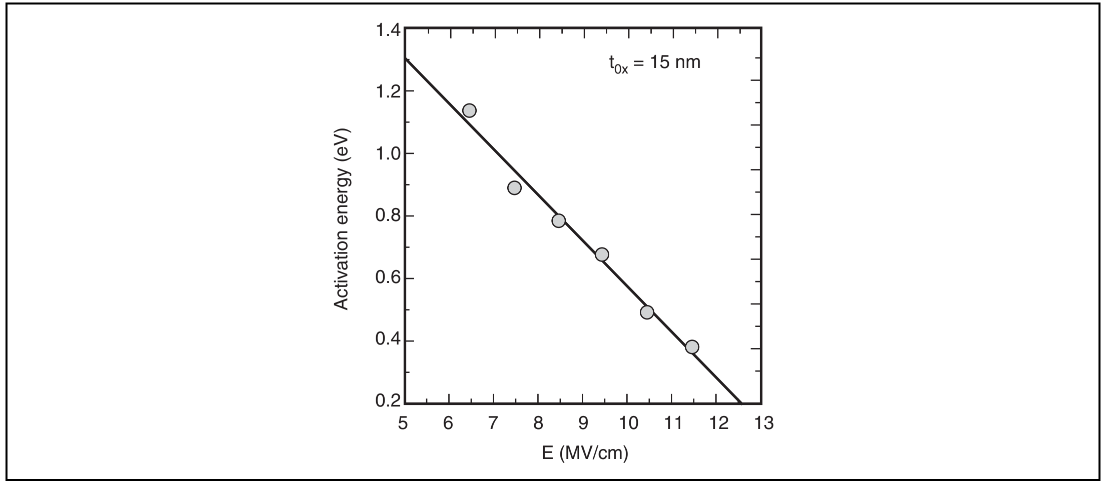

Figure 4.12 Electric-Field Dependency of Activation Energy[5]

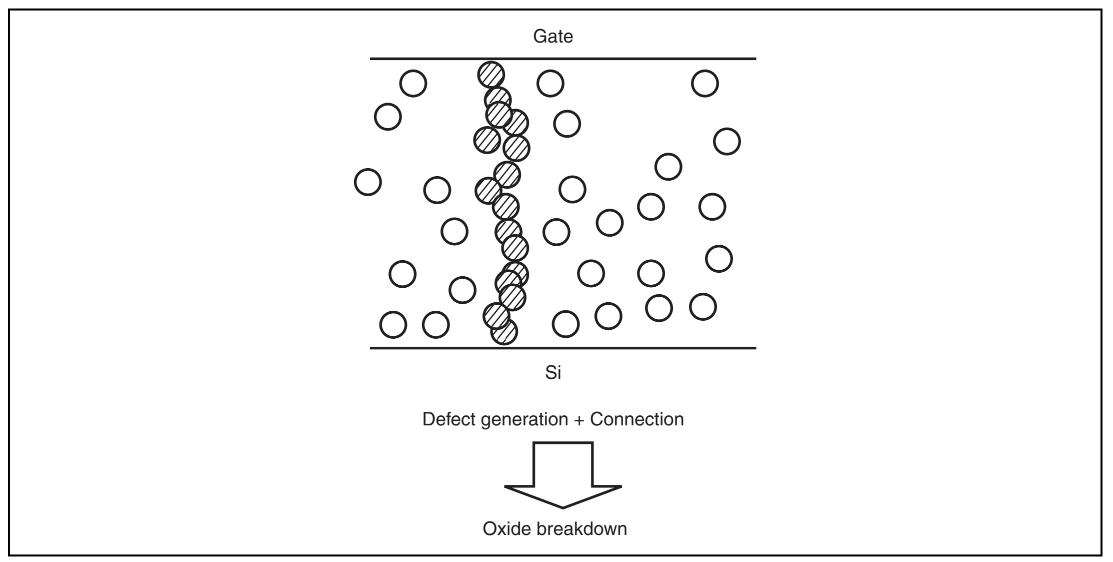

Figure 4.13 Dielectric Breakdown Mechanism[6]

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(2) Failure Mechanism

Although a variety of models have been examined for the TDDB failure mechanism, recently the percolation model has gained favor as the qualitative mechanism.

An electric field applied to an oxide film causes the injection of holes into the oxide film to occur on the anode side, and it consequently causes traps to be made in the oxide film. As the number of traps increases, an electric current via the traps is observed as an SILC (Stress Induced Leakage Current) due to hopping or tunneling. It has been reported that if the number of traps continues to increase and the traps connect between the gate electrode and the Si substrate, the connection carries a high current that causes the gate oxide film to break down (figure 4.13[6]).

Because the level of the traps (i.e. defect) in an oxide film strongly influences TDDB, it is necessary to characterize the oxide film quality with accelerated tests and feed the results into design rules. From the standpoint of the process, it is important to use SiO_2 film, which does not easily produce defects, and to develop a method of forming an oxide film thereby.

4.2.2 Hot Carrier

Although the density of semiconductor devices is increasing with advances in microfabrication technology, the supply voltage tends to be unsuitable for scaling (lower supply voltage) from the standpoint of system requirements and the reduction of internal signal levels.

Promoting miniaturization without scaling the supply voltage implies increasing the electric field intensity of the internal elements of a device. This is especially true in the case for MOS FETs, where the electric field intensity near the drain area increases and a hot carrier degradation effect occurs.

Carriers (electrons or holes) that flow into the high electric field area are accelerated by the strong field and gain substantial energy.

Some of the carriers become hot carriers, which means they have enough energy to overcome the electric potential barrier existing between the Si substrate and gate oxide film.

These hot carriers are injected into the gate oxide film (some are trapped), form a space charge, and over a period of time cause a change or degradation of MOS FET characteristics such as threshold voltage (V_{th}) and transconductance (gm).

These degradations cause the deterioration of all semiconductor device characteristics and ultimately lead to failure.

Injected carriers which are not trapped become gate current, while carriers flowing into the substrate are detected as substrate current.

Figure 4.14 illustrates hot carrier injection mechanisms. Figure 4.14 illustrates two major mechanisms: drain avalanche hot carrier injection and channel hot electron injection.

1. Drain avalanche hot carrier (DAHC) injection[7] [8]
2. Channel hot electron (CHE) injection[9]
3. Secondary generated hot electron (SGHE) injection[9] [10] [11]
4. Substrate hot electron (SHE) injection[12]

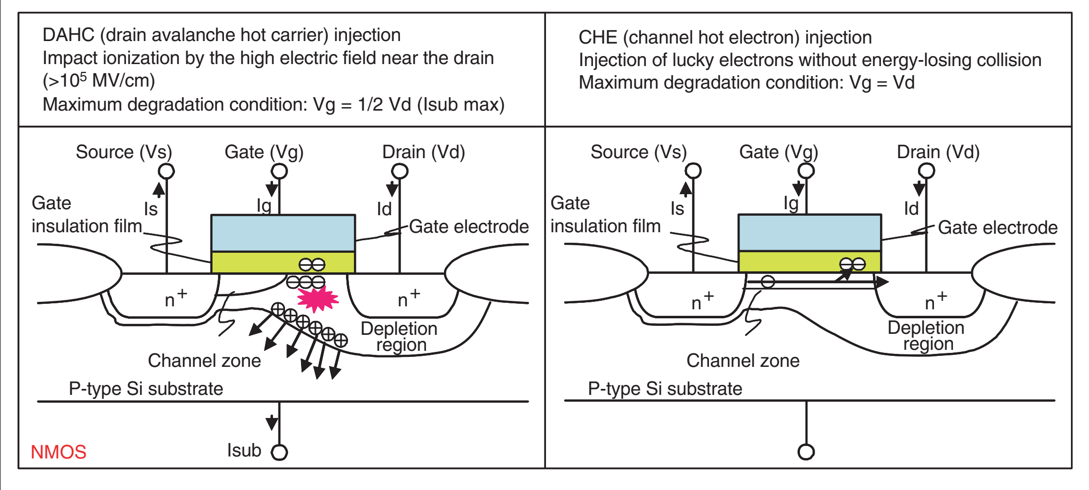

Figure 4.14 Major Mechanisms of Hot Carrier Generation

The hot carrier phenomenon will be explained using DAHC as an example, since it causes the worst degradation in the normal operating temperature range. Assume a sample case in which a high voltage is applied to a MOS FET drain with $V_G<V_D$ (equivalent to the case in which the channel does not extend to the drain edge and the gate voltage is less than the drain voltage), as shown in figure 4.14.

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A high electric field area is formed near the drain when a high voltage is applied to the drain. Electrons flowing out of the source cause impact ionization by the high electric field near the drain and generate electron-hole pairs. Most of the holes flow toward the substrate, becoming substrate current, but some electrons that gained high energy overcome the potential barrier and are injected into the oxide film where they become trapped. This causes degradation of the MOS FET threshold (V_{th}), transconductance (gm), etc., and leads to degradation of the Vcc minimum voltage in products. As shown in figure 4.15, the higher the drain voltage (power supply voltage from the point of view of a product), the greater the deterioration.

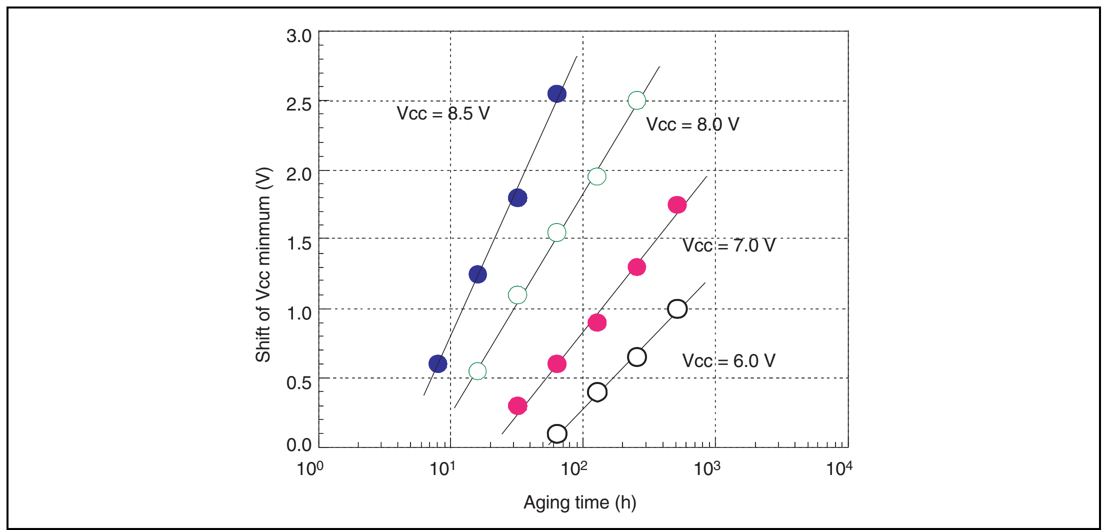

Figure 4.15 Supply Voltage (Drain Voltage) Dependency of Degradation

Typical equations for the life t of the degradation due to the hot carriers are as shown below. Values often reported are 3 or so for m and 100 to 200 for B.

$$t = C \times Isub^{-m} \qquad (4\text{-}2\text{-}2)$$

$$t = A \times e^{-B/Vds} \qquad (4\text{-}2\text{-}3)$$

where

A, B, C, and m: Constants

Isub: Substrate Current

Vds: Drain Voltage

In addition to the factors that influence hot carrier degradation, such as supply voltage and channel length, the ambient temperature and the presence of hydrogen in the protective films must also be considered.

Most semiconductor failure factors accelerate as temperature increases. However, hot carrier degradation tends to increase as temperature decreases. Specifically, when stress is applied to a MOS FET at low temperature (when the actual product is operated so that the stress is applied to the internal MOS FET), thermal vibration of the silicon lattice vibrations is reduced in comparison with high-temperature conditions, so the probability of collisions between electrons flowing in the Si substrate and the lattice is also reduced. This increases the mean free path in which the electrons travel, allowing them to absorb more energy.

Consequently, the number of high-energy hot carriers increases and the probability of carriers being injected into the oxide film becomes greater. In addition, impact ionization more readily occurs, so the number of secondary electrons is also increased. Since these secondary electrons become hot electrons, the number of carriers that are injected and trapped in the oxide film increases. In this way, degradation due to hot carriers is actually accelerated at low temperatures, making the evaluation of hot-carrier degradation under low temperature conditions important. However, with miniaturization, as the supply voltage decreases, the impact ionization mode has been changing so that a lower temperature does not always lead to severe conditions.[13] [14]

In advanced LSI chips, MOS FETs with the LDD (Lightly Doped Drain) structure shown in figure 4.16 have been used as a way to improve hot carrier degradation. This structure can reduce the field concentration at the drain edge of the MOS FET. In addition, as a device in the design stage, channel length is designed longer for MOS FETs in circuits with high electric-field intensity, and internal timing configurations are optimized in integrated circuits to reduce the occurrence of the hot carrier phenomenon.

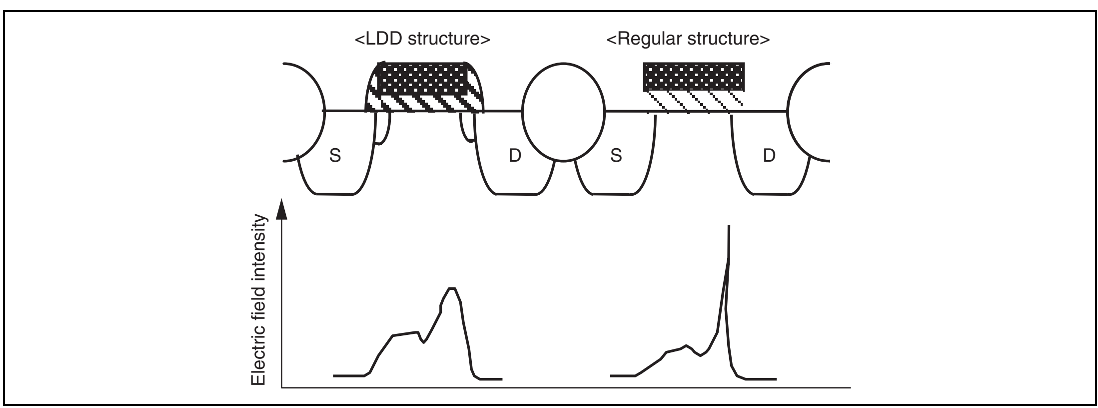

Figure 4.16 LDD Structure

4.2.3 NBTI (Negative Bias Temperature Instability)

Degradation (Vth/Gm shift) occurring due to negative biased BT (bias temperature) stress in P-MOS FETs is called the NBTI phenomenon. This phenomenon has become more obvious as the electric field intensity of internal MOS FETs has increased with the progress of miniaturization. It now counts as an important reliability factor.

(1) Failure Phenomenon

It has been reported that degradation due to the P-MOS FET NBTI phenomenon (Vth/Gm shift) is the result of an increase of the interface state and an increase of the positive charge in the gate oxide film.[15] [16] [17] [18]

The Vth degradation life τ in the NBTI phenomenon has a strong dependence on the gate electric field, and, in general, the following failure model equation is often used:

$$MTTF = A \times 10^{-\beta E} \times e^{Ea/(kT)} \qquad (4\text{-}2\text{-}4)$$

where

MTTF: Mean time to failure in hours (h)
A: Constant
E: Electric field intensity (MV/cm)
k: Boltzmann constant
Ea: Activation energy (eV)
β: Electric field intensity coefficient (cm/MV)
T: Absolute temperature (K)

In reality, however, the smaller the electric field, the higher the electric field dependence, as shown in figure 4.17, with the dependence proportional to the exponentiation of the electric field (the power law model).[19] Using β, obtained under a high stress in equation (4-2-4) results in a difficult market forecast. Although there is some slight variation due to the process, we have obtained approximately 1 eV for the activation energy and 1 to 1.5 for the electric field intensity coefficient β (cm/MV).

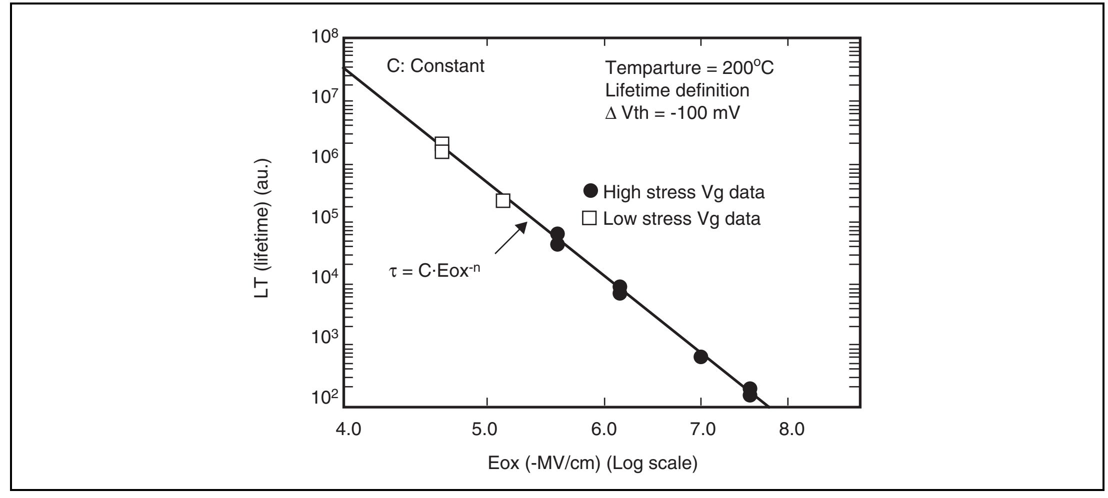

Figure 4.17 Electric field Dependency of Device Life[14]

(2) Failure Mechanism

The mechanism of the P-MOS FET NBTI phenomenon is thought to be as described below.[20]

The Si dangling bond on the SiO_2-Si interface is inactivated by hydrogen and exists as Si-H, but stress from a high temperature and a high bias and the existence of holes give rise to an electrochemical-reaction that frees the hydrogen. In this sequence, the Si dangling bond (Si^+) becomes an interface state and the hydrogen diffuses into the oxide film. Some of the diffusing hydrogen in the oxide film joins with defects in the oxide film to form traps. This increase of the interface state and the charge resulting from the traps in the oxide film are considered to be the factors that lead to Vth/Gm degradation.

Recovery from the Vth/Gm degradation caused by the NBTI phenomenon can be accomplished by removing the stress bias and applying a reverse bias.[21] [22] [23]

Accordingly, the NBTI phenomenon is particularly important in circuits in which DC stress is applied.

4.2.4 Electromigration

Most semiconductor integrated circuits use Aluminum (Al) metallization wires for their interconnects. Electromigration is a design concern for semiconductor integrated circuits because Al metallization films have a polycrystalline configuration with many grain boundaries. In addition, advances in function, speed, and processing on the sub-micron level have caused the current density in the Al metallization to increase to as much as 10^4 to 10^5 A/cm^2.

Electromigration is a phenomenon of the movement of metal atom due to the current flow in a metallization wire. In Al metallization wire, Al atoms move in the direction of electron flow. A void occurs near the negative electrode, and an open failure results. Near the positive electrode, hillocks are created, which lead to a short-circuit failure. Figure 4.18 shows a failure mechanism and figure 4.19 shows a photographic example.

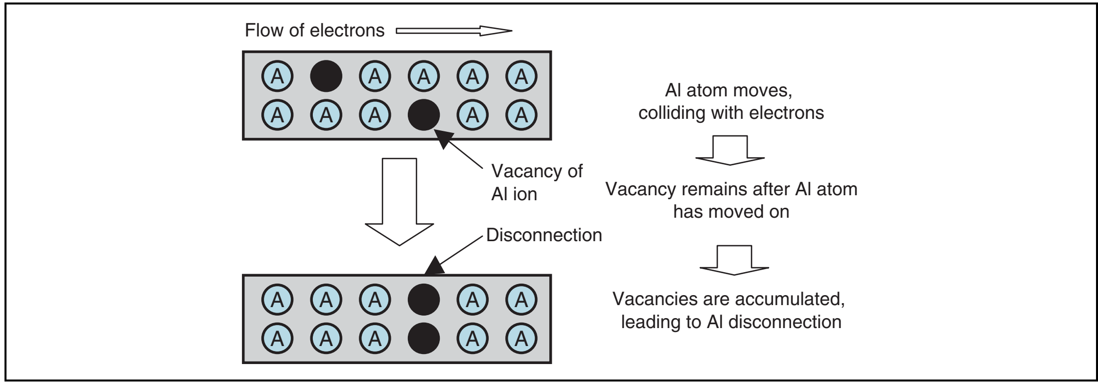

Figure 4.18 Failure Mechanism

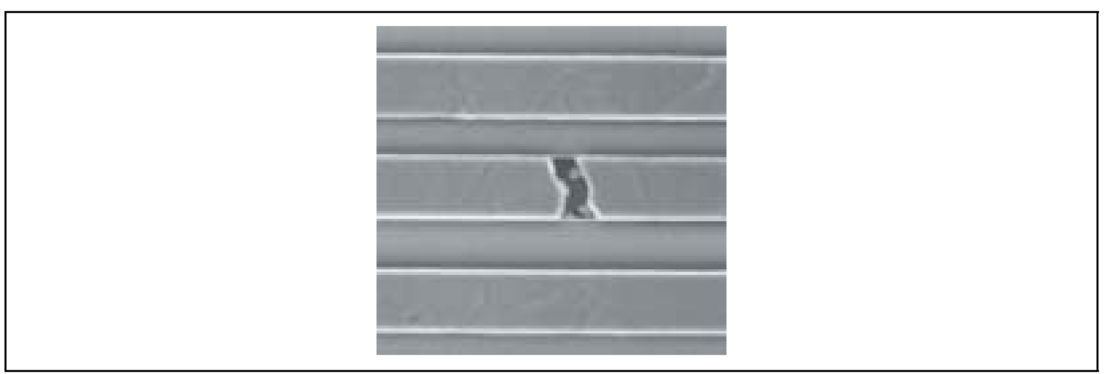

Figure 4.19 Electromigration of Al Wire

Al metallization wire has polycrystalline structure and diffusion of metal atoms is of three different types: lattice, grain boundary, and surface diffusion. See figure 4.20. In polycrystalline films there are many grain boundaries with possible defects and the metal atoms move easily on grain boundaries. Therefore, grain boundary diffusion is a primary factor of the electromigration in Al metallization wire. The thinner the films are, the greater the ratio of surface to volume of the conductor becomes, thus increasing the importance of surface diffusion.

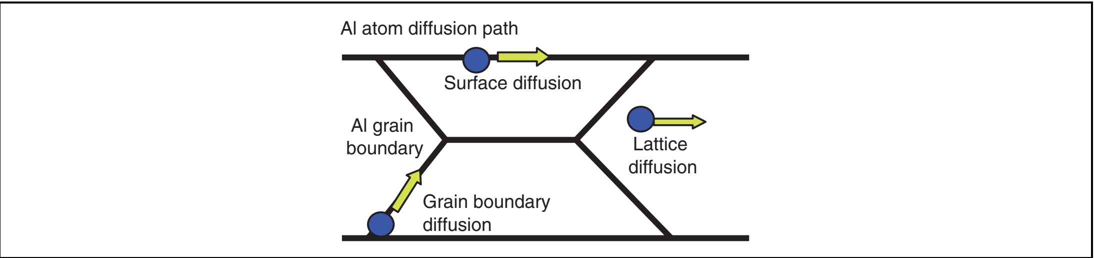

Figure 4.20 Lattice Diffusion, Grain Boundary Diffusion, and Surface Diffusion of Polycrystalline Al

The electromigration failure model equation is expressed (4-2-4) as

$$MTTF = A \times J^{-n} \times e^{Ea/kT} \qquad (4\text{-}2\text{-}5)$$

MTTF: Mean Time to Failure (h)

A: Constant Determined by Metallization Material and Structure

n: Constant (n = 2: refer to J. R. Black [24] [25])

Ea: Activation Energy (eV)

k: Boltzmann Constant

T: Absolute Temperature of Metallization (°K)

For the temperature dependency, an Ea value of 0.6 to 1.0 eV has been confirmed.[26] [27] [28]

Tolerance of electromigration, which has seemed to have reached the limits of miniaturization, is being improved by laminating layers of refractory metals like tungsten (W) and titanium (Ti) as barrier metals on the lower layer or upper layer, or on both layers of Al wiring, adding Cu to Al wiring (suppression of grain boundary diffusion), and using tungsten plugs or the like in via-holes.

4.2.5 Stress Migration

Stress migration is the phenomenon in which metal atoms migrate in the presence of thermal stress alone, with no electric current applied.[29] [30] Stress migration is caused by stress that occurs from a difference of the thermal expansion coefficients between the passivation film or interlayer dielectric film and Al wiring. Figure 4.21 shows the mechanism. The passivation film on the wiring causes tensile stress on the wiring, resulting in the movement of A1 atoms, the formation of voids, and eventually a disconnection. The lower the temperature, the greater the stress; the higher the temperature, the easier it is for the metal atoms to move. Consequently, long-term storage at a moderate temperature between 150°C to 200°C results in stress migration. This mode is referred to as the low-temperature long-term mode, which usually creates a slit-shaped disconnection. The thinner the wiring width, the more frequently the phenomenon occurs.[31] [32] There is also a high-temperature short-term mode that causes a wedge-shaped void in the heating process in semiconductor device production. Figures 4.22 and 4.23 show failure examples.

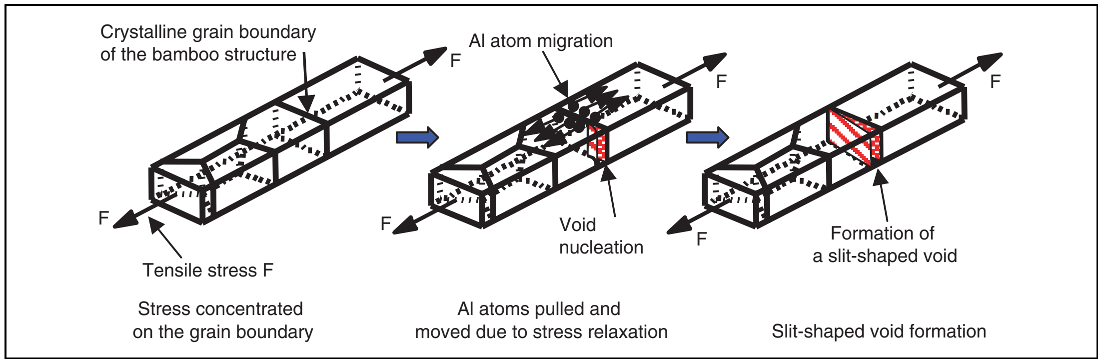

Figure 4.21 Mechanism of Slit-Shaped Void Formation

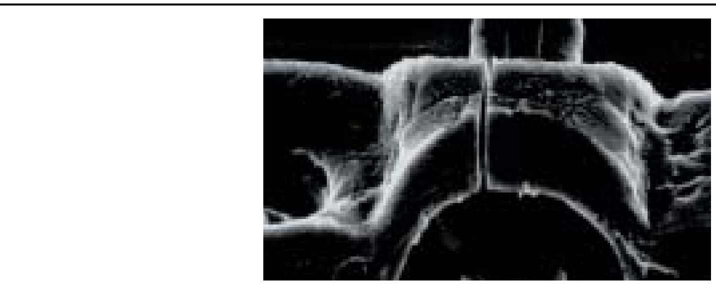

Figure 4.22 Slit-Shaped Void

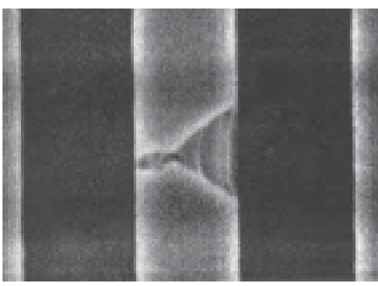

Figure 4.23 Wedge-Shaped Void

As with electromigration, stress migration tolerance is improving by the application of barrier metals, the addition of Cu to Al wiring (suppression of grain boundary diffusion), and the use tungsten plugs or the like for via-holes.

4.2.6 Soft Error

(1) Soft Error Caused by Alpha Particles

One of the problems which hinder development of larger memory sizes or the miniaturization of memory cells is the occurrence of soft errors that cause temporary malfunction due to alpha particles. This phenomenon was first described by T. C. May. [37]

U (uranium) and Th (thorium) are contained in very low concentrations in package and wiring materials and emit alpha particles that inverse memory data.

When alpha particles impinge on the memory chip, a large concentration of electron-hole pairs is generated in the silicon substrate and these electron-hole pairs are separated by the electric filed as shown in figure 4.24. If a PN-junction is present close to this place, the electrons move to the N-layer and the holes move to the P-layer. Finally, the memory information is reversed and a malfunction occurs. This error is not a permanent breakdown but recovered to normal operation by writing again.

Inversion of memory information is shown in figure 4.24.

The generated holes are pulled towards the substrate to which a negative potential is applied. Conversely, electrons are pulled to the data storage node to which a positive potential is applied. A dynamic RAM filled with charge has a data value of 0. An empty or discharged cell has a value of 1. Therefore, a data change of 1 $\rightarrow$ 0 occurs when electrons are accumulated in the data storage node. Such a malfunction is called the "memory cell model" of a soft error.

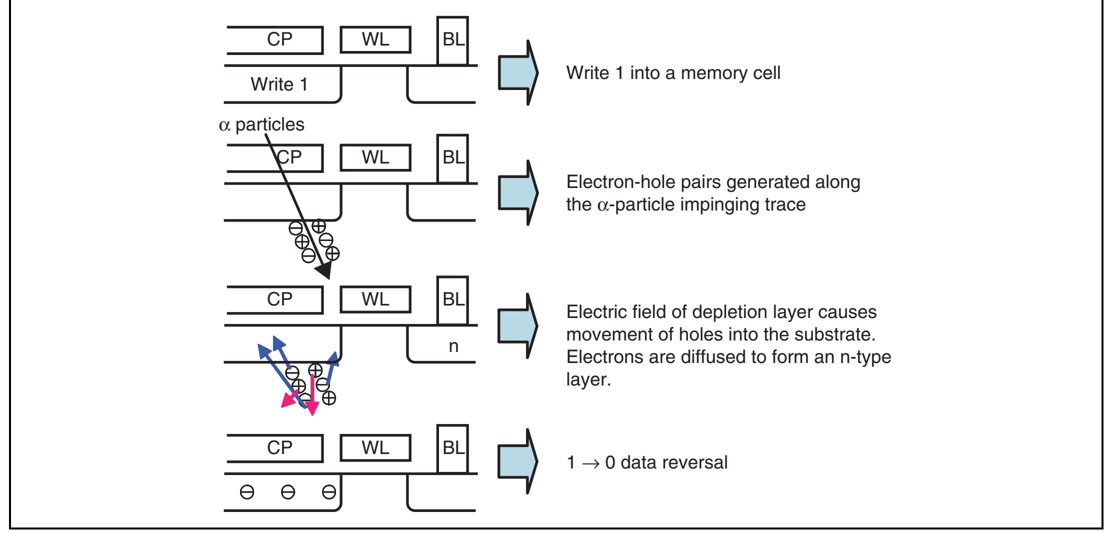

Figure 4.24 Incorrect Operation in Memory Cell

The "bit line model" occurs due to a change of the bit line electric potential.

The bit line's electric potential varies with the data of the memory cell during readout, and is compared with the reference potential, resulting in a data value of 1 or 0. A sense amplifier is used to amplify the minute amount of change.

If α-particles impinge on the area near the bit line during the extremely short time between memory read-out and sense amplification, the bit line potential changes. An information 1 → 0 operation error results when the bit line potential falls below the reference potential. Conversely, if the reference potential side drops, an information 0 → 1 operation error results.

The memory cell model applies only to information 1 → 0 reversal, while the bit line model covers both information 1 → 0 and 0 → 1 reversals. The generation rate of the memory cell model is independent of memory cycle time because memory cell data turns over. Since the bit line model describes problems that occur only when the bit line is active at data read-out, increased frequency of data read-out increases the potential for soft errors, i.e. the bit line model occurrence rate is inversely proportional to the cycle time.

(2) Soft Error Evaluation Methods

Evaluating soft errors due to α-particles is an important element of memory reliability.

Field tests using actual memory devices are the best source for evaluating memory soft error failure rates, but they require large sample sizes and long monitoring times. Specifically, a minimum of 20,000 hours and a sample size of 500 are required to evaluate the soft error rate of a product with a reliability performance of several hundred FITs.

For that reason, soft error rates are evaluated with two methods. One is the field test with a representative product for a manufacturing process. The other is accelerated test method with an α-particle source for quick evaluation. Figure 4.25 shows a test system. An α particle source is placed over the test chip and evaluated.

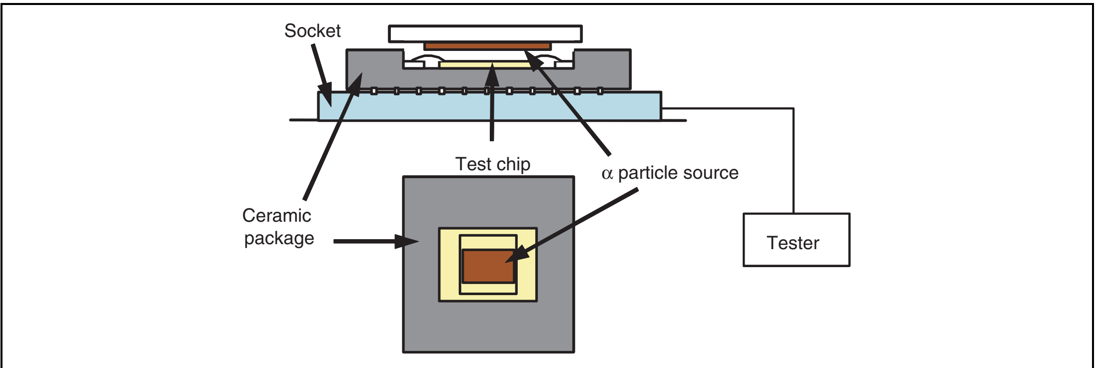

Figure 4.25 Accelerated Soft Error Evaluation System

(3) Countermeasures for Soft Errors

Methods for reducing memory soft errors due to α-particles include

1. Reduction of α-particles emitted from the highly pure materials for a package or wiring
2. Coating the chip surface with a material to block α-particle radiation from the package material
3. Reduction of the memory device's sensitivity to α-particles

The objective is to reduce α-particle emission, so chip coat technology is becoming indispensable in large memory sizes. In order to prevent radiation from the package material from reaching the chip, the chip surface is coated with a material that does not contain radioactive elements such as U or Th.

Renesas uses a polyimide coating as a countermeasure to α-particles. Figure 4.26 shows the effectiveness of polyimide film for prevention of soft errors. The failure rate decreases as polyimide film thickness increases.

In addition, the amount of accumulated charges that are used as memory cell data should sufficiently be assured to improve the resistivity to α-particles.

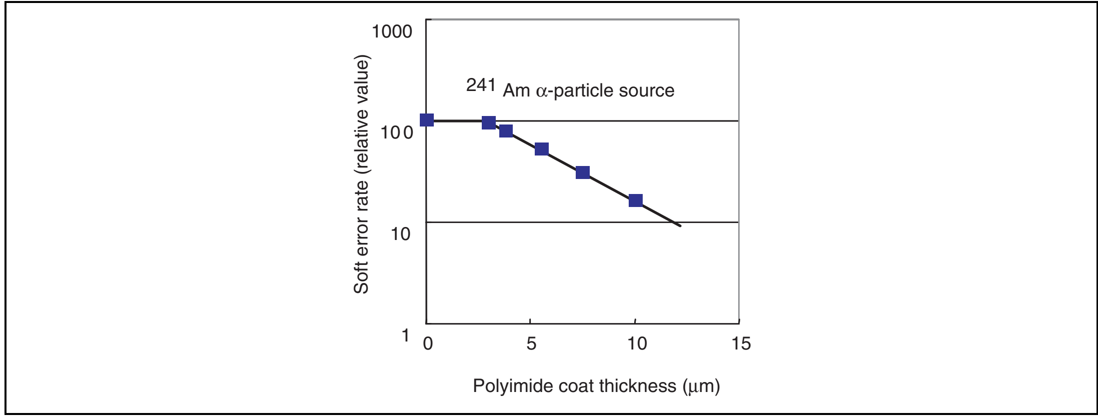

Figure 4.26 Soft Error Prevention Effect of Polyimide Coating

The main point of strengthening memory devices against α-particles is to maintain sufficient charge per bit.

However, the area occupied by one memory cell decreases as memory capacity increases, so it becomes ever more difficult to maintain sufficient charge per bit.

New memory cell configurations with trench and/or stack structures and improved dielectric films, instead of oxide films, are being used to maintain the charge and reduce sensitivity to α-particles.

More recently, other cosmic rays (mainly neutrons) and their effects on memory devices have become a matter of concern due to device miniaturization and low-voltage operation. [38] In response, JEDEC has released specifications of an evaluation method (JESD89), and JEITA in Japan is trying to standardize evaluation methods.

4.2.7 Reliability of Non-Volatile Memory

Non-volatile memories retain their data mainly by accumulating electrons in a floating gate within the memory cell, such as stack-type gate memory of figure 4.27, or by accumulating electrons/holes in an MNOS/MONOS gate, such as MNOS/MONOS-type gate memory of figure 4.28.

In recent years, FRAM with the polarization characteristics of ferroelectric materials, phase-change memory, and magnetic memory (MRAM) have been developed as non-volatile devices of the next generation.

The principle of writing into flash memory (stack type gate) is described in the next paragraph.

Generally electron injection into the floating gate of a flash memory is accomplished by supplying high voltages to the drain (V_D) and control gate (V_G), while the source is at ground potential (figure 4.27). Electrons flowing from the source gain sufficient energy in the high electric-field area near the drain to generate electron-hole pairs by impact ionization.

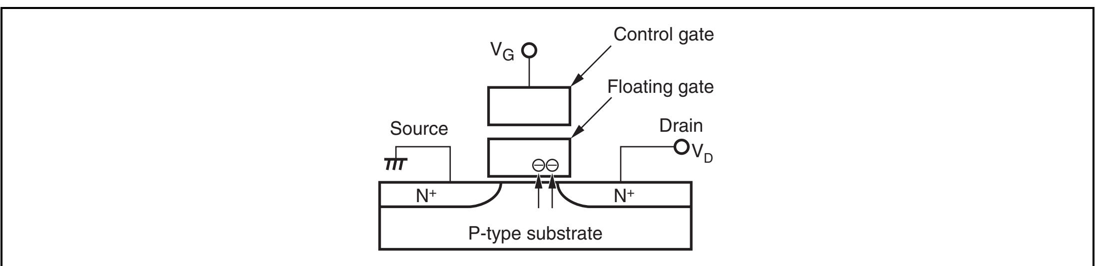

Figure 4.27 Stack Type Memory Cell Cross-section

The generated electrons are injected into the floating gate due to the high voltage on the control gate. Since the floating gate is insulated from its surroundings, the electrons become isolated.

The condition under which electrons were injected (write) is defined as data 0. A data 1 condition exists when electrons are not injected (erase).

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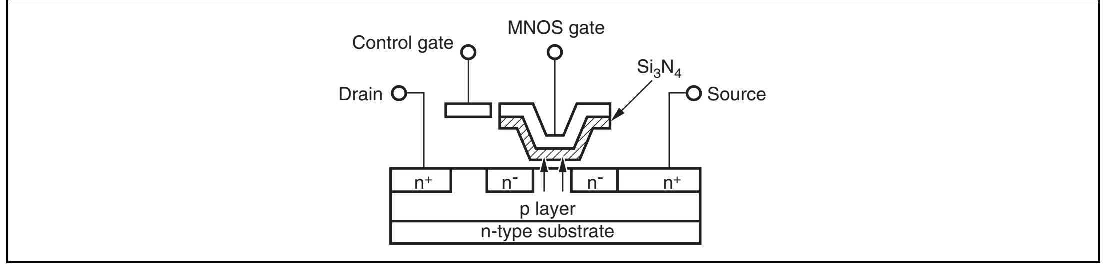


Figure 4.28 MNOS Memory Cell Cross-section

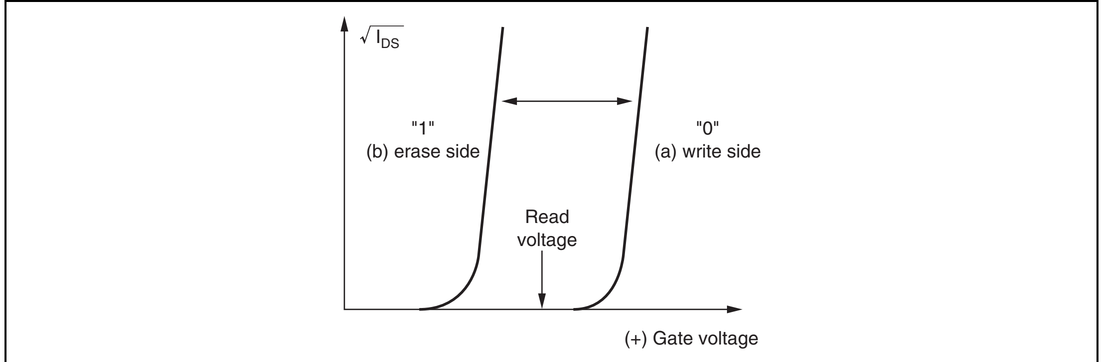


Figure 4.29 Stack-Type Memory Cell Vth Change

The write and erase conditions are shown with relation to memory threshold value (V_{th}) in figure 4.29. The threshold voltage V_{th} of a memory cell is high for written state, and low for the erased state.

(1) Data Retention Characteristics

Writing to stack-type gate memory is accomplished with hot electrons (or FN tunneling).

Although the ability to retain the written condition (electrons isolated in the floating gate) for long periods of time is expected, there is a finite probability that electrons stimulated by heat will be lost because the written condition is essentially non-equilibrium. Electrons isolated in the floating gate gain sufficient thermal energy to overcome the energy barrier of the surrounding oxide film. Consequently, the higher the energy barrier between the floating gate and the surrounding oxide film, the better the ability of the cell to retain data.

The thermionic excitation model expresses the loss of electrons from the floating gate due to thermal excitation (4-2-6):

$$V_{CC}(t)/V_{CC}(0) = N(t)/N(0) = \exp\,[-\nu \bullet t \bullet \exp\,(-Ea/kT)] \quad (4\text{-}2\text{-}6)$$

where

V_{CC}: Maximum operating voltage

N: Amount of charge on the floating gate

ν: Relaxation frequency (10^{12} cycles per second)

Ea: Activation energy (eV)

k: Boltzmann constant

T: Absolute temperature

The time in this data retention model has a strong correlation with temperature. In general, the Ea (activation energy) related to data retention characteristics is estimated to be 1 eV or greater.

(2) Failure Mechanisms

Data retention for ten years or more is the target specification if the device is operated within its specified operating temperature range.

However, if there are defects near the floating gate, the memory may not be able to retain data as mentioned above and a failure may occur due to charge loss or gain within a relatively short time period.

Causes of degradation in data retention characteristic can be divided into four broad categories:

1. Charge loss/gain due to an initial defect in the oxide film
2. Data retention degradation due to ionic contamination
3. Data retention degradation due to excessive electrical stress
4. Data retention degradation due to stress from too many writes/erasures

A defect (leakage path, particles, etc.) within the gate oxide film (figure 4.30) leads to gain or loss of charge because electrons are attracted from the substrate to the floating gate when a bias voltage is applied to the control gate.

If the defect is in the interlayer film, (figure 4.31), no failure occurs in the erased state, but failure is possible in the written state due to the loss of electrons from the floating gate through the defect.

Failure for both modes can occur in a short time at high temperatures. It is possible to eliminate initial data retention failures by the use of high-temperature baking (screening) at the manufacturing process.

Loss of electrons from the floating gate can also be caused by ionic contamination in the oxide film. The high-temperature baking (data 1 and 0 mixed pattern) is an effective screen for this failure mode also.

Another type of data retention degradation occurs in stack-type gate memory.

During each write/read cycle, high-energy electrons or holes pass through the oxide film. If this write/read cycle is repeated often enough (typically 1000 times or more), it is probable that electrons or holes will become trapped in the oxide film, reducing the difference between the threshold values of the 1 and 0 states. This causes an intrinsic degradation of data retention characteristics.

Furthermore, because the difference between the threshold values is reduced as the number of writes/erasures increases, there is a natural limit on the number of writes/erasures performed for stack-type gate memory. Accordingly, it is more effective for better reliability if rewrite counts are suppressed during use.

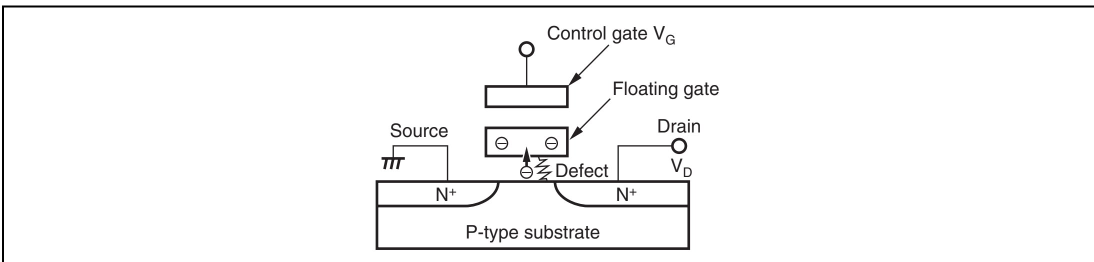


Figure 4.30 Gate Oxide Defect Mode (Charge Gain)

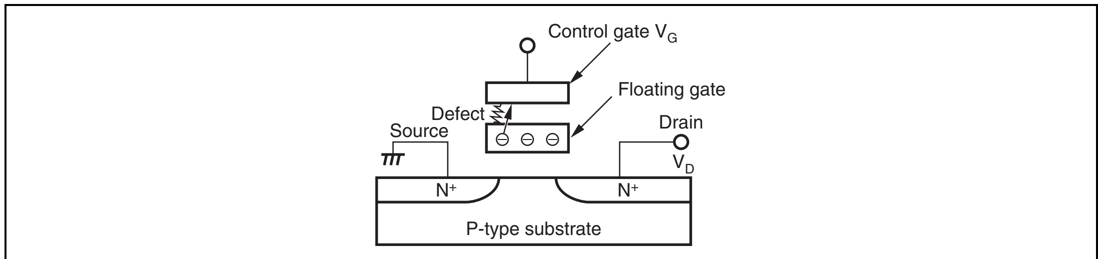


Figure 4.31 Interlayer Film Defect Mode (Charge Loss)

4.3 Failure Mechanisms related to the Assembly Process

4.3.1 Wire Bonding Reliability (Au-Al Joint Reliability)

(1) Introduction

To assemble a semiconductor device, a semiconductor chip is first die bonded on the die pad of a package, and then a surface electrode (Al pad) of the semiconductor chip and an inner lead (Ag or Au plated) of the package are bonded and connected with each other by using a fine metal wire (Au or Al). In the past, most of the semiconductor failures were attributed to the wire bonding process; however, recent technological progress in wire bonding is remarkable, with improvement in accuracy of the manufacturing equipment and automation of the manufacturing processes dramatically increasing the reliability of wire bonding.

Automated wire bonding removes dispersion in quality by worker, reducing the initial joint failures during manufacturing significantly. It is known, however, that in the joint made of an Au-Al binary system, the formation of an intermetallic compound causes a structurally unavoidable long-term life degradation phenomenon to occur; the intermetallic compound is generally known as purple plague.

This section explains the reliability of wire bonding in relation with the progress of diffusion of the Au-Al alloy.

(2) Theory

In the Au wire method, the joint between the Al electrode on a semiconductor chip and the Au wire forms an Au-Al joint. For such an Au-Al joint, it is known that long-term storage of a semiconductor device at a high temperature causes the contact resistance of the joint to increase, eventually resulting in breaks in the joint. Many instances of such failures have been reported because the breaks have led to fatal failures in the equipment in which a joint has been used.

In an Au-Al alloy joint, it is known that several intermetallic compounds are formed, as shown in figure 4.32. Table 4.4 shows the characteristics of intermetallic compounds, Au, and Al.

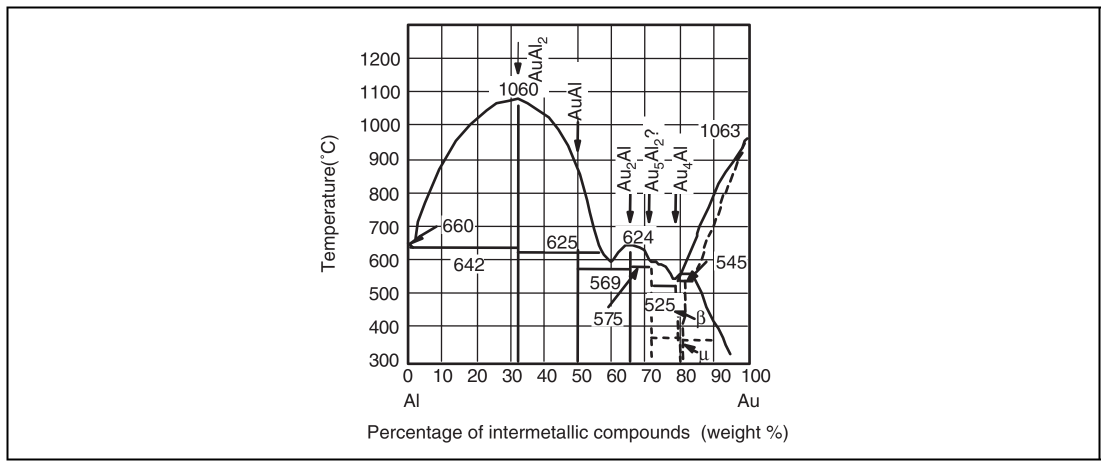


Figure 4.32 Phase Diagram for Au-Al Alloy

Table 4.4 Au-Al Alloy Characteristics

Chemical compound	Crystal structure	Expansion coefficient	Hardness (Hv)	Color
Al	f.c.c.	2.3×10^{-5}	20 to 50	Silver
$AuAl_2$	CaF_2 structure	0.94×10^{-5}	263	Purple
AuAl	ZnS structure	1.20×10^{-5}	249	Gray
Au_2Al	Unknown	1.26×10^{-5}	130	Yellowish golden
Au_5Al_2	γ-brass structure	1.40×10^{-5}	271	Ditto
Au_4Al	β-Mn structure	1.20×10^{-5}	334	Ditto
Au	f.c.c.	1.42×10^{-5}	60 to 90	Gold

(3) Failure Mechanism

The following are considered to be causes that lead to degradation of Au-Al alloy joints:

1. Several intermetallic compounds are produced in the diffusion layer as a result of the Au-Al diffusion; the difference in the expansion coefficient between the Au_5Al_2 and the Au_4Al layer causes the joint strength to lower;
2. The difference in the diffusion coefficient between Au and Al causes voids to be produced around the joint (Kirkendall effect); this in turn weakens the joint strength; and
3. The Au_4Al alloy layer is turned into a high resistance layer by the oxidization taking place with the bromine (Br), contained in the flame retardant in the resin material, as the catalyst

The diffusion processes are described below by using figure 4.33:

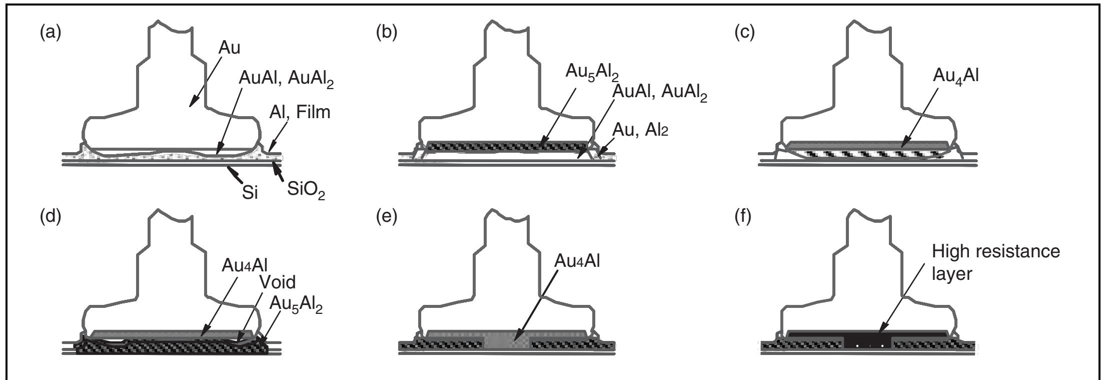


Figure 4.33 Au-Al Alloy State Chart

(a) At the early stage of bonding, a thin diffusion layer is formed between the Au portion and the Al film; the diffusion layer is purple-colored and estimated to consist of $AuAl_2$;

(b) Further heating causes the Au-Al diffusion to proceed, with Au diffusing into the Al thin film and thereby causing the pure Al layer to disappear. At the same time, an alloy layer distinguishable from the Au-Al alloy is formed on the Au ball side; this is estimated to consist of Au_5Al_2;

(c) The layer resulting from diffusion does not exceed a certain thickness; this is thought to be due to the limited supply of Al and the difference of the diffusion velocity between the direction toward Au and that toward Al. With D denoting the diffusion velocity, the following relation exists: $D_{Au \rightarrow Al} > D_{Al \rightarrow Au}$. With the initial thickness of Al evaporated film assumed to be 1 µm, the total thickness of the diffusion-formed portion is about 4-5 µm. Further heating causes Au to diffuse into the diffusion layer to form Au_4Al on the Au ball side, which grows into the semiconductor chip side;

(d) Further heating causes the Au diffusion into the diffusion layer to proceed and thereby the entire diffusion layer to be formed of Au_5Al_2 and Au_4Al. In addition, voids are created around the diffusion layer as a result of the Kirkendall effect caused by the difference in the diffusion velocity between $D_{Au \rightarrow Al}$ and $D_{Al \rightarrow Au}$.

(e) With the heating still continued, the Au diffusion into the diffusion layer is intensified except where voids are created, leading to formation of an Au_4Al layer in the central portion.

(f) With resin molded IC's, it is known that Br contained in flame retardant agents in resin materials acts as a catalyst to oxidize Al in the Au_4Al layer. Br penetrates from voids into the joint and oxidizes Al in the Au_4Al layer, causing a high resistance layer to be formed at the interface between the center of the Au ball and the alloy layer; this leads to a disconnection failure. Figure 4.34 shows the section of a joint under such condition.

Figure 4.34 Cross-section of Au-ball Joint (SEM Image)

The following Arrhenius equation holds between the thickness X of the diffusion layer, the storage temperature T, and the storage time t:

$$X^2 = D \bullet t,\ D = D_0 \bullet \exp(-Ea/kT) \qquad (4\text{-}3\text{-}1)$$

where

D: Diffusion coefficient;

Ea: Activation energy;

D_0: Frequency factor; and

k: Boltzmann's constant.

Based on the activation energy obtained in the measurement results of the diffusion layer thickness, an Ea of 0.56 to 0.8 eV was reported for ceramic packages and an Ea of 1.0 eV or greater was obtained for plastic packages. However, because metal reactions progressed depending on compound factors such as process type and material type, the Ea cannot be regarded as fixed.

The following three points must be taken into consideration to improve the reliability of the Au ball bonding:

1. An initial bonding joint should be processed in a time as short as possible and at a temperature as low as possible to minimize the Au-Al mutual diffusion;
2. Mechanical shocks should be avoided where possible during the bonding process and prior to the resin sealing; and
3. After package sealing, heating an element should be avoided where possible.

(4) Summary

The Au-Al wire bonding is subject to structural life limits imposed by the alloy used. Under the real-life conditions of use, however, the life as described above may not pose serious problems. To improve the reliability of bonding, it is more important and effective that the control of manufacturing equipment and selection of materials be properly conducted to secure the initial joint properties and that unnecessary heating on semiconductor devices after the bonding process be avoided.

4.3.2 Ag Ion Migration

(1) Introduction

Ag ion migration is a phenomenon in which metal ions move under an electrochemical effect. It is referred to as electrochemical migration (in this section, "ion migration") in order to distinguish it from the electro/stress migration that takes place in Al wiring on semiconductor chips. Ion migration can occur with electrode materials other than Ag, such as Cu, solder materials, and Au, if conditions are adverse. However, since it is Ag and Cu that trigger the migration most easily, these tend to pose problems.

This section describes Ag ion migration.

(2) Phenomenon

When Ag, in the form of foil, plating, or paste, is subjected to a voltage under high humidity and temperature, the electrolytic action causes Ag to migrate and grow like an ink blot or dendrite on the surface of the insulator as is shown in figure 4.35. This may cause the electrical insulation resistance between the electrodes to decrease or be short-circuited.

In a typical case of migration, the ink blot growth starts in the anode side while the dendritic crystal growth starts in the cathode side. In reality, however, due to the effects of difference in the types of insulator, environmental conditions, and the like, the Ag ions eluted from the anode side may be reduced halfway to precipitate as metallic Ag and the material precipitated from the cathode side may grow not dendritically but in blot. Furthermore, because Ag reacts easily with sulfur (S) and chlorine (Cl) in the atmosphere, these elements are simultaneously detected on analysis by the XMA or otherwise in many cases.

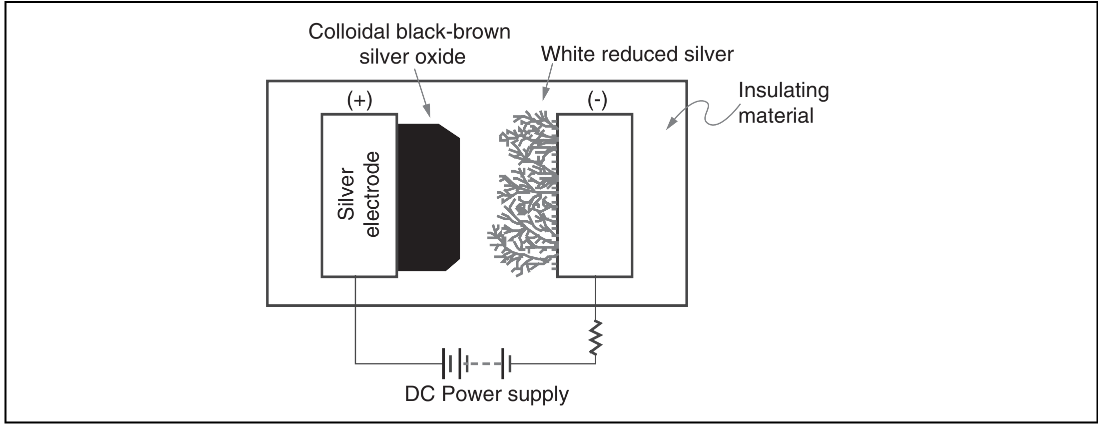


Figure 4.35 Generation of Silver Ion Migration

(3) Generation mechanism

Initially, when moisture settles between Ag electrodes under voltage application, the chemical reaction given by Equation 4-3-2 takes place on the anode:

$$Ag+OH^{-} \rightarrow AgOH+e^{-} \quad (4\text{-}3\text{-}2)$$

Since the silver hydroxide (AgOH) generated in this reaction is very instable, the decomposition as given by Equation 4-3-3 takes place:

$$2AgOH \rightarrow Ag_2O+H_2O \quad (4\text{-}3\text{-}3)$$

The colloidal silver oxide (Ag_2O) generated in turn reacts as given by Equation 4-3-4:

$$Ag_2O+H_2O \leftrightarrow 2AgOH \leftrightarrow 2Ag^{+}+2OH^{-} \quad (4\text{-}3\text{-}4)$$

The colloidal Ag_2O generated and the Ag ions move slowly (Ag ions, in particular, are pulled by the electric field), until they reach the cathode to be reduced there to silver metal:

$$Ag^{+}+e^{-} \rightarrow Ag \quad (4\text{-}3\text{-}5)$$

The silver precipitated exhibits white dendritic growth as shown in figure 4.35. The electric-field intensity at the tip of a dendrite increases with the growth; therefore, the growth, once initiated, proceeds with acceleration.

(4) Acceleration Factors and Countermeasures

Listed below are the factors that accelerate the occurrence of ion migration. These factors must be studied if they are to be addressed, and those having greatest influence must be removed.

(a) Potential difference and electrode distance

As a type of electrolytic reaction, ion migration poses problems only when DC voltage is applied between electrodes. In addition, the time to short-circuit between electrodes is roughly inversely proportional to the potential difference and proportional to the distance.

(b) Temperature

Although temperature is less of a factor than humidity, a higher temperature accelerates the chemical reaction and hence the migration of ions.

(c) Humidity (specifically, condensation)

Humidity greatly affects ion migration. In general, ions do not migrate when the relative humidity is 50% or less, but when the relative humidity is 70% or more, migration accelerates rapidly.

(d) Types of insulating material

Like moisture, the properties of insulation materials greatly affect ion migration. In general, ion migration occurs in highly hygroscopic phenolic resin laminated materials and nylon materials, but does not often occur in poorly hygroscopic materials such as glass epoxy substrates.

(e) Dust and water properties

Because dust, in addition to being a retainer of moisture, also itself contains water-soluble matter, it accelerates ion migration. A higher concentration of electrolytes in water also accelerates ion migration.

(5) Summary

Measures against Ag migration should be examined and put into practice in consideration of the working conditions (the environment and voltage, in particular), the scope of the areas affected, and the quality requirements to reduce its potential. Some of the measures already known or reported include reduction of ionic impurities, control of the amount of Pd in Ag, and the addition of ion traps.

4.3.3 Cu Ion Migration

(1) Introduction

For semiconductor devices, and multi-pin plastic packages in particular, leadframes bonded with a heat-resistant polyimide tape are used to prevent the deformation of leadframes during production and the short-circuiting between inner leads that results from deformed leads. However, for Cu leadframes, the adhesive that secures Cu to the polyimide tape causes the migration of Cu ions in the test environment. This section describes Cu ion migration.

(2) Phenomenon

Applying a voltage to a multi-pin package that has Cu leadframes in a high temperature environment causes the Cu metal to be ionized because of the effects of solvent elements contained in the adhesive. As shown in figure 4.36, the Cu ions migrate from the pins of the inner leads with a positive potential and to those with a negative potential.

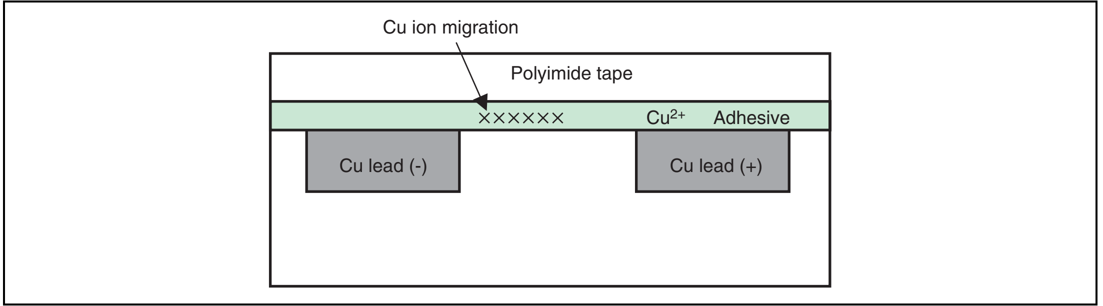


Figure 4.36 Cu Ion Migration (Package Cross-Section)

(3) Failure Mechanism

In the adhesive used for polyimide tape, chemical reactions represented by equations (4-3-6) and (4-3-7) take place at the cathode and anode when a voltage is applied at a high temperature in the presence of Cu because of the organic solvent (alcohol group (R-OH), etc.) that remains.

Anode: $Cu \rightarrow Cu^{2+} + 2e^{-}$ (Cu elution) (4-3-6)

Cathode: $Cu^{2+} + 2e^{-} \rightarrow Cu$ (Cu deposition) (4-3-7)

Cu ions elude on the anode side and the difference in electric potential between the inner leads causes Cu metal to be deposited on the cathode. (See figure 4.37.)

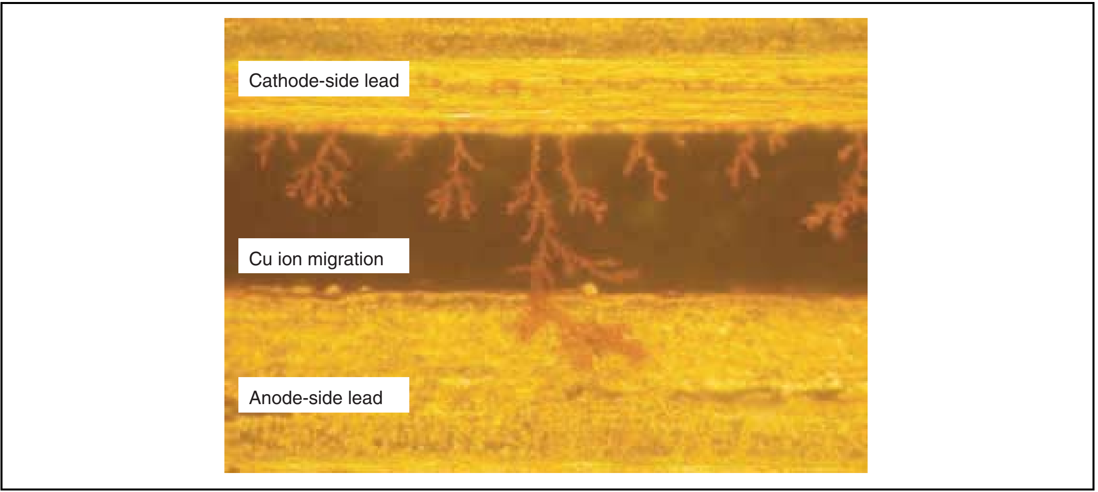


Figure 4.37 Example of Cu Ion Migration between Inner Leads

(4) Acceleration Factors

Listed below are the factors that accelerate the occurrence of Cu ion migration. These factors must be studied if they are to be addressed, and those having the greatest influence must be removed.

(a) Potential difference and electrode distance

As a type of electrolytic reaction, Cu ion migration has the characteristic that the time to short-circuit between electrodes is inversely proportional to the potential difference and proportional to the distance.

(b) Temperature

For the chemical reaction on the anode side, a higher temperature accelerates Cu ion migration.

(c) Impure ions

The greater the concentration of impure ions (anions) contained in the taping adhesive, the greater the acceleration of the Cu icon migration.

(5) Summary

To avoid Cu ion migration in the inner leads and taping adhesives, Cu elution must be prevented. For the material, selecting an adhesive with fewer remaining organic solvents is a good measure. In the assembly process, baking the remaining organic solvents and rejecting at a high temperature is a possible measure.

4.3.4 Al Sliding

(1) Introduction

In a temperature cycle environment, failure phenomena in which a shearing force causes the semiconductor chip surface to push toward the center of the chip surface can occur. These phenomena, of which Al sliding is one, are due to the contraction stress of the mold resin at a low temperature. Metallic wiring materials such as Al are deformed easily by an external force and do not tolerate external stresses. If a horizontal stress is applied to the center of the chip surface and to the wiring around it, it is not the Al wiring that withstands the stress, but the passivation film on the surface. Therefore, when the Al wiring is wide, a protective film with structurally low strength is destroyed and the Al wiring slides. This failure phenomenon is known as Al sliding and causes cracks in the passivation film. These cracks can lead to circuit damage and subsequently device malfunction. This section describes the Al sliding phenomenon caused by a stress from the mold resin [39].

(2) Phenomenon

Because the semiconductor chip, passivation film, and molding resin have different coefficients of thermal expansion, external thermal stress causes stress to occur between the different layers. When a chip is stored at a lower temperature, the contraction stress from the resin acts on the chip, causing the Al wiring to slide toward the center of the chip. In the chip corner in particular, where the stress on the chip coming from the resin becomes large, the Al sliding phenomenon is more remarkable than at the center of the chip. Furthermore, this phenomenon is more remarkable on a wide Al conductor on which stress is concentrated. The Al sliding and the cracks in the passivation film are closely related. Because Al wiring deforms easily, if a stress from the resin due to a temperature change is put on the passivation film, causing cracks on the passivation film, the Al wiring deforms and can no longer be restored to its original state (elastic deformation). As a result, the Al sliding phenomenon takes place. Figure 4.38 shows an example of Al sliding. Figure 4.39 shows the failure mechanism. This phenomenon is accelerated by the temperature cycle test.

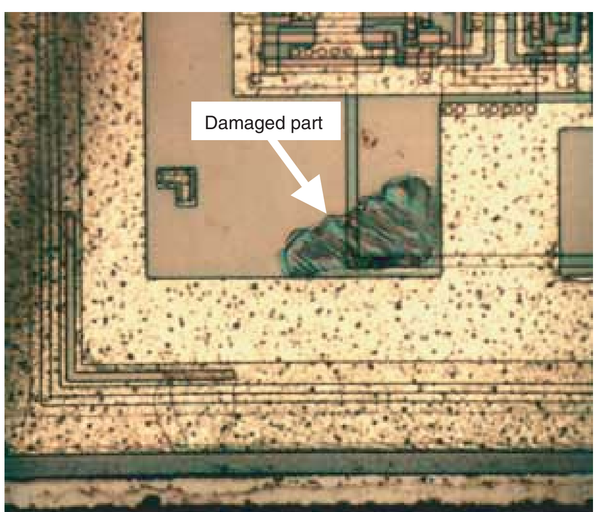


Figure 4.38 Example of Al Sliding

(3) Failure Mechanism

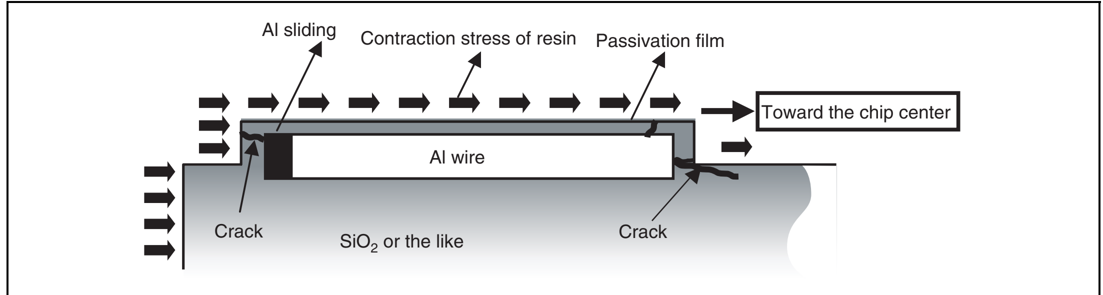


Figure 4.39 Chip Corner Al Wiring Cross Section

Since Al sliding is affected only by a temperature change, its failure model is based on the Eyring model equation.

$$\text{Life (L)} \propto (\Delta T)^{-n} \qquad (4\text{-}3\text{-}8)$$

For the acceleration coefficient n, n = 4.4 to 8.1 has been reported.[40]

(4) Summary

The Al sliding phenomenon is caused by the difference in the coefficient of thermal expansion between materials forming a semiconductor device, giving rise to passivation cracks from the resulting stress. The following methods can be used to address these problems:

1. Set the coefficient of thermal expansion of the mold resin as close as possible to that of the chip.
2. Set a limit on the Al wire width at the chip corners to prevent wide Al wires from being placed there.

4.3.5 Mechanism of Filler-Induced Failure

(1) Introduction

Mold resins include a filler that secures strength and has a thermal expansion coefficient close to that of the chip. When a filler of approximately 100 μm is located on the chip surface by molding, the filler presses the chip surface due to the temperature cycle and other factors, damaging the chip surface and possibly causing a failure.

(2) Phenomenon

When a mold resin includes large and pointed filler elements, and if the filler elements contact the surface of the chip during molding at a high temperature (while the mold resin is melting), the filler elements cannot damage the chip.

Thereafter, the resin around the filler shrinks gradually as it hardens. If the tip of a pointed filler element is facing the chip surface, as shown in figure 4.40, the pointed tip moves (is displaced) closer to the chip surface as the resin shrinks. Thereafter, when the temperature falls, the resin shrinks more (the coefficient of thermal expansion of the resin is several times larger than that of the filler). Moreover, when the temperature drops in the temperature cycle, the resin shrinks more and the pointed tip of the filler element is pressed out over the chip surface. If the amount of displacement exceeds the thickness of the protective layer on the chip surface, the circuits on the chip surface are damaged and fail. Because the amount of displacement of a filler element tip correlates with the size of the filler element, the smaller the filler element, the less the displacement. Filler elements with a round tip can never be displaced by breaking through the resin. To avoid this problem, it is usually effective to make large filler elements round and to remove filler elements that exceed a certain size.

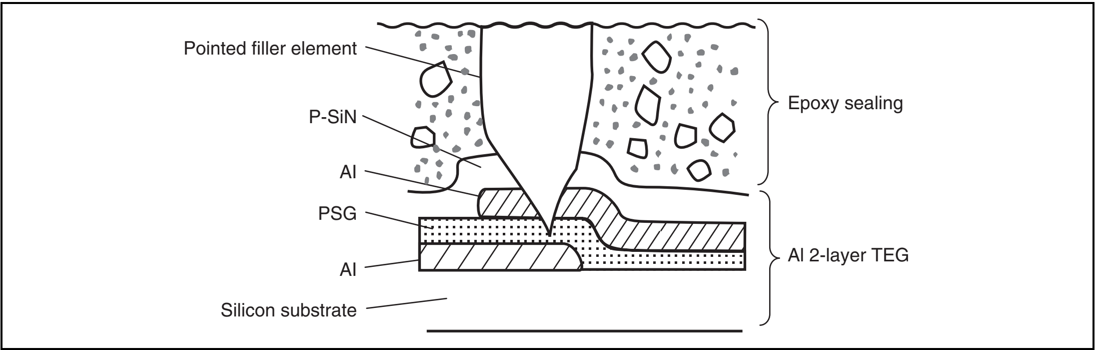


Figure 4.40 Cross Section of a Semiconductor Device in the Vicinity of the Chip Surface

(3) Summary

Failures arising from the filler have the potential of occurring in resin mold semiconductor devices. To cope with this problem, it is important to mitigate the stress which semiconductor chips undergo by implementing the measures described above.

4.3.6 Whiskers

For conservation of the environment, solders used for mounting electronic components on boards tend to be as Pb-free as possible. From the standpoint of plating reliability, however, since Pb provides a significant benefit related to tin whiskers, a Pb-free policy requires that measures be taken for tin whiskers that satisfy values, conditions, and other factors existing in the marketplace. Although the mechanism of tin whisker generation has not been clearly determined yet, it has been demonstrated experimentally that the environmental factors in accelerated whisker growth (see figure 4.41) are temperature, humidity, and stress. The most popular whisker generation mechanism is the one described below.

When the lead base material is Sn-plated Cu, Cu diffusion grows two kinds of intermetallic compounds: Cu_6Sn_5 and Cu_3Sn. At normal temperature, the volume of Cu_6Sn_5 is larger than that of Cu, and changes in its volume are the compressive stress that generates needle-like whiskers. At high temperature, the volume of Cu_3Sn is less than that of Cu. This characteristic is a factor in suppressing whisker generation due to the increase in Cu_6Sn_5 volume, whereas at comparatively normal temperature the growth of whiskers is facilitated.[41]

The following are the principal measures for preventing whiskers:

1. Addition of atoms that can replace Pb (Bi, Cu, Ag, etc.)
2. Thicker plated film
3. Heating after plating
4. Substrate-plating

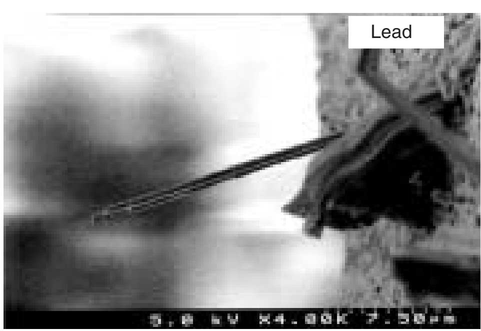


Figure 4.41 Example of Whisker Generation

4.3.7 Moisture Resistance of Resin Mold Semiconductor Devices

(1) Introduction

Semiconductor devices are generally put in resin mold type packages. At an early stage in the development of packages, resin mold devices were subject to such moisture resistance related problems as corrosion of Al electrode wiring corrosion and increased leakage current, but these problems have been largely solved.

This section describes the moisture resistance of a resin mold device in terms of mechanisms of its failures, the acceleration of failures under actual conditions of use, the effects of bias application, and the evaluation methods.

(2) Failure Mechanism

(a) Water Penetration Path

As described below, two water penetration paths are possible in a resin mold device: one of them passes straightforward through the resin and leads to the chip surface (moisture absorption/permeation of resin, or the moisture diffusion effect). The other is a path from the interface between the resin and leadframe to the chip surface via the interface between the resin and metal wire (figure 4.42). In the latter case, the moisture becomes a caustic solution containing impurities (such as flux and cleaning fluid) that adhere to the package surface. The solution corrodes the bare Al electrodes and wires on the chip surface.

Reports so far[49] [52] on the relative significance of these two paths indicate that the resin and frame materials used and the package structure affect the relative significance. Recent data shows that a greater role is played by the path passing through the resin than the path passing the frame interface because adhesion between the frame material and the resin has improved.

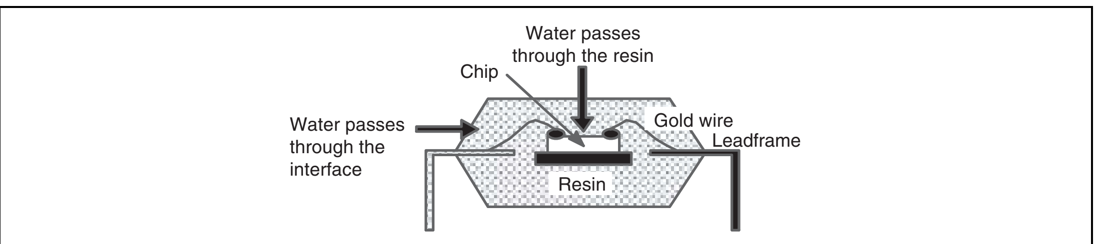
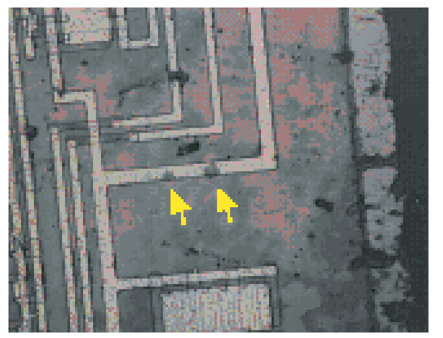


Figure 4.42 Water Penetration Path in a Plastic Mold Device

(b) Al corrosion

During storage in high-humidity and high-temperature conditions, moisture that reaches the chip surface may cause corrosion (sometimes referred to as pitting) of Al on the bonding pads and internal wiring patterns exposed by passivation defects with pinholes and cracks. This type of corrosion does not cause a rapid increase in failures even after extended hours of storage, and the cause of any failures found is considered to be an initial defect on package/chip due to fluctuations occurring in production. It has been confirmed that delamination of the adhering interface between the chip surface and the resin sealing or an impurity on the chip surface might result in a similar failure pattern.

The two Al corrosion modes are moth-eaten corrosion and beltlike-shape corrosion, and are shown in figure 4.43. It is assumed that these corrosion modes are due to the penetration of water containing chlorine and other impurities that has a pH 4 or higher from the Al crystal grain boundary.



Moth-eaten

Beltlike-shape

Figure 4.43 Al Corrosion During Storage with High Humidity and High Temperature

Aluminum is chemically a very active metal; left in dry air, it causes alumina (Al_2O_3) to be formed on its surface. Since this Al_2O_3 acts as a surface protection film, the reaction no longer proceeds. In the presence of sufficient water, on the other hand, aluminum hydroxide ($Al(OH)_3$) is formed. The $Al(OH)_3$ thus formed is amphoteric, dissolving both in acids and in alkalis; therefore, it dissolves easily into water containing impurities. The following are typical corrosive reactions involving aluminum[42]:

$$2Al+6HCl \rightarrow 2AlCl_3+3H_2\uparrow$$

$$Al+3Cl^- \leftrightarrow AlCl_3+3e^-$$

$$AlCl_3+3H_2O \rightarrow Al(OH)_3+3HCl$$

$$2Al+2NaOH+2H_2O \rightarrow 2NaAlO_2+3H_2\uparrow$$

$Al+3OH^{-} \rightarrow Al(OH)_3+3e^{-}$

$2Al(OH)_3 \rightarrow Al_2O_3+3H_2O$

$2AlO_2^{-}+2H^{+} \rightarrow Al_2O_3+H_2O$

High temperature and high humidity bias tests induce simultaneous Al corrosion on the anode and cathode sides, often leaving a metallic luster in places on the Al wiring. This corrosion mode consists of Al wiring corrosion (pitting) on the anode side and corrosion on the cathode side that progresses from the crystal grain boundary (intergranular corrosion, or imbricate corrosion). Figure 4.44 shows these two modes of corrosion. Once failure begins by pitting corrosion, almost every device suffers a wear-out failure in a comparatively short time. It has been confirmed that the time to failure correlates with the volume resistivity of the resin to the absorption of moisture. Note that intergranular corrosion (imbricate corrosion) tends to occur on the cathode side.

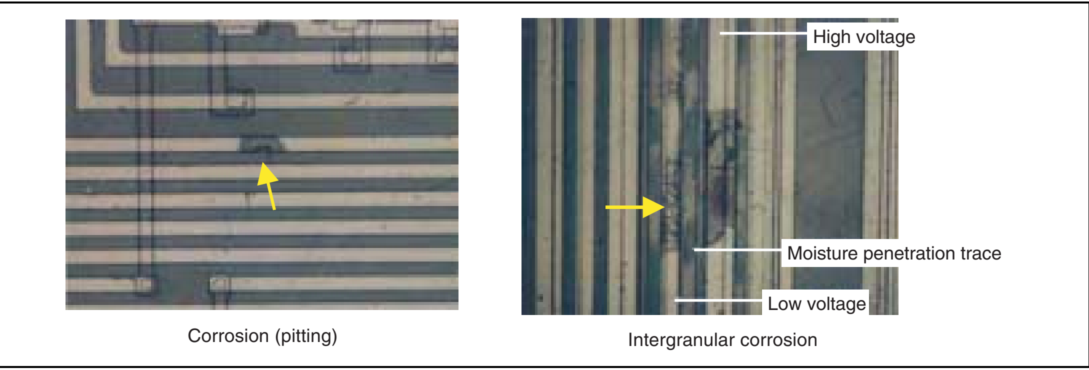


Figure 4.44 Al Corrosion on High Humidity and High Temperature Bias

(c) Chip surface leakage due to moisture absorption by resin

Chip surface leakage current due to moisture absorption by the mold resin is caused by

- Insulation resistance degradation of resin
- Formation of a water film in the gap between chip surface and the resin

Leakage currents of less than 5 pA indicate that the resin has absorbed moisture, reducing its resistance as an insulator. Greater values indicate that potential differences between electrode wiring runs on the chip's surface are producing charge leakage between the runs, in turn generating a potential on the oxide film. In particular, for MOS and other devices that have surface activity, the surface potential can set up an inversion layer on the surface of the Si substrate under the oxide film, causing current to flow between the source and drain of the parasitic MOS FET and thus increasing the leakage current. The mechanism is shown in figure 4.45.

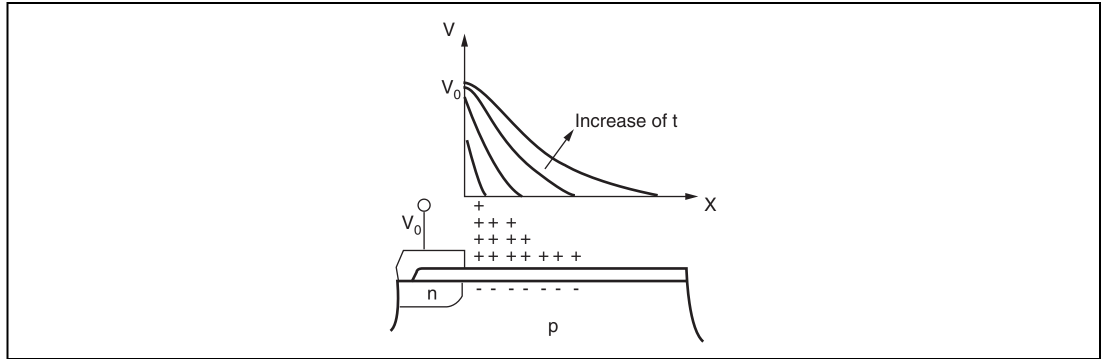


Figure 4.45 Surface Charge Expansion Phenomenon

(d) Examples of the effects of bias application modes and the values of the applied voltage on moisture resistance

Figures 4.46 and 4.47 show the results of a study that was made on the effects of bias application modes and the values of the applied voltage on moisture resistance by using a resin-mold bipolar device.[43] [44] As the figures show, device life depends to a great extent on the bias application mode and the value of the voltage applied. The following reaction equation is proposed as a model representing intergranular corrosion on the cathode side[45]:

Anode side: $2H_2O \rightarrow 4H^+ + 4e^- + O_2$

Cathode side: $2Al + 6H^+ \rightarrow 2Al^{3+} + 3H_2$

$2Al^{3+} + 6H_2O \rightarrow Al(OH)_3 + 6H^+$

$6H^+ + 6e^- \rightarrow 3H_2$

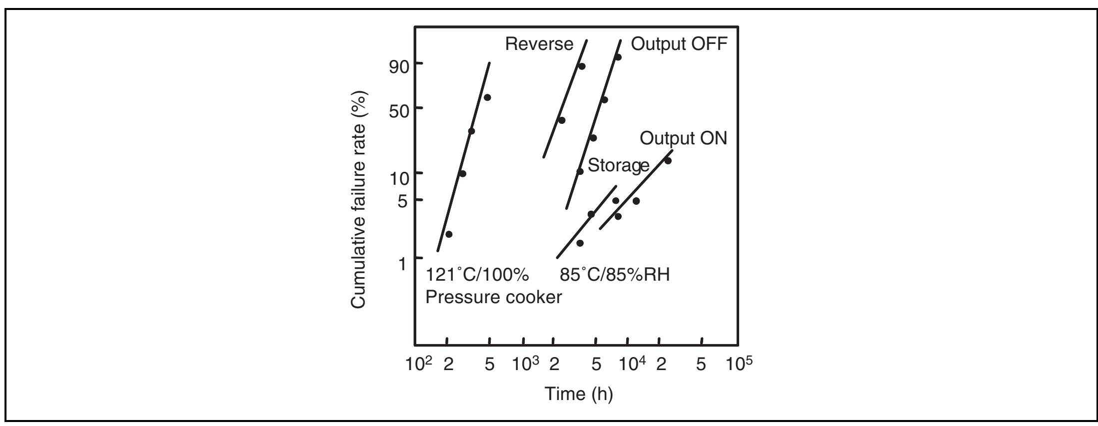


Figure 4.46 Effects of Bias Application Conditions

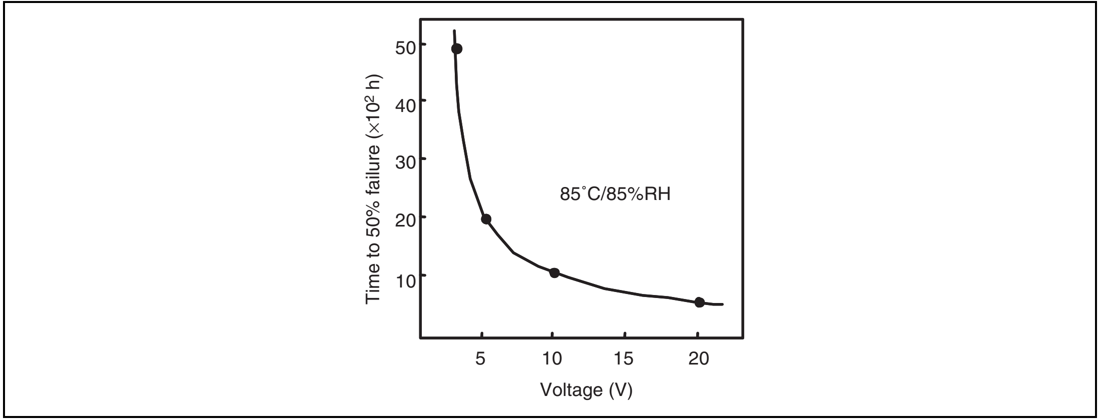


Figure 4.47 Effects of Bias Voltages

(3) Conditions for Practical Use and Acceleration

Several acceleration models for predicting the reliability of resin mold semiconductor devices have been introduced on the basis of moisture-resistance test data, as follows:

1. The mean time to failure, MTTF, is affected separately by the junction temperature Tj (K) and the relative humidity RH (%).[46]

   Relationship between MTTF and Tj: Based on Arrhenius' model (Ea≈0.8eV).

   Relationship between MTTF and RH: The values of logMTTF and logRH are in a linear relation.

   These are called relative humidity models and are expressed by the following equation:

   $$MTTF \propto exp\ (\Delta E / kT) \bullet RH^{-n}$$

   where k is Boltzmann's constant, T is the absolute temperature, and n is a constant between 4 and 6.

2. The time to a given cumulative failure rate t relates to the vapor pressure V_P.[47] to [49] This is called an absolute vapor pressure model and is expressed by the following equation, where m is a constant for which m ≅ 2 is used:

   $$t \propto V_P^{-m}$$

Figure 4.48 shows the relationship of relative lifetimes at respective humidity/temperature points as an example of acceleration in a case where m = 2.

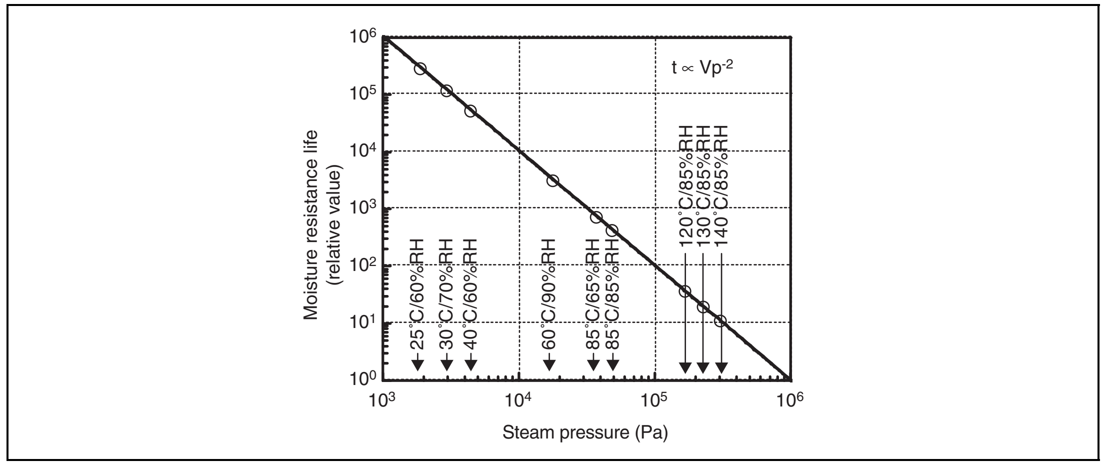


Figure 4.48 Example of Acceleration

Although various acceleration models including those described above have been proposed, the acceleration in each of them depends on the particular resin material, package structure, conditions of metallization and passivation, etc., which makes it difficult to determine a generalized acceleration coefficient.

(4) Methods for Evaluating the Moisture Resistance

Since various methods for evaluating the moisture resistance are available, the appropriate method for the intended purpose has been used. Table 4.5 shows the major test methods. The methods generally used are the pressure cooker storage test, the pressure cooker bias test (primarily for the unsaturated condition, sometimes called HAST (Highly Accelerated Temperature and Humidity Stress Test)), the high temperature and high humidity storage test, the high temperature and high humidity bias test, and, very rarely, varying combinations of these tests.

Furthermore, in response to widespread use of surface mount devices (SMD), an evaluation method has been proposed in which the moisture resistance tests listed above are preceded by a pretreatment consisting of a sequence of moisture absorption and thermal stress tests. When SMDs are mounted on a circuit board, an IR reflow or other method is used. This type of mounting method results in heat stress to the entire device as well as delamination of the leadframe interface to the resin or the adhesive interface between the chip surface and mold resin. The result is degradation of the moisture resistance life. To check the SMD moisture resistance level, an evaluation method in which moisture absorption and heat stress tests are performed as a preprocess has been used.

Table 4.5 Major Methods for Evaluatating the Moisture Resistance

Evaluation method	Example of test conditions	Features
High temperature and high humidity storage test	85°C/85%RH	Has substantial correlation with actual conditions of use. Requires a long time for the evaluation.
High temperature and high humidity bias test	85°C/85%RH/ with bias applied	Has substantial correlation with actual conditions of use. Requires a long time for the evaluation.
Pressure cooker storage test	130°C/85%RH	Has substantial correlation with actual conditions of use.
Pressure cooker bias test (HAST)	110°C/85%RH/ with bias applied 120°C/85%RH/ with bias applied 130°C/85%RH/ with bias applied	Has substantial correlation with actual conditions of use. Allows the effects of the biasing to be evaluated.

Note: The saturation-type pressure cooker storage test (100% RH) is not recommended due to market correlation problems.

(5) Summary

Various acceleration tests have been used to check the moisture resistance of resin mold devices under conditions of practical use. Recently, moisture resistance levels have improved so remarkably that they are sufficient for practical use without any critical problems.

4.4 Failure Mechanisms related to the Mounting Process and During Practical Use

4.4.1 Cracks of the Surface-Mounted Packages in Reflow or Flow Soldering

(1) Introduction

As electronic devices become thinner, smaller, lighter, and multi-functional, surface-mounting techniques have become essential techniques for increasing the density of mounted parts. Most semiconductors now use surface-mounted packages.

Soldering methods for surface-mounted packages are roughly classified as partial heating and full heating. Partial heating applies heat only to sections to be soldered whereas full heating applies heat to both the printed circuit board and packages. Full heating methods consist of reflow soldering methods and the flow soldering method.[50] [51]

- Reflow soldering methods

  The reflow methods consist of the infrared reflow method, the hot-air reflow method (air reflow method), and a method that combines the infrared reflow method and hot-air reflow method.

  In the infrared reflow method, devices to be mounted are soldered by directing infrared rays over the entire printed circuit board with devices installed. This method is suitable for mass production because separate parts can be soldered at one time. The disadvantage of the infrared reflow method is temperature differences when only infrared sources are used. To address this problem, infrared reflow machines that also use a hot air heater have come into widespread use.

  In the hot air reflow method (air reflow method), solder reflows by the circulation of hot air in a furnace. The advantages of this method are little difference in temperature of printed circuit board and parts and the ability to control the temperature deviation between components within a specified degree.

- Flow soldering method

  The flow soldering method is a low-cost soldering method. The parts to be soldered are temporarily fastened to a printed circuit board with an adhesive, the parts side is turned face down, and the printed circuit board is passed through molten solder (flow solder). However, since the flow soldering method cannot handle certain device sizes or dimensions, it is not suitable for high-density mounting of devices.

These full heating methods apply high temperatures to the packages as well as to the points to be soldered. Because the temperature actually applied exceeds 210°C, the surface mount devices can be subjected to severe stress. The following three reliability problems can therefore arise in the production of surface mount devices:

1. Resin cracks in the package
2. Lowering of moisture resistance
3. Adverse effects on the wire bonding strength

To ensure the reliability of surface mount devices after they have been mounted, special management is required at each process from storage to mounting.

(2) Package Cracks

These cracks arise from the combination of the moisture that the package has absorbed and heat applied during soldering.[52] [53] As shown in figure 4.49, ambient moisture diffuses into the resin during storage in a warehouse, etc. and moisture reaches to the interfaces such as between resin and die pad. When packages with absorbed moisture pass through the reflow oven and are heated, the resin-die adhesive strength drops, differences in thermal expansion coefficients of the different materials give rise to a shear stress, and microscopic area separation or delamination results. Since the speed of moisture diffusion increases at high temperatures, moisture is forced out of the resin into the delamination, and with a rise in pressure there, the delamination region expands and the molding compound becomes increasingly swollen. The swelling stress is concentrated at the periphery of the die pad and eventually a crack in the resin results. The stress varies greatly with the amount of moisture content in the resin near the rear surface the die pad, the die pad size, and the temperature and heating time.

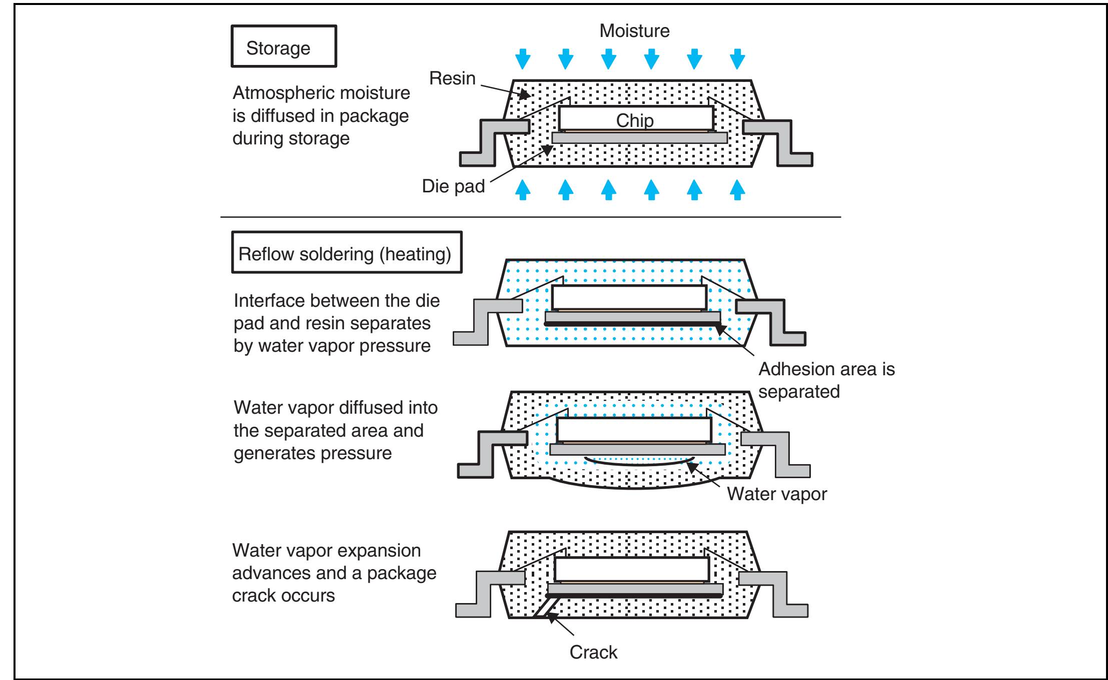


Figure 4.49 Model of Crack Generation in Reflow Soldering[54]

Although the model above shows an example of a crack on the backside of a package, cracks can occur on the front surface of a package due to expansion of the chip surface in the same sequence.

(3) Package Moisture Soaking Characteristics

Package cracks are caused by the diffusion of water around the die pad's rear surface and the chip's surface. To predict occurrence of cracks, the quantity of water in resin should be obtained. We use the diffusion model assuming that water diffuses from package surfaces toward the die pad's rear surface and the chip's surface (figure 4.50). [55] to [59]

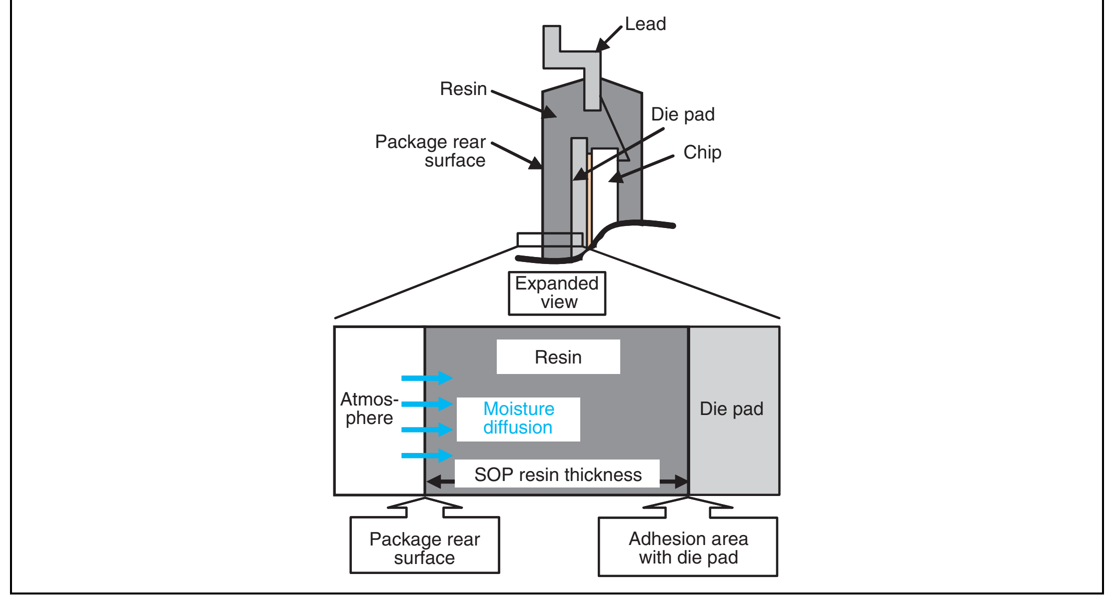


Figure 4.50 Model of Moisture Diffusion at Humidification[54]

The concentration of water in resin (moisture content per unit volume) can be determined using Fick's diffusion equation.

In case of a one-dimensional diffusion model with resin thickness as x (the distance from the center), the diffusion equation is as follows (equation 4-4-1).

$$\frac{\partial C(x,t)}{\partial t} = D \frac{\partial^2 C(x,t)}{\partial x^2} \qquad (4\text{-}4\text{-}1)$$

Where

C(x, t): Water Concentration at Coordinate x, at Time t

D: Diffusion Coefficient

This equation is solved with boundary conditions of before and after moisture absorption. Water concentration inside the package is calculated using the solution. For example, for the water concentration C(0, t) below the die pad (or the chip's surface), the solution is as follows (equation 4-4-2).

$$C(0,t) = Q_S \left[\frac{4}{\pi} \sum_{n=0}^{\infty} \frac{(-1)^n}{2n+1} \exp\left(- \frac{(2n+1)^2 \pi \; D \cdot t}{4d^2} \right) \right] \qquad (4\text{-}4\text{-}2)$$

Where

Qs: Saturated water concentration in resin, which is determined by temperature and humidity of storage atmosphere

d: Resin thickness to the first interface

Exponential term of the equation (4-4-2) means speed of moisture absorption and it is inversely proportional to 2nd power of resin thickness *d*, so thinner packages become saturated quickly.

Qs and *D* are shown below.

$$Qs = P^n S_0 \exp (Es/kT) \quad (4\text{-}4\text{-}3)$$

$$D = D_0 \exp (Ed/kT) \quad (4\text{-}4\text{-}4)$$

Where

P: Pressure of Water Vapor

n, S_0, Es, D_0, Ed: Constants which are determined depending on the resin type. These values can be obtained by analyzing the absorption data of the resin.

Figure 4.51 shows the calculation result of the progress of moisture absorption in case of 1-mm resin thickness (from package rear surface to die pad). Water concentration near the first interface increases with elapsed time, saturating after about 2,000 hours.

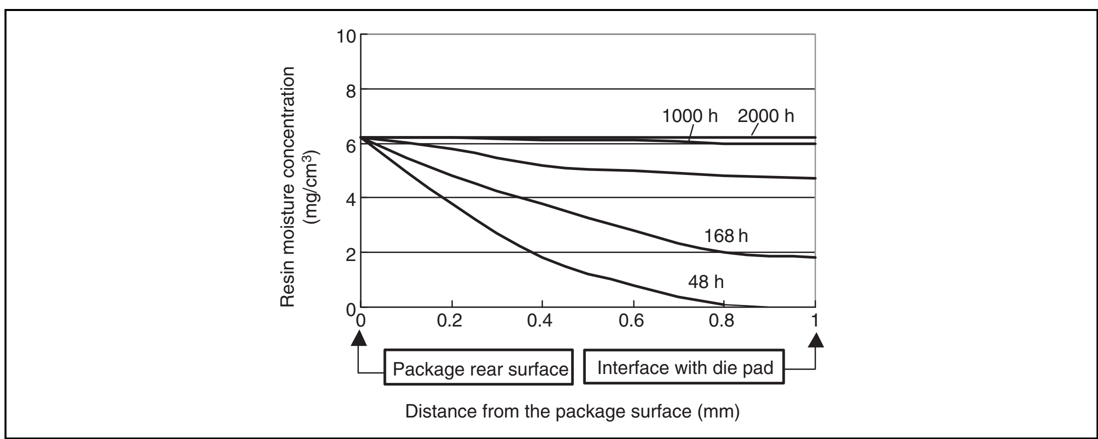


Figure 4.51 Example of Calculations of the Progress of Moisture Absorption for 1-mm Resin Thickness[54]

(4) Crack Generation and Inner Moisture Content Dependency

Moisture absorption rate (wt%) may be used as indicator of moisture absorption of a package.

$$\text{Moisture absorption rate} = \frac{W_1 - W_0}{W_0} \times 100 \text{ (wt\%)} \qquad (4\text{-}4\text{-}5)$$

Where

W_0: Dry (fully baked) package weight

W_1: Package weight after moisture absorption

The moisture absorption rate is calculated from the total weight change of a package and does not give enough information about the local water concentration near the first interface (top surface of die or rear surface of die pad), which actually causes the crack. The moisture absorption rate alone cannot be a proper indicator of the probability of cracking. It is essential to thoroughly understand the following issues.

For example, in a process in which a dry package gradually absorbs moisture (a moisture-absorption stage), regions near the periphery of the package absorb a large quantity of moisture, as is shown in figure 4.52 (a). However, moisture does not fully reach the surface behind the die pad. The overall moisture content is equal to the average value of the concentration of moisture from the periphery of the package to the surface behind the die pad. Accordingly, even if the moisture content is high, the concentration of moisture at the surface behind the die pad remains low. After sufficient time, the moisture absorption is saturated, and enough water reaches the first interface (figure 4.52 (b)). Conversely, during the drying process, the resin surface may have been dried but water still remains near the first interface (figure 4.52 (c)).

Even if the moisture absorption rates are the same (as shown in figure 4.52, the three shaded areas are the same), the quantity of water actually near the first interface is different, so risk of cracks is different. Figure 4.53 shows experimental results for the appearance of cracks vs. moisture content during moisture absorption (a) and drying process (c). These results indicate that cracks appear at a lower moisture content in the case of the drying process (c), confirming that the generation of cracks depends on the amount of internal moisture rather than on the overall moisture absorption rate.

(a) Halfway moisture absorption
The first interface
Package surface
Resin
Distribution of moisture content
Die pad
Moisture
(b) Saturated moisture absorption
Moisture
Moisture which causes the crack
(c) Halfway of drying or baking
Moisture

Figure 4.52 Moisture Distribution in Packages in Respective Stages (Comparison When Moisture Absorptivity Comparable)

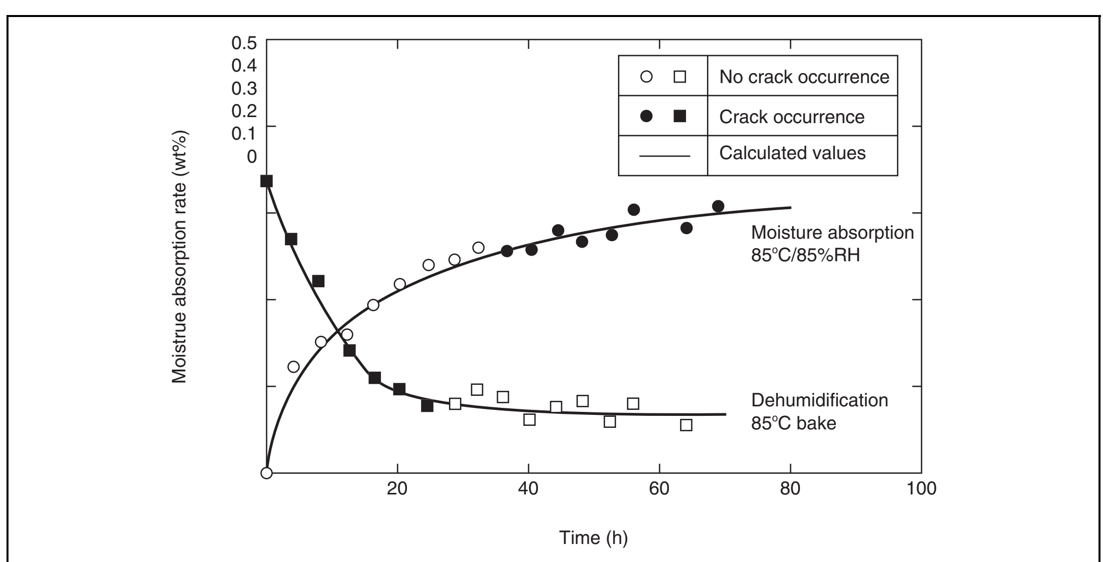


Figure 4.53 Moisture Absorptivity Changes for Moisture Absorption/Drying and Results of VPS Heating[56]

(5) Measures for Preventing Cracks and Methods for Observing Cracks

The following is an equation for simplifying package crack generation factors:

$$P \propto W \bullet H^2 \bullet \sigma_{FB} / L_V \qquad (4\text{-}4\text{-}6)$$

where P is the stress from moisture near the bottom of the die pad or near the chip surface caused by heat during mounting, W is the minimum length from the die pad edge to the package surface, H is the resin thickness under the die pad, L_V is the die pad length, and σ_{FB} is the bending strength of the package resin.

According to equation (4-4-6), package cracks occur if the stress P exceeds the limit on the right-hand side. When the value of the right-hand side of equation 4-4-6 becomes larger, or when the stress from vaporization on the left-hand side becomes smaller, package cracks can be suppressed. The following four measures are possible:

1. Lower the absorptivity of the package resin.
2. Improve the high-temperature bending strength and ductility of the package resin.
3. Use a low-stress package resin and reduce the stress on the interface from changes in heat.
4. Improve the adhesion of the package resin to the chip frame.

Explained next are the ways that package resin cracks can be observed. When cracks are remarkable, they become external and can be observed with a microscope. Note, however, that there may be cases where delamination between the resin and the chip or frame or cracks do not become external as well as cases where cracks are too minute to be observed with a microscope. The following are the general methods for observing cracks:

1. Observing external cracks with a microscope (figure 4.54).
2. Observing internal cracks/delamination by cross-section polishing (figure 4.55).
3. Observing internal cracks/delamination by scanning acoustic tomography (SAT) (figure 4.56).

   For the procedure, secure the device you want to observe in the water, direct ultrasonic beams at the device, and receive echoes from which you can form an image. This is a non-destructive method of observation.[60] [61]
4. Observing cracks/delamination using fluorescent penetration testing.

   Introduce a fluorescent penetrant into the package, then polish the cross section. Observe the cross section with an ultraviolet-ray (fluorescence) microscope for cracks and delamination. This method of observation is effective for finding very minute cracks and delamination because of its high sensitivity.

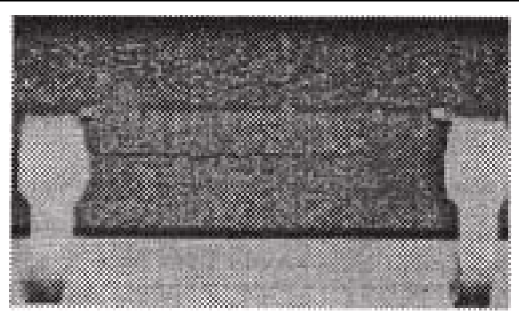


Figure 4.54 Example of Observing External Cracks with a Microscope

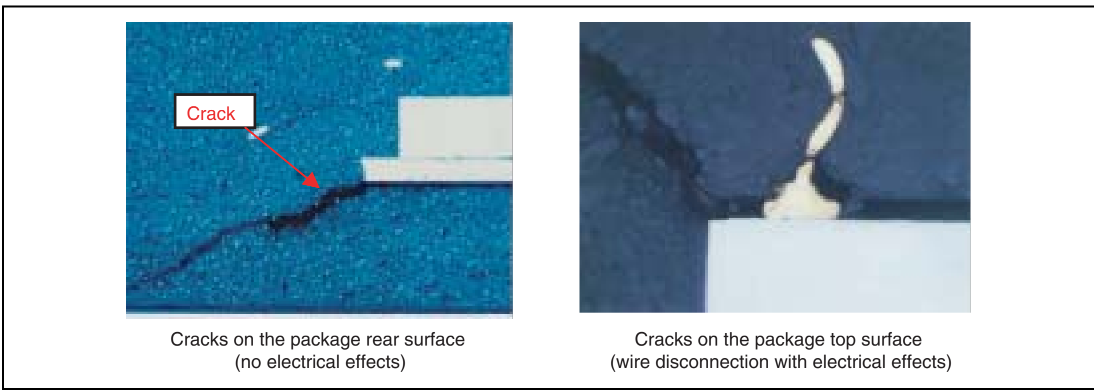


Figure 4.55 Example of Observing Internal Cracks/Delamination by Cross-Section Polishing[59]

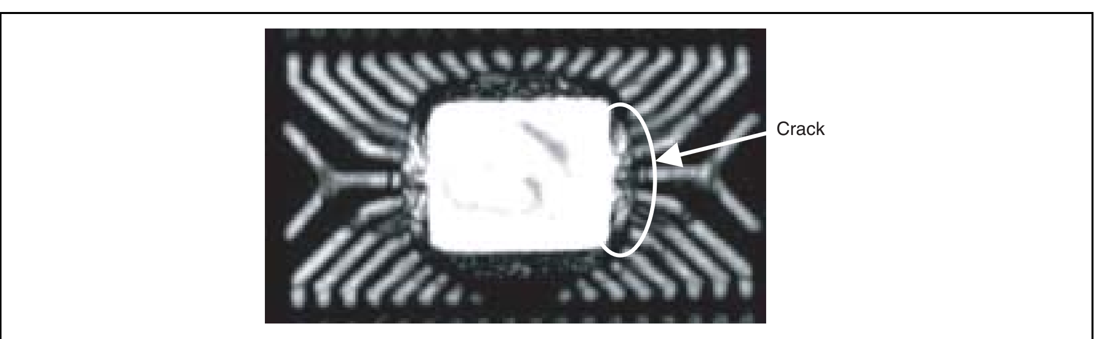


Figure 4.56 Example of Observing Internal Cracks/Delamination by SAT

(6) Problems Caused by Package Cracks

Various types of package cracks are considered and are listed in table 4.6. Quality problems differ, depending on the type of package crack. Package cracks confined to the rear surface occur most frequently. As the swollen unit pushes against the printed circuit board, it is displaced from the optimum assembly location and cannot be soldered correctly. The possibility of degradation of moisture resistivity with rear surface cracks is small, so this type causes the least damage. The resin used in Renesas's packaging adheres more strongly to the chip than to the die pad, so delamination occurs primarily between the die pad and the resin. This is why the proportion of rear-surface cracks originating at the die pad is high.

Table 4.6 Package Cracking Types and Problems[59]

No.	Package Crack Type	Shape	Problems
1	Package rear-surface crack		. Moisture resistivity degradation (least degradation)
2	Package side crack		. Moisture resistivity degradation (small degradation)
3	Crack intersecting a bounding wire		. Wire damage, open . Moisture resistivity degradation
4	Package top-surface crack		. Wire damage, open . Wire bond peeled off . Moisture resistivity degradation

(7) Measures for improvement in mounting

As described earlier, handling and storage after fabrication are very important for surface mount devices. However, controlling the environment alone is not sufficient. Because the packages absorb moisture during storage and cracks develop in the resin, the control of the storage time and baking prior to mounting are also necessary. Figure 4.57 shows the dehumidification characteristics of baked packages. As the figure shows, a baking process at 125°C lasting for 20 to 24 hours results in sufficient dehumidification. The dehumidification at 125°C depends on the resin thickness. Moisture-proof packing for protection from exposure to moisture during transportation and storage period is also effective. In addition, moisture-proof packing has the capability of satisfactorily preventing the external effect shown in figure 4.58.

In order to ensure quality (reliability), it is important to mount devices at as low a temperature as possible and in as short a time as possible while controlling the moisture absorption in the manner described above.

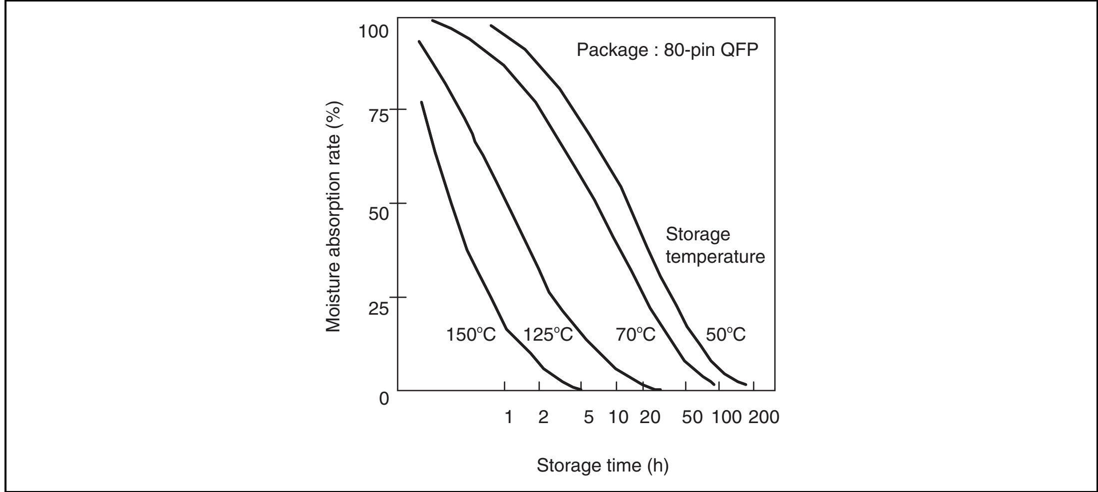


Figure 4.57 Dehumidification of Plastic Packages

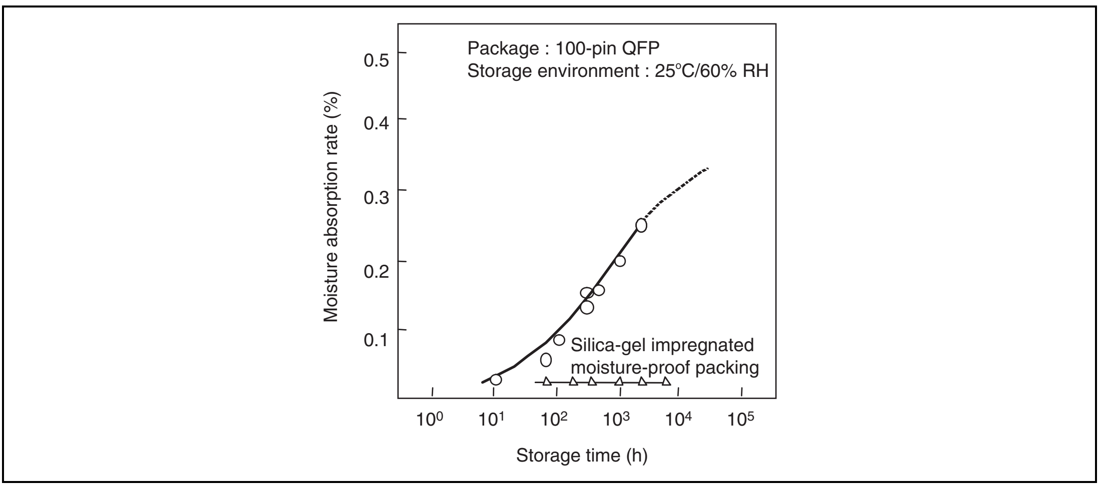


Figure 4.58 Effect of the Moisture-proof Pack

(8) Package Heat Resistance Test Method

In order to check the heat resistance of surface mount devices, it is necessary to reproduce the moisture absorption process, which progresses during storage through humidification, and then apply a heating process with conditions equivalent to those of the heat stress on soldering.

(a) About humidification

The allowable storage conditions for unpacked moisture-proof packing (level A to level S), shown in table 4.7, must be determined, and then their heat resistances evaluated after moisture absorption with the humidification conditions corresponding to the levels. The levels that products can satisfy depend on their types.

Table 4.7 Allowable Storage Conditions for Unpacked Moisture-Proof Packing

Level*[1]	JEDEC*[2]	Humidification Conditions	Classification	Storage Conditions after Unpacking
A	1	85°C, 85%, 168-hour storage	No moisture-proof packing required	30°C or less and 85% or less
B	2	85°C, 65%, 168-hour storage	1 year or less after unpacking	30°C or less and 70% or less
C	2a	30°C, 70%, (4 weeks + X) storage*[3]	4 weeks or less after unpacking	30°C or less and 70% or less
D	—	30°C, 70%, (2 weeks + X) storage*[3]	2 weeks or less after unpacking	30°C or less and 70% or less
E	3	30°C, 70%, (1 week + X) storage*[3]	1 week or less after unpacking	30°C or less and 70% or less
F	4	30°C, 70%, (72 hours + X) storage*[3]	3 days or less after unpacking	30°C or less and 70% or less
G	5	30°C, 70%, (48 hours + X) storage*[3]	2 days or less after unpacking	30°C or less and 70% or less
S	6	30°C, 70%, (Y + X) storage*[3]	Y days or less after unpacking	30°C or less and 70% or less

Notes: 1. Complies with JEITA standard EIAJ ED-4701/301 "Soldering Heat-Resistance Test (SMD)."

2. JEDEC-STD-020 levels corresponding to the moisture-sensitivity level (MSL) with moisture absorption conditions of 30°C, 60%.

3. X: Period of time including the storage time to moisture-proof packing after assembly and the storage time after packing.

Y: Length of warranty period of unpacked storage after delivery

(b) About heating

We perform a reflow heating process that simulates the mounting heat stress after humidification to confirm that there are no defects. Figures 4.59 and 4.60 show the conditions of the heating process. The packages must be mounted only under these conditions.

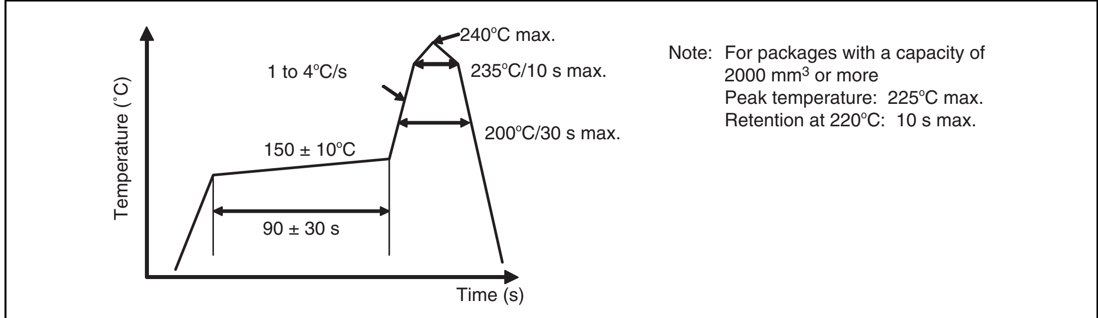


Figure 4.59 Reflow Heating Conditions for Eutectic Paste for Surface Mount Devices (Package Surface Temperature)

Specified point: Package surface

260˚C max.
255˚C/20 s max.
3˚C/s max.
217˚C/60 to 150 s
200˚C
150˚C
60 to 180 s
Package surface temperature (˚C)
Time (s)

Target packages: Small, Thin Package

QFP (less than 28 mm□), LQFP, TQFP, SOP, TSOP, TSSOP, BGA, CSP (FBGA), MPAK, CMPAK, SRP, URP, UFP, TEFP, LFPA, etc.

Specified point: Package surface

245˚C max.
Lead pin temperature: 260˚C max.
3˚C/s max.
240˚C/20 s max.
217˚C/60 to 150 s
200˚C
150˚C
60 to 180 s
Package surface temperature (˚C)
Time (s)

Target packages: Large, Thick Pacakge

QFP (28 mm□ or larger), QFJ, DPAK, LDPAK, HSOP, HTQFP1010, and RP8P

Notes:
1. During the storage period after opening the moisture-proof packing until reflow mounting, storage conditions are 30˚C/70% RH or less according to Renesas conventional moisture conditions. However, when following to the MSL standard of IPC/JEDEC, the storage conditions are 30˚C/60% RH or less.
2. The reflow condition for the large and thick packages, more than 28 mm x 28 mm, installed heat sink is shown below.
   Peak temperature: 240˚C max.
   Soldering temperature/time: 220˚C or more/30 to 50 s
   Pre-heating: 150 to 180˚C/60 to 120 s

Figure 4.60 Reflow Heating Conditions for Pb-Free Paste for Surface Mount Devices (Package Surface Temperature)

(9) Summary

In ensuring the quality (reliability) of surface mount devices, the following points are very important:

1. Control of moisture absorption of packages (after opening moisture-proof packs); and
2. Minute adjustment of mounting conditions.

To ensure the reliability of all our moisture-sensitive surface mount devices, the stress associated with the mounting process is mitigated by packaging them in moisture-proof packing cases containing a desiccant to protect from moisture. However, the following precautions should be taken:

1. To control the temperature and humidity of the place where semiconductor devices are stored and the duration of storage, and to use them within the specified time;
2. To use them as soon as the moisture-proof pack is opened; should devices be temporarily stored after the opening of the moisture-proof pack, they should be placed in the moisture-proof pack together with a desiccant, with the mouth of the pack folded over and sealed with a paper clip;
3. If devices are temporarily stored after the opening of the moisture-proof pack, they should be dried by the specified condition (high temperature baking) prior to mounting.
4. To mount devices at allowable heat conditions (refer to figure 4.59 for the eutectic paste and figure 4.60 for the Pb-free paste).

4.5 Mechanism of Failures Related to Handling

4.5.1 Electrostatic Discharge

Semiconductor devices are known for their miniature geometry. High-speed multi-functional devices are based on this miniature geometry. However, the fine structures of semiconductor devices are a weak point in that the devices are liable to be broken by generally possible levels of voltage or energy of static electricity.

This damage is a problem for both device manufacturers and electronic instrument manufacturers. Semiconductor manufacturers have designed protection circuits, but geometry constraints place a limit on their capability, so it is necessary to handle semiconductor devices carefully during processing, assembly and use to avoid damage due to electrostatic discharge.

(1) Damage by Electrostatic Discharge and Electrical Overstress

Devices can be damaged or destroyed by electrostatic discharge (ESD) as a consequence of the local heating caused by the discharge current flowing in the device and/or by device breakdown caused by the electric field.

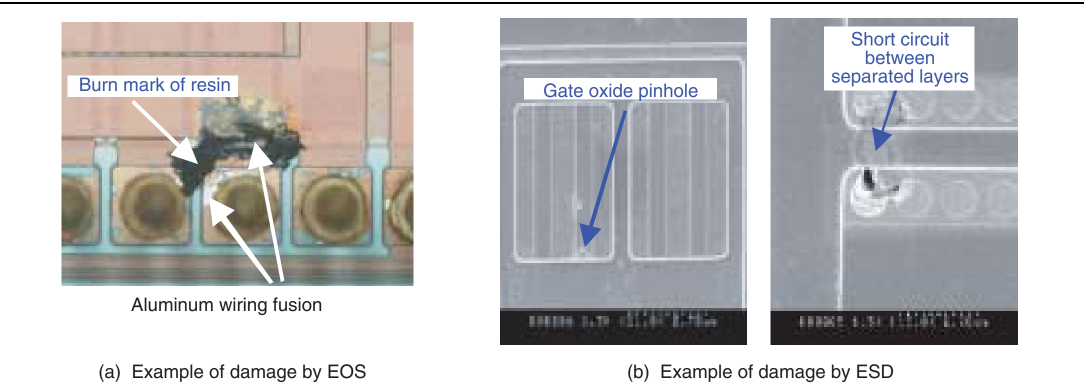
The Si and SiO_2 used as the primary materials in semiconductor devices can by nature withstand heat and voltage stress very well, but due to miniaturization of the devices, discharge current density is so high that melting and dielectric breakdown occur.

Dielectric breakdown is caused by the voltage drop due to currents flowing through resistances and by direct voltage application to the dielectric film. Device damage due to ESD is caused by an instant discharging of a charged conductor (or the device itself), and its small energy leaves behind traces of minute scars.

Table 4.8 MOS Device Failure Types from the Standpoint of Electric Stress Factors

Failure Mechanism	Stress Factors	Failure Modes
Bonding wire disconnection due to melting	EOS*	Occurred by high current. The broken ends of wire are rounded.
Melting metal disconnection	Mainly EOS	Occurred by high current. Metal balls as in electromigration are not seen.
Melting polysilicon disconnection	EOS or ESD	For polysilicon, as resistance values are large, power concentrates and melting occurs easily.
Contact section damage	EOS or ESD	Due to reverse bias current in junction, heat is transferred to contact section and aluminum metallization melts.
Heat degradation of oxide film	EOS or ESD	Junction reverse bias current heat is transferred to oxide film, resulting in degradation.
Junction degradation	EOS or ESD	Occurred by junction reverse bias current heat and the like
Hot electron, Trapping	EOS or ESD	Carriers accelerated by high electric fields are trapped in MOS transistor oxide films
Oxide film degradation due to electric field	Mainly EOS	Occurred by application of voltage to gate oxide film

Note: * EOS: Electrical overstress



(a) Example of damage by EOS

(b) Example of damage by ESD

Figure 4.61 Example of Comparison between EOS Damage and ESD Damage

As shown in table 4.8, damage due to ESD and electrical over-stress (EOS) such as surges result in similar failure modes, and it can be very difficult to determine which was the cause.

For example, high energy EOS is typically the cause of wires that have melted open as shown in figure 4.61 (a), but low energy EOS and ESD result in similar damage and failure analysis becomes complicated, and there are many cases where the true cause cannot be determined.[62] [63] EOS damage is not always caused by an electrical stress such as a surge. An incorrectly applied voltage due to incorrect handling, a short circuit caused by conductive particles, and other factors may cause EOS damage. If the extent of the EOS damage is serious, its cause may be not a surge or static electricity, in which case a wide-ranging investigation is required to determine the actual cause.

Device damage by ESD can be classified into melted interconnections (mostly considered as EOS), junction breakdown, dielectric film breakdown, and parametric drift due to charges being injected into the oxide films. Because the energy is small, as shown in figure 4.61(b), it is usually difficult to see traces of the damage with light microscopy. Accordingly, ESD damage analysis is not easy.

The mechanisms of junction, metallization film, and oxide breakdown are somewhat different from each other, but heat generated at discharge is one of the causes common to all.

For example, the well-known Wunsch & Bell model explains that junction breakdown is caused by the melting of silicon at a junction when the local temperature exceeds the melting point of Si, which is 1415°C. The temperature rise is due to the heating caused by the reverse bias ESD current.

The allowable applied power per unit area of the junction (P/A) is expressed in the following equation.[64] [65] [66]

$$\frac{P}{A} = \sqrt{\pi \cdot K \cdot \rho \cdot Cp} \ (Tm\text{-}Ti) \cdot t^{-1/2} \qquad (4\text{-}5\text{-}1)$$

where

- P: Applied Power (W)
- A: Junction Area (cm^2)
- K: Thermal Conductivity near the Junction (Si: 0.306 W/cm • K)
- ρ: Junction Density (Si: 2.33 g/cm)
- Cp: Specific Heat of the Junction (Si: 0.7566 J/g • K)
- Tm: Junction Melting Temperature (Si: 1688 K)
- Ti: Junction Initial Temperature (Room temperature = 298 K)
- t: Pulse Width (ESD duration)

All values with the exception of the pulse width (t) are constant in equation (4-5-1), so power tolerance per unit area at the junction is proportional to $t^{-1/2}$.

Figure 4.62 shows a plot of experimental values, which fall between those calculated from the equation above and 1/10 of those values.

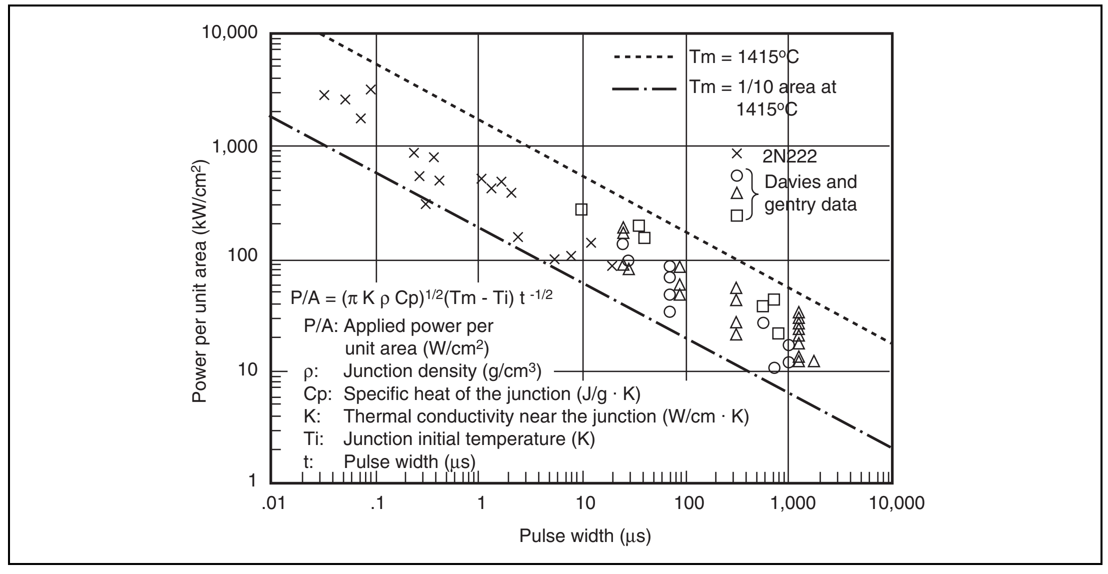


Figure 4.62 Wunsch & Bell Plot

As just described, damage due to heat depends on the amount of heat generated, specific heat, heat conductibility, and allowable temperature limit. These factors indicate that damage is fundamentally avoidable only by diffusion at heat-generated locations. However, when it is understood that most actual electrostatic discharges have pulse widths shorter than those indicated in figure 4.62 and that their energy is small, measures other than those dealing only with heat, such as protective elements, need to be considered.

By contrast, the cause of damage to a dielectric film is thought to be due to eventual destruction by Joule heat after the current leakage in the dielectric film increases over time in a high electric field. Because the gate oxide films of most MOS devices have a breakdown voltage of 10 to 20 V, which results in damage when an excessive voltage is applied, protective elements are required to prevent damage.

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Variation in device characteristics due to charge injection refers to the phenomenon of changes in characteristics due to the acceleration of carriers by locally generated potential differences so that the carriers become trapped in the oxide film. Such changes may recover or anneal out at elevated temperatures. Failure analysis is difficult since there are no visual indications for this failure mode.

(2) Charging Phenomena Requiring Caution When Handling Devices

From the standpoint of handling devices, the causes of charging are classified as types (a) to (c) below. The figures in this section (figures 4.63 to 4.65) illustrate charging on a device. Charging on a printed circuit board, tool, human body, or any other conductive substance can be substituted.

(a) Charging by friction or delamination

Figure 4.63 illustrates the well-known charging by friction/delamination phenomenon. A charged conductor discharges when it comes close to another conductor. In addition, it sometimes charges the other conductor by electrostatic induction or contact charging. On the other hand, a charged insulator does not discharge, but it may charge a conductor by electrostatic induction.

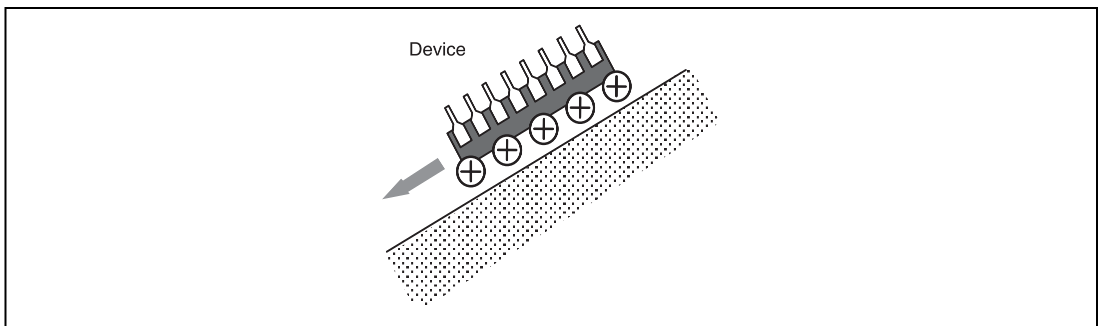


Figure 4.63 Triboelectric Charging

(b) Electrostatic induction phenomena

Electrostatic induction is a frequent phenomenon whenever devices are handled, but because it is not generally understood, attention needs to be paid to its causes.

As shown in figure 4.64, when a device, human body, tool, or other conductor in the floating state comes close to a charged conductor, electrostatic induction occurs in the conductor even though its total amount of electric charge is zero. If the conductor then contacts another conductor, it induces a discharge equivalent to that which would occur if it were charged. As a result, the discharge charges the device, and the device is in danger of discharging.

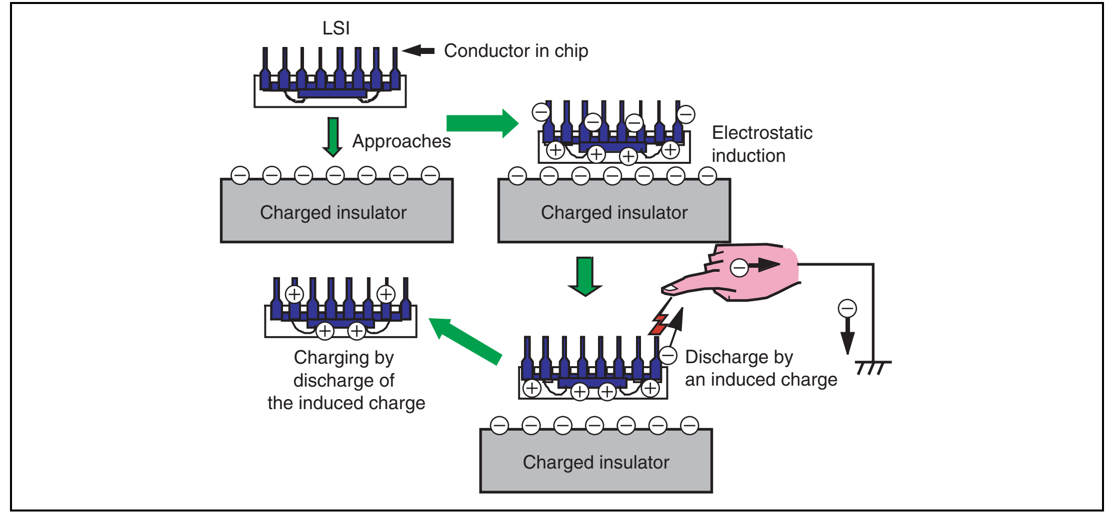


Figure 4.64 Discharge by Electrostatic Induction and Charging

(c) Contact charging

When an uncharged conductor contacts a charged conductor, the conductor becomes charged. Figure 4.65 illustrates an example of a case where a charged human body charges a device when the device is grasped.

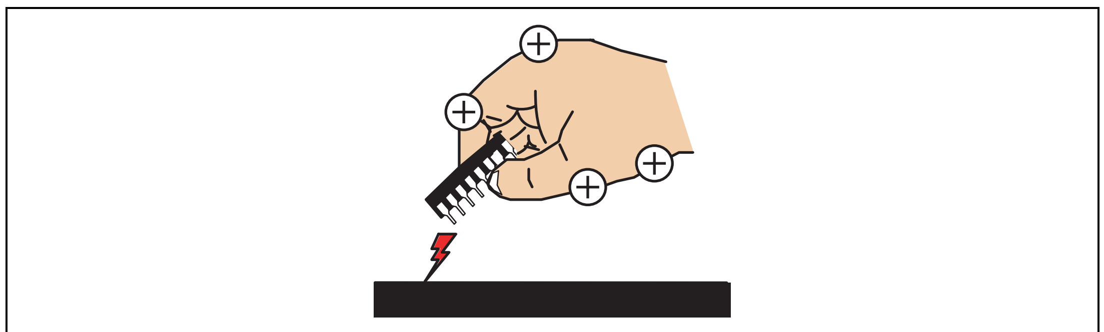


Figure 4.65 Contact Charging and Discharging

(3) ESD Phenomena that Can Damage a Device

An electrostatic discharge of a device occurs when a discharged current flows in the device. The higher the electric current, the easier it is for damage to occur. In the environments in which semiconductors are handled, since there are various conditions under which large currents flow, it is likely that, in most cases, good conductors (metal conductors in general) may be involved.

Two models exist for the types of discharge paths in devices. Figure 4.66 shows a model in which a conduction current flows between device pins, and figure 4.67 shows a model in which a conduction current flows between pins and a displacement current flows in the device capacitor. The model in figure 4.67 has a long discharge path and the capacitance and inductance are distributed on the path, so the model has a slower discharge than the model in figure 4.66.

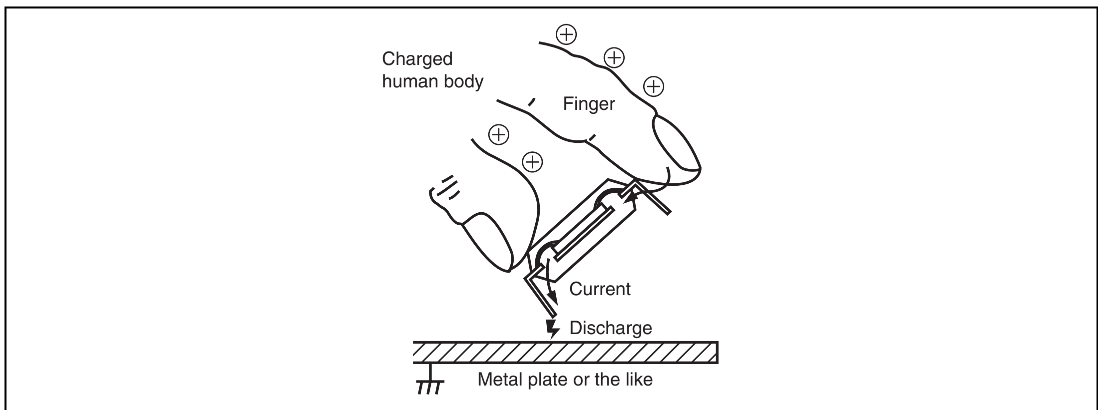


Figure 4.66 Discharge Model with Human Body
(Model in which a Conduction Current Flows between Device Pins)

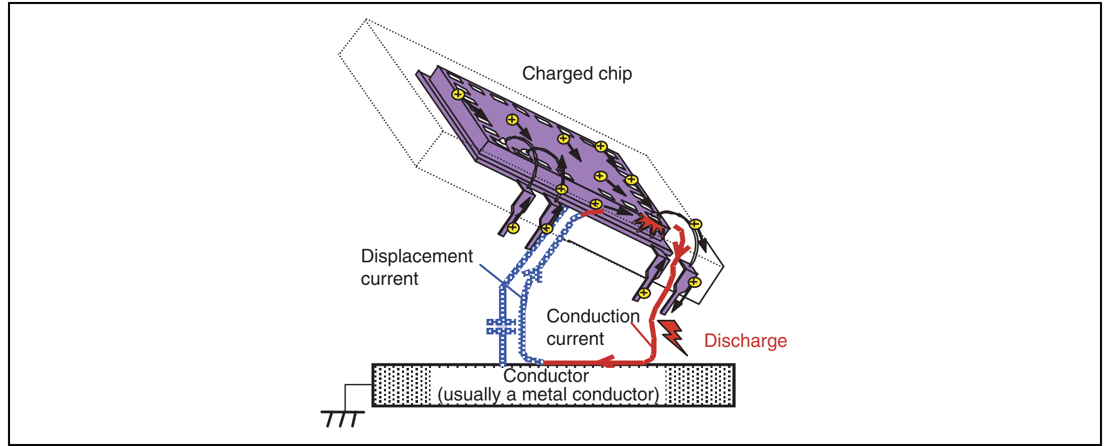


Figure 4.67 Discharge Model for Changed Device
(Model in which an Conduction Current Flows to the Discharging Pin
and a Displacement Current Flows to the Device Capacitance)

Figure 4.66 illustrates an example of a discharge current between a human body and a device pin. Figure 4.67 illustrates an example of a discharge between a device and a conductor (usually a metal conductor). As shown in the example, when a low-resistance substance such as a metal is involved, a discharge current flows easily and damage occurs easily. In addition, for the case in figure 4.66, when GND to which the current flows is a metal, damage occurs easily. Therefore, in environments in which devices are handled, it is necessary to pay attention not only to charged objects but also to objects to which the device comes into contact.

(4) Actual Discharge and Test Methods

Three major types of applicable test methods are currently available as practical electrostatic discharge models[67] [68]:

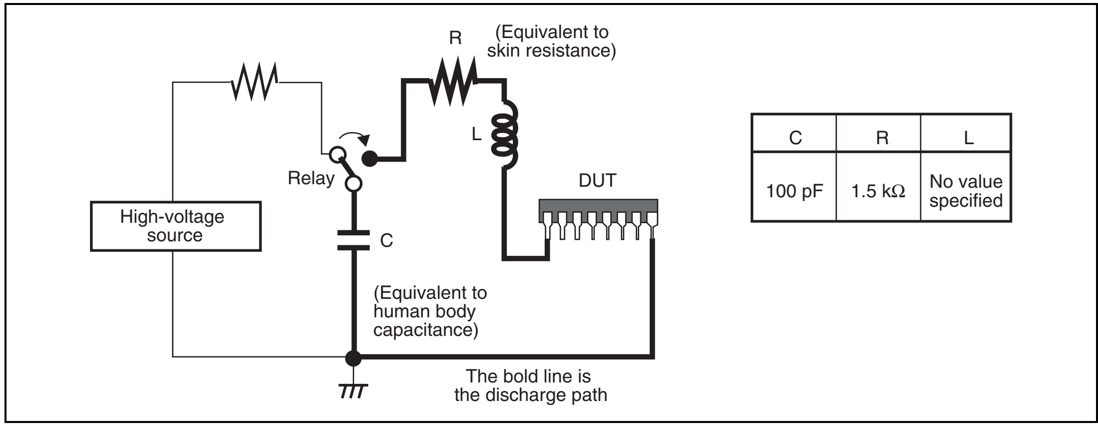
- Human body model: HBM
- Machine model: MM (replaces HBM)
- Charged device model: CDM

(a) Human body model test method

Figure 4.68 shows the Human Body Model (HBM): A human body charged with static electricity touching a device and discharging to a device pin.

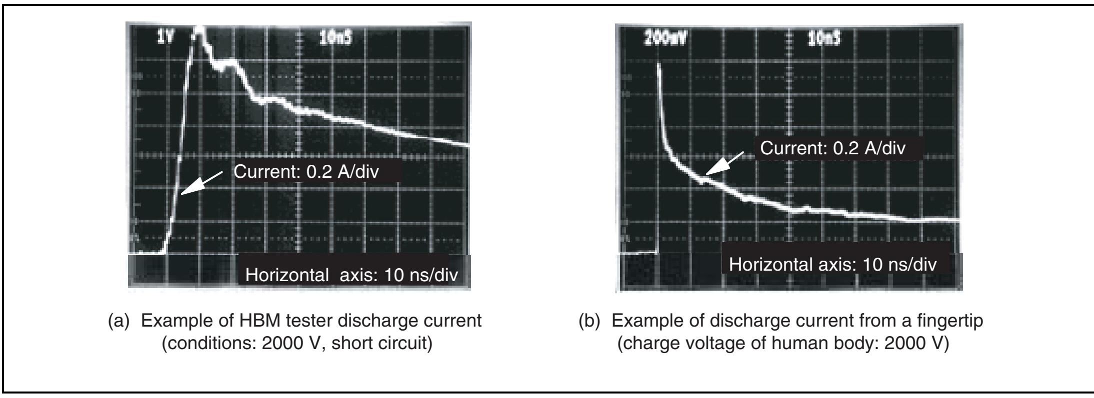
If any of the other pins are grounded or connected to a potential, a discharge current passes through the device and the device can be destroyed.

The ESD test circuit for the HBM is illustrated in figure 4.68. The charge on capacitor C represents the amount of charge on a typical human body. The resistor R simulates the skin resistance. JEITA, JEDEC and MIL standard specify 100pF and 1,500Ω.



C	R	L
100 pF	1.5 kΩ	No value specified

Figure 4.68 Test Circuit for Human Body Model



(a) Example of HBM tester discharge current (conditions: 2000 V, short circuit)

(b) Example of discharge current from a fingertip (charge voltage of human body: 2000 V)

Figure 4.69 Comparison of Human Body and HBM Tester Discharge Currents[72]

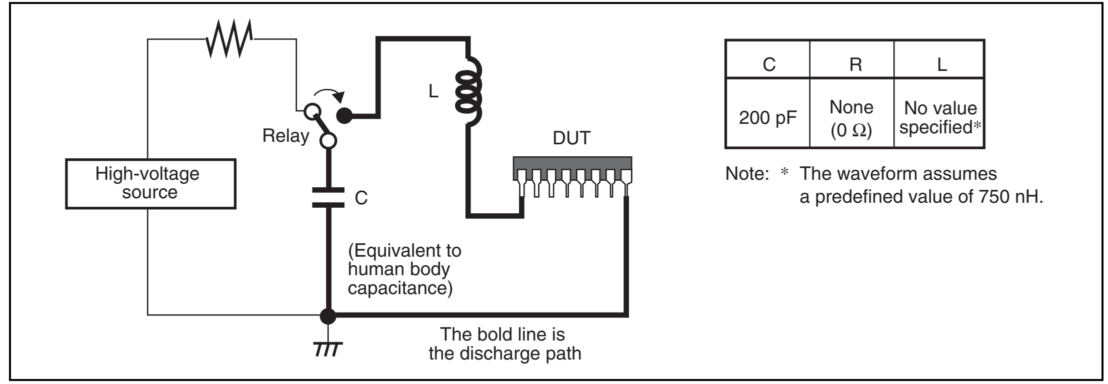
Figure 4.69 shows an example of the waveforms of discharges from the human body and the electrostatic discharge tester. The capacitance of the human body was about 300 pF (DC measurement method), but analysis of the discharge waveform reveals that the capacitance in the period during which a device-destroying high current is generated is effectively about several pF to several tens of pF. Since a full discharge takes several seconds, it is thought that the discharge proceeds through peripheral high-resistance elements. By contrast, since the tester has a single 1.5-kΩ resistor, the example shows a simple attenuating waveform, and its energy aspect is several times to 10 times severer than the human body discharge. Due to the wiring configuration, the example also shows a delayed rising edge by the inductance and other factors.[73]

Because the peak current influences the voltage generated in the device, and the peak current period influences the electrical power generated in the device, the HBM test method tends to emphasize destruction by electric power rather than actual device destruction.

(b) Machine model test method

The machine model test method is a human body test method that has been long used in Japan (figure 4.70). We have records indicating that Machine Model (MM) test methods were applied in our in-house tests in the latter half of 1960s as a test method that could reproduce a discharge from the human body or the like with a low voltage. Later, in 1981, it was standardized by EIAJ (present JEITA).

In countries other than Japan, the test method was named the MM method in the latter half of 1980s because the 200 pF and 0 Ω conditions did not take into account the skin resistance (0 Ω was assumed). The name "Machine Model," which implies a metal discharge, was therefore applied through a misunderstanding. You need to make sure that you understand this method is not related to a metal discharge. In 1996, JEDEC standardized this type of test method in the U.S. The background of the JEDEC's MM test method standardization was that the various types of MM test methods existing at the time needed be unified in response to many requests for test data from Japanese semiconductor users. AEC-Q-100 and other certification test standards attach importance to CDM and HBM and do not recommend this machine model for electrostatic discharge testing.



C	R	L
200 pF	None (0 Ω)	No value specified*

Figure 4.70 Machine Model Test Circuit

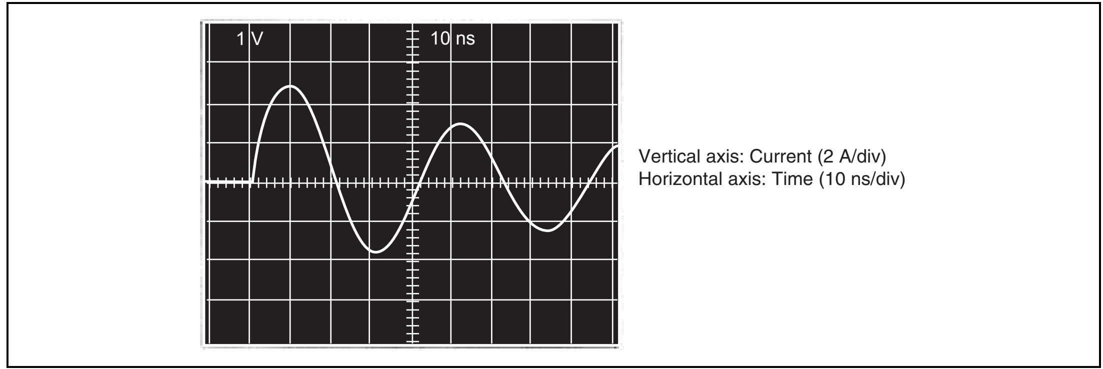


Figure 4.71 Discharge Waveform for Machine Model Test (Example with a Low Inductance L)

Output waveforms of the machine model test form a damped oscillation due to the influence of the test circuit inductance. Figure 4.71 shows an example of a waveform on a tester with shorter wiring than that specified by JEDEC and with a rapidly rising edge.

In semiconductor handling processes, however, it is thought that the metal objects easily picking up a charge are tools and implements. Since large components are grounded, they never pick up a charge as long as their grounding is not disconnected or otherwise compromised. Figure 4.72 shows an example of a discharge waveform of charged metal tweezers. A feature of the waveform is an extremely short rise time of about 100 ps, which is very close to the limit that a 3.5-GHz oscilloscope can measure. Other small metal tools produced a similar waveform. Discharges of metal substances are very rapid like this and similar to the CDM discharge described later. The reason is that charged metals have very little inductance.[71] [72]

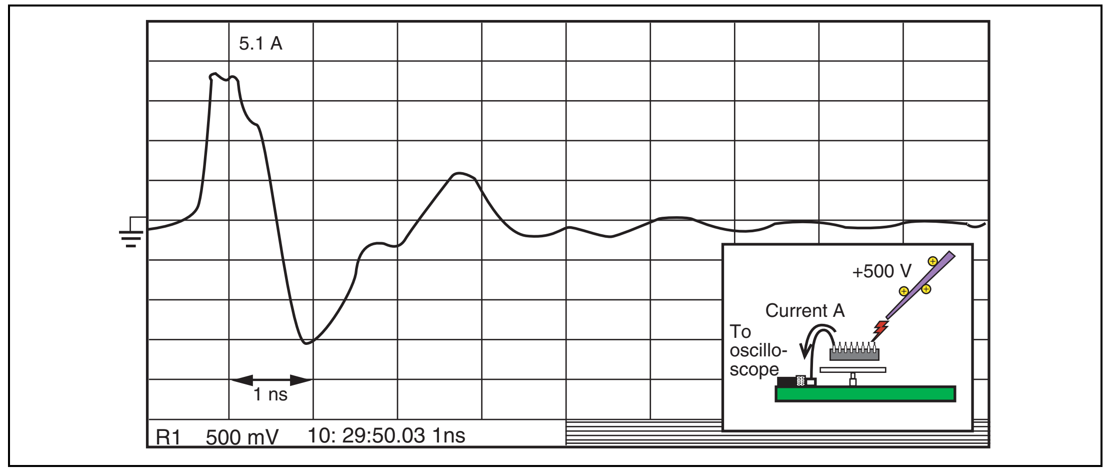


Figure 4.72 Discharge Waveform of Charged Metal Tweezers (Completely Different from That of the Machine Model)

As described earlier, the machine model test method indicates discharge characteristics completely different from those of a metal discharge that the method's name implies. It produces waveforms that are unusual in ordinary semiconductor handling processes, and provides no observable correlation between test and field. For these reasons, it has been demoted to a reference test model in the JEITA specifications.

(c) Charged device model test method

As the automation of assembly increases, there are fewer operations in which humans touch devices and ESD damage due to HBM has been declining. Conversely, however, the occasions on which devices encounter friction and/or electrostatic induction and come into contact with metal substances has increased.[69] [70] [74]

In view of this increase in CDM discharge from contact between a charged device and a metal substance as the trend toward process automation continues, the CDM is a discharge model that needs to be treated with caution.

As shown in figure 4.73, a CDM discharge is caused by a charged device that makes contact with a machine, tool, or other metal object. The discharge is very rapid, and an oscilloscope that supports bands over 1 GHz is required to observe it. Figure 4.74 shows the measurement result of the waveform of the CDM discharge example shown in figure 4.67. The rise time of the waveform is less than 100 ps, which is the limit the oscilloscope can measure. This indicates that the rise time is faster by two or more orders of magnitude than the rise time of the human body model or machine model.

However, as already mentioned, the CDM discharge is similar to the metal discharge shown in figure 4.72.

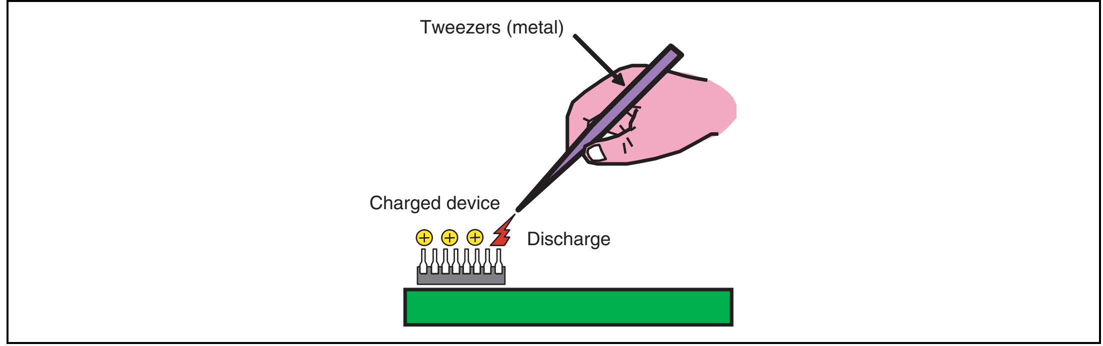


Figure 4.73 Discharge Example of the Charged Device Model (Example of a Discharge to a Metal Tool or the Like)

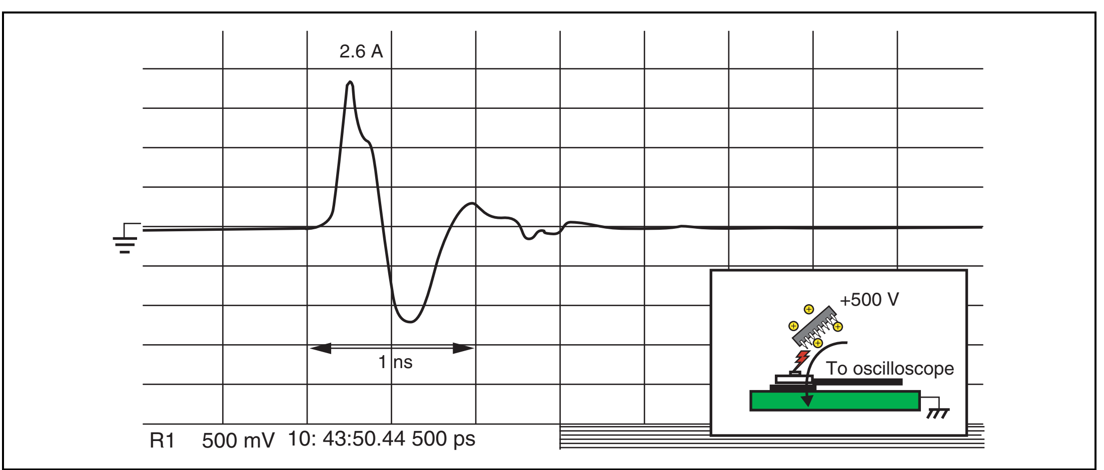


Figure 4.74 Discharge Waveform for Charged Device Model (Measured with a 3.5-GHz Oscilloscope)

ESD damage due to CDM discharge is caused by the current concentration discharging all of the stored charge through the pad of the discharge pin.

The discharge current waveform shows high-speed oscillations, and is accompanied by severe transients within the device. Dielectric breakdown of oxide films results in most cases due to excessive voltage spikes, but thermal damage sometimes occurs due to energy concentration.

Figure 4.75 shows an example of a CDM test circuit that we developed. In this test circuit, the ground bar corresponds to the tweezers or tool assumed in figure 4.73 for simulation of a realistic form of discharge.

Figure 4.76 shows the relationship between a fraction defective and a JEITA-standardized CDM test result. The fraction defective is based on one of our device package assembly processes that was a problem in the 1980s, when CDM problems had not been clearly identified and adequate measures had not been taken for them. As the figure shows, the CDM test clearly correlates with the process fraction defective, and the corner pins of the device have the potential to easily touch another substance and discharge.[70]

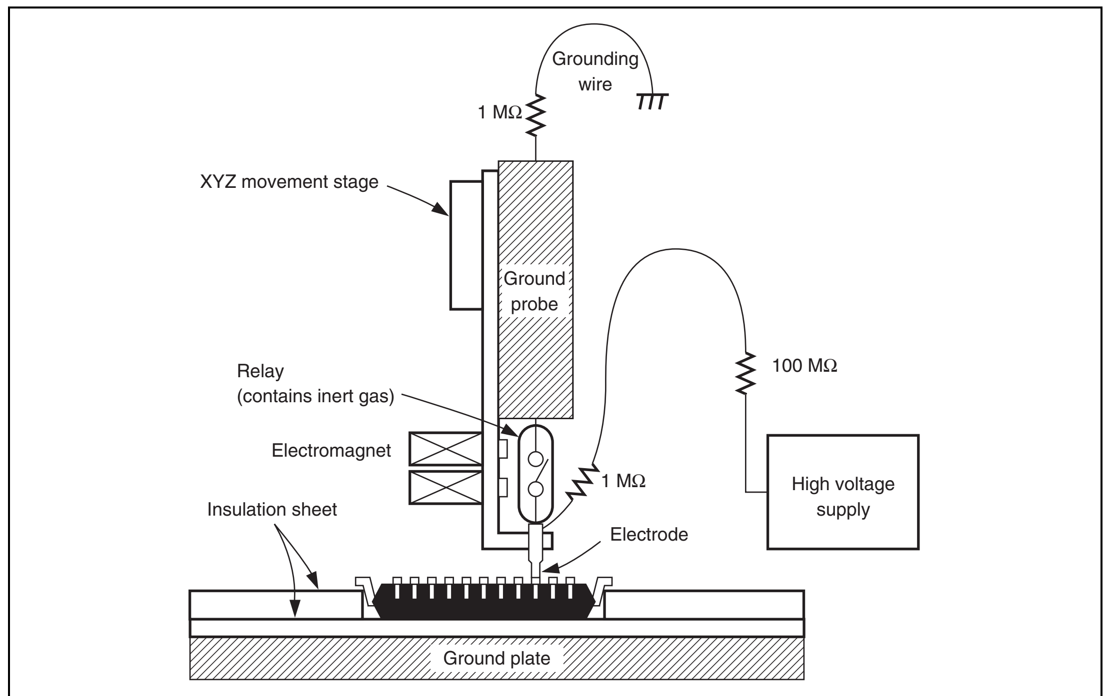


Figure 4.75 Example of CDM Test Circuit (Device is Charged from High-Voltage Source, Relay is Closed, and Device is Discharged to a Ground Bar)

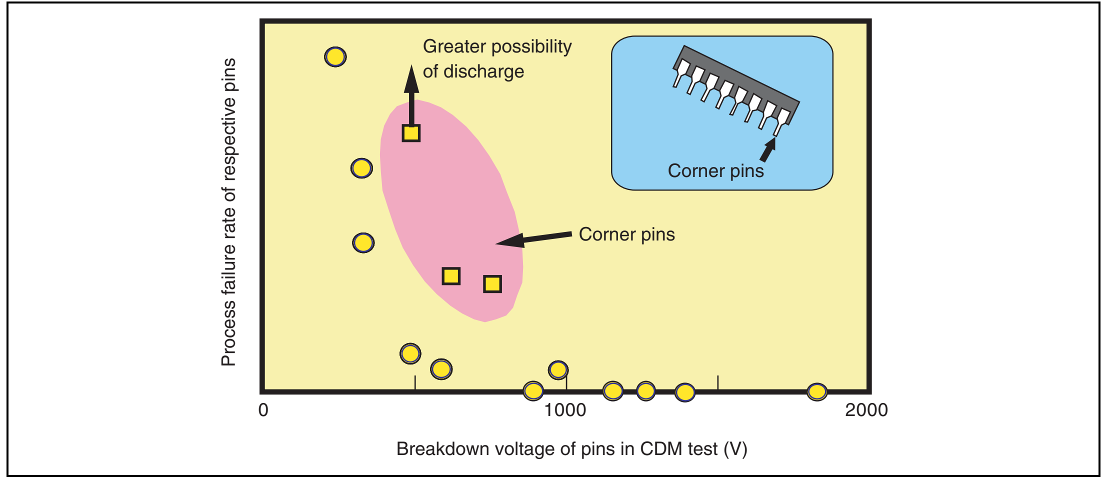


Figure 4.76 Relationship between Fraction Defective in Package Assembly Process and CDM Test Intensity

(d) Complex discharge, including CDM discharge

It is natural to suppose that, as shown in figure 4.77, the discharge resulting from a charged person touching a pin of the device in his hand to a metal object is purely an HBM type of discharge. Close investigation reveals that it contains, in fact, components equivalent to both HBM and CDM discharges. The following describes the complex discharge process.

When the metal plate and device pins come into contact, the electric field is propagated to the device, and the charge accumulated by the device begins to be discharged through the pins. This portion is equivalent to CDM discharge. Then, after the device charge has been transferred to the person, the charge on the person flows through the device and out the pin to the metal object. Figure 4.78 shows the resulting waveforms. In the example, the current discharged from the human body is small and the time is longer because of the influence of skin resistance. Accordingly, the CDM discharge current shows a higher value.

In cases other than the example above where a conductor touches another conductor with a different electric potential, a discharge equivalent to a CDM discharge is also observable. This may be one of the reasons why the CDM failure rate is high compared with other rates of failures in the market.[71] [72] [73]

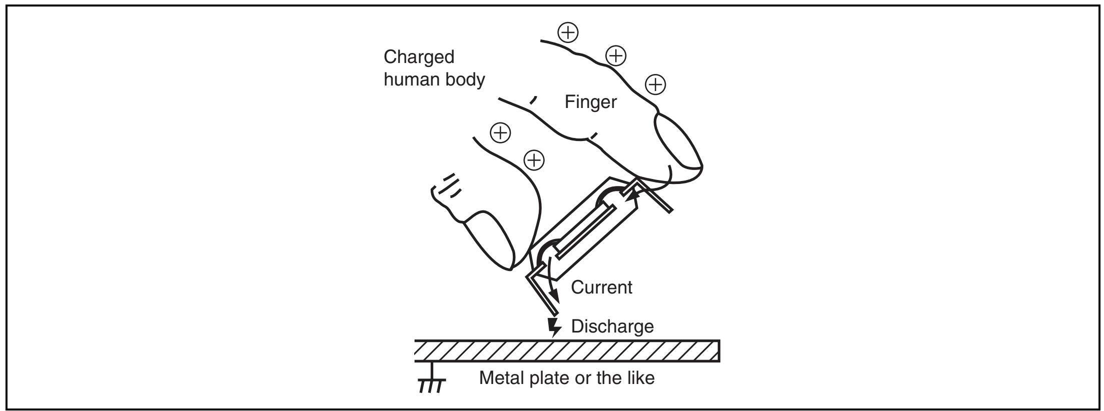


Figure 4.77 Example of Complex Discharge on HBM and CDM

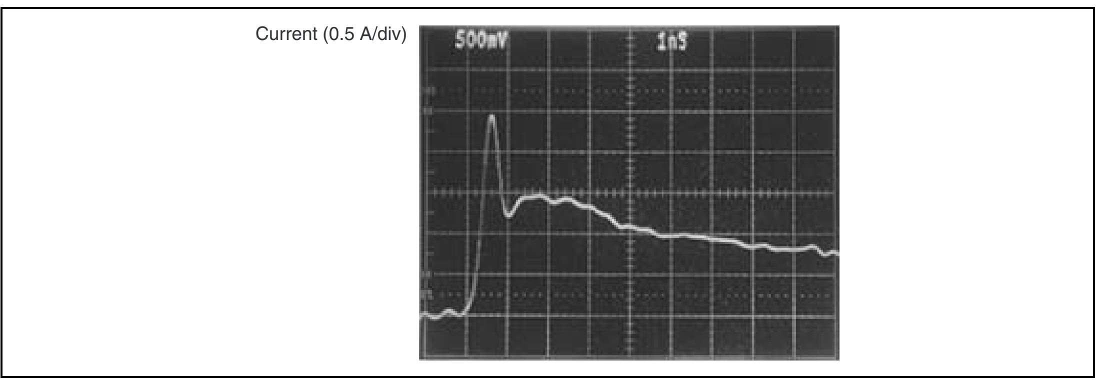


Figure 4.78 Example of Complex Discharge Current Waveform

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4.5.2 Latchup

(1) Introduction

Due to their low power consumption and wide noise margin, CMOS devices are widely used in low power and high performance applications. Large capacity memory chips and high performance microcontrollers are made using miniaturized CMOS technology.

A CMOS device includes parasitic NPN and PNP bipolar transistors in the input and output circuitries. Those transistors combine to form a parasitic thyristor. In a CMOS device to which power-supply bias has been applied, sufficient noise in the form of e.g. an external surge can turn the parasitic thyristor on, causing a continuous excessive flow of current through the power supply line. This phenomenon, called latchup, is seen for example in inspection processes after the chip has been mounted on a circuit board, and can destroy the device. Since the miniaturized structures of recent LSI circuits make them particularly susceptible to the effects of such parasitic elements, these factors must be fully considered in the design process.

(2) Mechanism

Because basic CMOS devices use inverters made from MOS transistors with two different characteristics as basic elements, parasitic bipolar transistors occur everywhere on a chip.

Equivalent circuits differ slightly depending on the parasitic element combinations, but one example of a cross section is shown in figure 4.79. Figure 4.80 shows the equivalent circuit for the parasitic transistor circuit in the cross-section example.

First we will consider the case where a sufficiently large positive DC or pulse current is applied to the output pin:

1. Transistor TR3 base-emitter junction is forward biased. TR3 turns on.
2. Current Ig flows through TR2 base resistance R_P to V_{SS}.
3. TR2 base potential increases due to R_P voltage drop. TR2 turns on.
4. Current flows from V_{CC} to V_{SS} through resistance R_N of TR1.
5. Due to voltage drop across R_N, TR1 base potential increases, and TR1 turns on.
6. Current flows from V_{CC} through turned on TR1 and base resistance R_P to V_{SS}.
7. The TR2 base current is biased again by this current.

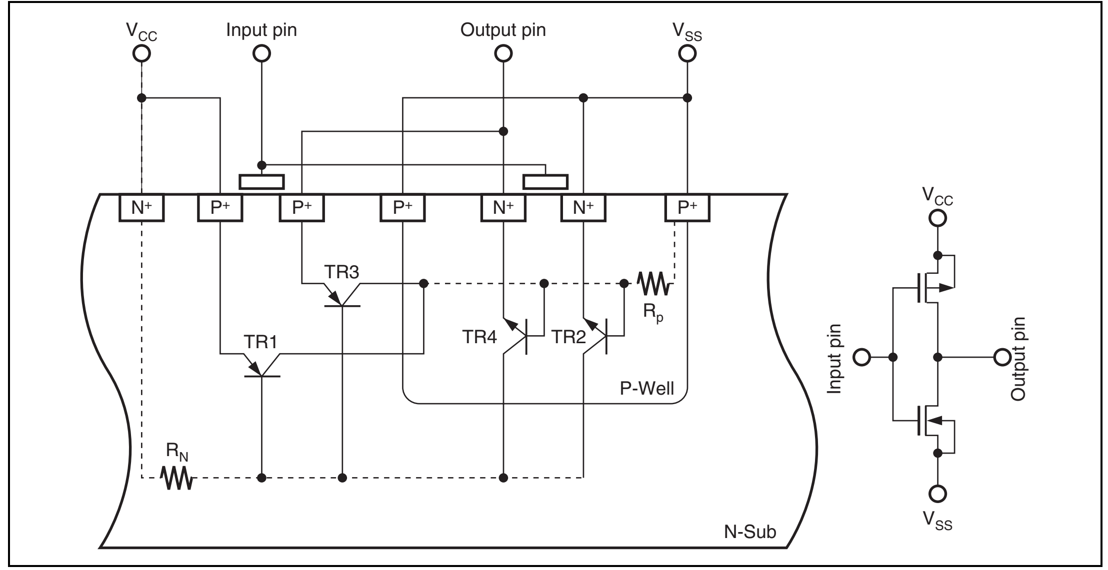

Figure 4.79 Cross Section of CMOS Inverter

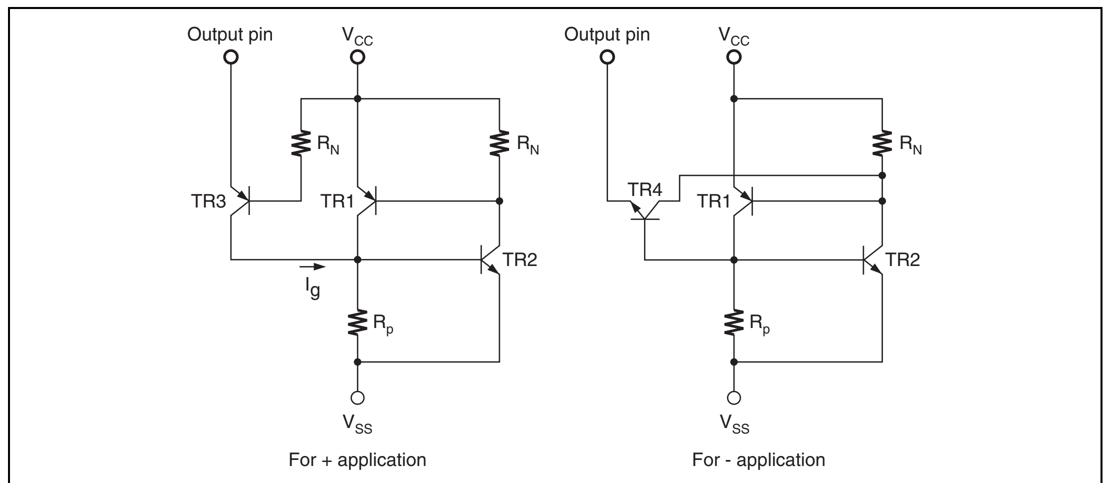

Figure 4.80 Parasitic Thyristor Equivalent Circuit

Positive feedback in the TR1-TR2 closed loop circuit maintains the current flow between V_{CC} and V_{SS} even if the trigger stops. TR4 transfers negative triggers. Positive feedback in the TR1-TR2 closed loop circuit maintains current flow just as in the case of the positive trigger.

(3) Evaluation Method

There are various methods to evaluate a circuit's susceptibility to latchup. Two methods defined in EIAJ ED-4701-1/test method 306, and EIA/JEDEC/JESD78 are explained below.

(a) Current pulse injection method

A trigger pulse is applied to the input or output pin of a device with the specified supply voltage applied, as in figure 4.81. The current of the trigger pulse is increased until latchup occurs.

If input/output resistances are high and the trigger current cannot be injected, the application of the output voltage from the trigger pulse current source is stopped at a maximum value (clamp voltage) to prevent destruction of the device. Care must be taken not to cause destruction due to excessive current injection. After the latchup test it is important to confirm that the device being tested has not been destroyed.

(b) Excessive supply-voltage method

The excessive supply-voltage method is shown in figure 4.82. The device is evaluated with its supply voltage set to the absolute maximum rating to measure the resistivity to latchup.

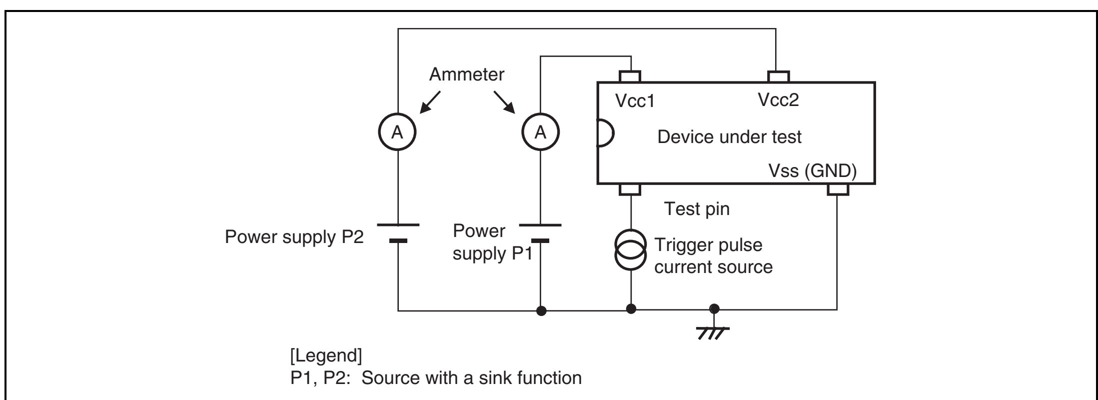

Figure 4.81 Latchup Test Circuit (Pulse Current Injection Method)

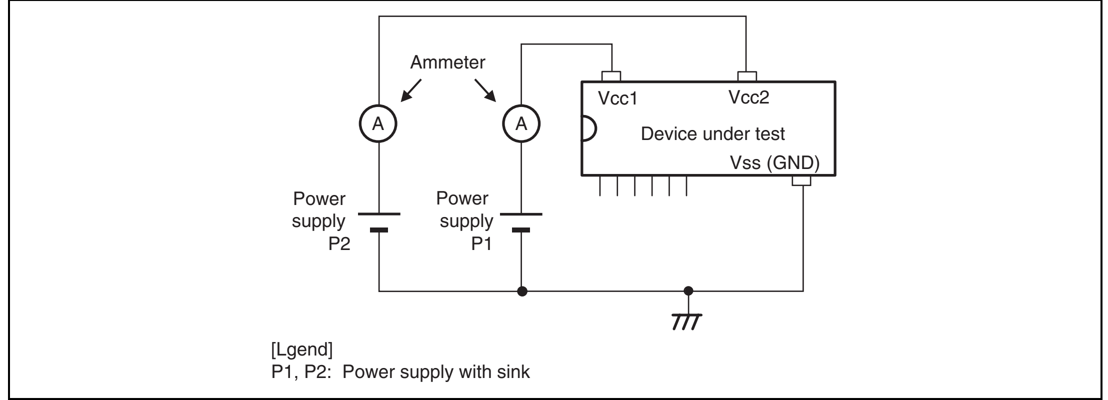

Figure 4.82 Latchup Test Circuit (Excessive Supply-Voltage Method)

4.5.3 Power MOS FET Damage

Power MOS FETs are superior power devices with excellent high-speed switching characteristics and a negative temperature characteristic. Power MOS FETs are therefore widely used in switching power supplies and motor controls where high efficiency and accuracy are important considerations. Their uses in electrical equipment for automotive application, office automation (OA), and lighting are expanding.

However, damage occurs in high frequency and high power applications due to the miniaturized cell design peculiar to power MOS FETs (figures 4.83 and 4.84).

(1) Inductive Load Damage (Avalanche Breakdown)

Avalanche breakdown of a MOS FET can be caused by the back electromotive force generated in high-speed switching applications by inductive loads such as transformers and motors. When the back electromotive force generated at inductance L causes avalanche breakdown between the drain and source of the MOS FET, the MOS FET is destroyed by the operation of the parasitic transistor that is inherent in the structure of the power MOS FET.

While the MOS FET is in the process of avalanche breakdown, part of the drain current flows as an avalanche current through the base resistance R_B under the source region (N^+). When the voltage drop across resistor R_B becomes large enough, the parasitic bipolar transistor is turned on, producing a concentration of current that destroys the MOS FET.

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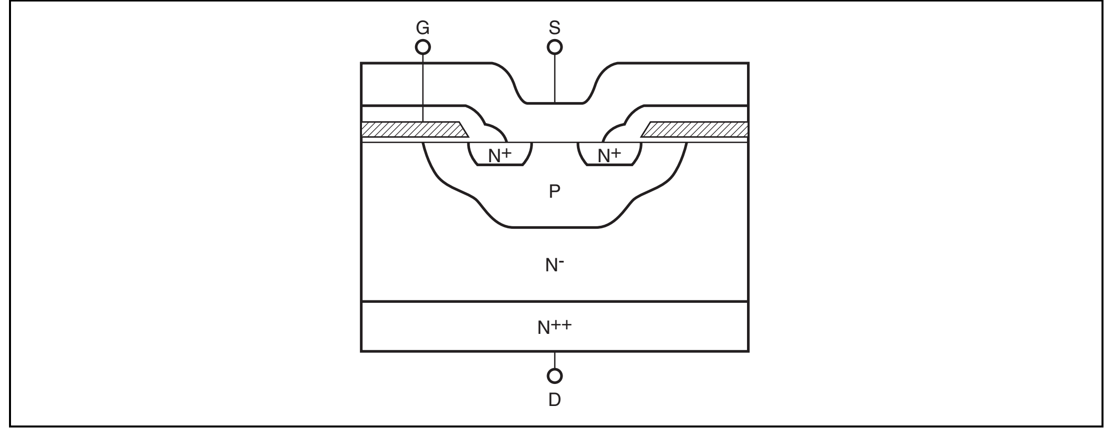

Figure 4.83 Cross Section of a Power MOS FET

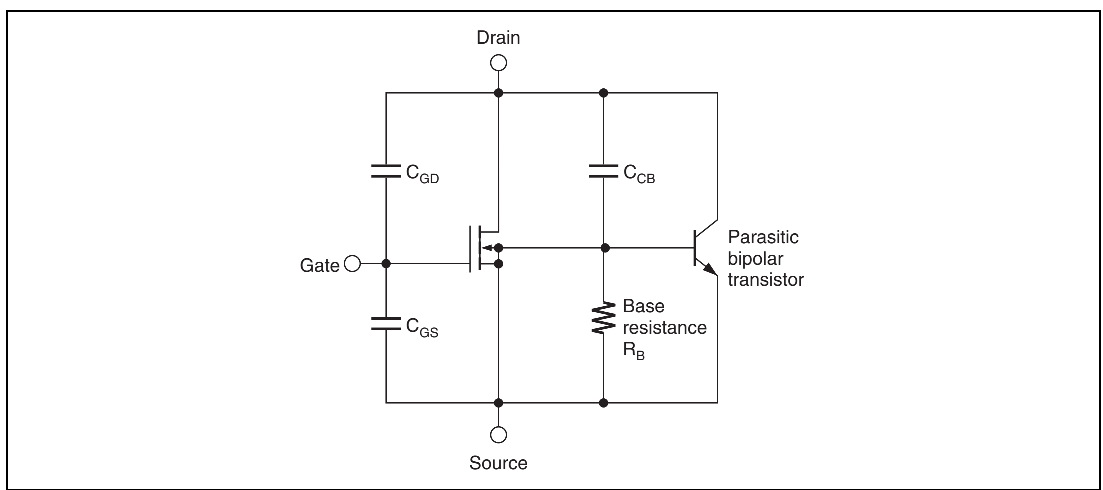

Figure 4.84 Equivalent Circuit of a Power MOS FET

(2) Evaluation Method

An evaluation circuit diagram and operating waveform are shown in figures 4.85 and 4.86. When the MOS FET is turned off and the gate voltage is decreased to the threshold voltage or lower, the drain current I_D flowing through the inductance L decreases, and the drain voltage V_{DS} rises rapidly. Once the voltage reaches $V_{DSX(SUS)}$, an avalanche breakdown occurs in the power MOS FET, and the drain voltage becomes constant. Energy stored in inductance L is released as heat and dissipates within the power MOS FET. Avalanche tolerance is the ability to dissipate the energy stored in inductance L without destroying the power MOS FET.

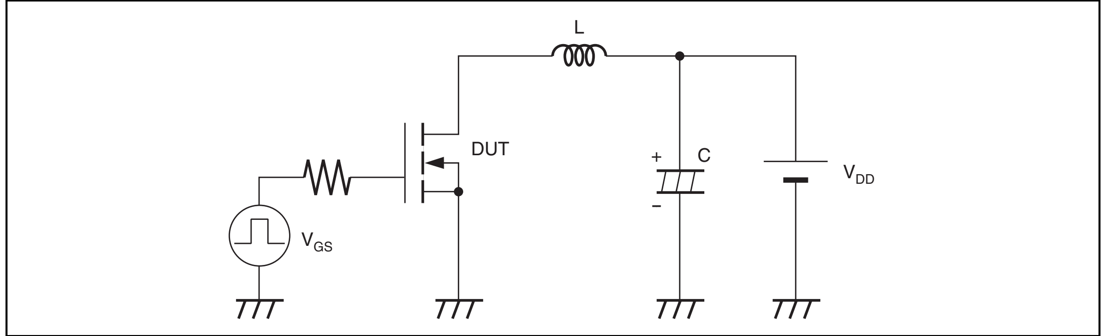

Figure 4.85 Avalanche Tolerance Evaluation Circuit Diagram

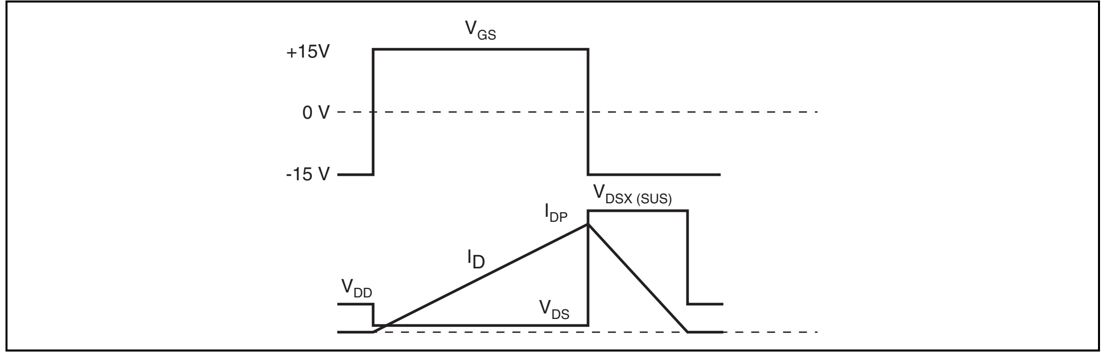

Figure 4.86 Avalanche Waveforms

(3) Electrostatic Discharge of Gate Oxide Film

Power MOS FETs are power elements, but they are susceptible to damage due to electrostatic surges or excessive gate voltages because they incorporate MOS structures.

Gate protection structures are necessary for device reliability. However, a vertical-type power MOS FET with the DMOS structure is optimized for high-voltage and high-capacitance applications, so incorporation of protective elements using PN junctions is difficult due to their parasitic effect.

Resistance to ESD can be improved through the use of polycrystalline silicon elements above the dielectric film (figure 4.87).

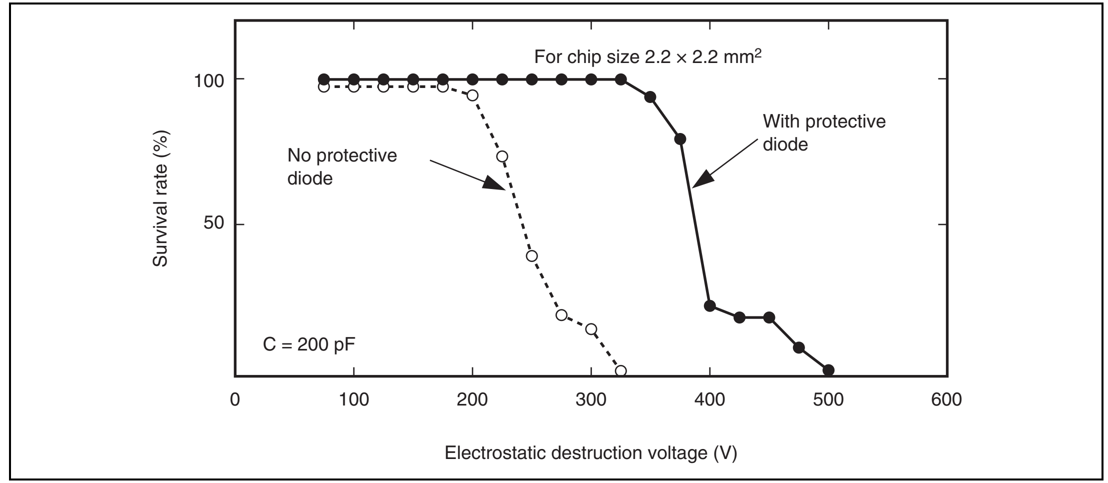

Figure 4.87 Electrostatic Discharge Strength of a Gate Oxide Film

(4) Damage by Operating Voltage Drop in Practical Use

In practical use, the gate voltage for most applications is about 10 V. (Low-voltage applications use a gate voltage around 4 V.) Should the gate voltage be allowed to drop, the device may then operate in the active operation range and out of the Area of Safe Operation (ASO) in practical condition (depends on the heat radiation condition), potentially damaging the device (see figure 4.88). Therefore, it is necessary to check the excessive load, and that the gate voltage has not been lowered transitionally due to the change of the power supply voltage at power-on.

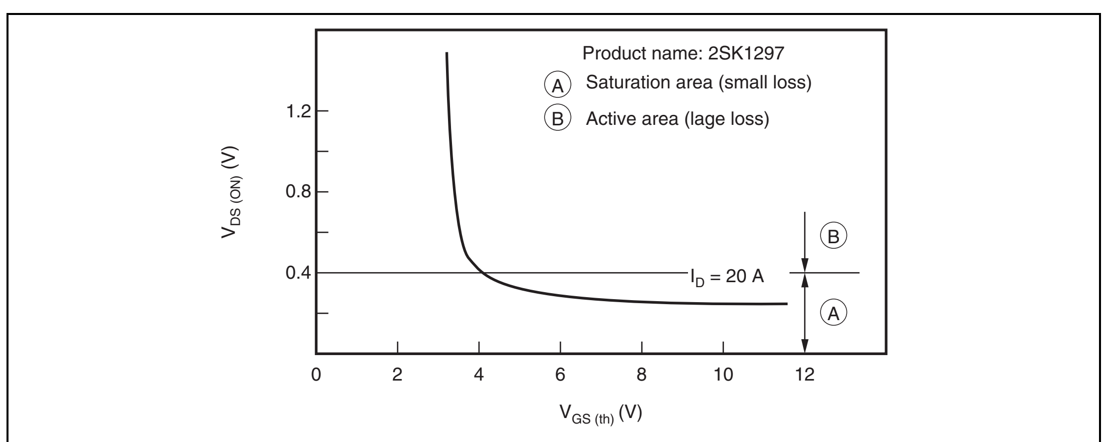

Figure 4.88 $V_{ds(ON)}$ - $V_{gs(th)}$ Characteristics in Practical Use

References:

[1] R. H. Dennard et al: "Design of Ion-Implanted MOS FET's with Very Small Physical Dimensions," IEEE Journal of Solid State Circuits SC9, p. 256-268, 1974

[2] Reliability Center for Electronic Components of Japan: "Report on Failure Model and Acceleration Factor of Reliability Test for LSI," R-2-RS-02 (1990)

[3] Reliability Center for Electronic Components of Japan: "Report on In-process Reliability Technique for ICs," R-6-RS-02 (1995)

[4] E.Wu et al.: "Polarity-Dependent Oxide Breakdown of NFET Devices for Ultra-Thin Gate," Proc 2002. IEEE IRPS p. 60-72

[5] John S. Suehle et al.: "Field and Temperature Acceleration of Time-Dependent Dielectric Breakdown in Intrinsic Thin SiO2," Proc 1994, IEEE IRPS p. 120-125

[6] H. Satake et al.: "Impact of TDDB Distribution Function on Lifetime Estimation in Ultra-Thin Gate Oxides," SSDM, Sendai, p. 248-249, 2000

[7] T. H. Ning: "Hot-carrier Emission Currents in N-channel IGFET's," Int. Election Device Meet. Tech, Dig., p. 144-147, 1977

[8] E. Takeda, H. Kume, Y. Nakagome and S. Asai: "An As-P (n+n-) Double Diffused Drain MOS FET for VLSIs," 1982 Symp. on VLSI Tech. Dig., p. 40-41, Sep. 1982

[9] A. Toriumi, M. Yoshimi and K. Taniguchi: "A Study of Gate Current and Reliability in Ultra-Thin Gate Oxide MOS FET's," 1985 Symp. on VLSI Technology, Tech, Dig., p. 110-111, May, Kobe.

[10] S. Tam, F. C. Hsu, P. K. Ko, C. Hu and R. S. Muller: "Hot-Electron Induced Excess Carriers in MOS FET's," IEEE Electron Device Letters, Vol. EDL-3, No. 12, Dec. 1982

[11] Y. Nakagome, E. Takeda, H. Kume and S. Asai: "New Observation of Hot-Carrier Injection Phenomena," Jpn. J. Appl. Phys. Vol. 22, Supplement 22-1, p. 99-102, 1983

[12] T. H. Ning, C. M. Osburn and H. N. Yu: "Emission Probability of Hot-Electron from Silicon into Silicon Dioxide", J.Appl. Phys., p. 286 - 293, Vol. 48, 1977

[13] E. Li et al: "Hot Carrier Induced Degradation in Deep Submicron MOS FETs at 100°C", Proc 2000, IEEE IRPS p. 103-107

[14] P. Su et al: "Excess Hot-Carrier Currents in SOI MOS FETs and Its Implications", Proc 2002, IEEE IRPS p. 93-97

[15] H. Aono, E. Murakami et al.: "NBT induced Hot Carrier (HC) Effect:Positive Feedback Mechanism in p-MOS FET's Degradation," Proc 2002, IEEE IRPS p. 79-85

[16] J. H. Stathis et al.: "Broad Energy Distribution of NBTI-Induced Interface States in P-MOS FETs with Ultra-Thin Nitrided Oxide," Proc 2004, IEEE IRPS p. 1-7

[17] V. Huard et al.: "Evidence for Hydrogen-Related Defects during NBTI Stress in p-MOS FETs," Proc 2003, IEEE IRPS p. 178-182

[18] J. S. Lee et al.: "Hydrogen-Related Extrinsic Oxide Trap Generation in Thin Gate Oxide Film during Negative-Bias Temperature Instability Stress," Proc 2004, IEEE IRPS, p. 685 - 686

[19] H. Aono, E. Murakami et al.: "Modeling of NBTI Degradation and Its Impact on Electric Field Dependence of the Lifetime," Proc 2004, IEEE IRPS, p. 23-27

[20] K. Jeppson and C. Stenssen: "Negative Bias Stress of MOS Devices at High Electric Fields and Degradation of MOS Devices," J. App. Phys., Vol. 48, p. 2004, 1977

[21] Huard and M. Denais: "Hole Trapping Effect on Methodology for DC and AC Negative Bias Temperature Instability Measurements in pMOS Transistors," Proc 2004, IEEE IRPS, p. 40-45

[22] G. Chen et al.: "Dynamic NBTI of PMOS Transistors and its Impact on Device Lifetime," Proc 2003, IEEE IRPS, p. 196 - 202

[23] S. S. Tan et al.: "A New Waveform-Dependent Lifetime Model for Dynamic NBTI in PMOS Transistor," Proc 2004, IEEE IRPS, p. 35-39

[24] J. R. Black: "Physics of Electrmigration," Proc. 1974, IEEE IRPS, p. 142-159

[25] J. R. Black: "Electromigration-A Brief Survey and Some Recent Results," IEEE, ED-4, (1969) p. 338-347

[26] Matsumoto, Iwasaki, Sawada, and Otsuki: "Disconnection of Al Thin Film Due to Electromibration (2)," 5th Symposium on Reliability, Integrity Proc., p. 393 (1975)

[27] Matsumoto, Takano, Iwasaki, Nishioka, and Otsuki: "Disconnection of Al Thin Film Due to Electromibration," Japan Science Technology Association 4th Symposium on Reliability, Integrity Proc., p. 391 (1974)

[28] T. Makihara, T. Ichiki, and T. Miyakawa: "Confirmation of Effectiveness of Short-Term Electromigration (EM) Evaluation Methods with Wafer Level Reliability (WLR) Technique," Japan Science Technology Association 35th Symposium on Reliability, Integrity Proc. p. 29 - 32 (2005)

[29] J. Klema, R. Pyle and E. Domangue: "Reliability Implications of Nitrogen Contamination during Deposition of Sputtered Aluminum/Silicon Metal Films," The 22nd Annual Proc. of International Reliability Physics Symp., p. 1-5 (1984)

[30] J. Curry, G. Fitzgibbon, Y. Guan, R. Muollo, G. Nelson and A. Thomas: "New Failure Mechanisms in Sputtered Aluminum-Silicon Films," The 22nd Annual Proc. of International Reliability Physics Symp., p. 6-8 (1984)

[31] S. Mayumi, T. Umemoto, M. Shishino, H. Nanatsue, S. Ueda and M. Inoue: "The Effect of Cu Addition to Al-Si Interconnects on Stress Induced Open-Circuits Failures," The 25th Annual Proc. of International Reliability Physics Symp., p. 15-21 (1987)

[32] Nishikubo, Ogami, Miyamoto, Maki, and Matsumoto: "Al Thin Film Wiring Electro/Stress Migration Failures," Japan Science Technology Association 19th Symposium on Reliability, Integrity Proc., p. 255 (1989)

[33] E. T. Ogawa et al.: "Stress Induced Voiding Under Bias Connected To Wide Cu Metal Leads," Proc. 2002 IEEE IRPS, p. 312-321

[34] A. V. Glasow et al.: "The Influence of Te SiN Cap Process on The Electromigration and Stressvoiding Performance of Dual Damascene Cu Interconnects," Proc. 2003 IEEE IRPS, p. 146-150

[35] K. Y. Y. Doong et al.: "Stress-induced Voiding and Its Geometry Dependency Characterization," Proc. 2003 IEEE IRPS, p. 156-160

[36] C. J. Zhai et al.: "Stress Modeling of Cu/Low-k BEOL-Application to Stress Migration," Proc. 2004 IEEE IRPS, p. 234-239

[37] T. C. May, et al: "A New Physical Mechanism for Soft Errors in Dynamic RAMs," Proc. 1978 IEEE IRPS, p. 33-40

[38] S.Yamamoto et al.: "Neutron-Induced Soft error in Logic Devices Using Quasi-Mono energetic Neutron Beam," Proc. 2004 IEEE IRPS, p. 305-309

[39] S. Okikawa, M. Sakimoto, M. Tanaka, T. Sato, T. Toya, and Y. Hara: "Stress Analysis of Passivation Film Crack for Plastic Molded LSI Caused by Thermal Stress," Proc. of ISTFA, p. 275 (1983)

[40] M. Tanaka, H. Ozaki, S. Oyama: "History of LSI's Cyclic Resistance to Temperature and Ideal Reliability Tests," Japan Science Technology Association 31st Symposium on Reliability, Integrity Proc. July, 2001, p. 107-112

[41] Report on Achievement of Expenses for Commission of Ministry of Economy, Trade, and Industry Priority Field R&D, 2002: "Standard Authentication R&D - Standardization of Reliability Evaluation Methods with New Junction Techniques for High-Density Mounting," Japan Electronics and Information Technology Industries Association, May, 2003, p. 76-99

[42] Kolesar, S. C.: "Principle of Corrosion", *The 12th Annual Proc. of International Reliability Physics Symp.*, p. 155 (1974)

[43] Iwamori, Mizoguchi, Nishioka, Kawatsu, and Otsuki: "Influence from Bias Application Conditions to Plastic Mold IC Moisture Resistance," *IEICE Collected Papers of Lectors on General Conference*, Lecture No. 406, (1978)

[44] Iwamori, Mizoguchi, Nishioka, Kawatsu, and Otsuki: "Plastic-Sealed IC Moisture Resistance Evaluation and Test Methods," Japan Science Technology Association 8th Symposium on Reliability, Integrity Proc. p. 71 (1978)

[45] W. M. Paulson and R. W. Kirk: "The Effects of Phosphorus-Doped Passivation Glass on the Corrosion of Aluminum," *The 12th Annual Proc. of International Reliability Physics Symp.*, p. 172 (1974)

[46] D. S .Peck and C. H. Zierdt: "Temperature-Humidity Acceleration of Metal-Electrolysis in Semiconductor Devices," *The 11th Annual Proc. of International Reliability Physics Symp.*, p. 146 (1973)

[47] F. N. Sinnadurai: "The Accelerated Aging of Plastic Encapsulated Semiconductor Devices in Environment Containing A High Vapor Pressure of Water," *Microelectronics and Reliability*, Vol. 13, p. 23 (1974)

[48] N. Lycoudes: "Practical Uses of Accelerated Testing," *The 13th Annual Proc. of International Reliability Physics Symp.*, p. 257 (1975)

[49] J. L. Flood: "Reliability Aspects of Plastic Encapsulated Integrated Circuits", *The 10th Annual Proc. Of International Reliability Physics Symp.*, p. 95 (1972)

[50] M. Tanaka, T. Shoji, R. Kimoto, H. Kawakubo, and K. Ishigaki: "Resistance to Wave-Soldering Heat Test Method for SMDs," 3rd RCJ Reliability Symposium, p. 21-26, 1993

[51] K. Okada, T. Shoji, and M. Tanaka: "Schematization of Soldering Methods as Viewed from Heat Stress of Surface Mounted LSIs," Japan Science Technology Association 26th Symposium on Reliability and Integrity Proc. p. 39-44, 1996

[52] A. Suzuki, G. Murakami, and M. Sakimoto: "Higher Reliability of Flat Package ICs in View of Soldering," Japan Science Technology Association 14th Symposium on Reliability and Integrity Proc. p. 303-306, 1984

[53] M. Tanaka, M. Sakimono, and K. Nishi: "Surface Mount Package Reflow Soldering Heat Evaluation through Non-Destructive Inspection," Semiconductor World, Monthly, August 1987, p. 90-96

[54] M. Tanaka, M. Sakimoto, H. Konishi, K. Nishi, K. Ohtsuka, and T. Yoshida: "Investigation of Surface Mount Package Reflow Heat Tolerance Evaluation Methods," Japan Science Technology Association 18th Symposium on Reliability, Integrity Proc., p. 165-172, 1988

[55] K. Nishi, I. Anjo, M. Ogata, M. Kitano, and T. Yoshida: "Surface Mount Package Reflow Crack Mechanism Analysis and Countermeasures," Japan Science Technology association 18th Symposium on Reliability, Integrity Proc., p. 173-178, 1988

[56] K. Kitano, A. Nishimura, S. Kawai, and K. Nishi: "Analysis of Package Cracking During Reflow Soldering Process," Proc. 1988 IEEE IRPS, p. 90-95

[57] Y. Orii, O. Suzuki, A. Nakanishi, K. Takahashi, R. Kimoto, T. Nishita, M. Tanaka, and M. Sakimoto: "An Advanced Evaluation Method of Soldering Heat Resistance for Ultra Thin Plastic Encapsulated LSIs," 1991 ISTFA, p. 213-220

[58] M. Tanaka, M. Sakimoto, H. Ishida, Y. Orii, and T. Nishita: "An Advanced Evaluation Technique of Resistance To Soldering Heat for Ultra Thin Surface Mount LSIs," JUSE 22th Reliability and Maintainability Symposium, p. 155-160, 1992

[59] M. Tanaka, M. Sakimoto, Y. Nishi, and K. Otsuka: "Surface Mounted LSI Soldering/Heat Resistance Evaluation Methods Established," Nikkei Electronics No.516, p. 143-165, 1990

[60] M. Tanaka, M. Sakimoto, S. Okikawa, T. Yoshida, M. Mutoh, Y. Oki, and Y. Orii: "A Novel Method of Evaluating Moisture Resistance of Soldered Plastic Encapsulated LSI by a New Ultrasonic Inspection System," Proc. of ISTFA, p. 173-177, 1986

[61] T. Nonaka and S. Okigawa: "Development of Ultrasonic Inspection Images," Technical Report (Reliability) by the Society of Electronic Data Communications, R86-68, p. 31-36, 1987

[62] M. J. Middendorf, T. Hausken: "Observed Physical Effects and Failure Analysis of EOS/ESD on MOS Devices," 1984 ISTFA Proc., p. 205-213

[63] D. C. Wunsch: "The Application of Electrical Overstress Models to Gate Protective Networks," IEEE 16th Annual Proceedings Reliability Physics, April 1978, p. 47-55

[64] N. Murasaki: "Electronic System Electrostatic Damage Countermeasures Resource Collection, Revised Edition," Dai Ichi International Corp., 1982

[65] "Report on Investigation Results for Semiconductor Device Electrostatic Destruction Phenomenon and Its Evaluation Methods," Japan Electronic Part Reliability Center, 1985

[66] D. C. Wunsch and R. R. Bell: "Determination of Threshold Failure Levels of Semiconductor Diodes and Transistors due to Pulse Voltages," IEEE Trans., Nuclear Science Vol. NS-15 No.6 Dec 1968, p. 244-259

[67] P. R. Bossard, R. G. Chemelli, B. and A. Unger: "ESD Damage From Triboelectrically Charged IC Pins," 1980 EOS/ESD Symposium Proc., p. 17-22

[68] B. A. Unger: "Electrostatic Discharge of Semiconductor Devices," IEEE 19th Annual Proceedings Reliability Physics, p. 193-199 1981

[69] M. Tanaka, H. Konishi and K. Ando: "A New Electrostatic Discharge Test Method for Charged Device Model," 1989 ISTFA Proc., p. 177-182

[70] M. Tanaka, M. Sakimoto, I. Nishimae, and K. Ando: "An Advanced ESD Test Method for Charged Device Model," EOS/ESD Symposium 1992, p. 76-87

[71] M. Tanaka, K. Okada, and M. Sakimoto: "Clarification of Ultra-high-speed Electrostatic Discharge & Unification of Discharge Model," EOS/ESD Symposium 1994, p. 170-181

[72] M. Tanaka, K. Okada, and M. Sakimoto: "Phenomenon of ESD Failure with Displacement Current," 3rd RCJ EOS/ESD Symposium, p. 21-28, 1993

[73] M. Tanaka: "Consideration of Correlativity between Device Electrostatic Breakdown Tests and Practical Electrostatic Phenomenon," 7th RCJ EOS/ESD Symposium, p. 163-170, 1997

[74] Y. Fukuda and N. Otsuki: "Electrostatic Charged on IC Package Damages IC," Nikkei Electronics, 1984. 4.23

Section 5 Failure Analysis

5.1 Why Failure Analysis Is Necessary?

Failure analysis of semiconductor devices is necessary to clarify the cause of failure and provides rapid feedback of this information to the design and manufacturing process stages. With the demand for higher reliability in the market and the development of devices with higher integration density and larger chip sizes, advanced technologies are required for failure analysis.

It is clear that reliability must be built into the device at the design and manufacturing process stages to ensure reliability. However, it is impossible to eradicate failures during the manufacturing process and at field use. Therefore, failure analysis must be performed to provide timely information to prevent the recurrence of similar failures.

The wafer fabrication and assembly process involves more than 100 steps using various types of materials. This, combined with the fact that devices are used in a variety of environments, requires a wide range of knowledge about the design and manufacturing processes.

5.2 What Is Failure Analysis?

The failure analysis begins when a device under observation is determined to have lost its basic functions according to the failure criteria. Failures include complete loss of functions and various levels of degradation. As the electronic equipment becoming more sophisticated, failures are not limited to individual components but also complicated failures with respect to an entire system. Failure analysis without considering these factors could result in erroneous corrective actions.

Failure analysis is an investigation of failure mode and mechanism using optical, electrical, physical, and chemical analysis techniques. Before starting the analysis, it is necessary to collect details of the failure circumstances and symptoms. This includes investigation of variations in electrical characteristics and other historical data leading to the failure, operating environment, stress conditions, mounting, and possibility of human errors. These factors may suggest the potential failure mode and mechanism. Based on this assumption, the most appropriate method and procedure are determined. Insufficient information on the failure circumstances and symptoms may lead to an unsuitable choice of analysis technique, consequently waste of valuable material and time. Comparing failure devices with good devices is another technique that can speed up the analysis process.

As mentioned, the analysis depends on many factors of the failure. Figure 5.1 is the flowchart of failure analysis procedure. A failure device first undergoes a visual inspection of the package. Electrical characteristics are checked to analyze electrical and functional failure modes. If the failure can be verified, the package is opened and the chip is analyzed according to the failure mode. Optical microscopes and scanning electron microscopes (SEMs) are used to observe the failed point (physical analysis). Finally the failure mechanism is determined and corrective actions defined.

5.3 Procedure of Failure Analysis

The following sections describe the details of the failure analysis procedure (figure 5.1).

5.3.1 Investigation of Failure Circumstances

The circumstances of the failure must be investigated by checking the following items:

1. Lot verification (production date, inventory period, and storage conditions)
2. Location and time of discovery of failure (process, line, or field use, and date of discovery)
3. Production records (process conditions in wafer fabrication and assembly process, delivery date, conditions and results of acceptance inspection, conditions through mounting and/or assembly, and records of similar failures occurred so far)
4. Conditions of use (operating conditions, thermal/mechanical stress, operating environment (indoors/outdoors, temperature, humidity, atmosphere), operating period before failure occurred)
5. Details of failure (type of failure (degradation of characteristics, complete, intermittent), failure rate, and lot characteristics)

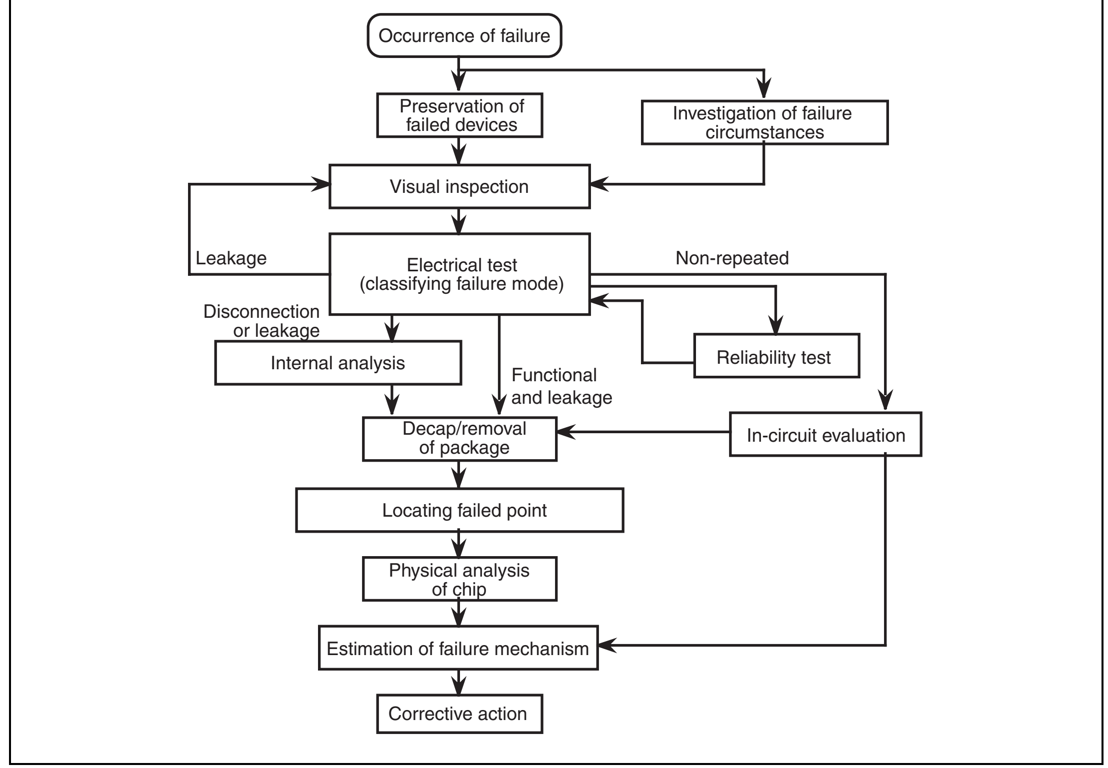

Figure 5.1 General Failure Analysis Procedure

5.3.2 Preservation of Failed Devices

For failures resulting from mechanical damage or environmental corrosion, the original condition of the device must be maintained by taking photos. To avoid progress of failure, the sample should be handled and stored with great care so that the environmental (by temperature and humidity), electrical, and mechanical damages to the device are prevented. Mounting jigs and fixtures can be useful for handling small devices.

5.3.3 Visual Inspection

Visually inspecting the external condition of the device often provides valuable information for subsequent analysis. First the device is inspected by eyes to check for any differences from good ones. Then microscopic inspections are carried out for detailed observation. A stereomicroscope with magnifying power 4 to 80 is used. Illumination from various angles is used to obtain the best view of the sample. A regular microscope with higher magnification power (50 to 2,000) is sometimes used to search for failure spots. If further observation is required to detect package cracks, surface wear, particles, whiskers, discoloration, or migration, a scanning electron microscope (SEM) is used. If elemental analysis is required and a sufficient amount of sample is available, atomic absorption photometry is performed. If the failure is limited in a very small area and it is difficult to obtain the substance in question, electron probe micro analysis (EPMA) should be used.

The following items should be observed in visual inspection.

(1) Dust

The presence of metal, metal oxide, or ash indicates the device has been used in a severe environment such as at a steel mill or power plant. This can be one of the causes of characteristic deterioration.

(2) Contamination

Small remaining traces of water, oils, solder flux, or spray liquids (e.g. insulating materials) can cause poor connections or leakage.

(3) Lead Discoloration

The leadframes are usually plated to improve solderability and resistance to corrosion. Plating discoloration often indicates oxidation by heat, sulfurization, flaws in the base material, incomplete preprocessing, or defective plating.

(4) Lead Cracking by Stress Corrosion

If Cu-Zn alloy and many other copper-based alloys under external stress or internal residual stress are exposed to ammonia, amines, moist air, and/or high temperature environment, stress corrosion can occur. It is diagnosed by observing the morphology of the cracks and feature of the grain boundary using an SEM.

(5) Mechanical Lead Damage

This damage mode depends on the external form of the lead, load, and the environment. Major breaking types are fatigue breakage, shock breakage, and creep breakage. The fatigue breakage is caused by repeated stress and the creep breakage by stress applied over a long period of time. Other breakage includes brittle fractures and elongation breaks. The brittle fractures involve rapid formation of a break without plastic deformation. The elongation breaks develop gradually following plastic deformation. It is important to carefully examine how the breakage occurred to determine the type of breakage. The cracked surface or the surface of broken ends sometimes exhibits a wave pattern, which indicates mechanical fatigue. A disk or ratchet-shaped pattern implies a stress concentration at this point.

(6) Package Cracking

Cracks are the cause of leakage of moisture into the device. Glass cracks in the hermetic seal are easy to overlook. Inspection using penetrant dyes is effective for small cracks.

(7) Metallic Migration

When an electric field is applied at high temperature and high humidity, metallic ions in the insulation material or at its surface migrate from the positive terminal to the negative, where they are reduced and deposited. This can ultimately lead to a short circuit between two terminals. A metallograph and electron probe micro analysis (EPMA) are used to observe this phenomenon.

(8) Whisker

In most cases, solder plating is applied to the lead pins. Accordingly, there is a possibility of tin whiskers being generated regardless of whether the solder is eutectic or Pb-free. The generation of whiskers from conventional eutectic solder plating can be suppressed by adding Pb. However, Pb-free solder plating must be monitored for whisker generation by using, for example, SEM.

5.3.4 Evaluation for Electrical Characteristics

(1) Evaluation using an LSI Tester

This test evaluates detailed electrical characteristics of the sample test equipment and sequence used in mass production and when necessary further test programs which have been created for design evaluation. The test results may suggest the failure mode, failure mechanism, and refine the estimation made from the failure circumstances. At the same time, the test enables the choice of onward analysis method, as shown in figure 5.1.

Detailed evaluation of electrical characteristics is very important. In the case of memory devices, these tests can locate an exact failure spot on the chip.

(2) DC Characteristics Test

This test evaluates the DC characteristics of the chip using a curve tracer, picoammeter, and oscilloscope. In an LSI, the current flow may not follow the equivalent circuit because of parasitic diodes that are not drawn in the equivalent circuit inside of the chip. For this reason, tests should be performed using non-defective devices as a comparison.

(3) Logic/Failure Simulation Analysis

When a function test performed by an LSI tester or by DC characteristics evaluation results in a fail, the data obtained in the function test is analyzed to locate the faulty module in the chip. The failure mode is then examined according to the voltage, temperature, frequency, and other test conditions. A procedure that makes use of the information obtained by the analysis and examination in a logical simulation or failure simulation environment to accurately determine the faulty logical function module is generally called failure diagnosis. The accuracy of locating the failure improves if it is assumed in the failure diagnosis that the location of the failure is in the order of 10 cells or 10 nets in the chip. There are four types of failure diagnosis methods: the failure dictionary method, which is used with a failure simulator, the tracing diagnosis method, the guided probe diagnosis method, and the IDDQ test diagnosis method[1] to [5]. The IDDQ test is a technique that makes a pass-fail judgment by measuring current values in a static operating state by applying the fact that a perfect CMOS structure has no DC path on the source lines. IEEE has defined it as a quiescent power supply current in MOS circuits. This test method is a historical test method developed after the invention of CMOS.

Figure 5.2 shows a failure analysis flow based on failure diagnosis. The failure diagnosis flow roughly divides into function test failure steps and current system (DC/IDDQ) test failure steps. For a function test failure, a failure analysis is performed with a failure simulation, and the failure is located by EB testing, LVP, TRE and other types of operation analysis. For a current system test failure, light-emission analysis, OBIRCH analysis, and other static analyses are performed (for these measures for locating failures, see section 5.3.6, Locating a Failure Point in Chip).

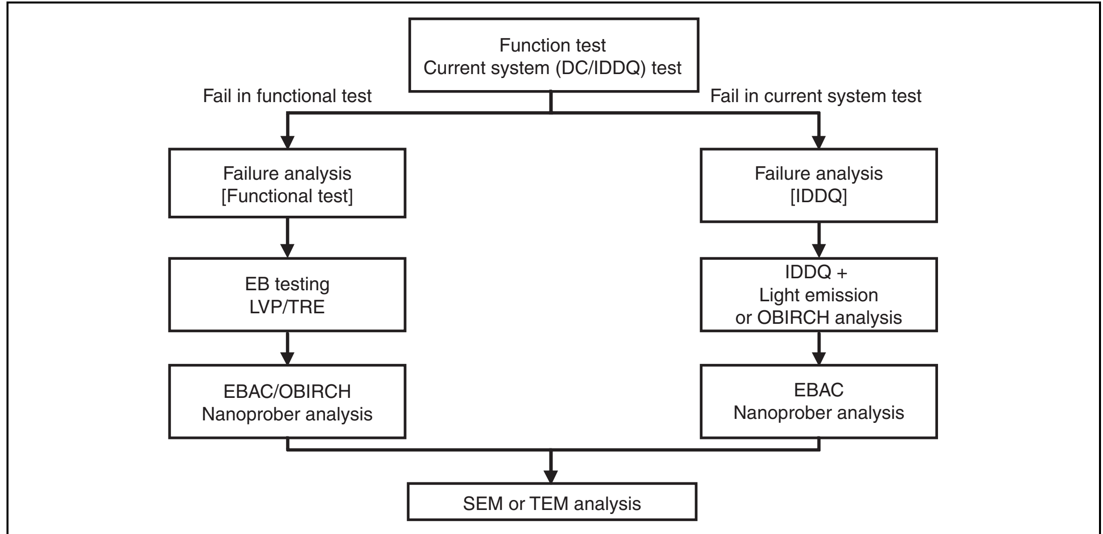

Figure 5.2 Analysis Flow with Failure Diagnosis

Figures 5.3 and 5.4 provide overviews of the failure diagnoses that we are using for function test failures and current system testing (IDDQ test failures). Function test failures require such procedures as logical analysis and failure dictionary creation for each failure condition, so analysis takes a long time. However, for faulty products that were made by other manufacturers and for malfunctions in systems already on the market, the method is effective as well as required for reproducing the operations of a customer's system to locate a failure. IDDQ test failures can be diagnosed quickly because a failure dictionary for failure diagnosis has been created. In addition, no logical and functional analysis is required. IDDQ test failures are also appropriate for hardware analysis machines and have the advantage that a failure can be located in less time than a function test failure.

Process A
Tester fail log
Tester test vector
Function test fail log analysis
Possibly failed modules
Verilog Netlist
Failure simulation
Failure dictionary
Process B
Process C
Indication list creation
10 indications or less
End
Indication list
More than 10 indications

<<Process A: Narrowing down of number of possibly failed modules>>

Narrow down the number of possibly failed modules for which a failure dictionary is to be created based on the function test failure information. The faulty module can be roughly determined by the test vector type of the test that resulted in a fail. For an MCU or MPU, instruction codes are extracted from test vectors and disassembled, and then the operation sequence is analyzed to improve the accuracy of assumptions.

<<Process B: Creation of failure dictionary>>

Process B is run more than one time. The first iteration roughly narrows down the range by creating a failure dictionary that covers tens of steps up to the first fail step by using information about modules likely to be faulty from Process A as input. In the second and later iterations, the creation of failure assumptions for the logic narrowed down in the first iteration reduces the number of failure assumptions required to create a failure dictionary with coverage up to the final fail step. The reduction is accomplished by using the test vectors employed in the first iteration or the test vectors from other tests resulting in a fail.

<<Process C: Creation of failure candidate list>>

A list of logic for failure candidates is created from the failure dictionary. Since the first failure candidate list is based on the failure dictionary with coverage up to the first fail step, there are usually hundreds of candidates. Feeding the first failure candidates into the second and later creations of the failure dictionary as input reduces the number of failure assumptions by a factor at least 10. When the number of failure candidates has dropped to 10 or less after the n-th iteration, the narrowing-down sequence ends.

Figure 5.3 Function Test Failure Diagnosis Flow

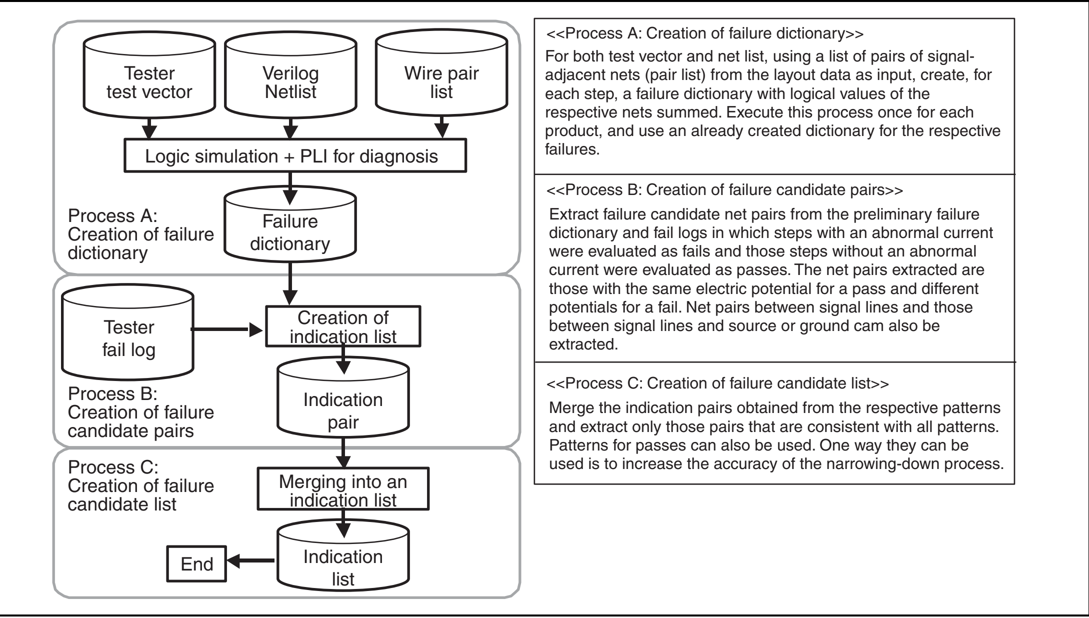

Figure 5.4 Current System Test Failure Diagnosis Flow

(4) Experiment for Failure Reproduction Using Actual Equipment

If a product is evaluated as a pass in the tests described above, an experiment must be conducted with actual equipment to reproduce the failure. It is possible that the failure cannot be reproduced because the circumstances of the failure cannot be adequately simulated in the tests. It is also possible that the failure occurred due to a problem related to use of the device (for example, a malfunction due to a circuit constant or noise). For some types of failure, an experiment with actual equipment might cause secondary damage, so care must be taken.

5.3.5 Internal Analysis of a Package

(1) Nondestructive Internal Analysis

Techniques used to check the internal state of a device without opening or removing the package include X-ray examination, infrared microscopy, and scanning acoustic microscopy.

X-ray examination uses the fact that X-ray penetration varies according to the type of material and thickness (i.e., the smaller the atomic weight, the greater the penetration). The differences create an X-ray image. This method is effective for detecting particles, breakage or looping of bonding wires, and voids or peeling in mold resins or the die bonding section inside the plastic sealed package (figure 5.5).

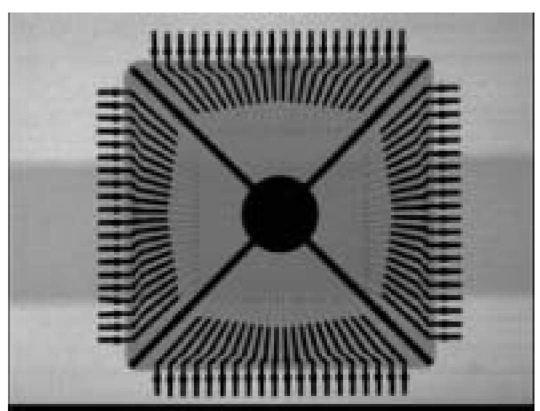

Figure 5.5 X-ray Image of the Inside of a Plastic Sealed Package

Infrared light passes through silicon but is reflected by metals and mold resins. When inspecting plastic sealed packages, the chip is sometimes exposed by removing the plastic with a solvent. However, the solvent also removes foreign particles and wiring, which makes failure detection difficult. In the infrared microscopy, a part of the package is removed by grinding the bottom to expose the silicon chip. The infrared examination of the chip shows the state of the metal wiring and any abnormalities in the bonding pads.[6]

An ultrasonic wave divides into reflected wave and penetrating wave at a boundary between different materials. The reflected wave has different intensity and phase according to the difference of acoustic impedance of the two materials (if the acoustic impedance of the first material is higher than the second, the phase inverts). This test emits ultrasonic waves to the plastic sealed device submerged in water. There are reflected waves from the package surface, chip surface, and lead surfaces. If there is a layer of air at the boundary, the intensity and phase of the reflected wave greatly differs. This test shows the location and conditions of any voids, peeling, and cracks inside the package (figure 5.6).[7]

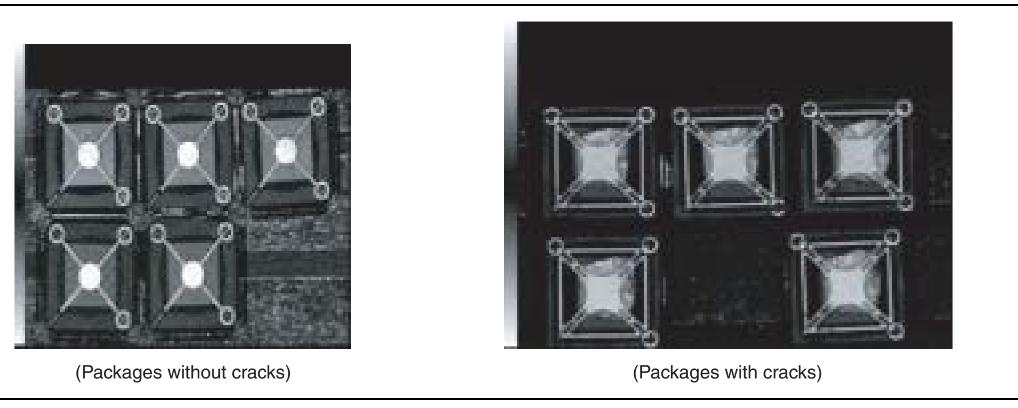

Figure 5.6 Observation of Package Cracks by Scanning Acoustic Microscope

(2) Analysis of Residual Gas

If contamination of the chip surface is suspected to be the cause of failure in metal or ceramic packages, the gas inside the casing should be investigated by opening a hole in the lid.

(3) Airtightness Test

Metal or ceramic packages are sealed with dry air or nitrogen gas enclosed to shut out the external atmosphere. Since the presence of water facilitates the movement of impurity ions and can cause degradation of device characteristics as well as corrosion of aluminum leads, the amount of water in the atmosphere inside the package is kept under several hundred ppm and gas leakage from the package is minimized. There are two airtightness test methods: helium tracer method to measure fine leaks and the fluorocarbons method to measure gross leaks.

For measuring fine leaks ranging from 10^{-8} to 10^{-9} atm • ml/s, a helium tracer leakage detector is used. It can measure leakage less than 10^{-9} atm • ml/s.

For measuring relatively large leaks from 10^{-3} to 10^{-5} atm • ml/s, a fluorocarbons leakage detector is employed. A depressurization/pressurization container is required for leaks under 10^{-5} atm • ml/s.

These techniques can detect small cracks in the package, voids in welding or solder materials, pinholes in the welding flange section, and faults in the hermetic seal.

5.3.6 Locating Failure Points In A Chip

(1) Overview

In failure analysis of a chip, the point of the failure is located using fault isolation techniques. Then physical analyses, including structural analysis and composition analysis, are carried out to determine the cause of the failure.

Fault isolation uses electron beam testing, LASER Voltage Probing (LVP), emission/thermal analysis, Optical Beam Induced Current (OBIC), and Optical Beam Induced Resistance Change (OBIRCH) techniques. These techniques involve emission of an electron beam onto the chip surface and detection of the light emitted from the chip surface. Therefore, the chip must be exposed without taking it out of the package. This requires some preprocessing such as disassembly of the package and removal of the chip coating.

A different fault isolation technique is used for each type of failure. Electron beam testing or LVP is used for a functional failure in which the logic generates an erroneous output. Emission analysis or OBIRCH is employed for a leakage failure with an increased power current. Recently, the nanoprobe method, which directly measures electrical characteristics of minute circuits, and other methods have made it possible to locate a failure with more precision after narrowing down the failure location with the techniques already mentioned.

(2) Opening of The Package

(a) Metal packages

The top edge of a package is ground off using a motor grinder or filed off to the desired thickness so that the package can be cut with a metal scissor. After a small hole is opened at the top, the tip of the metal scissors is inserted and the top cut off. Care must be taken not to drop any metallic shavings into the package and not to damage the inner leads and silicon die.

(b) Ceramic packages

Since it is extremely difficult to dissolve ceramic with chemicals, mechanical methods must be used. An easy-break ceramic joint and glass seal, which is made with low-melting-point glass, can be broken with pliers, but care must be taken not to allow fragments to get into the device.

(c) Plastic packages

There are two methods: dissolving with solvents and plasma etching. Fuming nitric acid is normally used to dissolve an epoxy resin plastic package, but recently fuming sulfuric acid has also been used. Since these methods generate toxic vapors, an exhaust system must be used and the waste solvent should be disposed of appropriately. After drilling a hole using a commercially available package opener or a drill, drip in the fuming nitric acid to open up only the chip area. When this is done, care must be taken not to electrically damage the device. Plasma can also be used to open a package and has the advantage that the chip surfaces are better preserved than when the dissolving method is used. However, etching takes considerable time.

(3) Removal of the Chip Coating Film

Plastics are broadly classified into silicone and polyimide resins. Uresolve Plus (trade name) is used for removing silicone resins and PIQ Etchant (trade name) is used for polyimides. A polyimide resin can also be dissolved with fuming nitric acid that is generally used to open the plastic package. For plastic molded packages, therefore, resins are almost totally removed when the package is dissolved.

(4) Fault Isolation

(a) Mechanical probing

This method uses a thin metal needle to measure the voltages of internal wiring. Although an old technique, it is the only way to detect absolute voltages inside the chip. This method requires exposure of the chip. Plasma etching is normally used to remove the passivation coating. Use of reactive ion etching (RIE) enables removal of the dielectric film between layers, without removing the upper wiring, so that the lower wiring voltages can also be measured.[8] However, removal of the dielectric film reduces the capacitance between wires, which can prevent reproduction of the failure and failure analysis. If possible, form a tungsten pad that provides a connection to the lower layer wiring on the chip surface and detect the voltage through the pad by contacting a needle. This method uses a focused ion beam (FIB), which can perform local etching of the dielectric film and deposition of tungsten film in a small area.[9]

(b) Nanoprober analysis

The nanoprober uses submicron probe needles to connect to an electrode, wire, or contact from which a passivation film has been removed, and thereby enables evaluating the electrical characteristics of single devices (figure 5.7). This technology can narrow down the location of a failure to the TEM observation level and facilitates a physical search for the cause of the failure. Moreover, because it allows the electrical characteristics of a failure location to be evaluated directly, it provides important guidance for the analysis of the failure mechanism from the cause of the physical failure up to the occurrence of the failure symptoms. The nanoprober can detect failures in both the development and mass production stages, and has a high degree of certainty in the analysis of customer failures. Table 5.1 shows the major nanoprober specifications.

This technology is a unique Renesas technology developed and implemented in collaboration with Hitachi Central Research Laboratory, and has been marketed by Hitachi High-Technologies Corporation since November 2004. Because the prober has an SEM for observing the probe tips and the surface under test, the prober unit is placed in a vacuum chamber, and replacement rooms are provided for quick replacement of the device under test and the probe. The prober also includes a CAD navigation system that allows the point of evaluation to be determined on an SEM image (figure 5.8). Figure 5.9 shows an analysis example. For SRAM, since one bit consists of six MOS-transistors, TEM observation cannot be used even if a faulty bit is located. In the example provided, a failure in a contact (C) was identified from a faulty bit and the characteristics of the MOS-transistors around it. Because of the failure identification, TEM analysis of the faulty contact could be used, and appropriate measures could be taken for the process.[10] to [13]

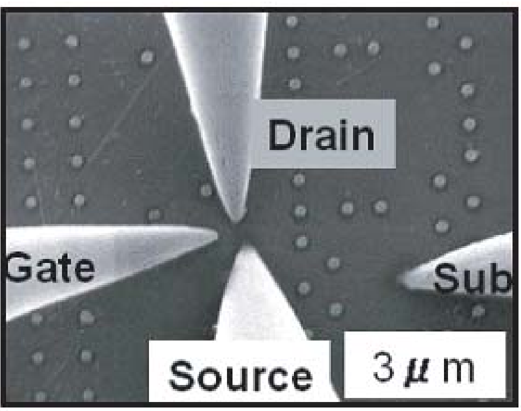

Figure 5.7 SEM Image of a Nanoprober in Use

Table 5.1 Major Nanoprober Specifications

Evaluation target	Any chip from 65 nm
Number of probes	6 maximum
Lower limit of current detection	< 10^{-14}A

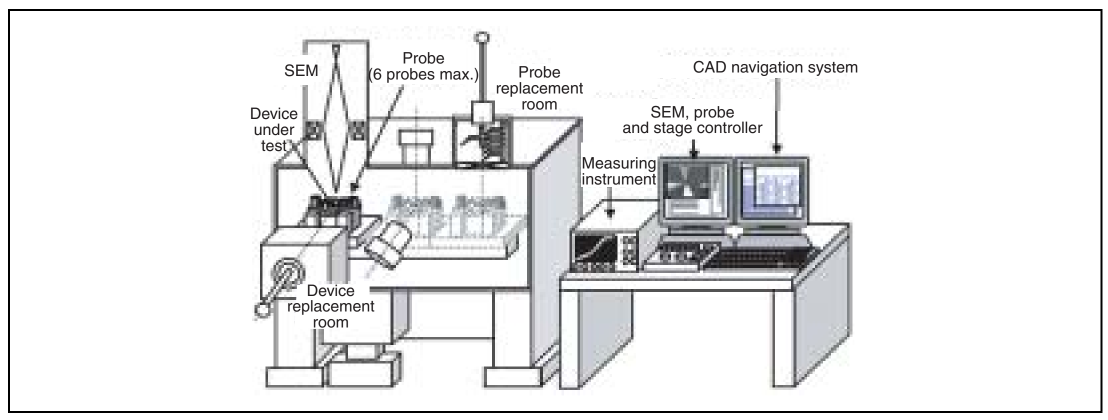

Figure 5.8 Nanoprober System

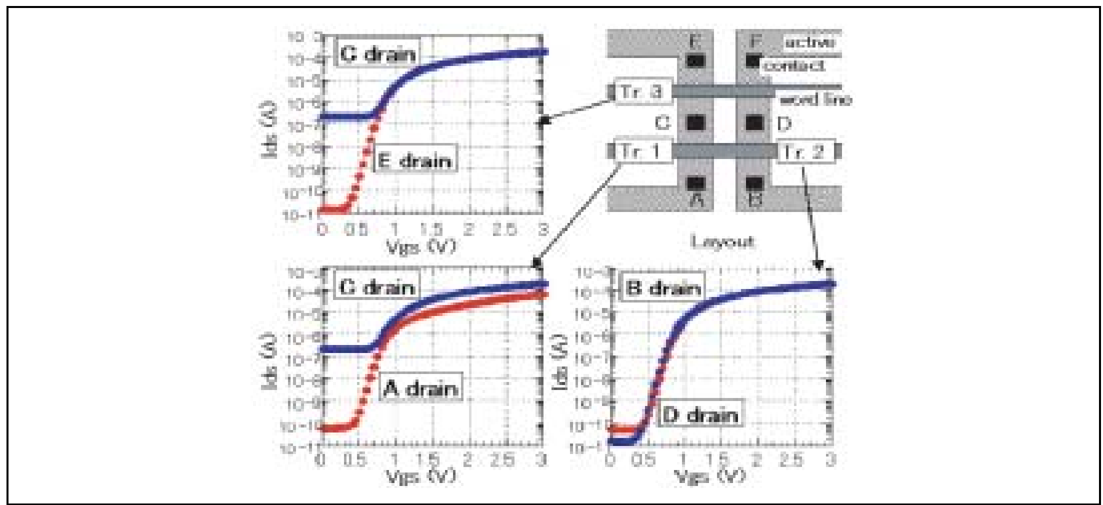

Figure 5.9 Example of Measurements Using a Nanoprober

(c) Electron beam testing

This method emits a thin focused electron beam with a diameter of about 0.1 μm onto the chip surface while the device operated with an LSI tester or the like in order to measure the voltage distribution and waveform of the internal wiring (figure 5.10).[14] Since the method is contactless, it is easier to use than the conventional probing methods, and it allows measuring at high impedance (without load), which is especially suitable to measure waveform timings at high precision (frequency band: up to 7 GHz).

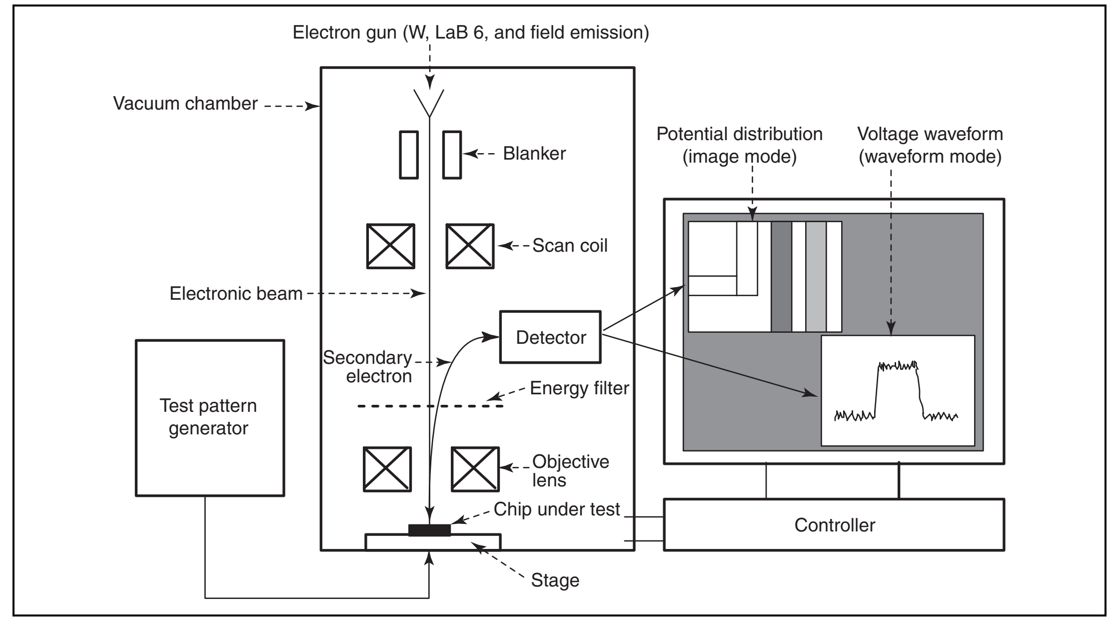

Figure 5.10 EB Tester Schematic Diagram

When an electron beam is emitted, wiring with a negative potential generates high-energy secondary electrons and wiring with a positive potential generates low-energy secondary electrons. An energy analysis reveals that the number of secondary electrons detected from the negative potential is greater than the number detected from the positive potential. The contrast in electrons indicates the voltage distribution shown in figure 5.11. To detect the information about the potential, electron beam pulses are emitted while the timing is shifted. Doing this allows the voltage (timing) waveform shown in figure 5.12 to be obtained according to the same principle that a sampling oscilloscope uses. Electron beam testing provides logical and timing information such as waveforms. This information must be compared with the expected values to find the failure spot. Several techniques, including comparison of potential distribution of defective and non-defective devices [15] and comparison of measured and logically simulated waveforms,[16] are used to trace the wiring (node) and locate the failure point. Recently, a CAD navigation tool (figure 5.13) linked with layout or net information has become indispensable for supporting large-scale logic devices, while lower layer wiring exposure and pad placement by FIB (focused ion beam) has become indispensable for supporting devices with multilayer interconnections. In addition, with the development of chip bottom processing techniques such as mechanical polishing, laser, and FIB, approaches in which measurement is done from the bottom surface are being examined.[17], [18]

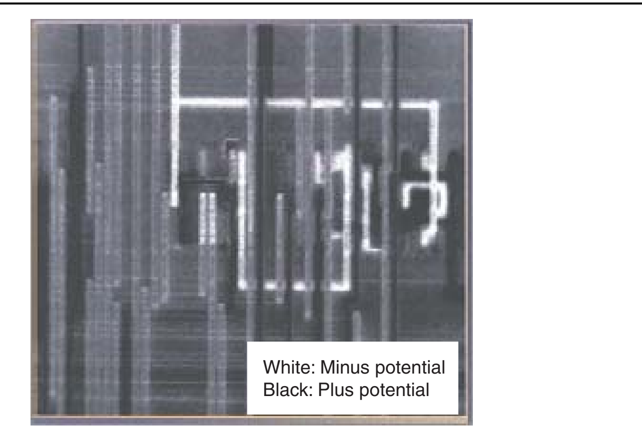

Figure 5.11 EBT Potential Distribution

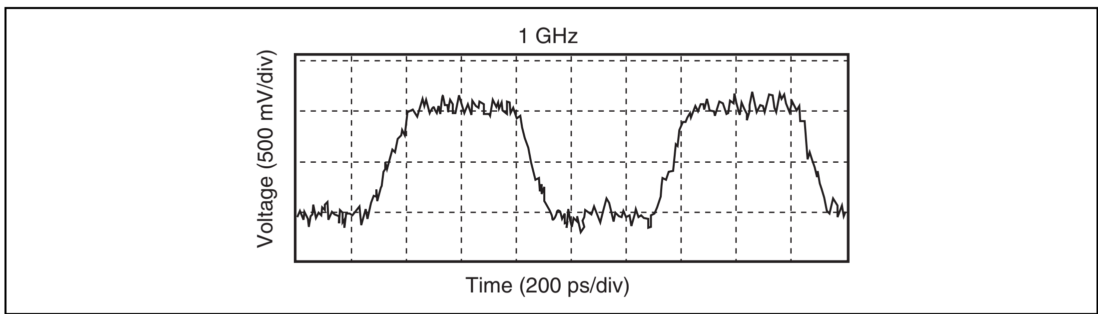

Figure 5.12 EBT Voltage Waveform

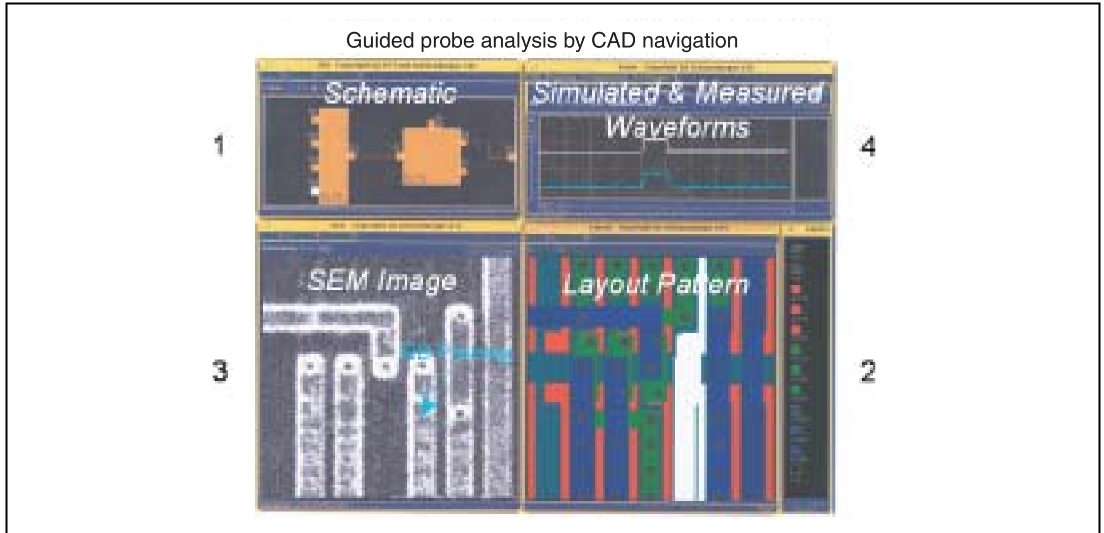

Figure 5.13 CAD Navigation Tool

(d) Laser voltage probing and time resolved light emission analysis

These methods optically measure potential waveforms and timings from the bottom surface of a flip-chip device or multilayer interconnection device whose waveforms are unobservable using electron beam testing (EBT). Like the EBT method, these methods make possible no-load, high-impedance measurement with an LSI tester or equivalent tool while the device is operating as well as, among other things, high accuracy measurements for waveform timings (frequency band: up to 9 GHz).

- Laser voltage probing (LVP):

  After the bottom surface of a chip has been mirror-polished to about 100-µm thickness, the LVP measurement method is used to penetrate pulsed near-infrared laser beams of 0.5-0.7 µm in diameter (1064-nm wavelength) from the bottom surface of the Si substrate into the operating transistor diffused layer (drain) and to detect the light that is reflected (figure 5.14). When an electric field is applied to a pn-junction, the bandgap degrades and the incident laser absorption increases, after which the reflected light intensity decreases (Franz-Keldysh effect). Moreover, a phase difference occurs in the reflected light due to a change in carrier density from the potential difference of the pn-junction. Detecting changes of phase difference and reflected light intensity by the Franz-Keldysh effect for the temporal axis makes possible contactless measurements of potential waveforms in the transistor diffused layer inside the chip.[19], [20] Laser scanned images are used for pattern observation and probing (figure 5.15), but like EBT, LVP allows information about waveforms and logic and timing to be obtained (figure 5.16). Therefore, comparison with expected values is required to locate a failure. A CAD navigation tool linked with the layout and net information needs to be used to trace the transistor and narrow down the range of possible failures.

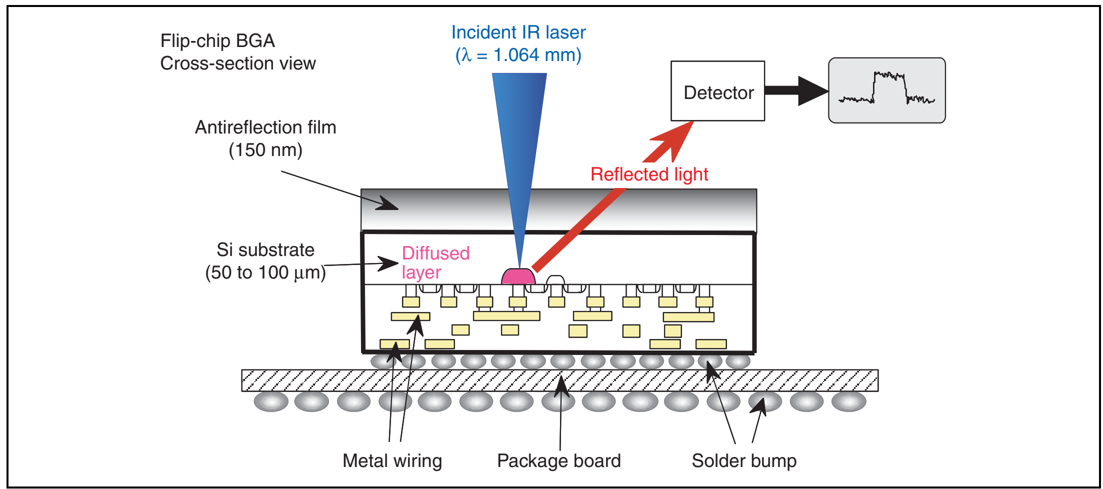

Figure 5.14 LVP Principle

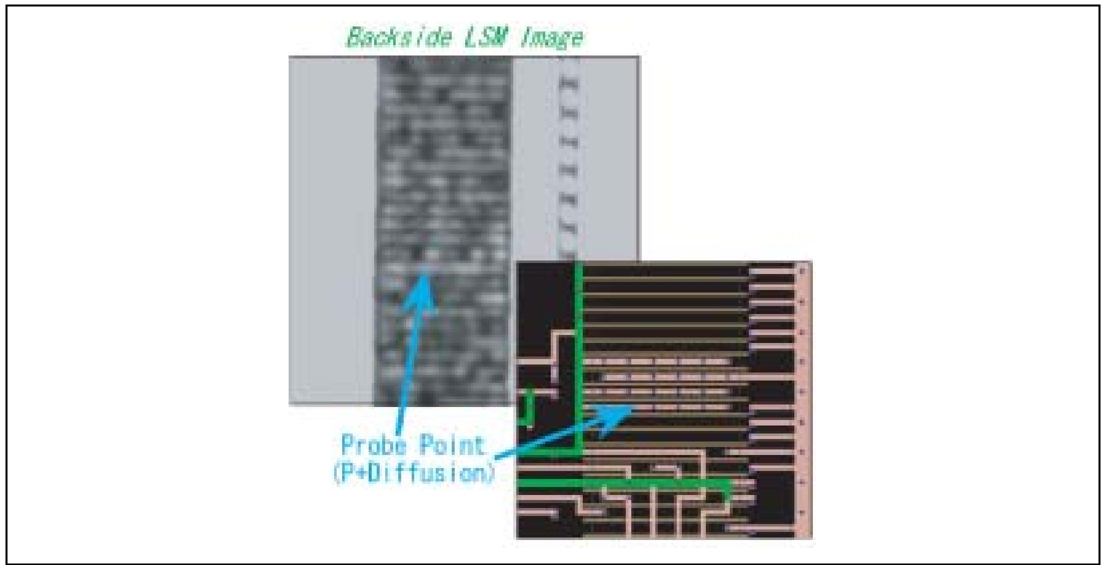

Figure 5.15 Laser Scanned Image/Layout

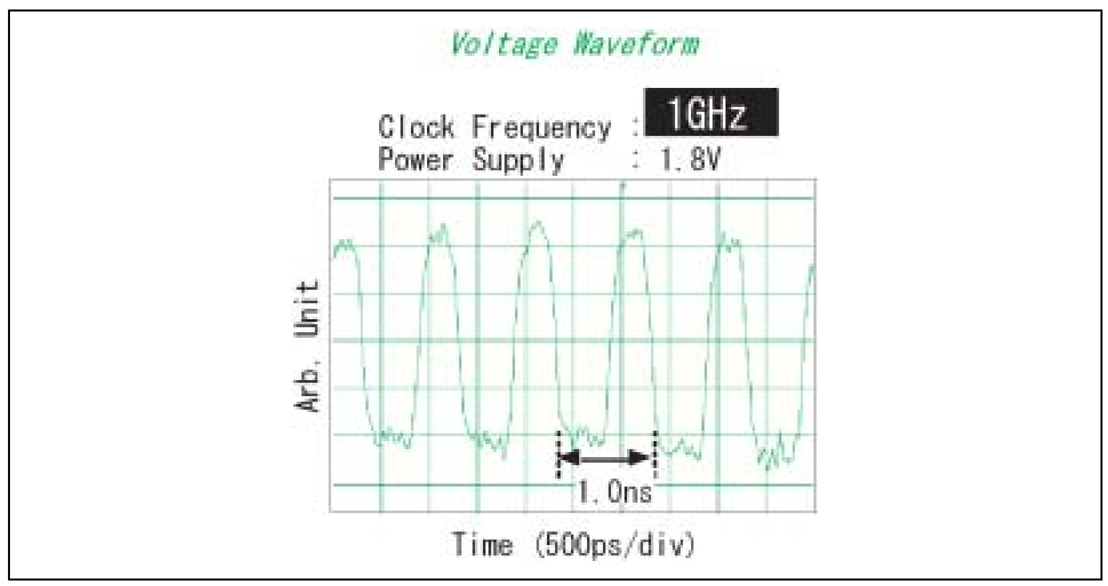

Figure 5.16 LVP Potential

- Time Resolved Light Emission (TRE) Analysis:

  After the bottom surface of a chip has been mirror-polished to about 100-μm thickness, the TRE method is used to capture subtle near-infrared emissions in the order of ps that occur at transistor switching (status transition) from the bottom of the Si substrate and to measure operational timing (figure 5.17).[21] An ultrasensitive time-resolved infrared camera with quantum efficiency of about 60% is used to capture photons that leak slightly from the bottom surface of the chip, while the condensation effect of a SIL (solid immersion lens, NA=2.45) is employed for greater sensitivity and spatial resolution (figure 5.18).[22] TRE allows data about emission intensity to be obtained for the temporal axis when switching occurs (and not data about signal waveforms that EBT and LVP provide). This data indicates the timing of transistor operation. Like EBT and LVP, TRE requires a comparison of values with the expected values to locate the failure. A CAD navigation tool linked with the layout and net information needs to be used to trace the transistor and narrow down the range of possible failures.

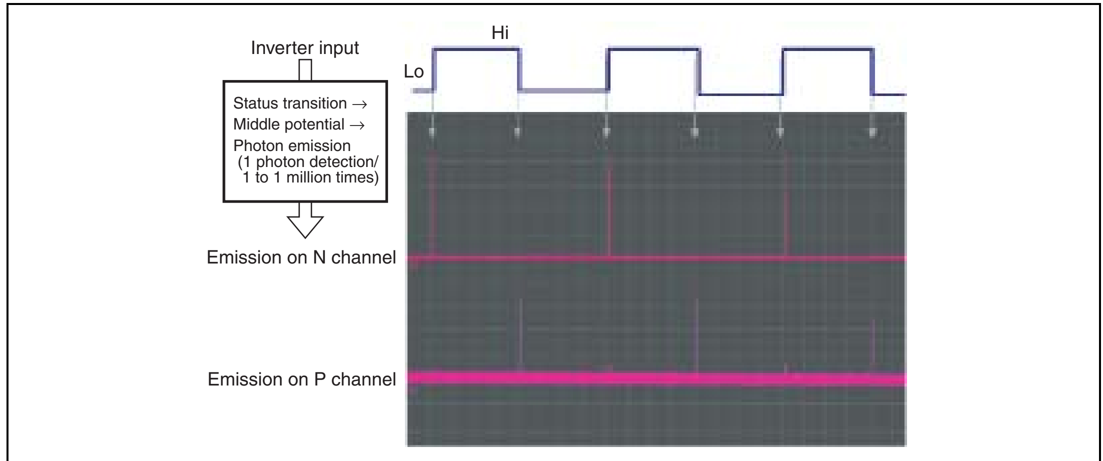

Figure 5.17 TRE Waveform for Nch/Pch Transistor

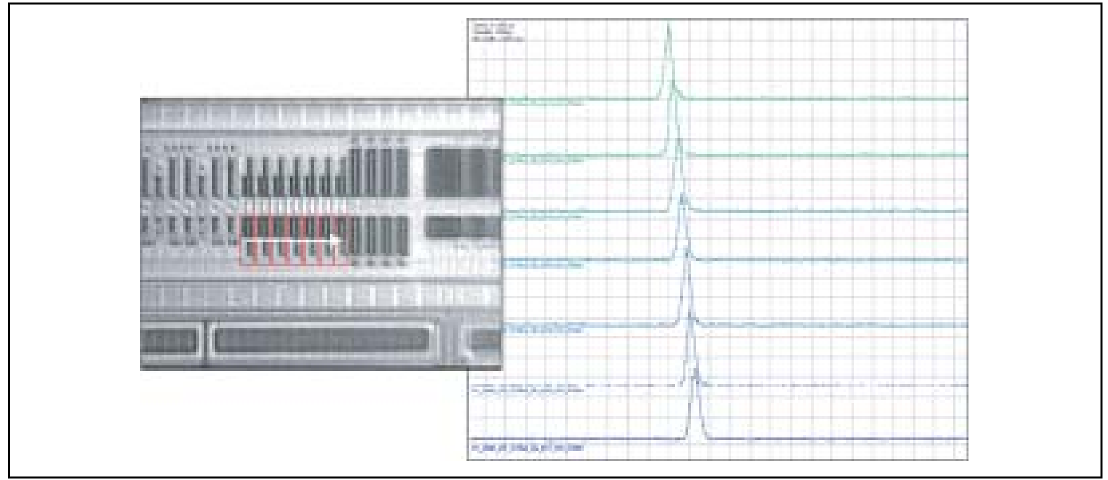

Figure 5.18 SIL-Employed Inverter Chain TRE Waveform Measurements

(e) Photo emission analysis

Light emission analysis is a technique that locates the point at which a failure has occurred by detecting the very feeble light emitted together with a current leakage and by capturing the location and intensity as two-dimensional images. After the light is detected with a high sensitivity detector capable of counting photons (photon counter), a light emission image and a pattern image (optically reflected image) are composed to locate the point on the chip emitting the light (figure 5.19). Luminous phenomena in Si caused by current leakage can take one of two forms: light emission by hot carrier generation in a high electric field caused by a transistor channel leakage or pn-junction leakage, and light emission by carrier recombination that occurs when a forward current flows in a pn-junction (similar to the CMOS latchup phenomenon). In the insulating film, it is known that light can be emitted as a result of microplasma generation in a high electric field, as, for example, in emission by gate dielectric film leakage and by a micro-short-circuit between metal wires or the like. These types of light emission cause white light that depends on the electric field at the point of leakage, and they usually have a broad spectrum distribution that extends from the visible range to the near-infrared range (the light emission by carrier recombination results in a wavelength distribution with a steep peak near the wavelength of 1 μm that corresponds to Eg of Si).[23] to [26] Since it has become difficult recently to detect light from the top surface due to the multi-layered metal wiring, detectors with high sensitivity to near-infrared light (with a wavelength of 1 micron or higher) that penetrates the Si substrate have been developed to detect light emitted from the bottom surface. These devices are now coming into wide use. Automated detection of emitted light at the wafer level makes wafer mapping of failures possible and has become an important measure for yield improvement analysis (figure 5.20).[27]

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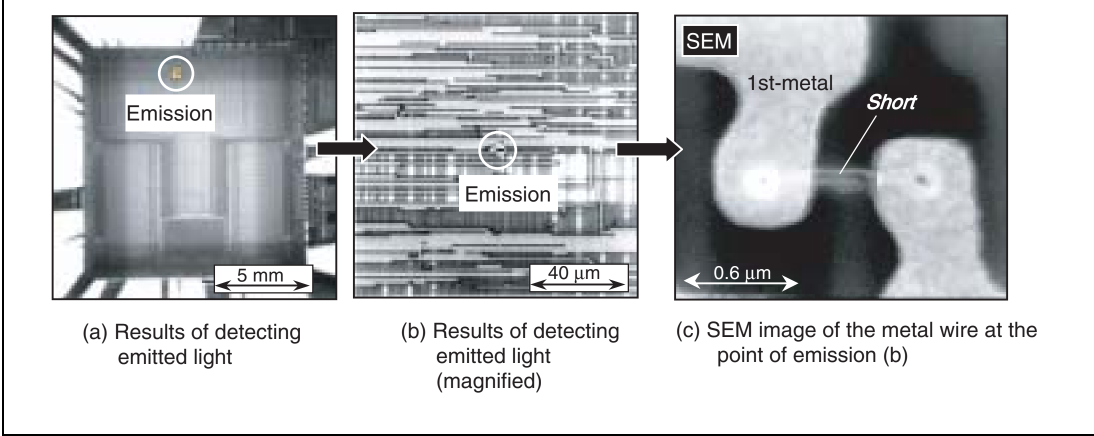
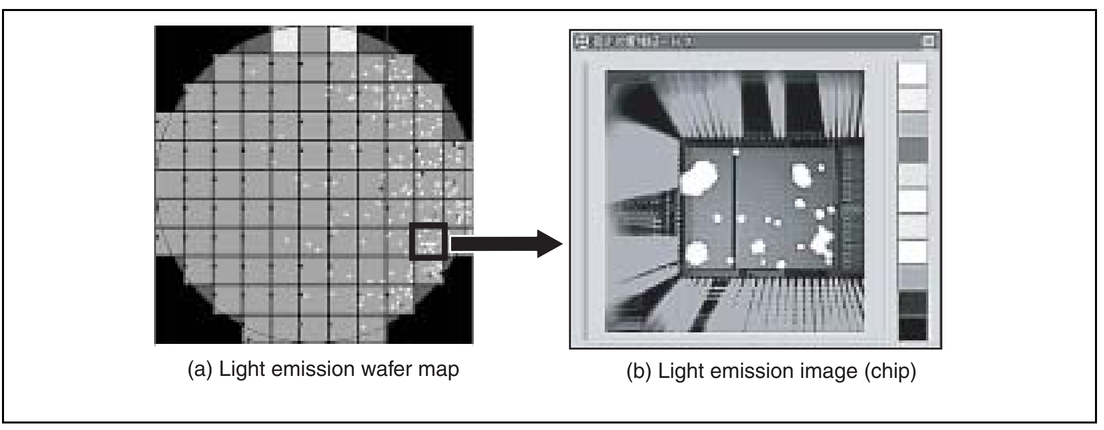


(a) Results of detecting emitted light

(b) Results of detecting emitted light (magnified)

(c) SEM image of the metal wire at the point of emission (b)

Figure 5.19 Examples of Light Emission Detection and Physical Analysis for a Leakage Failure



(a) Light emission wafer map

(b) Light emission image (chip)

Figure 5.20 Examples of Distribution of Light Emission Detected

Although light emission analysis has been used mainly for standby (leakage) power supply current failures, it is also a useful tool for locating functional failures when used together with device operation tests. The intra-chip logic state changes each time the test vector is updated in synchronization with the clock signal. The power-supply current Idd increases at the moment the internal logic state changes, but if the logic between switching operations is fixed, very little current flows (in a CMOS circuit). However, when the electric potential reaches the level where the failure point is activated, Idd increases. Therefore, if the current Iddq (quiescent power-supply current) is observed in a static state while the operation is in progress, the clock is stopped at the vector where the failure is observed, and the light emission is observed while the internal logic is retained, the point of failure can be located.[27] to [29] As techniques for locating logic device failures, a software-based diagnosis method providing the test results mentioned in 5.3.4 (3) and a method of inner electric potential waveform observation that uses electron beam testing (5.3.6 (4)(C)) are available. However, the light emission analysis method that employs Iddq is simple and has the advantages of placing no restrictions on multiple failures and of observability.

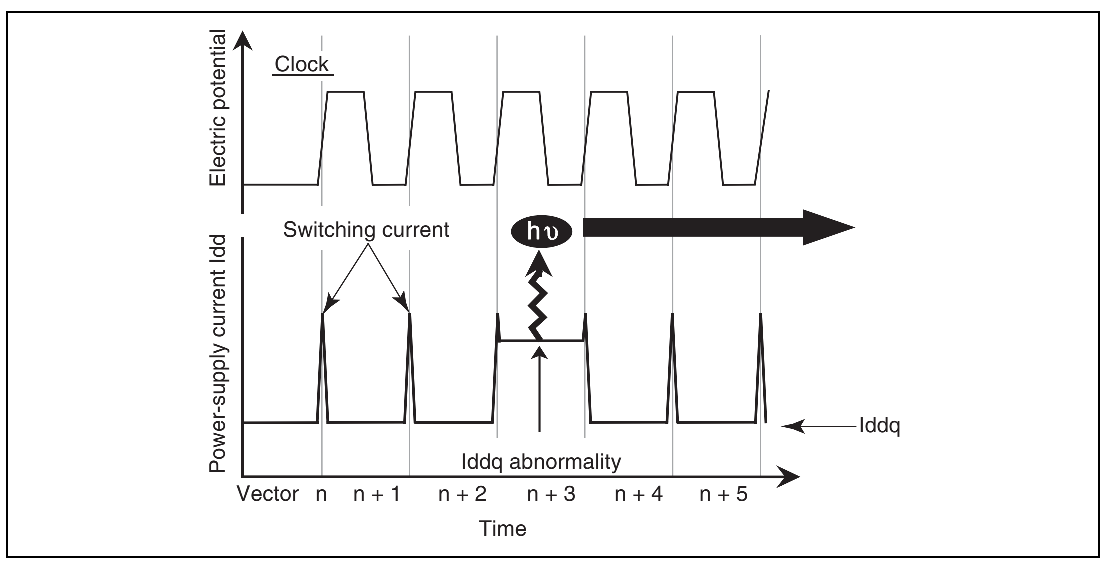


Figure 5.21 Extraction of Light Emission Observation Vector by Iddq Observation

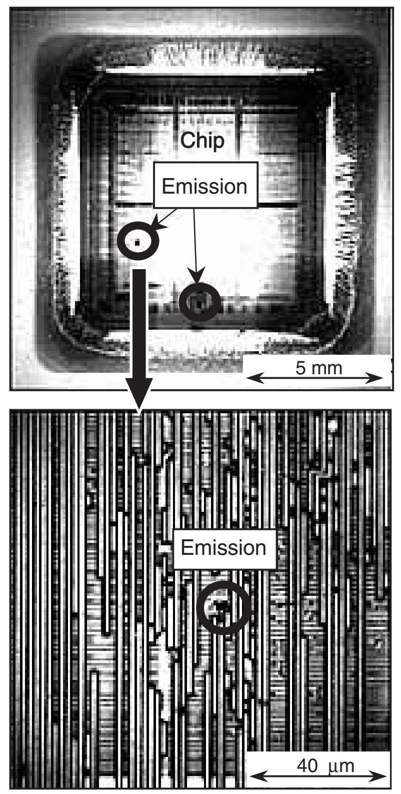


Figure 5.22 Example of Logic Failure Point Detected by Iddq + Light Emission Analysis

(f) Thermal analysis

This method locates the hot spot due to leakage current. It uses liquid crystal or an infrared microscope.

The liquid crystal changes its optical characteristics from birefringent to isotropic when a temperature reaches the phase transition temperature. This change can be observed using a polarizing microscope. After applying liquid crystal on the chip surface, power is applied to the chip. The heating area can be detected as a hot spot (black spot).[30], [31]

The infrared microscope locates the hot spot by detecting infrared light (wavelength of 3 to 5 μm) from the chip surface (figure 5.23). This method has been widely used for locating failures of printed circuit boards. However, with the improvement of special resolution and sensitivity, it is also used for detecting leakage on the chip and measuring temperature distribution of an aluminum wiring test element group (TEG).[32]

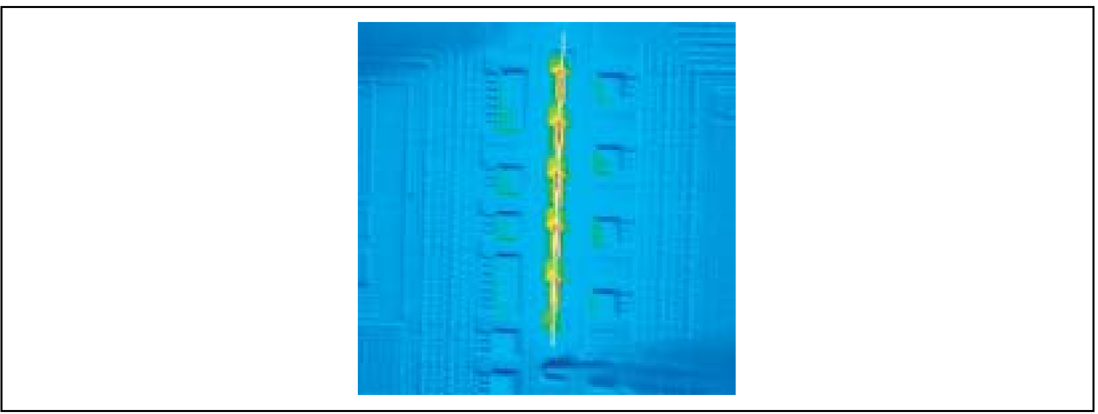


Figure 5.23 Observation of Temperature Distribution Using an Infrared Microscope

(g) Laser microscope analysis

Laser microscope analysis is a technique in which the device is irradiated by a laser and failures in the device are located by converting the resulting changes in current into images. The physical phenomena brought about by laser irradiation result from two effects, light excitation and heat, and the appropriate use of these makes it possible to detect different failure modes. A method that uses electromotive currents caused by light excitation is known as Optical Beam Induced Current (OBIC) analysis, and has been used to locate pn-junction leakage and gate oxide film leakage points based on the fact that electromotive currents are influenced by a crystal defect or electric field in the Si substrate (figure 5.24). OBIC analysis visualizes a failure point by capturing feeble changes of electromotive currents, and therefore, unlike light emission analysis, requires no electric field to be applied to the point of leakage. However, it cannot be used in operational states where the current from the power supply is varying and is subject to certain other restrictions, including a range of analysis limited to the vicinity of the Si substrate's surface. On the other hand, methods that use the thermal effects of laser irradiation have been established and have been widely used in recent years to locate metal wire failures and via hole failures (in high resistance points). The most popular method is the Optical Beam Induced Resistance Change (OBIRCH) analysis, which uses the fact that changes of electrical resistance due to heat generated by laser irradiation are different at failure points.[33] to [35] At high resistance points like a void, the steepness of the temperature rise due to laser irradiation is higher than at other points, resulting in a larger change (increase) in the electrical resistance. Capturing the change in electrical resistance as a change in an observation current and making a luminance conversion for synchronization with a beam scan makes it possible to image the failure point. This method requires an electric current to be applied to the point of failure, but since the wires on which the electric current flows are made visible, the method can be used to detect a leakage current path (faulty node) (figure 5.25).

Another method that has been used visualizes failure points by directly detecting very feeble electromotive currents generated by the thermoelectric effect from heat generated by laser irradiation.[36] to [38] These methods need to detect very feeble changes to the OBIC and therefore use a laser beam with a wavelength of about 1.3 microns, which is not influenced by an electromotive current. As described in the previous section on light emission analysis, the multi-layered metal wiring has made it difficult to make an inspection from the top surface. Accordingly, near-infrared light (with a wavelength of 1 μm or more) has been generally used from the bottom surface.[39] to [42]

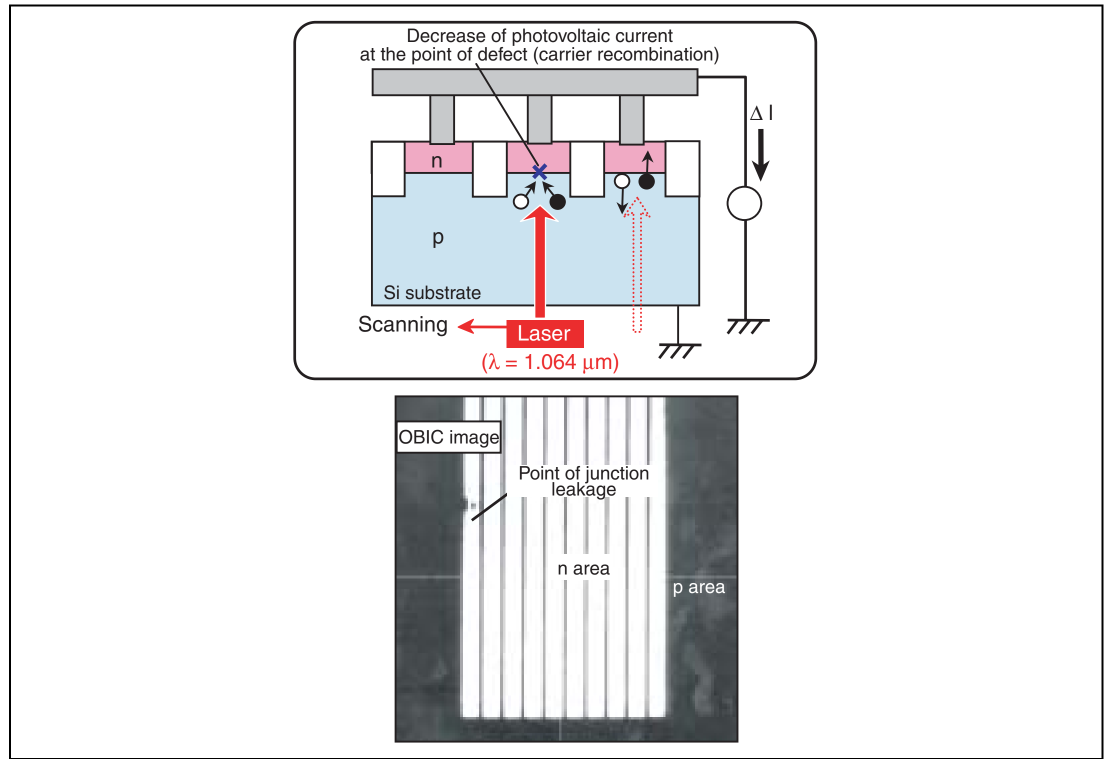


Figure 5.24 Example of Bottom Surface OBIC Analysis (pn-junction leakage)

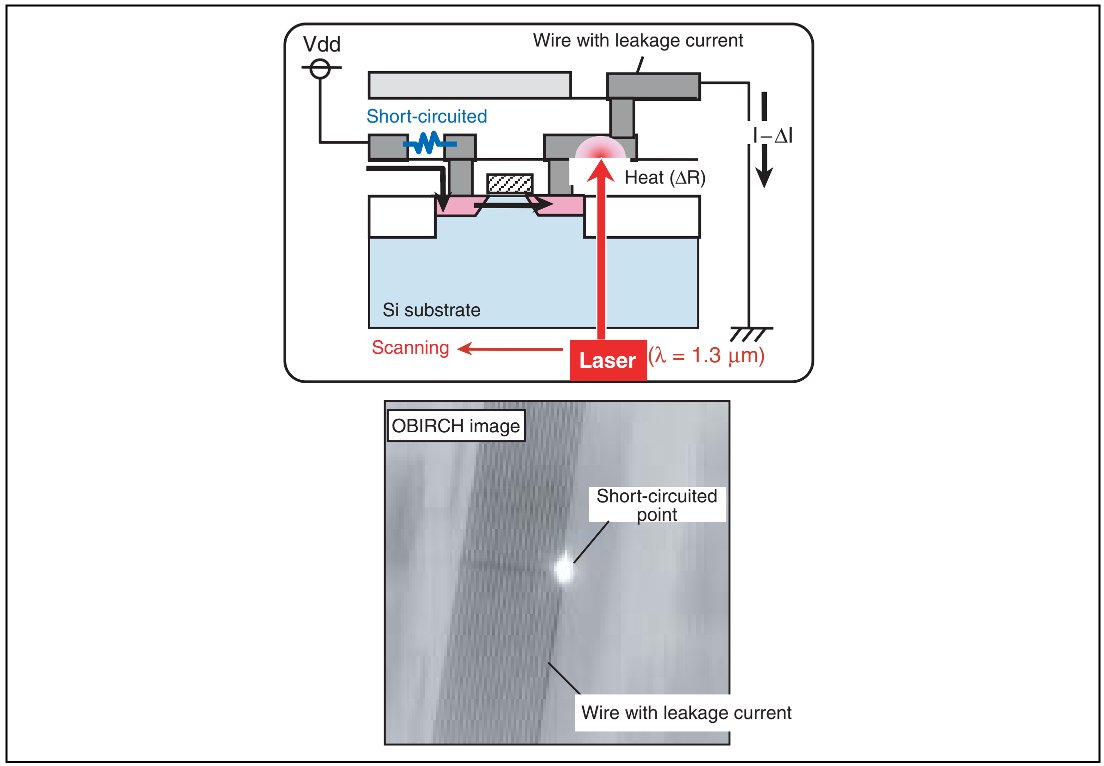


Figure 5.25 Example of Bottom Surface OBIRCH Analysis (leakage path detection)

5.3.7 Physical Analysis

(1) General

The physical analysis observes and analyzes the failed point by performing physical treatments on the chip. Its purpose is to clarify the cause of failure. It provides final information that is fed back to the design and manufacturing processes.

The physical abnormality, which is the cause of failure, sometimes exists between the surface and lower layers. In such a case, the dielectric film and metallic wiring must be removed. This procedure is performed while observing the spot using an optical microscope or SEM. It is sometimes necessary to observe the cross section of the chip with Focused Ion Beam (FIB). If any discoloration or particle is found at the failed location, composite analysis is carried out to clarify how it happened.

(2) Internal Structure Analysis

(a) Removing films

This procedure etches each film from the top. The difference between the etching ratios, the thickness of each film removed, and the etching speed must be carefully selected. The result is checked with an optical microscope or SEM. Table 5.2 lists typical chip films and their etching methods. For advanced LSI devices produced with the Chemical Mechanical Polishing (CMP) process, a popular process for miniaturized and multilayer LSI devices, polishing methods have come into more frequent use than chemical/physical etching methods to remove a film.

Table 5.2 Typical Chip Films and Etching Methods

	Type of Film	Etching Method
Passivation film	SiN	H_3PO_4 • plasma
	SiO_2	HF • plasma
Wiring	Al	HCl/H_2O_2
	Ti / TiN	H_2SO_4/H_2O_2
	Poly-Si	KOH • plasma
Dielectric film	Oxide film (e.g. SiO_2, BPSG, or TEOS)	HF • plasma

(b) Surface observation

The surface observation is a basic physical analysis. It is one of the indispensable methods to resolve the failure mechanism. An optical microscope or a scanning electron microscope (SEM) is used for this purpose.

- Optical microscope

  Optical microscopes have been used as a simple and easy observation tool. Optical microscopes are still an effective tool for physical observations (stain-like contamination, etc.) in a macro view that SEM cannot support and for checking of a preprocessed state prior to SEM observation.
- Scanning Electron Microscope (SEM)

  The SEM emits an electron beam onto the sample and detects the secondary electrons released from the surface. The number of secondary electrons is converted into brightness to form an image. This number increases with the atomic number. It is also affected by the surface conditions, so that the shape can be observed. The SEM has a greater depth of focus than the optical microscope, with the spatial resolution reaching several angstroms.
- Electron Backscatter Diffraction Pattern (EBSP)

  The EBSP method is an SEM-applied technique that observes crystal orientations by analyzing diffraction patterns (Kikuchi lines) due to an increase of reflection electrons on a crystal lattice surface. Recently, as SEM machines have improved and CPUs have advanced, the EBSP method has come into greater use for the ease with which it can analyze measurement data. This method is effective in metal wiring grain observation and has been used to evaluate and analyze electro-migration.
- Scanning Probe Microscopy (SPM)

  SPM is a general term covering evaluation methods that obtain information by scanning a sample surface with pointed probes. The best-known SPM methods are STM and AFM, which are described later. In addition, various types of microscope applications have been developed, among them SCM (Scanning Capacitance Microscopy), which measures capacitance between probes and the sample to map capacitance, and SSRM (Scanning Spread Resistance Microscopy), which measures the currents flowing between probes and the sample to map resistance. These methods are now used not just as a geometry evaluation tool, but as a way to visualize impurity-diffused regions on Si substrates and to locate defects in a gate oxide film and high-resistance via holes. More SPM evaluation models are expected.

- Scanning Tunneling Microscopy (STM)

  STM is a technique used to observe the surface unevenness of a sample by scanning the sample surface with the tip of a probe placed close to it and moving the probe vertically, so that the tunneling current is consistent between the tip of the probe and the sample. The resolution of an STM is high (vertical direction: 0.001 nm, horizontal direction: 0.1 nm), but in principle it can handle only conductive samples.

- Atomic Force Microscopy (AFM)

  AFM is a technique used to observe the surface unevenness of a sample by detecting vertical probe movements caused by the atomic force between the tip of the probe placed close to the sample surface and the sample. The resolution of AFM is slightly lower than that of STM (vertical direction: 0.01 nm, horizontal direction: 0.1 nm), but it can make measurements on insulating substances.

(c) Cross-sectional observation (FIB, SEM, and TEM)

This observation is used to investigate the metallic wiring, transistors, via-contacts, and wire bonding. For contaminated chips, this method is used to investigate the process in which the chip was contaminated. There are various grinding, cleaving, focused ion beam (FIB), and transmission electron microscope (TEM) methods used.

1. Grinding/polishing

   If the sample is large enough, it is cut and ground. However, most samples are small and difficult to handle. In such cases, they should be embedded in a piece of resin or fixed with a jig. Vertical grinding provides only a small area of observation. Angle grinding is often preferable. The finish requires much care because it greatly affects the quantity and quality of information gained from the sample. Initial rough grinding scrapes off surrounding part. Then use finer abrasives, rotating the direction of grinding by 90 degrees to smooth the former grinding marks. Care must be taken to avoid any scratches or scoring. Slight scoring can be removed by etching. In semiconductor device failure analysis up to now, grinding has been used mainly for wire bonding cross-section observation, but recently, with the improvement of polishing machines and materials, it is being used in a preprocess for analysis sufficient for LSI internal observation.

2. Cleaving

   To observe the fine structure of metallic wiring, pn-junctions, and transistors, cleaving the chip using a diamond cutter is effective. Although the position to be observed is not precisely specifiable with this method, plasma etching and chemical etching can be applied to clarify the outlines of transistors after the chip has been cleaved.

3. FIB

This method etches a certain area on a chip by emitting a thin focused ion beam onto the chip surface to cause a spattering effect. Secondary electrons emitted from the surface can be used to generate an image similar to an SEM image. With these two features (etching and image monitoring), the cross section of a very small area can be exposed.[43] Etching while monitoring the surface image makes it possible to specify the location of the cross section to be observed with high precision (i.e. 1 μm or smaller). To observe the finished cross section, an SEM is used because it has higher spatial resolution than FIB (figure 5.26).

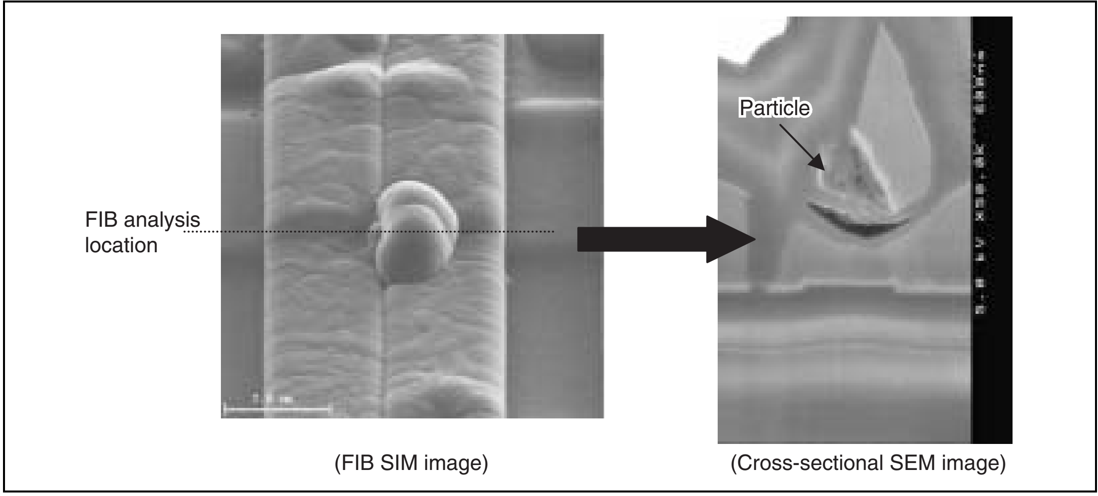


Figure 5.26 SEM Observation of Cross Section of a Chip Exposed with FIB

4. TEM

The TEM is an electron microscope that emits an electron beam accelerated with high voltage and detects electrons passed through the sample. It has a very high spatial resolution (0.2 nm at 200 keV). However, the sample must be 0.1 μm or thinner vertically to observe the cross section of a chip. The FIB method is used to create a thin film sample and it can specify the area to be treated with high precision.[44] This method provides higher spatial resolution than the FIB treatment plus SEM observation.

(d) Points of observation

1. Breaking, short circuit, and leakage by excess voltage or current

   Abnormal external voltage or current can melt the metal wiring and polycrystal silicon resistors. In some cases where the current is very high, the internal lead wires blow out. Abnormal alloy generation is occasionally observed at a pn-junction (between emitter and collector for a bipolar transistor). Other cases include dielectric breakdown of an oxide film and a short circuit between metal terminals.

2. Breaking of internal lead wires

   This failure is located by X-ray then investigated using a microscope after the package is removed. If the wires are detached from the bonding, the alloy formation of the detached part and misalignment of bonding should be checked. Gold and aluminum forms various Au-Al compounds at high temperatures. As the diffusion rate of gold is slower than aluminum, mass movement between two layers shifts the boundary, which generates a hole (Hartley-kirkendall effect). It can reduce the strength of bonding, increase the resistance, and cause detachment.

3. Corrosion of aluminum wiring

   Penetration of moisture, phosphoric acid (P_2O_5 disengaged from passivasion film) and chlorine ion, insufficient chemical treatment in process, cell effect and electric field caused by contact of different metals can corrode aluminum, which results in disconnection. In many disconnection cases, aluminum elutes completely and sometimes a short circuit occurs between adjacent wiring. Corroded aluminum often turns black. It can be easily found by observation of the chip surface using an optical microscope. This failure mode should be handled with care. Inappropriate selection of etching time, temperature, and solution when removing mold resin can promote aluminum corrosion. For this reason, plasma etching is sometimes used.

4. Chip cracks

   Heat stress often causes cracks in a silicon chip, which result in disconnection, short circuit, and leakage. These cracks are random lines crossing the chip surface, which is sometimes missed in observation with low magnification. The passivation film must be removed to observe the cracks because cracks can be limited in this film. Observation with an infrared microscope makes strain around the crack more distinguishable.

5. Mask misalignment

   Misalignment in diffusion, contact holes, or metal wiring can cause various failures. To investigate this defect, the alignment of pn-junctions, contact holes, and wiring must be checked carefully.

6. Via-contact failure

   This failure includes disconnection or ohmic failure at a step of a contact hole, and increased contact resistance due to the generation of a high-resistance layer and a closed via-contact hole caused by an inappropriate wafer fabrication process. Observation of a cross section using FIB is useful for investigating this type of failure.

7. Particle

   A particle on the chip surface or inside the chip can cause failure. Locating the layer where the particle exists and analyzing its composition may provide some clue to estimate the process and reason of contamination. Observation of a cross section using FIB clarifies the contaminated layer. Electron Probe Micro-Analysis (EPMA) or scanning auger microscopy (SAM) is useful for analyzing the particle contamination. However, care must be taken not to contaminate the sample further during analysis.

8. Electrostatic discharge

   The gate oxide film of metal-oxide semiconductor (MOS) is very thin and has low dielectric resistance. Electrostatic pulses generated by a human body or inspection instruments can break the device. This breakage can be detected by the increase of input current or change in Vth. In case of a bipolar transistor, the junction deteriorates and a part of the junction melts. Other symptoms include increased leakage current, deteriorated breakdown voltage, and hFE, and increased noise. If the aluminum wiring at the failed point has turned black, it is easily detected using an optical microscope. For other cases, emission microscopy and OBIC are effective for locating the failed point.

9. Electro/stress migration

   Excess current or stress to aluminum wiring can cause a hillock or voiding. A hillock may result in a short circuit within a layer or between layers. Voiding can lead to increased wiring resistance or disconnection. It is easy to locate the disconnection spot with electron beam testing. It is also possible to locate the voiding or disconnection using heat by laser irradiation, in which changes in resistance or thermoelectromotion of aluminum wiring are detected [18], [19].

10. Junction failure

    Stress by oxide film disengagement or abnormal growth of alloy, contamination, and crystal defects of silicon substrate can cause defective junctions. The junction is observed from the chip surface or the cross section depending on the type of failure. Wright-etching after the junction is exposed facilitates the observation.

11. Oxide film breakdown

    Destruction of an oxide film occurs when a strong electric field stress is applied to a transistor or capacitor block of an LSI device. Possible causes of the stress are external noise such as ESD, a design-based defect, a defect in the wafer process, time degradation, and other various factors. Since the symptom of an oxide film breakdown is a leakage failure, light emission analysis, OBIC (OBIRCH), or the like are effective methods.

(3) Impurity and Composition Analysis

For impurity and composition analysis of a semiconductor chip, an electron beam, X-ray, or ion beam is emitted onto the sample. Then secondary electrons, X-ray, and ions are detected and analyzed.

(a) Electron Probe Micro-Analysis (EPMA)

Irradiating an electron beam with energy of several to dozens KeV onto the surface of a solid sample causes the various quanta shown in figure 5.27 to be emitted. EPMA detects characteristic X-rays. It can analyze elements from boron (B) to uranium (U). The minimum area of analysis is approximately 1 µm or less and the depth of analysis is 1 µm to several µm. This method can perform qualitative and quantitative analyses of elements of 0.1wt% to 0.01wt%.

The electron beam (primary electrons) irradiated onto a solid sample strikes some electrons around the nucleus and drives them out, creating holes. Then outer electrons move to fill the holes to restore the stable state (figure 5.28). This state transition generates energy, which emits characteristics X-rays. Since their wavelength, or energy depends on the type of element, measuring the energy clarifies the element on the surface of sample. EPMA is usually carried out with SEM. It is the simplest method for analyzing the sample surface.

(b) Scanning Auger Microscopy (SAM)

As another type of energy emission, electron beam irradiation onto a solid sample causes auger electrons to be emitted as shown in figure 5.28. Auger electrons are electrons that have escaped from the same orbit where the electrons that have moved to fill the holes resided. As with characteristic X-rays, measuring the energy of auger electrons identifies the element.

Since auger electrons have relatively small kinetic energy, they can be detected only at a depth of 2 to 3 nm from the surface, as shown in figure 5.27. The minimum area of analysis is as small as 30 nm because the method measures the electrons from the surface layers that are not affected by the diffusion of an electron beam in the sample. SAM is more sensitive to the surface state than any other type of surface analysis. It is effective for investigating contamination of the chip surface. This method combined with spatter etching enables analysis under the surface.

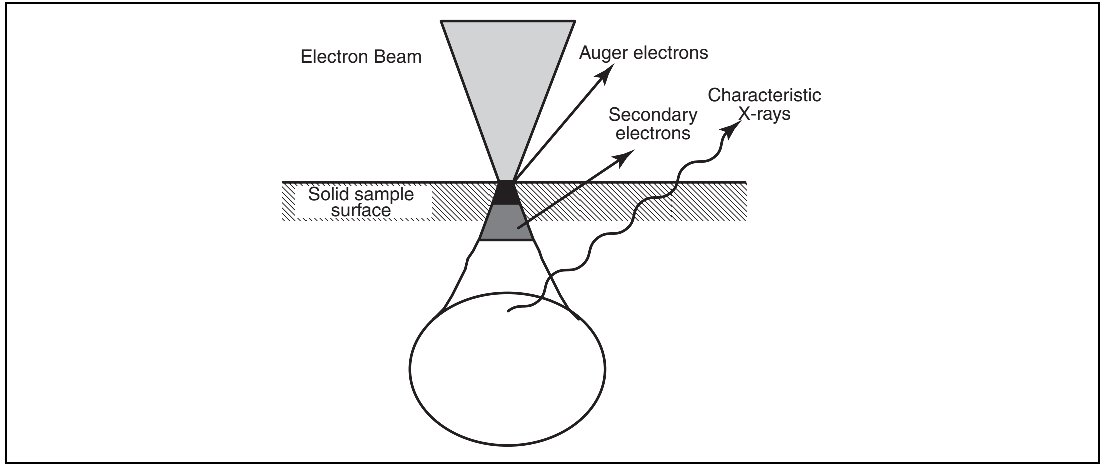


Figure 5.27 Quanta Emitted by Electron Beam Irradiation onto Solid Sample Surface

Nucleus
Electron
Primary electron
Secondary electron
Energy emission
Auger electron
Characteristic X-ray
(a) Generation of characteristic X-rays
(b) Generation of auger electrons

Figure 5.28 Generation Mechanism of Characteristic X-rays and Auger Electrons

(c) X-ray Photoelectron Spectroscopy (XPS)

This method measures the kinetic energy of photoelectrons generated by irradiation of X-ray's onto the surface of a solid sample. It determines the binding energy of electrons on the sample surface. As the binding energy depends on the type of element, the method can detect the elements on the surface. The minimum area of analysis is 10 µm, which is relatively large, because it is very difficult to focus the X-ray beam as compared to the electron beam. However, this method can detect even small shifts of binding energy, which enables estimation of chemical bonds. Similar to SAM, combining with spatter etching can analyze under the surface.

(d) Secondary Ion Mass Spectroscopy (SIMS)

This method irradiates an ion beam on a solid surface and detects the secondary electrons emitted from the surface. It uses a mass spectrometer to analyze the secondary electrons. The minimum area of analysis is several µm because of the difficulty to focus the ion beam. However, the SIMS can analyze any elements including hydrogen and helium, which the SAM and EPMA cannot analyze, with a high sensitivity of several ppbs. This method can analyze elements under the sample surface with the spatter effects by ion beam. The SIMS is the most sensitive surface analysis method. It is used to analyze contamination of chip surface and evaluate the impurity distribution in the direction of depth into the silicon substrate.

5.3.8 Establishment of Failure Mechanism

A careful investigation is required to determine the abnormalities discovered by various failure analysis techniques as the true cause of the device failure. The investigation must be conducted from a variety of angles to prove a consistent explanation of the device failure in terms of the electrical characteristics of the failure identified. It is rare that all of the detected abnormalities are directly linked to the failure, and an incorrect judgment results in incorrect corrective action being taken without any improvement.

As the integration density of semiconductor devices and the level of circuit complexity increase, the nature of failures has also become more complex. That makes discovering the cause of failure more difficult. Clarifying the failure mechanism requires failure verifying simulations and a database of previous failure analyses. A design to facilitate testing (analysis) at the development stage also contributes to the resolution of failure mechanism.

5.3.9 Appendix (List of Analysis Techniques)

1. List of Failure Analysis Techniques

Item	Technique (Equipment)	Description	Purpose
External visual check	• Observation by eyes • Stereomicroscope • SEM	• Detects secondary electrons emitted by electron beam irradiation	Checking the external conditions
	• EPMA	• Analyzes the wavelength and energy of characteristic X-rays generated by electron beam irradiation	Analyzing contamination between leads and element analysis (i.e. metallic migration)
Electro characteristics evaluation	• Functional characteristics (With LSI tester) • DC characteristics (With curve tracer) • Logic simulation		Evaluating functions, DC characteristics, and internal logic analysis
Internal check before opening package	• X-ray • Infrared (Microscope) • Ultrasonic (Scanning acoustic microscope)	• Radioscopic observation • Observes infrared radiation reflected at the reverse side of the chip. • Detects reflected ultrasonic wave	• Observation of bonding wires • Observation of bonding pads • Investigation of voiding, peeling, and cracks
	• Fine leak measurement • Gross leak measurement	• Uses helium tracer gas • Uses fluorocarbons	Evaluating of airtightness of metal and ceramic packages

Item	Technique (Equipment)	Description	Purpose
Opening package and locating fault point	• Opening a hole in a mold package (With opener)	• Upper resign	• Removing only upper resin
	• Plasma etching	• Chemical reaction by plasma	• Removing passivation film
	• RIE	• Removes dielectric film between layers with anisotropic etching using upper aluminum as a mask.	• Exposing lower layer aluminum
	• FIB processing	• Ion beam spattering using W (CO_6) gas to form W	• Forming pads for probing
	• Nanoprober-based analysis	• Evaluates electrical characteristics of the internal circuitry of an LSI device using a submicron probe.	Logical measurement and locating disconnection of internal wiring
	• Electron beam testing (With EB tester)	• Analyzes distribution of secondary electrons emitted by electron beam irradiation	
	• LVP	• Detects the light reflected by pulsed laser irradiation (effective for backside/flip-chip analysis)	
	• TRE	• Detects a weak light in the order of picoseconds generated when a transistor switches; used to analyze the operating timing (effective for backside analysis).	
	• Emission analysis (With emission microscope)	• Detects faint light emission.	Locating leakage at oxide film and pn-junctions, or short circuits of wiring
	• Thermal analysis (Liquid crystal and infrared microscope)	• Detects heat.	
	• OBIC/OBIRCH	• Detects optically excited current by electron beam irradiation • Detects the change of resistance (current) using the thermal effect	
	• EBAC	• Detects and produces an image of the absorption current generated by electron beam irradiation (effective for wiring breaks).	

Item	Technique (Equipment)	Description	Purpose
Physical analysis and observation of shape and state of chip	• Optical microscope observation • SEM observation • EBSP	• Detects secondary electrons emitted by electron beam irradiation • Observes the crystal orientation by analyzing the diffraction pattern of the reflected electron increase at the crystal lattice.	Surface observation
	• Grinding • FIB processing • TEM	• Spattering by ion beam irradiation • Detects electrons that pass through the sample	Surface observation
Elemental analysis	• EPMA	• Analyzes the wavelength and energy of characteristic x-rays generated by electron beam irradiation.	• Analyzing components of particles
	• SAM	• Analyzes the energy of auger electrons generated by electron beam irradiation.	• Analyzing contamination and impurity on the surface (less than 1 nm to several nm deep)
	• XPS	• Analyzes the energy of photoelectrons generated by x-ray irradiation.	• Investigation of the conditions of chemical bonds
	• SIMS	• Analyzes the mass of secondary electrons generated by ion beam irradiation.	• High sensitivity analysis of impurity

2. List of Failure Analysis Techniques (the tables on pages 42 and 43 are right-hand columns of the tables on pages 40 and 41)

Technique	Probed particle	Observed particle	Principle and method
Electron Probe Micro Analysis (EPMA)	Electron (Dozens kV)	X-ray	Surface topography by scanning Element analysis by characteristic X-ray
Scanning Electron Microscopy (SEM)	Electron (Dozens kV)	Secondary electron	Surface topography by scanning EBIC and stroboscopic
Transmission Electron Microscopy (TEM)	Electron (Up to 200 V)	Electron	Magnified observation of surface topograph using replica method Evaluation of crystallinity using diffraction image
Auger Electron Spectroscopy (AES)	Electron (Several hundred to several kV)	Auger electron	Element analysis by measuring energy of auger electrons
Scanning Auger Microprobe (SAM)	Electron (1 to 10 kV)	Auger electron	Element analysis by measuring energy of auger electrons
Reflection High Energy Electron Diffraction (RHEED)	Electron (Dozens kV)	Scattered electron	Scattering and angled incidence/reflection by surface thin layer atoms
Secondary Ion Mass Spectroscopy (SIMS)	Ion (Several hundreds to 20 kV)	Secondary ion	Mass spectrometry of spatter ions
Rutherford Back Scattering (RBS)	He^+ or H^+ Ion (Up to 1 MV)	Back scattering ion	Analysis of intensity and energy of back scattering ions
X-ray Photoelectron Spectroscopy (XPS)	Characteristic X-ray	Photo-electron	Determination of shell levels by measuring photoelectron energy
Ultra Violet Photoelectron Spectroscopy (UPS)	Ultra violet	Photo-electron	Determination of shallow shell levels by measuring photoelectron energy

Technique	Probed particle	Observed particle	Principle and method
X-ray Fluorescence Spectroscopy (XRFS)	X-ray	X-ray	Spectrometry of characteristic X-ray generating by photoelectric effect by X-ray irradiation
Scanning Acoustic Microscopy (SAM)	Ultrasonic wave	Ultrasonic wave	Analyzing elasticity by measuring ultrasonic propagation
Infrared Spectroscopy (IR)	Infrared	Reflected infrared spectral	Measuring infrared absorption spectral in surface reflection
Cathode-ray Luminescence (CL)	Optical spectral	Electron	Measuring spectral of light generated by electron collision and band excitation
Focused Ion Beam (FIB)	Ion (Up to 50 kV)	Secondary electron	Spattering by ion beam irradiation

Information obtained	Sensitivity	Area of analysis	Depth of analysis	Description
Surface topograph and element distribution elements analyzed: B-U	100 to 1000 ppm 10^{-2} ML*	10^{-3} to 0.3 mmϕ	Up to 1 μm	Quantitative compensation established. High sensitivity for heavy elements. Submicrometer resolution is impossible.
Surface topograph, crystal defect, carrier lifetime, and signal propagation of device in operation	Secondary electron: Up to 0.6 nm	10^{-3} to 0.3 mmϕ	Up to 1 μm	High-resolution observation of the surface of a bulk sample. Various information including electromotive current.
Surface topography characteristics, crystallinity evaluation, and internal structure	Lattice image: Up to 0.14 nm Particle image: Up to 0.2 nm		Several μm	Sample must be a thin film. Sharp contrast of crystal defect. High resolution.
Surface element determination and depth distribution	10^{-3} ML* 0.01 to 0.1 %	30 to 1 mmϕ	Dozens angstroms	High sensitivity for light elements. High mass sensitivity. Difficult to determine heavy elements because of complex spectral. Combined with ion spattering provides composite distribution along the depth of limited area.
Surface element determination, depth distribution, and three-dimensional element distribution	0.1 to 1 %	5×10^{-4} to 0.1 mmϕ	Dozens angstroms	High sensitivity for light elements. High mass sensitivity. Difficult to determine heavy elements because of complex spectral. Combined with ion spattering provides composite distribution along the depth of limited area.
Symmetry of surface atoms and absorption atoms, and atomic interval	10^{-2} ML*	0.5 to 5 mm^2	Dozens to several hundreds angstroms	Surface structure and chemical composition.

Information obtained	Sensitivity	Area of analysis	Depth of analysis	Description
Element determination, surface element distribution, topography elements analyzed: From H to U	10^{-5} ML* ppb to ppm	10^{-3} to 1 mmϕ	ML* to several ML*	Easy measurement of element distribution on surface and along depth. Applicable to all elements. Drawback: Large difference of secondary ion generation rate among elements. (>10^{3})
Element determination, quantitative and depth analysis	10^{17} to 10^{14} atom/cc	Up to 1 mmϕ	Up to 1 μm Depth accuracy: Up to 15 nm	Nondestructive qualitative, quantitative, and depth analysis. Secondary analysis is impossible. Huge equipment.
Element determination and chemical shift	2×10^{-3} ML*	100 μm^2 to 0.3 mm^2	5 to 2 nm	Measurement of chemical bonds and compounds using chemical shifts. Low sensitivity but nondestructive.
Band structure and vibration level	2 to 10^{-3} ML*	Up to 0.1 mm^2	ML* to 3 nm	Band structure information can be obtained. Element analysis is impossible. Sensitive to surface conditions.
Element determination elements of quantitative analysis: From F	Heavy elements: 5 ppm Light elements: 500 ppm		Dozens μm	Quick nondestructive qualitative and quantitative analysis.
Crystal defect and multi-layer structure analysis			Dozens μm	Nondestructive analysis of cross-sectional structure.
Surface molecular structure and bonding state	10^{-3} to 10^{-7} g	Several mm to dozens mmϕ	Up to 1 μm	Chemical type and orientation of surface absorbed substances.
Energy band structure and wave length change by structure	Up to ppm	0.1 to 1.0 μmϕ	Up to 1 μm	Only applicable to measurement of light emitting substances and solid plasma emission.
Cross-sectional structure	Secondary electron: Up to 5 nm			Cross-sectional observation of limited areas.

Note: * ML: Mono Layer

References:

[1] T. Ishiyama and K. Shigeta: "Application of a Route Tracing-based Failure Diagnosis Method to Single Failures," LSI Testing Symposium (2000)

[2] I. Yamazaki, H. Yamanaka, T. Ikeda, M. Takakura, Y. Sato: "An Approach to Improve the Resolution of Defect-Based Diagnosis," Proc. 10th Asian Test Symposium, p. 123-128 (2001.11)

[3] T. Ishimura, M. Sanada, K. Nakamae and H. Fujioka: "EB Tester-based Failure Tracing Algorithm of a Combination Circuit Using Failure Simulation," LSI Testing Symposium, p. 80-85 (1998)

[4] M. Sanada and K. Uehira: "Identifying Tr in a Circuit Block and Short-circuited Pair of Wires Using IDDQ," LSI Testing Symposium, p. 195-200 (2003)

[5] A. Uchikado, et al.: "Method of Fault Diagnosis Using the Fail Log of Functional Testing," LSI Testing Symposium, p. 259-264 (2004)

[6] S.H.Lewis: "Infrared Microscopy as Applied to Failure Analysis of P-DIP Devices," IEEE 24th Annual Proc. Rel. Phys. Symp., p. 99-101 (1986).

[7] H. Nonaka and S. Okikawa: "Development of an Ultrasonic Survey Imaging System," Technical Report of IEICE of Japan, R86-68, p. 31-36 (1987)

[8] S. Morris and E. J. Widener: "Anisotropic Etching for Failure Analysis Applications," Proc. of the 15th Internat. Symp. for Testing and Failure Analysis, ASM Internat., p. 161-166 (1989)

[9] Y. Mashiko, H. Morimoto, H. Koyama, S. Kawazu, T. Kaito and T. Adachi:"A New VLSI Diagnosis Technique: Focused Ion Beam Assisted Multilevel Circuit Probing," IEEE 25th Annual Proc. Rel. Phys. Symp., p. 111-117 (1987)

[10] Y. Mitsui, F. Yano, Y. Nakamura, K. Kimoto, T. Hasegawa, S. Kimura and K. Asayama, Ext. Abst. IEDM, p. 329 (1998).

[11] F. Yano, H. Yanagida, T. Mizuno, F. Arakawa, Y. Ogawa, S. Terada and K. Asayama: LSI Testing Symposium, 2003 Minutes, p. 273 (2003)

[12] H. Yanagida, T. Mizuno, F. Yano, K. Asayama, E. Uzaki, T. Agamura and Y. Mitsui: LSI Testing Symposium, 2004 Minutes, p. 359 (2004)

[13] T. Mizuno, H. Yanagida, F. Yano and K. Asayama: LSI Testing Symposium, 2004 Minutes, p. 363 (2004)

[14] K. Ura and H. Fujioka: "Electron Beam Testing Handbook," Electron Beam Study Vol. 7, Japan Society for the Promotion of Science, 132nd Committee, 98th Workshop (1987)

[15] T. Nakamura, Y. Hanagama, K. Nikawa, T. Tsujide, K. Morohashi and K. Kanai: "Novel Electron-Beam Image-Based LSI Fault Technique without Using CAD Database: Development and Its Application to Actual Devices," Proc. Int. Symp. Testing and Failure Analysis (ISTFA), p. 49-54 (1992).

[16] A. C. Novel: "IDA:A tool for Computer-Aided Failure Analysis," IEEE Proc. Internat. Test Conf. (ITC), p. 848-853 (1992).

[17] Peter Ullmann, et al.: "A New Robust Backside Flip-Chip Probing Methodology," Proc. Int. Symp. Testing and Failure Analysis (ISTFA) (1996)

[18] E. Yoshida, et al.: "Direct Detecting of Dynamic Floating Body Effects in SOI Circuits by Backside Electron Beam Testing," Internat. Electron Devices Meeting (IEDM) Tech. Dig., p. 567-570 (1998).

[19] Mario Paniccia, et al.: "Novel Optical Probing Technique for Flip Chip Packaged Microprocessors," IEEE Proc. Internat. Test Conf. (ITC), p. 740-747 (1998)

[20] E. Yoshida, et al.: "Study of the Backside Probing Methodology," LSI Testing Symposium, 2000 Minutes, p. 94-99 (2000)

[21] J.C. Tsang, J.A. Kash: "Picosecond Hot Electron Light Emission from Submicron Complementary Metal-Oxide-Semiconductor Circuits," Applied Phys. Lett., 70, 889 (1997)

[22] S. Kawanabe, et al.: "Evaluation and Case Studies Of Time Resolved Emission Analysis," LSI Testing Symposium, 2004 Minutes, p. 315-320 (2004)

[23] J. Komori, J. Mitsuhashi, M. Hatanaka and N. Tsubouchi: "Analysis of the Hot Carrier Degradation Effect by Observing Emissions" The Institute of Electronics, Information and Communication Engineers, SDM90-38, p. 15-18, 1990

[24] Toriumi, "Experimental Study of Hot Carriers in Small Size Si-MOSFETs," Solid-State Electronics, Vol. 32, No. 12, 1989, p. 1519-1525

[25] S. Tam and C. Hu: "Hot-Electron-Induced Photon and Photo-carrier Generation in Silicon MOS FETs," IEEE Trans. Electron devices, Vol. ED-31 (1984), p. 1264-1273

[26] H. Ishizuka, M. Tanaka, H. Konishi, and H. Ishida: "Advanced Method of Failure Analysis Using Photon Spectrum of Emission Microscopy," Proc. Int. Symp. Testing and Failure Analysis (ISTFA), p. 13-19, 1990

[27] T. Yoshida, T. Koyama, J. Komori, Y. Mashiko and A. Onoyama: "Analysis of Wafer-Level Failure Distribution by High-Sensitivity Detection of Backside Emission," LSI Testing Symposium, 2002 Minutes, p. 137-142, 2002

[28] M. Sanada and H. Fujioka: "Yield Enhancement for Logic LSI by Killer Defect Diagnosis Technique Using Abnormal IDDQ Phenomenon," LSI Testing Symposium, 1998 Minutes, p. 208-213, 1998

[29] M. Sanada and H. Fujioka: "Yield Enhancement for Logic LSI by Killer Defect Diagnosis Technique Using Abnormal IDDQ Phenomenon," Proc. International Symposium on Semiconductor Manufacturing (ISSM), p. 265-268, 1998

[30] N. Hirayama, K. Nikawa, M. Nakagiri and N. Saito: "Development and Sample Analyses of a Liquid Crystal Application Failure Analysis Device," 16th Union of Japanese Scientists and Engineers, Reliability and Maintainability Symposium of Japan, p. 409-412 (1986)

[31] N. Hoshino: "Analysis Technique and Examples of ESD Failures of Semiconductor Devices," RCJ 1st EOS/ESD Symposium of Japan, p. 21-26 (1991)

[32] S. Kondo and H. Kaneko: "High-Resolution Temperature Measurement of Void Dynamics Induced by Electromigration in Aluminum Metallization," Jpn. J. Appl. Phys. Vol. 67, p. 1606-1608 (1995)

[33] K. Nikawa and S. Tozaki: "Novel OBIC Observation Method for Detecting defects in Al Stripes Under Current Stressing," Proc. Int. Symp. Testing and Failure Anal. (ISTFA), p. 303-310, 1993

[34] K. Nikawa, C. Matsumoto and S. Inoue: "Novel Method for Void Detection in Al Stripes By Means of Laser Beam Heating and Detection of Changes in Electrical Resistance," Jpn. J. Appl. Phys., Vol. 34, Part 1, No. 5, p. 2260-2265, 1995

[35] K. Naito, N. Asatani and T. Miyagawa: "Application of OBIRCH Analysis to Memory Devices," LSI Testing Symposium, p. 219-223 (2003)

[36] T. Koyama, Y. Mashiko, M. Sekine and H. Koyama: "OBIC Analysis Using Thermoelectric Power," Japan Society for the Promotion of Science, 132nd Committee, 125th Workshop (LSI Testing Symposium), 1995, p. 221-226

[37] T. Koyama, Y. Mashiko, M. Sekine, H. Koyama and K. Horie: "New Non-Bias Optical Beam Induced Current (NB-OBIC) Technique For Evaluation Of Al Interconnects," in Proc. Int. Rel. Phys. Symp. (IRPS), 1995, p. 228-233

[38] T. Koyama, K. Sonoda, J. Komori, and Y. Mashiko: "Detection of Defects in Metal Interconnects by Nonbias-Optical Beam Induced Current Technique," Journal of Applied Physics, Vol. 86, No. 11, 1 December 1999, p. 5949-5956

[39] T. Ishii, K. Azamawari and K. Miyamoto: "Study of Dynamic Test Technique from Bottom Side of LSI Chip using the Infrared-OBIC Method," The Institute of Electronics, Information and Communication Engineers of Japan (IEICE), R91-34, p. 29, 1991

[40] T. Koyama, M. Umeno , J. Komori, and Y. Mashiko: "Evaluation of Silicide Morphology by Near Infrared Laser Optical Beam Induced Current (IR-OBIC) Technique," Japan Journal of Applied Physics, Vol. 40, Part 1, No. 11, p. 6446-6452 (2001)

[41] K. Nikawa and S. Inoue: "LSI Failure Analysis Using Focused Laser Beam Heating," Microelectron. Reliab, Vol. 37, No. 12, p. 1841-1847, 1997

[42] E. I. Cole Jr., P. Tangyunyong and D.L. Barton: "Backside Localization of Open and Shorted IC Interconnections," Proc. Int. Rel. Phys. Symp. (IRPS), 1998, 129-136

[43] K. Nikawa, K. Nasu, M. Murase, T. Kaito and T.Adachi:"New Application of Focused Ion Beam Technique to Failure Analysis and Process Monitoring of VLSI," IEEE 27th Annual Proc. Rel. Phys. Symp., p. 43-52 (1989)

[44] R. J. Young, E. C. G. Kirk, D. A. Williams and H. Ahmed: "Fabrication of Planar and Cross-Sectional TEM Specimens Using A Focused Ion Beam," Mat. Res. Soc. Symp. Proc. Vol. 199, Materials Research Society, p. 205-216 (1990)

Section 6 Usage Precautions

The quality and reliability of semiconductor devices is heavily influenced not only by the quality inherent to the devices themselves, but also by the "use" conditions, environmental conditions and how the selected circuits will be handled by the customer.

This section discusses all related precautions to be considered when deciding on parts for use during system design, assembly, mounting and other component handling, during storage, or at other times, including specific examples.

6.1 Device Selection

6.1.1 Maximum Ratings

Maximum ratings for semiconductor devices are defined as values which even momentarily must not be exceeded. In this handbook, the concept of maximum ratings includes that of the absolute maximum ratings. If a maximum rating is exceeded even for an instant, degradation or failure may result. The subsequent lifetime of the device may be greatly shortened. In addition, differences in the strength of individual products may mean that even though some products may withstand the stress imposed when exceeding a maximum rating, others may abruptly fail.

In designing an electronic circuit with semiconductor devices, devices should be selected, or the circuit designed, such that maximum ratings specified for devices are not exceeded, even given fluctuations in external conditions during use.

In addition to DC maximum ratings, devices should be used with voltages, currents, power, and times in the safe operating range at all points on the load locus curve. The power supply and ground line serve as reference points for the semiconductor device operation. Special care should be exercised to ensure that maximum ratings are not exceeded, including transient states.

6.1.2 Derating

The quality and reliability of semiconductor devices are greatly influenced by the environment of use. That is, products with the same quality may be less reliable in harsh environments, and more reliable when the usage environment is less harsh. Even when used within the maximum ratings, if a device is used under extremely stringent conditions equivalent to lifetime tests, wear-out-like failures may result. Hence the concept of derating is extremely important.

Derating may be approached from two perspectives: derating with respect to design limits, and derating with respect to manufacturing defects.

1. Derating with respect to design limits

   When usage conditions become extremely harsh, the wear-out failure range may be entered during the time of actual use, and if derating is not employed, it may become necessary to schedule replacement of all devices as part of maintenance after operation for a certain length of time in the application.
2. Derating with respect to manufacturing defects

   Although the wear-out failure range is not entered while in the marketplace, if conditions of use are harsh, the probability of occurrence of defects in the random failure range may no longer be negligible.

Standard approaches to derating are described in table 6.1. In the "Temperature" row, junction part temperatures assume intermittent use (for approximately three hours per day) over about 10 years. Conditions for high-reliability applications, shown in parentheses, assume round-the-clock operation over approx. 10 years.

Table 6.1 Standard Examples of Derating Design*[1]

Derating Element*[2]		Diodes	Transistors	ICs	HyICs	LDs
Temperature	Junction temperature*[3]	110°C or lower (Tj = 60°C or lower)			—	110°C or lower (Tj = 60°C or lower)
	Device ambient temperature*[3]	Topr min to Topr max (Ta = 0 to 45°C)				Topr min to Topr max Ta = individual specifications
	Other	Power consumption, ambient temperature, heat-dissipation conditions Tj = Pd × θja + Ta			—	—
Humidity	Rel. humidity	Relative humidity = 40 to 80%				
	Other	Normally, if there is condensation due to rapid changes in temperature or for other reasons, the printed circuit board is coated.				No condensation
Voltage	Breakdown voltage	Maximum rating × 0.8 or less (maximum rating × 0.5 or less)	Maximum rating × 0.8 or less	Conform to catalog recom-mended conditions	Conform to recommended delivery specification conditions	
	Overvoltage	Take measures to prevent overvoltage application, including electrostatic discharge				
Current	Average current	Ic × 0.5 or less (Ic × 0.25 or less)	Ic × 0.5 or less	Ic × 0.5 or less (especially power ICs)	Conform to recommended delivery specification conditions	
	Peak current	If (peak) × 0.8 or less	Ic (peak) × 0.8 or less	Ic (peak) × 0.8 or less (especially power ICs)	Conform to recommended delivery specification conditions	
	Other	—	—	Take fanout, load impedance into consideration	—	Take optical output Pomax into consideration

Derating Element*[2]		Diodes	Transistors	ICs	HyICs	LDs
Power	Average power	Maximum rating × 0.5 or less (especially Zener diodes)	Maximum rating × 0.5 or less (especially power transistors)	Maximum rating × 0.5 or less (especially power ICs, high-frequency ICs)	Conform to recommended delivery conditions	Vf × If × Duty
Pulse*[4]	ASO	Should not exceed individual catalog maximum ratings				
	Surge	If (surge) or less	Ic (peak) or less	Ic (peak) or less	Conform to recommended delivery conditions	

Notes: 1. Excludes special usage conditions, for example, extreme high temperatures.
2. These derating elements should be satisfied simultaneously wherever possible.
3. For applications requiring particularly high reliability, the values in parentheses ( ) should be used.
4. Generally where transient states are concerned, peak voltage including surges, current, electric power, and junction temperature should be below maximum ratings, and derating for reliability should be performed using the above average values. ASO (Area of Safe Operation) will differ with the circuit used; please consult with one of our engineers.

An example of derating for temperature is given in table 6.2. As the temperature rises, chemical reactions in the materials constituting a semiconductor device are accelerated, and may result in a failure. Generally reliability estimates are performed in terms of whether wear-out failure can be guaranteed not to occur, based on the results of reliability tests and standard usage conditions in the marketplace. Derating is performed after calculating the acceleration coefficient between the lifetime test data, which has been confirmed by assuming the activation energy for the chemical reactions for each failure mode, and the actual conditions of use. In general, temperature acceleration alone does not result in a sufficient acceleration rate, but is ordinarily used together with, for example, voltage and temperature difference. The acceleration limit for temperature must be carefully analyzed. This is because a mistake in judgment may be made by other failure modes governed by different reactions from that in the normal temperature range, such as the glass transition temperature of plastic materials.

Table 6.2 Temperature Derating Characteristics (Example)

<table>
<tr><td colspan="2">Example of Derating Application</td><td>Temperature Derating</td></tr>
<tr><td>Stress factor</td><td>Junction temperature</td><td rowspan="4">Times: 10000, 1000, 100, 10, 1, 0.1
Temperature (°C): 0, 100, 200
0.3 eV, 0.5 eV, 0.7 eV, 0.9 eV</td></tr>
<tr><td>Failure judgment criteria</td><td>Deterioration of electrical characteristics</td></tr>
<tr><td>Failure mechanism</td><td>Deterioration by chemical reactions</td></tr>
<tr><td colspan="2" rowspan="2">Outline

The abscissa shows the reciprocal of absolute temperature; the ordinate shows the time required to reach the prescribed failure rate at that temperature.

It is believed that defects are caused by chemical reactions of the material of which the devices are made. In general, in order for a reaction to take place energy has to be supplied from outside.

Chemical reaction theory holds that this energy comes from thermal kinetic energy. The distribution of thermal kinetic energy follows the Maxwell-Boltzmann law:

Lifetime = constant × exp (Ea/kT)

where Ea = activation energy (eV)
T: absolute temperature (degrees K)
k: Boltzmann constant
(8.617×10^{-5}eV/k)</td></tr>
<tr><td>How to calculate derating

Let us find the acceleration coefficients α in lifetime tests with Tj values of 150°C and 65°C. For the activation energy, the general value of 0.5 eV for dielectric breakdown of the oxidation film is used.

$\alpha = \frac{\exp [0.5/8.617 \times 10^{-5}/(273 + 65)]}{\exp [0.5/8.617 \times 10^{-5}/(273 + 150)]}$</td></tr>
</table>

An example of derating for humidity is shown in table 6.3. The primary purpose of this derating is to prevent corrosive breaks of Al wiring and to reduce any changes in solderability accompanying storage of package leads. Due to advances in plastic materials, corrosion and breakage of Al wiring hardly ever occurs any more in the marketplace; but even today, use under extremely harsh conditions may still result in wear-out failures within the expected period of useful life of a device.

Table 6.3 Humidity Derating Characteristics (Example)

Example of Derating Application	
Stress factor	Temperature, relative humidity
Failure judgment criterion	Deterioration of electrical characteristics
Failure mechanism	Metallization corrosion

Outline

Since absolute humidity is proportional to the number of water molecules contained in a unit volume, in this example we approximate the lifetime by the nth power of the stress that governs the failure rate.

Lifetime = constant × (absolute humidity) ^{n}

Taking the logarithms of both sides of this equation, we obtain

log (lifetime) = n × log (absolute humidity) + log (constant)

Taking the logarithm of absolute humidity as the abscissa and the logarithm of the time required to reach the prescribed failure rate at that absolute humidity as the ordinate, the resulting graph is approximately a straight line.

Absolute humidity is a function of temperature and relative humidity.

The absolute humidity can be obtained from the following equation:

Absolute humidity = saturation absolute humidity × relative humidity

Humidity Derating

Absolute humidity (mm Hg) (Source: Rikanenpyo)

Temperature/K	0	2	4	6	8
270	0.485	0.562	0.650	0.750	0.863
280	0.992	1.136	1.300	1.483	1.689
290	1.192	2.177	2.464	2.784	3.140
300	3.535	3.973	4.457	4.991	5.580
310	0.485	0.562	0.650	0.750	0.863
320	0.485	0.562	0.650	0.750	0.863
330	0.485	0.562	0.650	0.750	0.863
340	0.485	0.562	0.650	0.750	0.863
350	0.485	0.562	0.650	0.750	0.863
360	0.485	0.562	0.650	0.750	0.863

How to calculate derating

We calculate the acceleration under typical conditions used in tests of ability to withstand humidity (65°C/95% RH) and typical conditions in the marketplace (Ta = 25°C/65% RH).

From the table, the saturation vapor pressure at 65°C is calculated by the interpolation method to be 22.9 mmHg and the saturation vapor pressure at 25°C is calculated to be 2.8 mmHg.

The absolute humidity for value for each case is calculated by multiplying by 0.95 and 0.65, respectively.

Taking the ratio and using the typical acceleration constant n = 2 gives $\alpha = (21.7/1.8)^2$ = 145 times.

An example of derating for temperature differences appears in table 6.4. The failure mechanism assumes thermal fatigue failure of structural materials. This mode generally leads to wear-out failure modes, and so adequate derating calculations are important for power devices and other components. When designing thermal dissipation, the number of times heat stress is applied during the lifetime of the semiconductor device and the temperature difference of the heat stress must be taken into consideration.

Voltage, current, and power derating is especially effective in preventing failure phenomena. In particular, temperature-difference derating is strongly related to the occurrence of such failures, that is, failures to which stress-strength models apply. In these cases, robustness against failure is weakened by the development of structural defects, resulting in failure under stress which does not initially lead to failure.

In the marketplace, conditions of actual use are not so simple that they can be described by a single parameter. Moreover those conditions are not constant with time. Normally worst-case conditions are assumed when performing the derating to determine whether or not it can be used; but when conditions cannot be combined into a single parameter, conditions are converted into the following standard conditions (compound stress temperature-difference acceleration, cf. table 6.5; compound stress temperature acceleration, cf. table 6.6) and derating is performed.

Table 6.4 Power Transistor Power Cycle Derating Characteristics (Example)

<table>
<tr><td colspan="2">Example of Application of Derating</td><td>Power Transistor Temperature Difference Derating</td></tr>
<tr><td>Stress factor</td><td>Junction temperature difference</td><td rowspan="3">Example of a product having
the ability of 10,000 cycles at ΔTch = 90°C
No. of available cycles: 10^2, 10^3, 10^4, 10^5
Junction temperature difference (ΔTch): 10, 100, 1000
n=6, n=5, n=4, n=3, n=2</td></tr>
<tr><td>Failure judgment criterion</td><td>Deterioration of θch - c</td></tr>
<tr><td>Failure mechanism</td><td>Solder fatigue</td></tr>
<tr><td colspan="2">Outline
It is believed that the nth power of the temperature difference is proportional to the power cycle limit.
Number of cycle lifetimes =
constant × (temperature difference) n
Taking logarithms of both sides of this equation gives
log (number of cycle lifetimes) =
n × log (temperature difference) + log (constant)
Taking the logarithm of the junction temperature difference (ΔTch) at the time of power cycle ON or OFF as the abscissa and the logarithm of the limiting number of power cycles at that time as the ordinate, the resulting graph is approximately a straight line.
This line of reasoning permits us to estimate the number of years a device will last from the conditions under which the power transistor is used.
Conversely, we can determine the power transistor heat radiation conditions from the number of years the device is required to last.</td><td>How derating data are used
If we take Tc to have an actual measured value of 85°C, Pc to be 20 W and θch – c to be 1.0°C/W, Tjmax becomes 85 + 20 × 1.0 = 105°C; the difference from Ta = 25°C is ΔTj = 80°C.
The cycle lifetime at this time can be read from the graph and the number of cycles for which the component can be used obtained. In the case of a TO3PFM, this becomes about 5, so the acceleration rate between the conditions for reliability test datum = 85 and the conditions of actual use can be easily calculated.</td></tr>
</table>

Table 6.5 Compound Stress Temperature-Difference Derating Characteristics (Example)

<table>
<tr><td colspan="2">Example of Application of Derating</td><td>Power Transistor Temperature Difference Derating (Example)</td></tr>
<tr><td>Stress factor</td><td>Junction temperature</td><td rowspan="4">Temperature difference derating under multiple conditions

First, we find the acceleration coefficient between the market conditions and lifetime test conditions.

$\alpha 1 = [(175 - 25)/90]^5 = 21.4$ times
$\alpha 2 = [(125 - 25)/90]^5 = 1.88$ times

Letting m be the necessary number of cycles at $\Delta T = 90°C$, m = 50 times/year × 10 years × 21.4 + 365 days × 10 years × 5 times/day × 1.88.

In a lifetime test at $\Delta T = 90°C$, this becomes about 45,000 cycles.</td></tr>
<tr><td>Failure judgment criterion</td><td>Deterioration of $\theta ch - c$</td></tr>
<tr><td>Failure mechanism</td><td>Solder fatigue</td></tr>
<tr><td colspan="2" rowspan="2">Outline

Environmental variations under actual use conditions cannot necessarily be described in terms of constant conditions.

For example, in the case of the temperature difference in an automobile engine compartment, the worst case would be immediately after the engine has been turned off in a service area after the car was driven on an expressway in summer.

Let us assume that, for example, Tch in this case is 175°C, and that on average this situation occurs 50 times in a year.

Let us assume further that in normal use Tch is 125°C, and that the engine is turned ON and OFF 5 times per day on average.

When the reliability test condition is $\Delta T = 90°C$, we calculate how many cycles these correspond to the reliability test condition.

Assuming that (lifetime) = (constant) × (temperature difference) ^{n}, we solve for the case n = 5.</td></tr>
<tr><td>When the component is used under severe environmental conditions, the acceleration limit becomes a problem. In such a case, please consult with our company's Strategic Marketing Dept.</td></tr>
</table>

Table 6.6 Compound Stress Temperature Derating Characteristics (Example)

<table>
<tr><td colspan="2">Example of Derating Application</td><td>Compound Stress Temperature Derating (Example)</td></tr>
<tr><td>Stress factor</td><td>Junction temperature</td><td rowspan="4">Temperature difference derating under multiple conditions
$\alpha 1 =$ $\exp[0.6/8.517e^{-5}/(273 + 165)]$
$\exp[0.6/8.517e^{-5}/(273 + 175)]$
= 0.71 times
$\alpha 2 =$ $\exp[0.6/8.517e^{-5}/(273 + 125)]$
$\exp[0.6/8.517e^{-5}/(273 + 175)]$
= 0.14 times
The market condition t that correspond to reliability test times at 175°C:
t = 0.71 × 10 hours/year × 10 years + 0.14 × 365 days/year × 10 years × 5 hours/day
= 2620 hours
In lifetime testing it is extremely important to limit the time for testing up to 1,000 hours to guarantee the quality.</td></tr>
<tr><td>Failure judgment criterion</td><td>Deterioration of θch - c</td></tr>
<tr><td>Failure mechanism</td><td>Solder fatigue</td></tr>
<tr><td colspan="2" rowspan="2">Outline
Environmental variations under actual use conditions cannot necessarily be described in terms of constant conditions.
For example, in the case of the temperature difference in an automobile engine compartment, the worst case would be immediately after the engine has been turned off in a service area after the car was driven on an expressway in summer.
Let us assume that, for example, Tj in this case is 165°C, and that on average this situation takes 10 hours in a year. Let us assume further that in normal use Tj is 125°C, and 5 hours' driving per day on average.
If the reliability test condition is T = 175°C, we calculate how many hours these correspond to the reliability test condition.
Assuming that (lifetime) = (constant) × exp (Ea/kT), we solve for the case Ea = 0.6.</td></tr>
<tr><td>When the component is used under severe environmental conditions, the acceleration limit becomes a problem. In such a case, please consult with our company's Strategic Marketing Dept.</td></tr>
</table>

Assuming that the number of conditions that apply to practical use has been reduced to *n*,

ti = within the lifetime of a component, the cumulative time that the component has been used in the market under the *i*th condition, and let

αi = the acceleration coefficient derived from the standard conditions and the *i*th condition. The equivalent time that has elapsed under the standard conditions can be expressed as $ti \bullet \alpha i$. The following equation can then be obtained by converting every condition into its equivalent under the standard condition and obtaining the total.

$$t = \sum ti \bullet \alpha i$$

The lifetime under actual use conditions can be replaced with the test time in the accelerated lifetime test by substituting the reliability test conditions for the standard conditions in this formula.

6.1.3 Using a Device with Equivalent Function

Among semiconductor device characteristics, there are some that are listed in the catalogue and officially guaranteed, and others that, while not listed in the catalogue, are de facto conditions under which the device can be used. Before taking advantage of characteristics that are not listed in the catalogue, it is recommended that you thoroughly investigate those characteristics, including variation among individual devices.

Examples of this kind of situation would be using a standard digital circuit as an operational amplifier in an oscillator circuit, and using an output signal at a voltage at which operation is not guaranteed in a transient state when power is turned ON.

- Example 1
  Malfunction when a MOS IC is Used in an Analog Circuit

No. 1 Example	Malfunction when a MOS IC is used in an analog circuit
Type of device	MOS IC
Point	Caution is required as to the amount of margin in a circuit when the input leakage current fluctuates.
Outline of example/ phenomenon/cause	When a MOS IC was used as an oscillator circuit or analog switch, the allowable leakage current was less than that for a digital circuit; a leakage current that is too large can cause a malfunction. Not only leakage current in the device itself, but also between terminals of the printed circuit board (due to adhering dust) is a problem.
Countermeasures/ checking methods	1. Coat the printed circuit board so that dust will not adhere to it. 2. Improve the environment under which the device is used (reduce the humidity). 3. Design the printed circuit board so that the resistance between A and B will be 10^9 Ω or more.
Reference item	

- Example 2

  Erroneous Output from a Schmitt Trigger IC when Power is Turned ON

No. 2 Example	Erroneous output from a Schmitt trigger IC when power is turned ON
Type of device	TTL IC
Point	Exercise caution with regard to transitional phenomena when power is turned ON.
Outline of example/ phenomenon/cause	If the power to a circuit using a Schmitt trigger IC is turned ON while the input is at L level (0.8 V), even though the IC is an inverter the output became L. This phenomenon occurred because of the IC's hysteresis characteristics; if power is turned ON while the input is within the hysteresis range (about 0.7 V to 1.6 V) the output becomes unstable and the circuit does not operate normally. 5 V Output voltate 0.5 V input (outside hysteresis) 0.8 V input (within hysteresis) 0 V 5 V V_{CC}
Countermeasures/ checking methods	1. Keep the input outside of the hysteresis range until Vcc has reached a steady state. 2. Use a type of device that does not have hysteresis characteristics.
Reference item	

This applies also to recent microcontroller devices which include mask ROM versions, PROM versions, ZTAT and F-ZTAT versions, which have exactly the same functions but differ in the way of programming. Of course there are differences in the center values and dispersions of characteristics which are guaranteed, but there are differences in characteristics that are not stated explicitly in the specifications such as noise margin to prevent malfunction, noise generation, and stability of the oscillator circuit.

- Example 3

  Difference between ZTAT Version and mask ROM Version in Electromagnetic Emission (EME)

No. 3	Example	Deterioration when subjected to noise, caused by changing the mask
Type of device		Microcontroller
Point		It is necessary to ask, is there a problem with performance characteristics which are not specified in the standards when a mask is changed?
Outline of example/ phenomenon/ cause		In a ZTAT microcontroller, prototyping and initial mass production were completed and then there was a switchover to a mask ROM version with the same pin layout in order to proceed to full-scale mass production. When that was done, the level of noise generation increased, causing malfunction of the scanning station selection function of an adjacent FM radio (noise caused the radio to judge that there was a station at a frequency at which there was not). Adjustments were made in the printed circuit board ground wiring pattern layout and in the location of the bypass capacitor, tentatively solving the problem, but this caused delay in the timing of mass production, and in the meantime it was necessary to continue using the expensive ZTAT microcontroller.
Countermeasure/ checking method		The mask ROM version functional specifications have been adjusted to those of the ZTAT microcontroller as much as possible, but depending on the series used, there will be some products that differ somewhat in their functions. For example, even if the functions themselves are exactly the same, the products can differ in some characteristics that do not show up in official specifications (for example ability to withstand noise, latch-up, vulnerability to electrostatic breakdown, etc.), and these things must be checked out in advance using the actual device. If there are characteristics that make the device difficult to use or if improvements are necessary, please contact your Renesas sales office.
Reference item		

6.1.4 When a Device is Used in a Severe Environment

In particular, it is necessary to thoroughly consider the possibility that a failure may be caused by wear out. Unless derating is done correctly in the wear out region, the failure rate will increase rapidly with time when the device is actually used, causing serious trouble.

It is very important to provide for a long enough period of reliability testing by making sure that the equivalent periods obtained with the acceleration coefficients produce a period longer than the intended period of practical application. In the wear out failure period, once a failure starts to occur the failure rate increases rapidly with time. Conversely, it is possible to confirm that the failure rate in the practical use is very low even from a small number of samples, by using the data of little longer time (for example, double the time) than the required lifetime.

6.1.5 When Using a Device in an Application that Requires High Reliability

In applications that require high reliability, e.g. in cases where the occurrence of a single failure necessitates tracking down the reason and taking the required steps to improve quality, it is necessary to estimate the failure rate not only caused by devices wearing out but also in the region of randomly occurring failures. When failures occur randomly, it can be expected that if the conditions of use become more severe then the failure rate will increase. For example, even in the case of a product that has satisfied the quality requirement in the past, it is possible that if the conditions of use become more severe it will no longer satisfy the quality requirement.

In many cases, the random failure region appears as a result of screening the initial failure mode caused by manufacturing defects. Effective means of decreasing this failure rate include decreasing the density of defects in the manufacturing step, and optimizing of the screening method.

Of course the ultimate quality target is zero defects, but unfortunately this has not yet been achieved. When using a product in which the effect of a failure occurring in a component would be serious, preventive measures should be taken in the system.

- Example 4

  Quality Grade Selection

No. 4	Example	Quality grade selection
Type of device		All semiconductor devices
Point		It is necessary to ask whether the semiconductor device being used is suitable for the application.
Outline of example/ phenomenon/ cause		In an application in which zero defect quality is required, a semiconductor device intended for use in ordinary household appliances was used, and considerable trouble was caused by the chronic occurrence of defects whose probabilities are small. When a complaint that the failure rate was high was lodged, it was recommended that the user switch to a device intended for high reliability applications. Supplementary explanation: There are two types of differences in the quality of an LSI intended for high reliability applications and an LSI intended for ordinary applications. One is a case in which the design adds some additional margin to the limiting value itself to meet the requirements of the severe environmental conditions (temperature or environmental stress). The other is better selection to reduce the failure rate resulting from manufacturing fluctuations by using technology such as screening. As we stated above the ultimate goal for devices to be used in applications that require high reliability is zero defects, but at present this has not been reached. We would like to have feedback from our customers whenever a problem occurs so that we can work to improve quality.
Countermeasures/ checking methods		1. Please consult in advance with your Renesas sales office so that we can help you select the product that is best suited for your application. 2. Please take the necessary precautions in your system for fail-safe operation in case a failure occurs in a semiconductor product.
Reference item		

6.2 Preventing Electrostatic Discharge (ESD) Damage

Destructive defects are the most frequently occurring type of semiconductor device failure and it is very difficult to trace the cause of destruction from its aftermath. When the incidence of destruction is high, additional testing is conducted and specific measures are taken in an attempt to find the conditions that reproduce the same form of destruction, but in reality, it is extremely difficult to reproduce the forms of destruction that are exactly the same as those in the field.

This section, focusing on destruction mechanisms, summarizes the characteristics of destruction, and the approach to prevention and countermeasures. Correct, careful handling of sensitive semiconductor devices during production processes can be expected to have a large effect on the reduction of defects during both the clients' production processes and the period of initial failures in the field.

6.2.1 ESD Damage

Damage due to electrostatic discharge is the most frequently occurring mode of destruction defects. Following, we summarize the mechanisms that charge devices, the mechanism of damage and general precautions.

Damage of devices by electrostatic discharge is caused by sudden discharges resulting from excessive electrical voltages and excessive currents. Except for devices with extremely high frequencies, most devices have internal protective elements against static electricity. Damage of devices due to electrostatic discharge will still, however, occur when static electricity that exceeds the level of protection provided by the protective elements is applied to the device, or when a high-frequency surge exceeds the speed of the protective elements.

After a device has been installed on a circuit board or apparatus, from the concept of distributed-constant circuits, applied static electricity concentrates at the point of lowest impedance to become a stray current, and then causes destruction at the weakest point.

The semiconductor device itself is processed and manufactured at extremely high temperatures, so destruction will not result in a short time if the temperature rises. However, when energy consumed is intensely concentrated, the temperature rises locally and destruction occurs instantly. When the static electricity itself causes the destruction, the voltage is high and the amount of energy is comparatively low, so there is little sign of damage and, in many cases, it cannot be observed. If static electricity is applied when the electric power is on, the resulting electrostatic destruction will in some cases induce secondary thermal runaway and Area of Safe Operation (ASO) destruction.

(1) Mechanisms for the Generation of Static Electricity

Static electricity is the charging of a material by either excess or a shortage of electrons. When a material has an excess of electrons it is negatively charged, and when it has a shortage of electrons it is positively charged.

Materials generally have an electrical quality of either acquiring electrons or of giving them up (the series of frictional electrification). For this reason, when two materials rub, make contact, separate, or create friction, one material acquires electrons while the other gives them up (figure 6.1). When a conductive material comes into proximity with a charged material, local charging will occur because of electrostatic induction (figure 6.2). The amount of charge in the materials depends on the material properties, the surrounding conditions (temperature and humidity), and the conditions in terms of friction. However, large charges are generally generated in chemical fibers and plastics (these materials are easily charged). Since static electricity charges the surface of a material, the material's surface conductivity will also have a strong effect on charge transfer. When the surface conductivity is high, the charge will diffuse quickly. Table 6.7 shows examples of electrostatically generated voltages. Since surface conductivity increases with humidity, the higher the relative humidity the lower the electrostatic voltage.

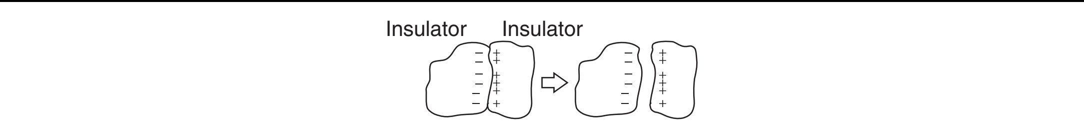


Figure 6.1 Frictional Electricity

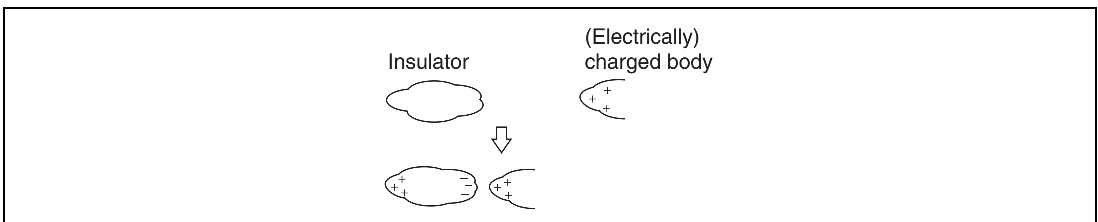


Figure 6.2 Electrostatic Induction

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Table 6.7 Examples of Typical Electrostatic Voltages

	Electrostatic Voltage Potential	
Source	**10 to 20%RH**	**65 to 90%RH**
A person walking on a carpet	35000 V	1500 V
A person walking on a vinyl floor	12000 V	250 V
A person working at a bench	6000 V	100 V
Vinyl covering	7000 V	600 V
Lifting a polythene bag from a bench	20000 V	1200 V
Polyurethane packed chair	18000 V	1500 V

(From DOD-HDBK-263)

(2) Charged-Device Model Mechanism

Recently the incidence of the ESD damage due to the charged-device model is increasing. This mode of destruction occurs when a charged device model discharges to a conductor. The device-charging mechanisms that induce discharges are described below.

(a) Frictional charging of package surfaces

Friction is often applied to a device in the manufacturing process or during assembly of devices into electronic instruments. Examples are friction with the rubber roller of the device-stamping machine, within the IC magazines, and device handling instruments. When friction is applied to plastic packages, the surface of the package becomes charged. When the package is charged, electric charge is electrostatically induced in the chip and its leads by electric fields within the package, and the leads discharge when they make contact with a conductor (figure 6.3).

(b) Device charging by electrostatic induction

In addition to description (a) above, figure 6.4 gives examples of charging that occurs even in the absence of friction. When a device is placed on a charged plastic board, electrostatic induction takes place in the chip and leads as shown in figure 6.4 (i). Then discharge occurs when tools or human bodies make contact with the leads of figure 6.4 (ii). If the device is charged, there is a further danger of discharge after it has been picked up from a board as shown in figure 6.4 (iii).

This shows that there is a danger of device discharge when charged materials are simply brought into proximity with each other. The containers into which devices or completed boards are placed, conveyor belts, and non-conductive gloves can all cause device discharge.

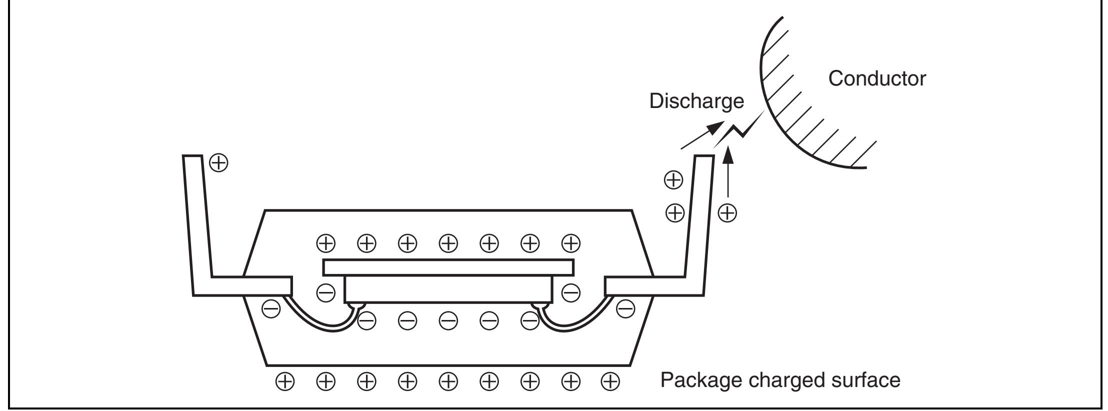

Figure 6.3 Internal Electrostatic Induction and Discharge when the Package Surface is Charged

Conductor (e.g. pliers)

Discharge

Charged plastic board

(i)

(ii)

After removal from the plastic board

(iii)

Figure 6.4 Process of Device Charging by Electrostatic Induction

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(3) General Precautions against ESD Damage

Caution is necessary in handling devices since they are generally susceptible to destruction due to electrostatic discharge. The possibility of electrostatic discharge is especially high in the cases listed below. Countermeasures, and confirmation of the conditions, are thus necessary to prevent destruction.

(a) Contact between devices and conductors

When conductors or devices are charged, discharge will occur between them. For the sake of protection, human bodies must be grounded through a high resistance of 1 MΩ or greater. For metals, the danger of destruction is greater because of the sharp discharges. Bringing devices into contact with metals must be avoided as much as possible, but, when this is unavoidable, the metal must be grounded and the charge must be removed from the devices.

(b) Device subjected to friction

Packages become charged when they are subjected to friction, and when the lead pins are rubbed, the chips and lead pins also become charged. It is necessary to reduce the amount of charge by preventing friction or changing the material that may be subjected to friction.

(c) When charged tools are brought into proximity with devices, the devices are charged by electrostatic induction. The material of tools must therefore be exchanged for anti-static material.

(d) Drops in the humidity of surroundings

When handling devices, if the humidity in the vicinity falls, devices or tools, once charged, do not easily return to their original condition. Since static electricity is invisible, it is not easy to institute perfect countermeasures to the above-mentioned factors (a)–(c). When executing these countermeasures, greater effectiveness can be expected if the humidity is also controlled.

(4) Caution in Handling Devices

The most effective method of preventing sharp discharge of semiconductor elements is to use anti-static mats. First of all, devices will not become charged, but, if they become charged then, they will not discharge sharply.

(a) The working environment

The occurrence of static electricity is closely related to humidity, and static electricity occurs more readily when the relative humidity drops. When there is a high-temperature area (in part of the working environment), the local level of humidity in that area will be low, and this leads to the possibility of large amounts of static electricity. Therefore, from the aspect of charge prevention, during handling and the mounting process when the possibility of charge is high, it is important to maintain a relative humidity of 45 to 55% by using humidifiers. When control of humidity is difficult, an air-ionizing blower (called an ionizer) is also effective. However, over dependence on the air-ionizing blower may lead to unexpected defects when failures do occur. It is more important to take other measures to prevent charging and at the same time continuously confirm the operation of the air-ionizing blower.

(b) Work

In the work place, easily charged insulators (especially chemical fiber and plastic products) must be avoided as much as possible, and conductive material should be used. For example, anti-static materials such as anti-static work gowns and the use of air-ionizing blowers are recommended. Also when handling semiconductor devices, it is necessary to use materials that prevent static electricity or provide anti-static containers (for example, electrostatic-shielded bags, anti-static mats, etc.) during storage or transportation.

1. Equipment and facilities

   Measuring and test equipment, conveyors, work platforms, floor mats, tools, solder baths and irons should all be thoroughly grounded to prevent electrostatic accumulation. Cover work benches and floors with grounded anti-static matting (10^5 Ω/□ to 10^9 Ω/□).

2. Human bodies

   Ground human bodies during work. However, to prevent electric shock, always include a 1 MΩ resistor or higher connected in series, and be sure not to touch high voltage parts. Always wear gloves and do not touch devices with bare hands. Gloves and work gowns must not be made of such easily charged materials as nylon. Shoes or sandals with a resistance of 1 MΩ to 100 MΩ are regarded as adequate, but such values may vary due to dirt, wear, and humidity.

3. Work methods

   For manual soldering, use a soldering iron for semiconductors (12 V to 24 V, i.e., low-voltage type), and ground the tip of the iron. In handling devices it is desirable to keep the frequency of handling and the time of handling a given device to a bare minimum, as working quickly can help to prevent destruction.

- Example 5

  ESD Damage during Measurement

No. 5	Example	ESD during measurement
Type of device		MOS IC (plastic encapsulation)
Point		Measure the amount of charge after exposure to friction and take countermeasures
Outline of example/ phenomenon/ cause		Because a plastic guide rail was used to feed the IC to an automatic measuring device, the IC's plastic materials became charged with static electricity as the IC slid along the guide rail. This charge was discharged at the measuring head (metal), and caused destruction of the IC's input circuit. This occurred at low levels of humidity, but not at high levels.
Countermeasures/ checking methods		1. Exchange the plastic guide rail for a metal one, to avoid the generation of electrostatic charge. 2. GND the guide rail. 3. If these measures do not sufficiently reduce the amount of charge, use an ionizing blower as well.
Reference item		

- Example 6

  ESD Damage during Storage and Transportation

No. 6	Example	ESD during storage and transportation
Type of device		MOS IC (Plastic encapsulation)
Point		Substances adjacent to the device must not be allowed to charge to high voltage.
Outline of example/ phenomenon/ cause		During the device production process the IC which was perfect after mounting onto the PCB and before assembly, becomes defective. When the PCBs were stacked for transportation or storage, charge in a capacitor facing the IC was discharged and caused destruction of the IC.
Countermeasures/ checking methods		1. Place insulators between the PCBs during transport. 2. Discharge the capacitor. 3. Separate the PCBs keeping some distance between them.
Reference item		

(5) Excess Voltage Destruction

Other than static electricity another cause of destruction is the application of excess voltage, commonly called excess voltage destruction. There are various causes and features of excess voltage generation, but generally the form of destruction is determined by the amount of discharged energy and the size of the energy consuming area. When the temperature of local areas of silicon (Si) exceed 200°C the leakage current is extremely high and permanent destruction results with a further increase in temperature. Physically, when the temperature rises above 500°C, fusion of the Al metallization or damage to the Si substrate occur. The damaged area is obviously related to the amount of surge energy involved in the destruction.

Excess voltage surge includes extraneous surges induced by the activity and the switching on/off of other devices, unexpected lightening, and circuit-induced surges due to the activity of the device itself. Surges also arise during measurement and testing, procedures which are unrelated to the normal activity of devices.

(6) Destruction due to External Surges

External surges are the most troublesome because incidence is generally extremely low, and investigating their causes or conducting simulation tests is difficult. To prevent the problem, it is necessary to record in detail the conditions of operation and the surroundings at the time trouble occurs.

- Example 7

  Destruction due to Voltage Surge

No. 7	Example	Destruction due to voltage surge
Type of device		CMOS analogue switch IC
Point		Confirm the IC tolerance to input surge.
Outline of example/ phenomenon/ cause		In a customer's system that collect analogue data, as the source of analogue signal is far away from the analogue/digital converter, an external surge was induced on the connecting line. A CMOS analogue switch with an excess voltage protection circuit was used on the analogue input, but the surge exceeded the breakdown voltage causing destruction. Several hundred meters CMOS analogue switch IC
Countermeasures/ checking methods		1. Isolation amplifier added to the input circuit. 2. Zener diode is added to the input circuit to absorb the surge.
Reference item		

(7) Precautions against Destruction by Self-generated Excess Voltage

Surge sometimes generates high voltages within circuits. This is the case when inductive load circuits are driven, such an applied surge is absorbed by the avalanche breakdown of transistors. In such a case, incorporate protective elements. When they are already installed, control the surge voltage and derate the energy to maintain reliability. Also by adding protective elements to the circuit derating, characteristics are checked.

When a capacitor with a large capacitance as the load is driven, excess voltage sometimes arise because of the inductive element of the load circuit.

- Example 8

  A Driven Inductance Load

No. 8	Example	A driven inductance load
Type of device		TTL IC
Point		Confirm the voltage and current waveform when the load circuit L is switched on and off.
Outline of example/ phenomenon/ cause		When an inductive load such as a relay is driven through a logical circuit, and when the current flowing into the coil in a relay is reversed, the resulting reverse voltage is not absorbed and the device will suffer electrical destruction. The situation is the same when transistors are used.
Countermeasures/ checking methods		1. Introduce a clamping diode. 2. Introduce a dumping circuit.
Reference item		

- Example 9

  Reactance Driven

No. 9 Example	Reactance driven
Type of device	TTL, CMOSIC
Point	Precautions against charging/discharging currents of capacitors
Outline of example/ phenomenon/cause	If a capacitor is connected to an IC output, a charging current flows as its level changes from low to high, and a discharging current flows as its level changes from high to low. In the former case, a current corresponding to I_{OS} flows. In the latter case, a voltage corresponding V_{OH} is applied to the V_{OL} level output current, causing destruction in the output transistor.
Countermeasures/ checking methods	1. Use a capacitor with a capacitance that is lower than the value. 2. Insert a resistor in series with the capacitor. 3. Design systems that do not use capacitive load.
Reference item	

- Example 10

  Destructive Defects due to Noise from the Power Supply to the LCD Driver

No. 10	Example	Destructive defects due to noise from the power supply to the LCD driver
Type of device		LCD-driver microcontroller
Points		1. Never reverse the voltage of the power supply to the LCD driver. 2. The voltage applied to the CMOS input must be between the value of the power supply and GND.
Outline of example/ phenomenon/ cause		An LCD driver which was used trouble-free at company A repeatedly failed, for unknown reasons, in product tests at company B. There was a big discrepancy between the fraction defectives of device types even of the same lot. The fraction defective also varied with the test pattern. By the failure analysis, the destruction of the power supply section is confirmed. Defect analysis confirmed that cause of destruction was a build-up of spiking noise in the power supply to the liquid crystal display due to a capacitor load, and the reversal of the potential difference across the power supply. A bypass capacitor was placed across the power-supply connection providing a reversed-voltage to synchronize with the noise. The destruction no longer recurred.
Countermeasures/ checking methods		1. In order to avoid, for even a moment, the reversal of the voltage applied to the power supply of a liquid-crystal display driver, use a capacitor with the same phase to eliminate the noise as described above. 2. Widen and shorten the wiring runs of the power-supply pattern, and under the most severe condition for the timing of changes in the column signal, use a high-speed operation probe to check the waveform for the presence of reversed voltages between the power-supply lines.
Reference item		

(8) Precautions against Excess Voltage Destruction during Measurement

When measuring semiconductor devices, it is necessary to apply the same considerations as applied to static electricity. In addition, particular care should also be taken with regard to the points listed below.

(a) Preventing destruction due to the power input sequence

If the power input sequence of semiconductor devices is faulty, device destruction may arise due to such phenomena as latchup. For a power supply which has the negative features of the electric current limitations, a voltage drop occurs due to a transient current, and as a result the device may malfunction depending on the combination of the device and characteristics. Refer to individual data books for details.

Even if the power input sequence for the test program is correct, the power input sequence may not proceed correctly due to a faulty connection between the device and the socket of the measuring instrument. The actual power input sequence may also be reversed due to a combination of the startup speeds of the power voltage and those of the input/output signal. Caution is needed.

- Example 11
  Destruction due to Mistiming of Power Input

No. 11	Example	Destruction due to mistiming of power input
Type of device		Linear IC
Point		Confirm whether the power input sequence is the same as the specifications.
Outline of example/ phenomenon/ cause		When switching the mode, a malfunction of unknown cause occurred. The IC that malfunctioned operates on two power supplies. Only power supply 1 is used in normal operation, while power supply 2 is designed to turn on and function when switching the mode. The relevant IC was designed in such a way that unless the output signal is muted (Mute) until power supply 2 rises to the high level (5 V), pulse noise occurs and excessive current flows. It was confirmed that these precautions for use had not been followed, and as a consequence the noise surrounding the power supplies caused the device to malfunction.
Countermeasures/ checking methods		Confirm and follow the precautions for use given in the catalog or specifications provided with the delivery documents. In the case that multiple power supplies are used, be especially sure to control the timing of each on/off event.
Reference item		

(b) Protection against voltage and current surges

Take care to ensure that surging voltages are not applied from testers during characteristic measurement, or use such countermeasures as adding clamping circuitry to the tester, or ensure that abnormal voltages are not applied due to faulty connections during current driving measurement.

- Example 12
  Destruction during Measurement

No. 12	Example	Destruction during measurement
Type of device		TTL IC
Point		Beware of voltage surges when power is applied.
Outline of example/ phenomena/ cause		1. When measuring the bus-driver output voltage V_{OL}, destruction occurred because the input current I_{OL} (100–300 mA) was kept constant. 2. When measuring the breakdown voltage (for an IC of 70 V or greater) with a current of 1 mA, the same destruction (as in (1) above) occurred. 3. When measuring the breakdown voltage (as in (2)), noise superimposed on the constant current source, entered the negative range and caused destruction.
Countermeasures/ checking methods		1. Use methods that apply voltages rather than currents. 2. Apply voltages, within the breakdown voltage and measure the current. 3. When a method that includes the application of a current must be used, it is effective to check the contacts in the previous sequence.
Reference item		

When capacitors are installed to prevent noise on input/output terminals and are connected carelessly, there is a chance that semiconductors will suffer electrical destruction because of peak currents that result from charging and discharging of the capacitor. For example, during intermediate inspections using board testers or in-circuit testers if the capacitor remains charged when the next board is tested, destruction of semiconductor devices may result. In cases where the capacitors on a board remain charged after a test, there is also a possibility of discharge later in the storage case, so all capacitors in the tester and on the board must be completely discharged. In the same manner, when a bypass capacitor with a large capacitance is inserted on the tester power supply, care must be taken to ensure that an unnecessary charge does not remain after the power supply is disconnected.

(c) Precautions against noise and oscillation

Normally, even in circuits that operate correctly, the load capacitance increases when devices are connected to oscilloscope probes or instruments for measurement. Noise or oscillation are generated and circuits malfunction, leading to the destruction of semiconductors. Therefore, caution is necessary.

(d) Prevention of conflict between semiconductor outputs and tester drivers

When measuring common I/O terminals, care is required so that the output of the semiconductor and tester do not conflict.

(e) Precautions against leakage from electrical equipment

Adequate control of electrical equipment is required so that leakage does not occur from AC power supplies to terminals of curve tracers, oscilloscopes, pulse generators, or stabilized DC power supply.

(f) General precautions

When measuring, avoid the misconnection of terminals, reverse insertion, and shorting between terminals. When checking board (substrate) operations, check that there are no solder bridges or particle bridges before switching the power on.

- Example 13
  Destruction during Measurement

No. 13	Example	Destruction during measurement
Type of device		Small Surface Mount IC
Point		Beware of contact defects when taking measurements
Outline of example/ phenomenon/cause		When the semiconductor device to be measured was inserted into the tester socket at an angle, a spike surge occurred due to contact defects between the pins of the device and the tester socket, resulting in destruction of the IC.
Countermeasures/ checking methods		Place the contact check for the very beginning of the testing program. When contact defects are detected, the inspection should be discontinued. In the case of reverse insertion, the inspection should also be halted.
Reference item		

- Example 14

  Destruction due to Faulty Connections

No. 14	Example	Destruction due to faulty connections
Type of device		Linear IC
Point		Ensure correct connection and clarify emergency measures against faulty connections.
Outline of example/ phenomenon/ cause		When installing a set, the GND line was open and the V_{CC} connected, an IC failed due to a contact between its output terminals and GND. The moment the output terminals made contact with GND, high currents were drawn through an electrolytic capacitor between V_{CC} and GND, causing destruction.
Countermeasure/ checking method		Place a clamping diode between the output terminals and GND.
Reference item		

- Example 15

  Destruction due to the Removal and Insertion of a Connector

No. 15	Example	Destruction defects due to the removal and insertion of a connector
Type of device		IC, LSI
Point		The removal and insertion of live connectors is strictly prohibited. If this cannot be avoided, the design must allow for this possibility.
Outline of example/ phenomenon/ cause		In user processing, failures occurred frequently so that a motor did not run (average failure rate was 2 to 5%). Examination revealed that IC inputs had been destroyed. During board inspection, the customer erroneously removed and inserted the connector while the DC supply was switched on. When this procedure was discontinued, the defects did not recur.
Countermeasures/ checking methods		1. Always disconnect the power supply before connecting the board. 2. Protective resistors were inserted at the input terminals of the destroyed IC.
Reference item		

6.2.2 Latchup

In devices in which the structures have a parasitic thyristor, such as CMOS circuitry, a failure mode called latchup often occurs. Latchup is a phenomenon in which parasitic currents that flow because of an external surge act as a trigger and switch the parasitic thyristor on. This leads to heat-induced destruction. Such parasitic currents don't flow as long as the potential on each signal line of the LSI is within the standard values. However, when the ground potential is floating, and the potential between the input/output signal and the power supply is reversed, the current flows. As the thyristor itself acts as a normal semiconductor element, if the power supply is cut before the structure breaks down because of heat, this does not lead to destruction. Once the thyristor has been turned on, unless the power is cut the problem can not be resolved, even if the input/output voltage returns to normal.

- Example 16

  Destruction due to Latchup of LSI with Multiple Power Supplies

No. 16	Example	Destruction due to latchup of LSI with multiple power supplies
Type of device		CMOS LSI
Point		If the proper sequence for the application of power is not followed, latchup will result.
Outline of example/ phenomenon/ cause		After an LSI that had passed the acceptance inspection had been mounted on a printed board, the LSI suffered destruction during examination by an in-circuit tester. Normally, connections are made first and tests are carried out after adjusting the voltage in the –5 V generating circuit. In this case, however, the test was erroneously performed without the connection being made first. Consequently, –5 V was not being supplied to the LSI, latchup arose, an abnormal current flowed to ground, and the LSI suffered destruction. When using CMOS devices, assume the worst so that even if latchup does occur, the circuit is made fail-safe in terms of prevention of secondary damage, and protective resistors installed to limit self-generated heat. –5 V is lost due to failure and the LSI on the right causes latchup. T +5 V +12 V Power supply –5 V generating circuit LSI –5 V +5 V +12 V GND Printed circuit board
Type of device		CMOS LSI
Countermeasures/ checking methods		1. Define the proper sequence for supplying and cutting power with multiple power supplies LSI. 2. Insert protective elements in anticipation latchup occurring.
Reference item		

(1) Destruction Induced by Excess Current

Destruction that occurs because of Al metallization meltdown is generically referred to as excess current destruction. Al wiring has a positive temperature characteristic so its resistance is increased by the application of large currents. As a result, more energy is consumed in the wiring causing thermal runaway, the Al wiring exceeds Al-Si eutectic temperature and melts down. Transistors suffer destruction from excess current, also there are cases of a large current flow and generating excess current destruction. Alternatively, excess current causes the temperature to rise and as a result a eutectic mixture of Al and Si breaks through a junction and transistors are destroyed. It is difficult to determine the cause of the destruction from the resulting condition of the device.

- Example 17

  Destruction due to Large-Capacitance Capacitor

No. 17	Example	Destruction due to large-capacitance capacitor
Type of device		CMOS LSI
Point		If the GND does not function properly, the LSI will suffer destruction.
Outline of example/ phenomenon/ cause		During the debugging of programs, program development equipment was destroyed for unknown reasons. Regardless of how many times equipment was repeatedly replaced, several TTL and CMOS devices continued to be destroyed at the same time. It was determined that latchup occurred because a large-capacitance capacitor (2000 µF) was used and when the power was turned on, the LSI's ground potential rose to half of the power-supply level. Due to surge voltage, the wiring between the GND and the power supply becomes a resistor, and the GND voltage increases. Destroyed Potential of 1/2 the power supply LSI 2000 µF Input GND Low level (0.4 V approx.) LSI Output In the case of two power supplies GND: 2.5 V approx. Input: 0.4 V approx. Relative electrical potential is reversed.
Countermeasure/ checking method		Exchange the large-capacitance capacitors on printed-circuit boards for smaller-capacitance capacitors.
Reference item		

(2) Thermal Runaway

Thermal runaway is a thermal characteristic of any circuit where the positive feedback of power results in the temperature rising without limit until destruction occurs. It is no exaggeration to say that thermal runaway is the most common form of destruction. In addition to those cases where thermal runaway occurs because of local heating of a device, high-power devices have an additional risk of thermal runaway because of their structurally inadequate thermal dissipation. Caution must therefore be exercised in terms of heat-radiation (thermal management) design.

(3) ASO Destruction

ASO stands for Area of Safe Operation, and this is a destruction mode that typically occurs in bipolar devices. This is another kind of thermal runaway. In theory, due to the temperature characteristic of the base emitter voltage, when the temperature increases, the voltage V_{BE} falls, and the consumption of energy at the emitter increases locally. Further, as V_{BE} falls, local hot spots occur which lead to destruction.

In the case of a MOS device, since the ON resistance rises with temperature, one characteristic is the tendency to automatically equalize the generation of heat, this then greatly expands the area of possible ASO destruction.

(4) Destructive Avalanche

This is a failure mode which initiates an avalanche breakdown which in turn causes destruction due to the applied voltage exceeding the junction breakdown voltage of a semiconductor device. As with the time-dependent breakdown of dielectric film, when the yield energy is small, immediate destruction does not occur. It can be considered that the destruction occurs when the amount of energy passing through the junction exceeds a fixed value. Except in designs where it is specifically intended, using avalanche breakdown is prohibited by maximum ratings and other specifications, care is required.

6.3 Preventing Mechanical Damage

Semiconductor devices are mainly made up of a silicon chip which forms its core to perform its functions, bonding wires to carry electrical signals to and from the chip, lead wires, heat fins to reliably radiate heat away, and mold resin to hold the whole package together mechanically and protect it from external stresses. Since the constituent elements of the device differ considerably in such properties as hardness and thermal expansion coefficient, the mechanical strength margin is less than it would be for a device consisting of a single material. Consequently, all of the stages in mounting components—bending the lead wires, attachment to the heat-sink plate, cleaning after mounting to the printed circuit board, correcting the bending—harbor the potential for mechanical breakage.

External mechanical forces can loosen the adhesive bonding of the resin to the leadframe, and cause the subsequent deterioration of the margin for moisture resistance; transmission of the stress to the bonding wires can cause deterioration of resistivity to temperature cycles; and in a severe case wires can be disconnected. In addition, mechanical stresses applied to the heat-sink plate and to the whole package can lead to chip cracks.

In the assembly process, caution should be exercised when mechanical stress is applied, and the process should be designed so as not to permit defects caused by mechanical stresses. If it appears that destruction will be caused by mechanical stress during the assembly process, it is possible that some damage will be caused not only to the actual defective components but also to components that do not qualify as defective. In this case the product might become defective in the market, so caution is required.

In particular, in a type of product which is of hollow structure and bonding wires are not fixed in place, there is danger of breakage caused by ultrasonic cleaning and vibration stress. There is danger that narrow bonding wires will be disconnected by fatigue caused by resonance with ultrasonic waves, and that wire disconnection will be caused by vibration and flow of gel resin.

6.3.1 Lead Forming and Cutting

When semiconductor devices are mounted on a printed circuit board, there are cases in which outer leads are formed and/or cut in advance; if excessive force is applied to a lead during this operation, the semiconductor device can be broken or the seal can be damaged.

For example, if relative stress is applied between the package body and the leads of the device, an internal connection could be loosen or a gap could be produced between the package body and the lead, deteriorating airtightness and causing loss of reliability. In the worst case, the mold resin or glass could break. For this reason, the following precautions should be observed when lead forming or cutting lead wires.

1. When a lead is bent, fix the lead in place between the bending point and the package body so that relative stress will not be applied between the package body and the lead. Do not touch or hold the package body when bending a lead (see figure 6.5). When a lead forming die is used to perform lead forming for many devices, provide a mechanism of holding the outer lead in place and make sure that this outer lead pressing mechanism itself does not apply stress to the device body (see figure 6.6).

   Further, if the package body pressing mechanism is used when bending the lead, this method should support the package body around its periphery as shown in figure 6.7 to avoid concentrating stress on the chip. *t* is the distance between the lead forming support point and the chip.

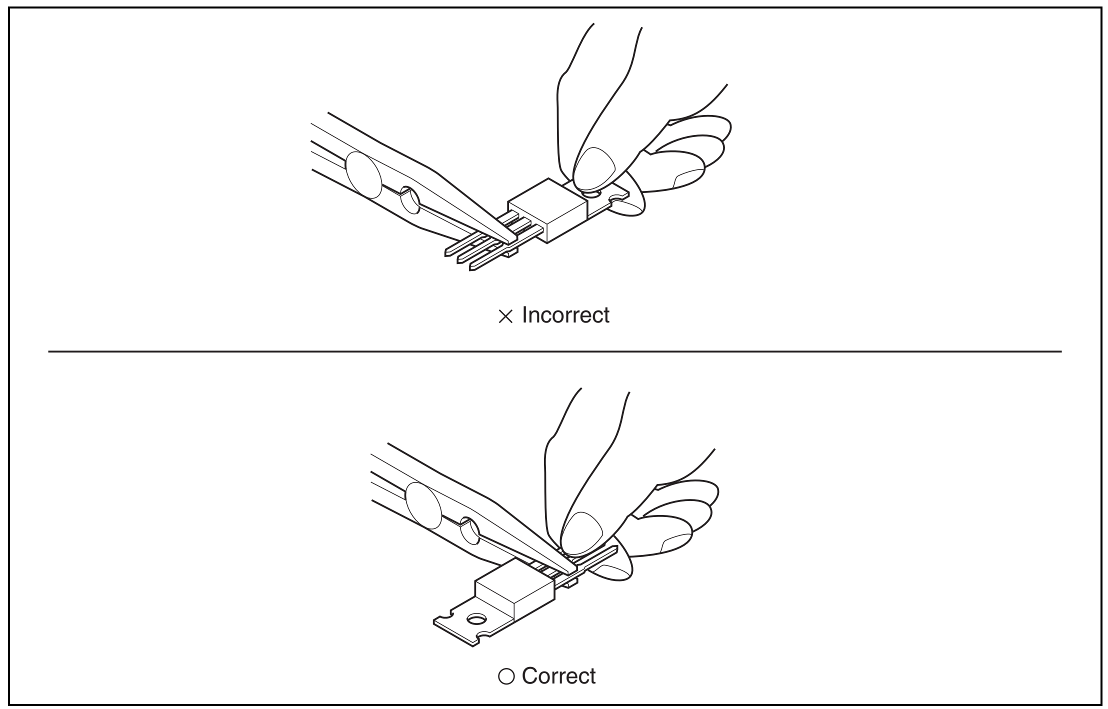


Figure 6.5 How to Bent Package Leads with Handling

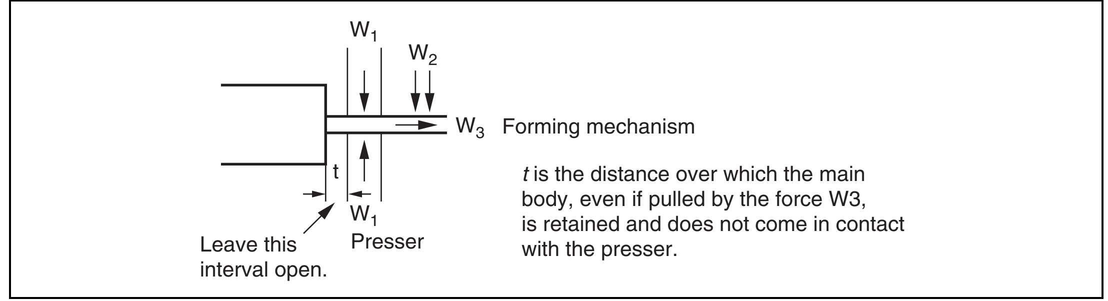


Figure 6.6 Using the Lead Forming Die

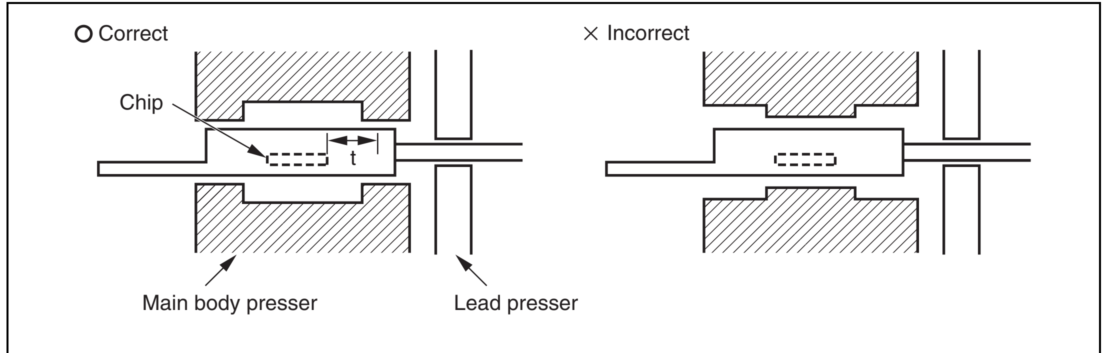


Figure 6.7 Example of the Lead Forming Die with the Package Body Presser

2. When the lead is bent to a right angle, it must be bent at a location at least 3 mm from the package body. Do not bend the outer lead more than 90 degrees (see figure 6.8A). When bending the lead less than 90 degrees, bend it at a location at least 1.5 mm from the package body (see figure 6.8B).

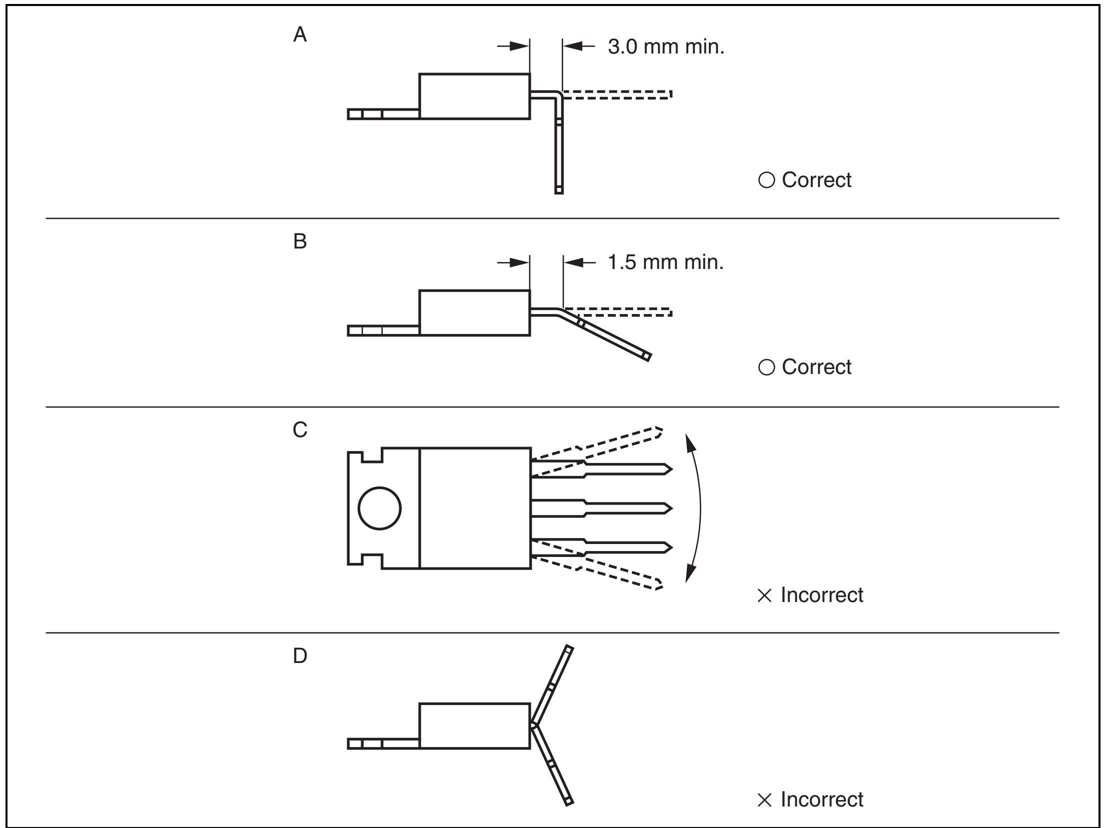


Figure 6.8 Locations and Directions for the Lead Forming of the Outer Lead

3. Do not bend a lead more than once.
4. Do not bend a lead in the side direction (see figure 6.8C).
5. A lead of a device can be broken by excessive stress (such as tension) in the axial direction, so do not apply more than the prescribed force. The prescribed stress will vary depending on the cross-sectional area of a lead.
6. Depending on the shape of the bending jig or tool, the plated surface of an outer lead can be damaged, so exercise caution. If the section that a lead contacts is on the order of 0.5 mmR, there is no problem.

Transistor and diode products can be supplied with preformed leads on request. If desired, please contact our company's sales representative.

- Example 18

  A Chip Crack Defect

No. 18	Example	A chip crack that formed during lead formation.
Type of device		Gate array
Point		When forming a lead on a surface-mounted package, check whether a mechanical shock is being applied to the package body.
Outline of example/ phenomenon/ cause		In a user's process, the leads of a surface-mounted package device were corrected before being placed on a circuit board using a lead correction machine. At this time, the clearance between the forming die pressing on the base of the lead and the package body was not left. For this reason, particles entered between the package body and the forming die and applied a stress, as a result of which a chip crack occurred.
Countermeasure/ Method of checking		Set the clearance between the package body and the forming die considering the size of specks of particles.
Reference item		

- Example 19

  Damage Caused by a Lead Forming Defect

No. 19	Example	Wire break caused by a lead formation defect
Type of device		Power transistor (Type TO-202)
Point		A lead must be held securely.
Outline of example/ phenomenon/ cause		When a transistor lead was formed, a lead presser was not used, so a disconnection defect was caused by loosening a pin. Since the pressing was insufficient, excessive tension was applied in the X direction and an internal bonding wire was disconnected when the lead wire was bent. Presser × Lead wire Transistor Bending Presser
Countermeasure/ Method of checking		When a lead forming, fix it in place between the main body of a transistor and the point where the lead wire is bent (see figure above).
Reference item		Precautions when bending (section 6.3.1)

6.3.2 Mounting on a Printed Circuit Board

When a semiconductor device is mounted on a printed circuit board, be careful so that excessive stress is not applied to the leads of the device.

The following are the principal precautions that need to be taken (see figure 6.9).

1. The intervals between device mounting holes on the printed circuit board should match the distance between outer lead so that excessive stress is not applied while the device is being inserted or after it is inserted.
2. When a device is inserted into a printed circuit board, do not pull on the leads with excessive force from the backside, and prevent excessive stress from being applied between the leads and the case.
3. Leave a suitable space between the semiconductor device and the circuit board. A good way to do this is to use a spacer.
4. After fixing the device to the printed circuit board, avoid assembling the unit in such a way that stress will be applied between the leads and the device package. For example, when a device is connected to the heat-sink plate after soldering the leads to the printed circuit board, fluctuations due to tolerances in lead length and printed circuit board dimensions can result in stress being concentrated on the lead. This results in the lead being pulled out, package damage or a lead becoming disconnected. For this situation, solder the lead after device is fixed in place.
5. When using automatic insertion equipment, one should be especially careful so that mechanical shock is not applied to the package body at the time of insertion. This will help prevent cracks from forming in the package or the chip due to shock. Also, when automatic forming equipment is used, one should observe the precautions given in section 6.3.1.
6. When the component is mounted in an IC socket and used under severe environmental conditions, the contact between the IC pins and the IC socket may degrade. One should avoid using an IC socket as much as possible. Also, when an IC socket is used to mount a multi-pin grid array package device to a circuit board, the package can break or pins may bend when the package is inserted or removed. Therefore it is strongly recommended that a commercially available insertion/removal tool be used. One of the Orgat TX8136 series is a good choice for an insertion and removal tool.

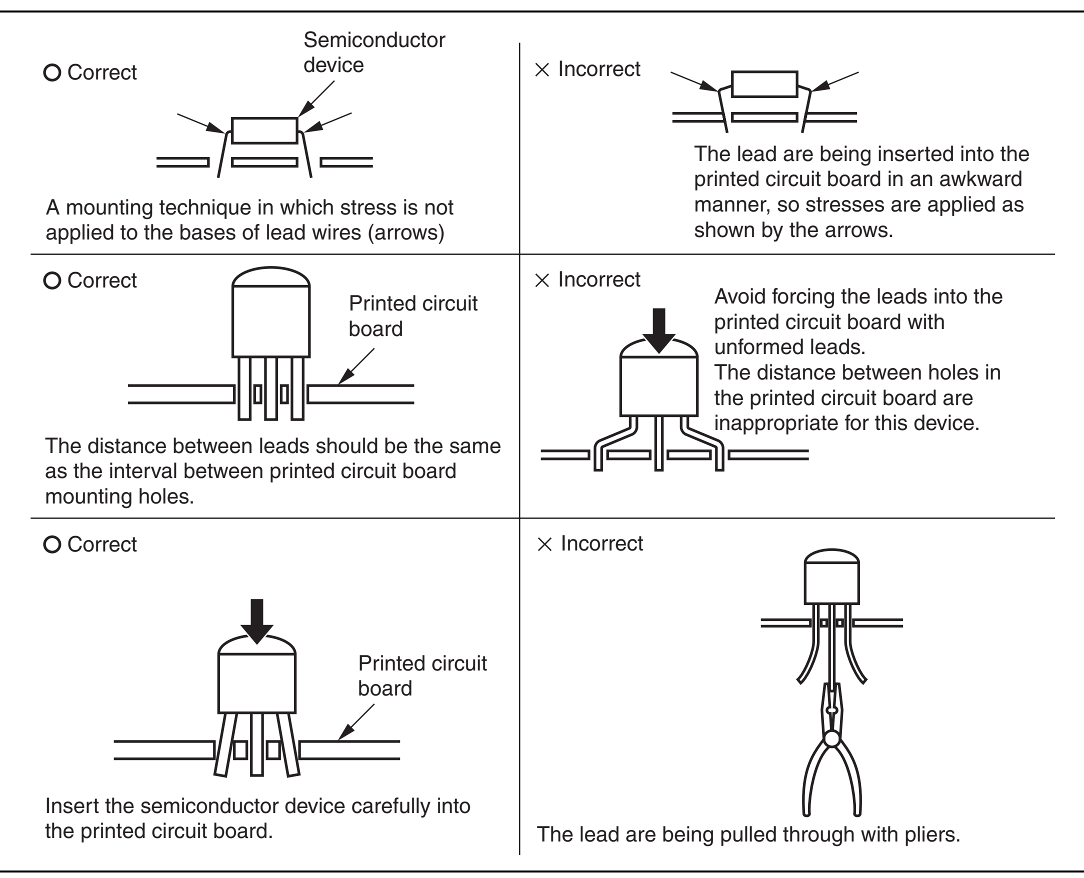


Figure 6.9 Methods of Mounting a Semiconductor Device on a Printed Circuit Board

- Example 20

  Damage of a Package by Automatic Insertion

No. 20	Example	Destruction of a package by automatic insertion
Type of device		Silicon diode (DHD type)
Point		Stress must not be applied to the main body of a device while a lead is being bent.
Outline of example/ phenomenon/ cause		In automatic insertion of a DHD type diode into a printed circuit board by a high-speed insertion machine, the package glass was broken either by excessive pressure on the device main body or by excessive force used to clinch leads on the rear side of the circuit board. Presser / Lead wire / Package glass / Printed circuit board / Lead clinching mechanism
Countermeasures/ Methods of checking		1. Adjust the position of the presser. Make the presser material that can provide a buffer against shock. 2. Keep the lead clinching force to a minimum.
Reference item		

- Example 21

  Solder Defect Caused by Warping of a Printed Circuit Board

No. 21	Example	Solder defect caused by warping of printed circuit board
Type of device		Microcontroller
Point		Be careful in correcting the warp of a circuit board by reflow.
Outline of example/ phenomenon/ cause		A defect involving the peeling off of solder under a surface-mounting reflow stress occurred. No matter how many times a solderability test was performed, no abnormality was detected, and the cause could not be determined. In the course of discussions the subject of warping following reflow was raised; examination of the circuit board involved showed that asymmetry of the copper pattern that positions the components was the cause and that the warping was abnormally large. It was judged that after reflow, while the circuit board was still hot, mechanical stress was applied to correct the warping. In reflow, the assembly stress on surface mounted devices can be quite large. These can develop into high stresses on the printed circuit board. If the circuit board undergoes large warping at the assembly stage which it is heated, even if the LSIs initially become bonded to the circuit board, they can become loose later. The user must keep control over the allowed amount of warping.
Countermeasures/ Methods of checking		1. The circuit board pattern and the component layout are adjusted to prevent warping. 2. The frame material is changed to increase the mechanical strength per pin with respect to the circuit board.
Reference item		

- Example 22

  Chip Cracking at the Time of Mounting a Component on a Circuit Board

No. 22	Example	Chip cracking at the time of mounting a component on a circuit board
Type of device		Power transistor (DPAK), Small-signal transistor (UPAK)
Point		It is necessary to determine if the exterior coating resin affects the stress on the device.
Outline of example/ phenomenon/ cause		When an exterior-coating resin was used in mounting a component on a circuit board, the difference in thermal expansion coefficients between the epoxy resin in the device and the phenol resin used for the coating caused an excessive stress to be applied to the inside of the element, ultimately leading to formation of a chip crack. Use of such a coating can adversely affect the device, depending on the coating material and thickness. Use caution in such cases.
Countermeasure/ Method of checking		When using an exterior-coating resin, apply a stress-absorbing resin between the coating resin and the epoxy resin in the device.
Reference item		

6.3.3 Flux Cleaning Methods

Flux residue remaining after soldering may affect the components and circuit board wiring reliability, so as a general rule the flux must be removed. Cleaning methods include ultrasonic cleaning, immersion cleaning, spray cleaning and steam cleaning. These have the following respective characteristics.

(1) Ultrasonic Cleaning

The product is immersed in a solvent and ultrasonic vibrations applied. This method is suitable for cleaning inside minute cracks, but in some cases can cause damage to the connections between components and the circuit board, so caution is necessary.

(2) Immersion Cleaning

The product is cleaned by immersion in a cleaning fluid. It is necessary for the cleaning fluid to have high purity.

(3) Spray Cleaning

A solvent is sprayed on the product under high pressure. When the clearance between components and the circuit board is small, the cleaning effectiveness can be increased by spraying at an angle.

(4) Steam Cleaning

A vaporized solvent is used for cleaning. This permits cleaning to be done with a solvent that does not contain impurities, so it is often used in the final cleaning step.

Normally a combination of these methods is used. The normal flow of cleaning is shown in figure 6.10.

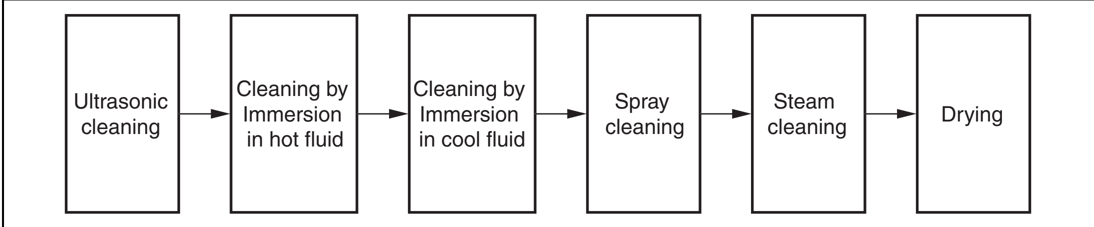


Figure 6.10 Normal Flow of Cleaning

One must pay attention to the following points when cleaning.

1. One example of the conditions under which ultrasonic cleaning is performed is given below, but to prevent damage to the device, caution is needed regarding the applied frequency, power (especially the peak power), time, and preventing the device from resonating.
   - Frequency: 28 to 29 kHz (the device must not resonate).
   - Ultrasonic output: 15 W/liter (one time)
   - Time: 30 seconds or less
   - The device and the printed circuit board must not directly contact the vibration source. In particular, ceramic package type QFNs (LCC) and QFPs (Ceramic) are cavity packages; when subjected to ultrasonic cleaning the connecting wires can resonate under certain conditions and become open or disconnected.
2. When cleaning is continued for a long time, the marking may be erased, so check the conditions that will be used by running an actual test before committing large amount of products.
3. When a solvent is used, public standards for the environment and safety must be observed.
4. It is recommended that the MIL standards summarized in table 6.8 be applied for the degree of printed circuit board cleanliness.

Table 6.8 Cleanliness Standards of a Printed Circuit Board

Item	Standard
Residual Amount of Cl	1 μg/cm^2 or less
Electrical Resistance of Extraction Solvent (after extraction)	2×10^6 Ω • cm or more

Notes: 1. Circuit board area: Both sides of printed circuit board + mounted components
2. Extraction solvent: Isopropyl alcohol (75vol%) + H_2O (25vol%) (before extraction) (electrical resistance of extraction solvent must be 6×10^6 Ω • cm or more).
3. Extraction method: Clean both surfaces of circuit board (for 1 minute or more) with at least 10 ml/2.54 × 2.54 cm^2 of solvent.
4. Measurement of electrical resistance of extraction solvent: With electrical conductivity meter

For details of the MIL standards, see MIL-P-28809A.

- Example 23

  Destruction by Ultrasonic Cleaning

No. 23	Example	Trouble in ultrasonic cleaning
Type of device		Ceramic package
Point		When cleaning a package with a cavity by ultrasonic, it is necessary to carefully monitor the power.
Outline of example/ phenomenon/ cause		After a ceramic package device was assembled, it was cleaned ultrasonically; the bonding wires resonated with the ultrasonic vibrations. The bonding wires suffered fatigue and become disconnected in a short time.
Countermeasure/ Method of checking		Specify a frequency, output and time at which resonance will not occur.
Reference item		

- Example 24

  Problem that Occurred when a Circuit Board was not Cleaned

No. 24	Example	Problem that occurred when a circuit board was not cleaned
Type of device		Linear IC
Point		Be careful of minute leaks.
Outline of example/ phenomenon/ cause		When components were soldered to a circuit board, flux adhered to the surface of the IC package; subsequently, flux that remained on the surface of the IC package absorbed moisture, the surface leakage current between IC terminals increased, and the circuit board became defective.
Countermeasure/ Method of checking		After a circuit board is soldered, the flux should be cleaned off.
Reference item		

6.3.4 Attachment of the Heat-Sink Plate

In a power device, a heat-sink plate can be used to radiate heat that is produced and thus lower the junction temperature. Attaching a semiconductor device to a heat-sink plate is an effective method of removing heat. To avoid loss of reliability, it is necessary to take the following precautions.

(1) The Selection of Silicone Grease

To improve heat conduction between the device and the heat-sink plate and increase the heat-sink effectiveness, silicone grease is uniformly applied in a thin uniform layer to the surface of the device that contacts the heat-sink plate. Depending on the device, in some cases the device can absorb oil from the silicone grease causing the chip coating material to swell. When selecting a silicone grease, we recommend the use of G746 made by Shin-Etsu Chemical co. Ltd., or equivalent. This grease has been formulated with an oil base that has low affinity for the package resin so that it will not cause the coating material to swell. Of course, an equivalent product may be used (however it is not necessary when using a metal can package).

If a different type of grease is used, it may not be possible to guarantee product quality. Use of a hard grease can cause resin cracking when a screw is tightened, so use caution. One should avoid applying more grease than necessary, since it can cause excessive stress.

(2) Use suitable torque when tightening.

If the applied torque is too low, the thermal resistance will increase, while if it is too high the device can deform. This can cause chip damage and lead to breakage. Use only appropriate torque to tighten within the limits given in table 6.9. The effect on thermal resistance between the thickness of insulating material and tightening torque is given in figures 6.11 and 6.12.

Table 6.9 Optimum Tightening Torque for Representative Packages

Package	Optimum Tightening Torque [kg • cm]
TO-3	6 to 10
TO-66	6 to 10
TO-3P	6 to 8
TO-3PFM	4 to 6
TO-220	4 to 6
TO-220FM	4 to 6
TO-126	4 to 6
TO-202	4 to 6
Power IC	4 to 8

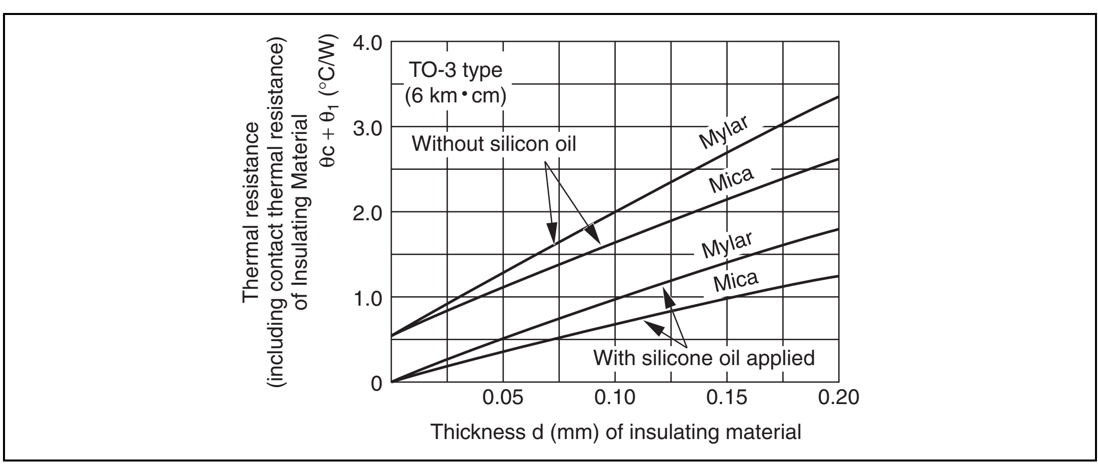


Figure 6.11 Relations between Thickness and Thermal Resistance of Insulating Material (Typical Examples)

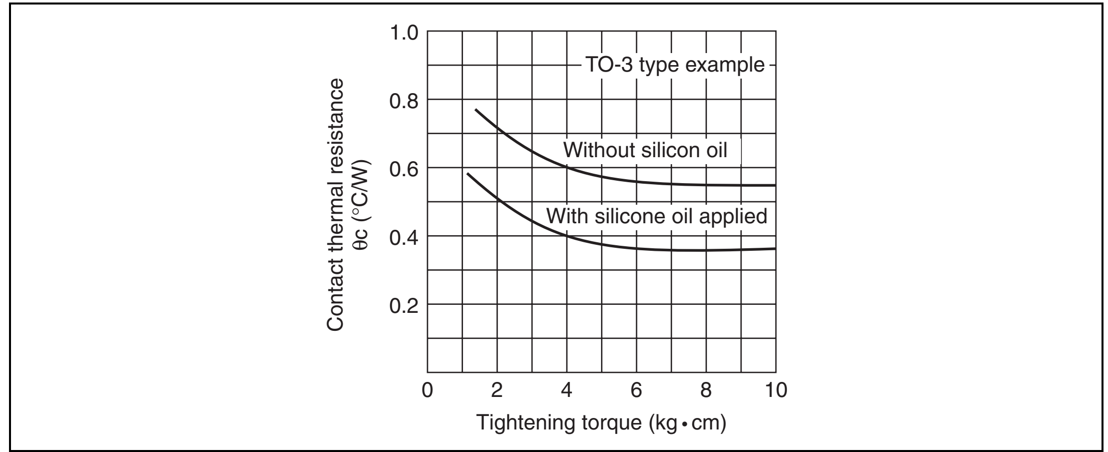


Figure 6.12 Relations between Tightening Torque and Contact Thermal Resistance

(3) Give adequate consideration to the flatness of the heat-sink plate.

If the heat-sink plate is not properly attached to the device, it will not effectively radiate heat away and can cause excessive stress. This can lead to deterioration of characteristics and package to resin cracks. Consequently, the following precautions should be observed with the heat-sink plate.

1. Neither concave nor convex warping of the heat-sink plate should exceed 0.05 mm in a horizontal distance between screw holes (figures 6.13 and 6.14). Also, the twist should not exceed 0.05 mm.

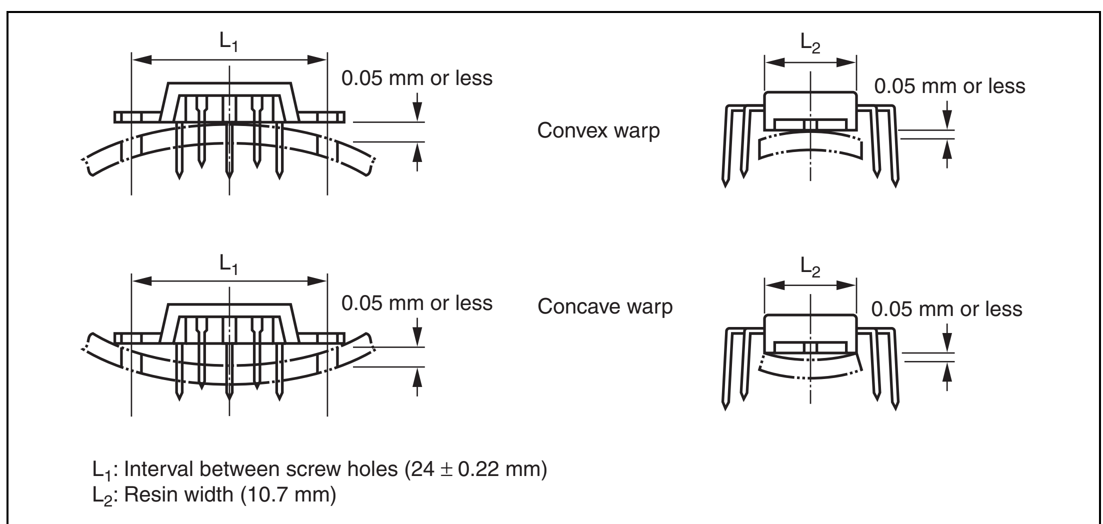


Figure 6.13 Warping of a Heat-Sink Plate—Examples of QIL and DIL Packages

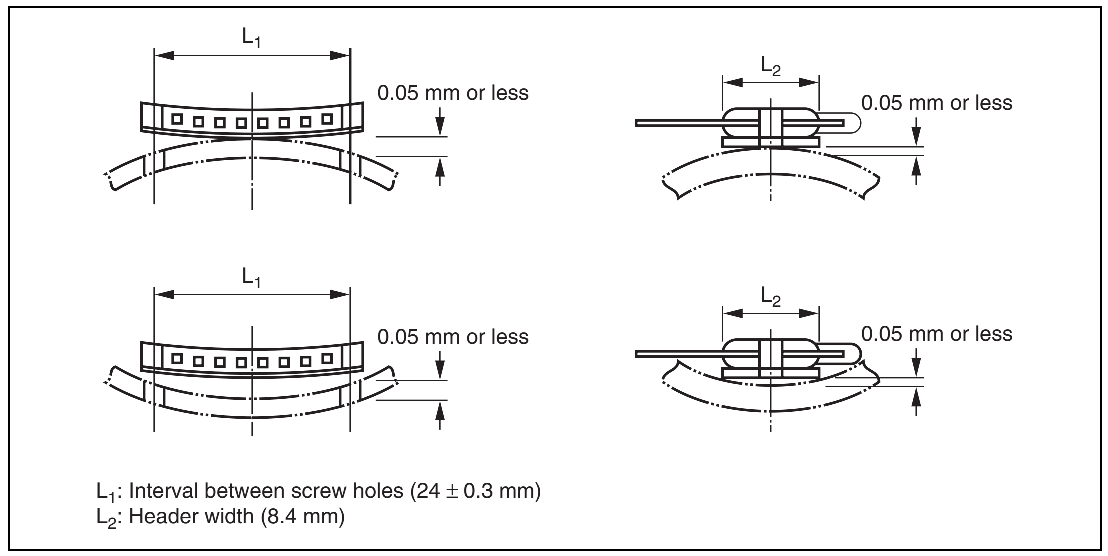


Figure 6.14 Warping of a Heat-Sink Plate—Example of an SIL Package

RENESAS

2. For the case of aluminum, copper or iron plates, verify that there are no residual burrs, and always chamfer the screw holes.
3. It is necessary to polish the surface that will contact the device until it is quite flat (▽▽ finishing).
4. Make certain there are no particles such as cutting filings caught in the space between the IC header and the heat-sink plate.
5. Design the distance between screw holes to be the same as the interval between device screw holes (for example in the case of a SP-10T type power IC, 24 ± 0.3 mm). An interval that is either too wide or too narrow can cause resin cracking.

(4) Do not solder anything directly to the device heat radiation plate.

If something were soldered directly to the device heat radiation plate, a great deal of thermal energy would be applied causing the device junction temperature to greatly exceed the temperature at which operation is guaranteed. This would seriously affect the device, shortening its lifetime or even destroying it.

(5) Do not apply mechanical stress to the package.

When tightening, if the tool used (screwdriver, jig, etc.) hits the plastic package directly, not only can cracks be produced in the package but the mechanical stress can be transmitted to the inside, accelerating fatigue of the device connection section and destroying the device or causing wire damage. One must always use caution not to apply mechanical stress.

(6) Do not attach any device to a heat-sink plate after lead wires are soldered.

If a device is attached to a heat-sink plate after leads are soldered to the printed circuit board, dispersions in lead length and differences in the dimensions of printed circuit boards and heat-sink plates can lead to excessive stress being concentrated in the leads. This can cause lead wires to be pulled out, packages to be destroyed and wires to be disconnected. Consequently, the device should be attached to the heat-sink plate first, and then the outer leads soldered.

(7) Do not mechanically process or deform a device heat-sink plate or package.

If a device heat-sink plate is cut or deformed, or a package is mechanically processed or deformed, the thermal resistance will be increased and abnormal stress applied to the interior of the device, causing failures to occur.

(8) When attaching a power device, use the recommended components (spacer, washer, lug terminal, screws, nuts, etc.) (see figure 6.15).

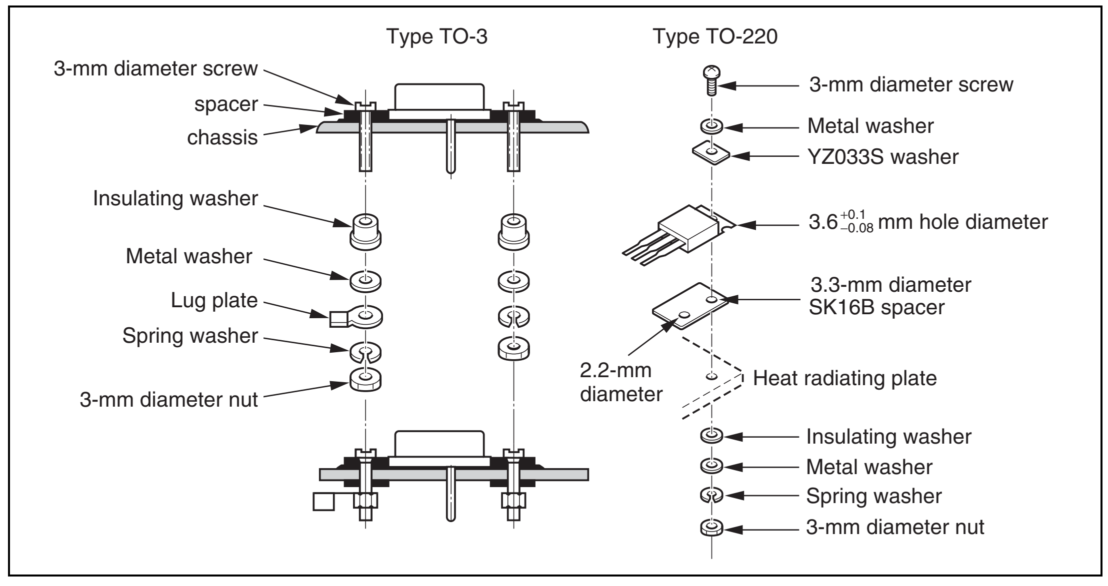


Figure 6.15 Example for Attaching a Power Transistor

(9) Screws that are Used

The screws that are used to attach the device to the heat-sink plate can be classified into cap screws and self tapping screws; the following precautions are needed in using these.

1. Use binding-cap screws conforming to the JIS-B1101 standard and screws that have heads equivalent to truss cap screws.
2. Absolutely do not use any flat-head screws since they will apply excessive stress to the device (figure 6.16).

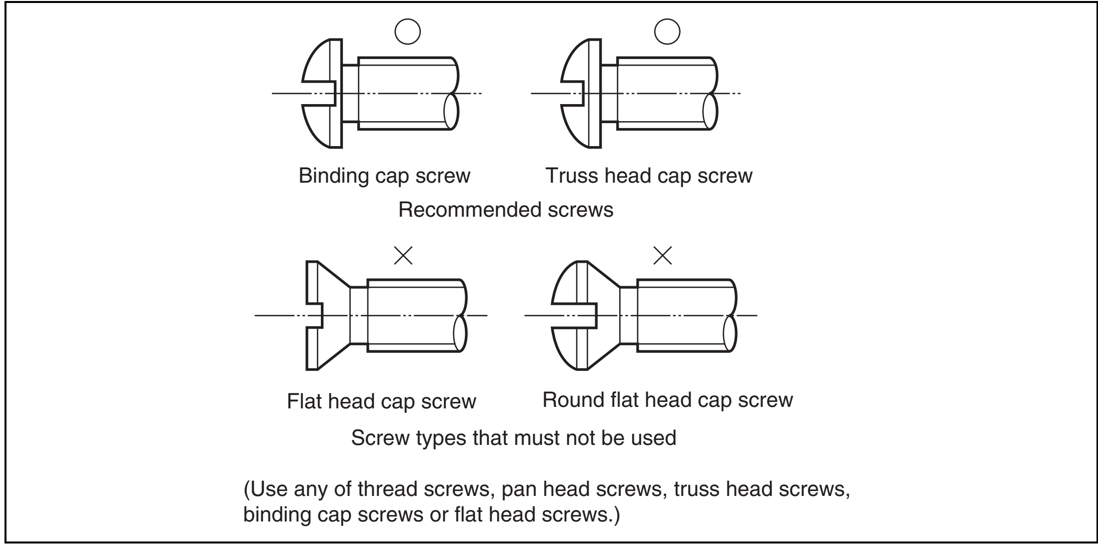


Figure 6.16 Types of Screws to be Recommended and not be Used

3. When self tapping screws are used, adhere strictly to the tightening torque given above.
4. When using self tapping screws, do not use screws that are larger than the hole diameter in the device attachment section. These screws tap not only the heat-sink plate but also the device attachment holes, which can cause trouble.

(10) Heat-Sink Plate Screw Hole Diameter

1. If the hole is too large: Do not make the heat-sink plate hole diameter or chamfering larger than the head diameter of the screws to be used. In particular, in a device that uses copper plating as the flange material (TO-220, power IC, etc.), the tightening torque can cause deformation of the copper plating and the plastic package.
2. If the hole is too small: In particular, if a self tapping screw is used, the tightening torque will increase and exceed the recommended tightening torque that was discussed above, or else the desired contact resistance will not be obtained.

(11) Other Precautions and Recommendations in Attaching Components to the Heat-Sink Plate

1. If two or more devices are attached to one heat-sink plate, the thermal resistance for each will increase (see figure 6.17).
2. The heat-sink plate must be of suitable size and shape for radiating heat away. In addition, forced air cooling must be provided as necessary. Measure the product case temperature under actual use conditions, calculate the junction temperature using the published thermal resistance value.

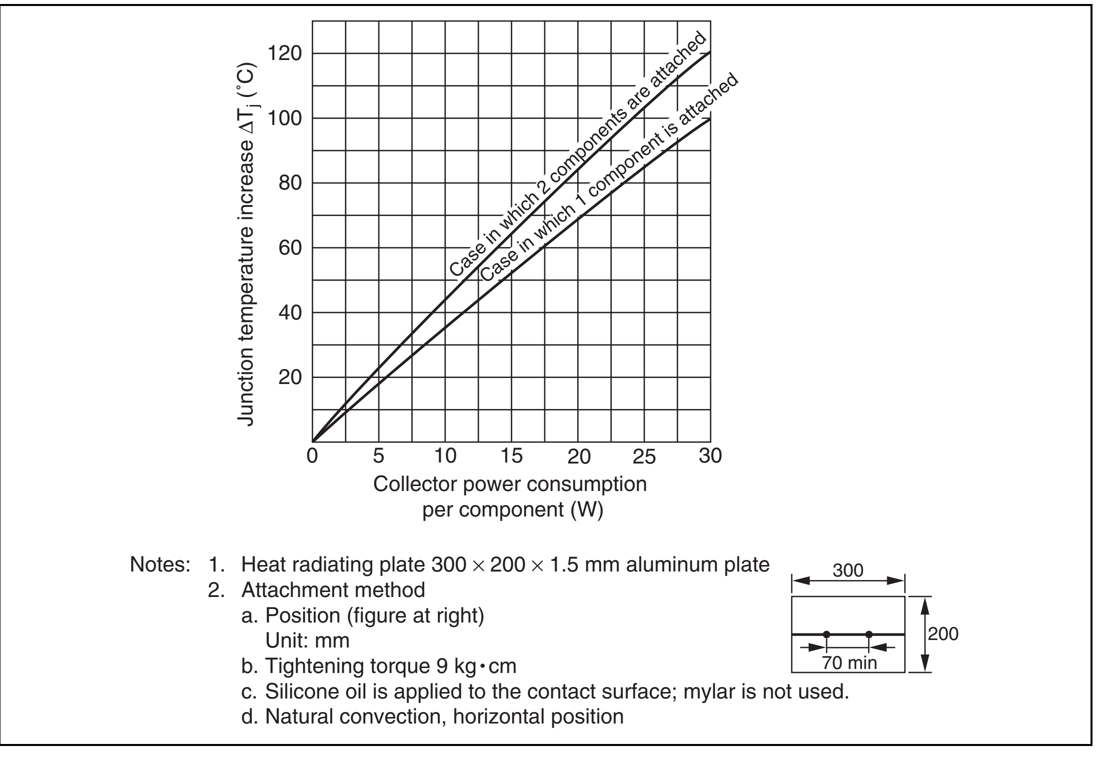


Figure 6.17 A Case in which Two Components are Attached to One Heat-Sink Plate

- Example 25

  Package Destruction during Mounting

No. 25	Example	Package destruction at time of mounting
Type of device		Power transistor (type TO-220)
Point		The torque used to tighten must be checked.
Outline of example/ phenomenon/ cause		When a power transistor was mounted, the compressed air screwdriver torque rose above 10 kg • cm and the mounting holes in the heat-sink plate were too large, so the header and the plastic boundary surface peeled off. Depending on the type of compressed air screwdriver, the dispersion in the tightening torque can become large. If the torque rises above 8 kg • cm, the heat-sink plate mounting holes are larger than the screw diameter, or if the heat-sink plate mounting holes are not sufficiently flat, the header can be deformed or separate from the plastic.
Countermeasure/ Method of checking		Use a torque within the recommended limits. For the type TO-220 the recommended limits are 4 to 6 kg • cm. Keep the flatness of the heat-sink plate mounting holes within 50 μm, make sure that the mounting holes do not open wider than the screw head diameter, and use the accessory metal washers (YZ033S).
Reference item		

- Example 26

  Chip Cracking at Time of Mounting to a Heat-Sink Plate

No. 26	Example	Chip cracking at time of mounting to a heat-sink plate
Type of device		Power transistor (type TO-3)
Point		Always check the tightening holes meet the recommended conditions.
Outline of example/ phenomenon/ cause		The heat-sink plate mounting holes were of large diameter and were excessively chamfered, so that when the transistor was mounted, one side of the heat-sink plate tightened around the screw hole dropped into the chamfered section and the stem became inclined. When the other side was tightened, the entire stem deformed. The result was that at least twice as much of typical stress was applied to the chip inside, causing a chip crack.
Countermeasures and/Methods to verify		1. Make the heat-sink plate hole diameter (including the beveled section) smaller than the screw head diameter. 2. Use the appropriate torque to tighten.
Reference item		

6.4 Preventing Thermal Damage

As it was stated above, because of its construction a semiconductor device is very sensitive to mechanical and thermal stresses. In addition, materials used in construction have different thermal expansion coefficients. These differences have the potential to cause the adhesive holding the different substances together to break. Repeated thermal stress on metals can cause fatigue fractures.

In particular, the recent emphasis on light, thin, short and small surface mounted devices has led to reduced margins for the following points.

1. As the temperature rises, the mechanical strength of plastic assembly drops considerably.
2. When the temperature exceeds 100°C, moisture in the resin vaporizes and the vapor fills gaps, causing steam explosions.

One should carefully check the storage conditions and assembly conditions for each product, and monitor them accordingly.

6.4.1 Soldering Temperature Profile

(1) Precautions during Soldering Attachment

In general, it is not desirable to expose a semiconductor device to a high temperature for a long time.

Also, when soldering, whether using a soldering iron or by a reflow method, it is necessary to do the processing at as a low temperature and in as a short time as possible to achieve the required attachment. The standard condition to determine the ability of a semiconductor device to withstand the heat of soldering is, to apply 260°C heat at 1 to 1.5 mm from the device package, 260°C for 10 seconds or 350°C for 3 seconds. When performing soldering, be careful not to exceed these values.

An example of temperature increase during soldering, the increase of temperature in the joint section when soldering is done on a low power plastic-package power transistor, is shown in figure 6.18. After heating in a soldering tank at 260°C for a specified time, the temperature of the joint section was measured. If the soldering temperature is high and/or the time is long, the temperature of the device increases; in some cases this can cause deterioration or breakage.

If the flux that is used for soldering is strongly acidic or alkaline, the leads can be corroded, the use of rosin flux is recommended, but in any case the flux should be removed thoroughly after soldering (see section 6.3.3).

The soldering iron that is used should either have three terminals including a ground terminal or the secondary voltage decreased using a transformer so that there is no leakage current at the tip of the iron. If possible, the tip should always be grounded. In this case, one must be careful that secondary damage is not caused by the ground (see figure 6.19). In addition, the soldering should be done as far as possible from the device package.

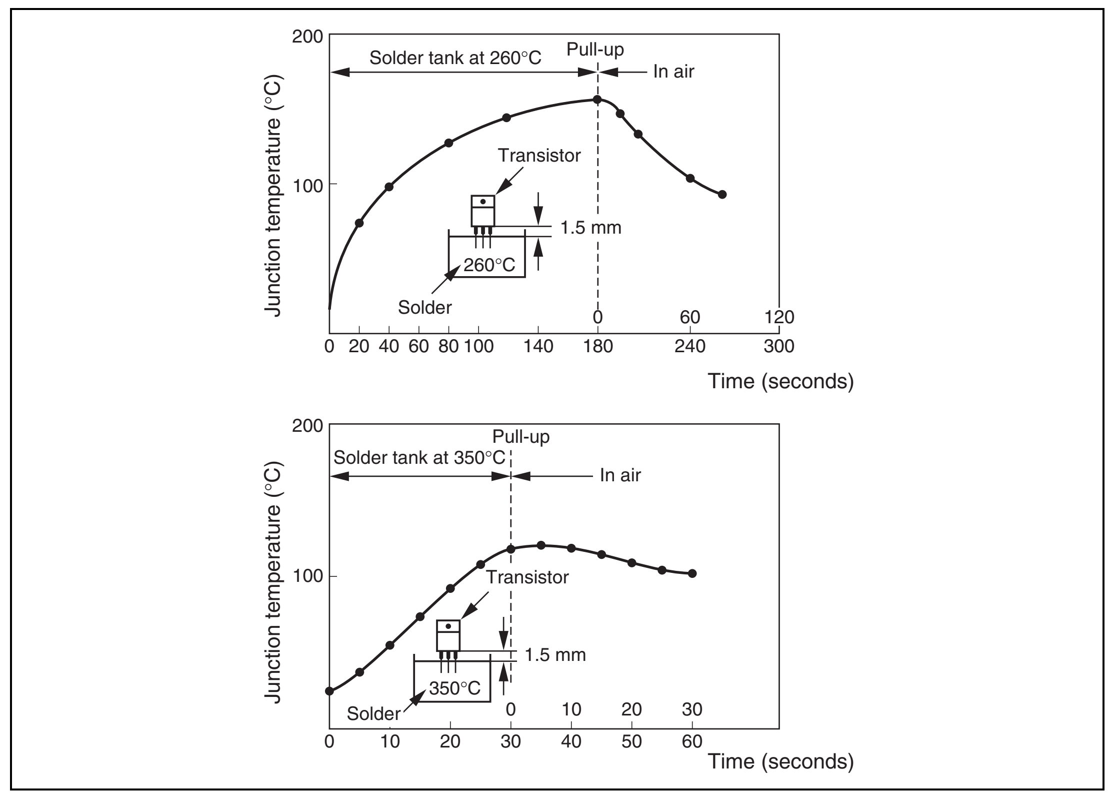


Figure 6.18 Junction Temperature during Soldering

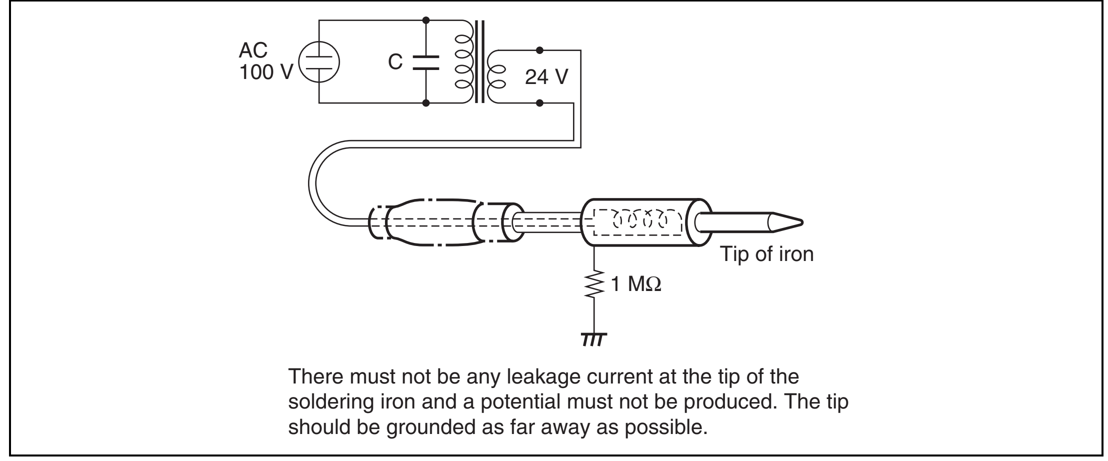


Figure 6.19 Grounding of the Tip of a Soldering Iron

(2) Soldering a Lead Insertion Type Package in a Wave Solder Tank

In this method, the soldering is done by immersing the soldering sections of the package leads below the liquid surface in the jet flow solder tank. If the solder jet comes into contact with the device, the package can break, so be sure that the solder does not come into direct contact with the device package.

In addition, when using a wave solder tank, the bottom surface of the board is heated by the hot solder, and the temperature difference between the top and bottom surfaces can cause the board to warp. If soldering is done while the board is warped, at the time of removal from the solder tank the board will try to return to its original shape, causing excessive stress being applied to the leads and the package. This in turn can cause the solder holding the joint together to crack and/or the leads and the package to break. For this reason, when a wave solder tank is used, the board should be held in place by brackets so that it will not be warped (see figure 6.20).

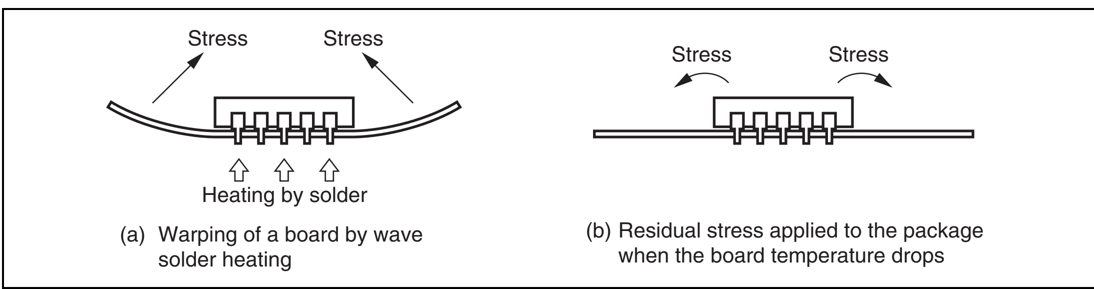


Figure 6.20 Warping of a Board in a Wave Solder Tank

(3) Soldering Surface-Mount Packages in a Wave Solder Bath

In this method, the products are first temporarily bonded to the board. The board is then turned over so that the products are fully bonded in the flow solder process. This method requires special measures because bridges will be formed due to excess solder between the leads and because high-temperature solder comes into direct contact with the samples, applying a severe thermal stress. Also note that the method is applicable to only a limited number of packages available from Renesas. Before using this method, therefore, you should consult Renesas to find out if it can be used for a particular product.

You must also be careful when selecting the bonding agent used to temporarily bond samples to the board. If, for example, the bonding performance is not strong enough, products that are being mounted might fall off when the board is turned over. As mentioned in 6.4.1 (1), products may be subject to unexpected stress from warping of the board caused by the heat from the solder jets and product might fall off. This is something else you need to consider when you select a temporary bonding agent.

6.4.2 Precautions in Handling a Surface-Mount Device

Here, we explain specific precautions and mounting conditions for surface-mount devices, the use of these has recently been expanding quite rapidly. A surface-mount device must be soldered from the side of the printed circuit board on which the parts are mounted. It is intrinsically easy for the device to be subjected to thermal stress during mounting. In particular, if the mounting method involves heating the whole package, the following precautions should be observed during mounting. For details please refer to our company's publications "Renesas Surface Mount Package User's Manual" and "Renesas Semiconductor Packages General Catalog."

(1) Absorption of Moisture by the Package

If the epoxy resin used in a plastic package is stored in a humid location, moisture absorption cannot be avoided. If the amount of moisture absorbed is sufficiently large, it can vaporize suddenly during soldering causing the resin to separate from the leadframe surface. In a particularly severe case, the package can crack (see section 4.4.1). Consequently, it is important to store surface-mount packages in a dry atmosphere.

Moisture –absorption sensitive products should be stored in vapor barrier packaging. This prevents moisture from being absorbed during transportation and storage. To prevent moisture absorption after opening the storage bag the packages should be stored in the prescribed environment and mounted by reflow soldering within the defined storage time limit.

The required storage environment conditions and storage time limit are ranked according to the ability of each product to withstand the storage temperature conditions. If a device is to be stored again in vapor barrier packaging, active silica gel (the type with an indicator that turns blue if moisture is absorbed) should be put inside with it. If the device has been out of vapor barrier packaging and exposed to outside air for several days, it will return to its original condition after being in the new vapor barrier packaging with the silica gel for three to five times the length of time it was exposed to ambient. To remove moisture that was absorbed during transport, storage and handling, it is recommended that the device be baked for 16 to 24 hours (4 to 24 hours in the case of an ultra thin package such as a TQFP or TSOP).

In the following cases, it is necessary to bake the device at 125°C before mounting and soldering it.

- The blue indicator in the silica gel desiccant cannot be seen at all through the desiccant bag.
- The permissible storage time after opening the package has been exceeded while the products are being stored under the conditions stated above.
- The attached label states that it should be baked.

  (There are some products attached to an ultra thin package or an extra large chip that need to be baked in any case.)

The magazine, tray, or tape and reel normally used in shipping cannot withstand much temperature, so the package typically cannot be baked as it is packed and received. Transfer the package to a heat resistant container. A tray with the words HEAT PROOF inscribed on it can be baked as is. However, avoid baking the package while it is inside vapor barrier packaging. Bake gradually, with the tray placed on a flat board, so that the tray will not warp.

(2) Dealing with Moisture Resistivity

Surface-mount products tend to have shorter distance from the outside lead to the inside IC chip than plastic-sealed DIP products, so in some cases consideration needs to be given to moisture resistivity. For example, in devices that are to be used outdoors or in which ability to withstand moisture is particularly important, an appropriate measure such as resin coating is employed. Coating materials include polyurethane and silicon resins. Stresses produced by hardening of the resin, contraction stress and the difference in thermal expansion coefficients between the resin and substrate can cause the element to crack, and the solder joint between the lead and the substrate to crack or disconnect. Therefore the coating material should be selected and applied carefully.

(3) Precautions with Taped Items

In the case of a taped chip component or IC (MPAK, SOP, etc.), electrical charging caused by separation of the cover tape or the carrier tape increases with the speed of the tape separation. To prevent the component from being damaged by static electricity, avoid rapid separation and friction as much as possible.

The recommended separation speed = 10 mm/s or less

(4) Precautions in Mounting

When relative humidity decreases, it becomes easier for objects to become charged with static electricity. Surface-mount products should be stored in a dry atmosphere to prevent moisture absorption. Since the packages are not subject to friction, they will not become electrostatically charged. During handling and mounting on a board, however, the relative humidity should be kept between 45% and 75% to minimize the possibility of ESD damage.

6.4.3 Using Reflow to Attach Surface-Mount Devices

On a predetermined pattern that is required for solder joint for lead pins of a printed circuit board, the specified amount of solder paste is applied to match the lead-pin pattern of the package. For example when using screen printing, the package is placed on top of the solder pattern. The package is temporarily held in place by the surface tension of the solder paste. Then, when the solder is reflowed, the package leads are joined to the pattern of the printed circuit board by both the surface tension of the melted solder and the self-aligning effect.

The design values of the pattern to which the leads are joined on the printed circuit board differ depending on the solder paste material that is used and the reflow conditions. As a rule, the pattern width should be 1.1 to 1.3 times that of the lead pins that will be soldered to it.

6.4.4 Recommended Conditions for Various Methods of Mounting Surface-Mount Devices

The most widely used methods of mounting surface-mount devices are the infrared reflow, the vapor phase reflow and the flow solder methods (wave soldering). These mounting methods all involve heating the entire package. Strong thermal stress is applied to the package. From the point of view of maintaining reliability, it is necessary to monitor the package surface temperature as well as the temperature of the solder joint. Our company's recommended mounting conditions include the package surface temperature in the case of the reflow method; the solder temperature and immersion time in the case of flow solder.

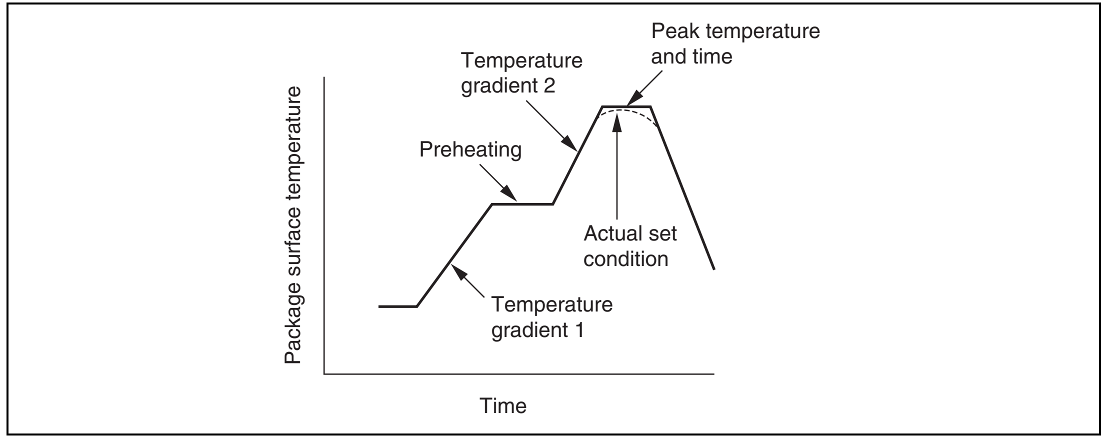


Figure 6.21 Example of Recommended Conditions

We will now present our thinking behind the recommended conditions, with reference to figure 6.21.

(1) Temperature Gradient 1

When the temperature increases suddenly rapidly, the temperatures of the different parts of a surface-mount device (such as the package surface, interior and rear) become different, so the package warps due to the difference in thermal expansion coefficients among the different materials, in some cases this leads to damaging the chip. Consequently, attention must be paid to the upper limit of the rate of temperature increase. The lower limit is determined by the operating efficiency of the reflow device.

(2) Preheating

The temperatures of the components and the board are kept below the melting point of the solder to stabilize the solder joint and lessen the thermal shock. In general, this is set near the rated temperature of the surface-mount device.

(3) Temperature Gradient 2

The upper limit of the rate of temperature increase is determined as in (1) above. The lower limit is determined by the need to keep temperature and the time within limits specified in (4).

(4) Peak Temperature and Time

These are the most important factors requiring attention to keep any damage suffered by the package to a minimum. The peak temperature directly affects the drop in strength of the package (due to the temperature characteristics of the resin) and the water vapor pressure inside the package, so as low a temperature as practical is desired. In addition, since the water vapor pressure increases with time, it is necessary to keep the time as short as possible. Figure 4.60 shows the heating conditions of the package thermal resistance evaluation that has been conducted at Renesas. Soldering should be performed in a way that does not exceed these conditions. Observe these conditions in determining permissible heating conditions in making of the solder joints, taking into account the characteristics of the board, the components to be mounted, the solder paste, and the reflow equipment.

- Example 27
  Chip Cracks in a Surface-mount Package

No. 27	Example	Chip cracks in a surface-mount package
Type of device		QFP package
Point		Whether the package surface temperature satisfies the recommended temperature
Outline of example/ phenomenon/ cause		When a semiconductor surface-mount package (QFP) is mounted on a board by hot air reflow soldering, the transient temperature difference (T_s – T_i = 60°C) that occurs inside the package during the sudden heating applied for reflow soldering causes the package to warp. This then produces a stress that can crack the chip.
Countermeasure/ Method of checking		Change the conditions so that the temperature increase during mounting becomes more gradual.
Reference item		

- Example 28
  Reflow Mounting Defects

No. 28	Example	Reflow mounting defects
Type of device		Surface-mount package diode and transistor
Point		Poor mounting balance will cause problems such as product displacement and float.
Outline of example/ phenomena/ causes		If the mounting balance is poor when a surface mounted package (URP, UFP, LLD, etc.) is mounted using reflow soldering, mounting problems can occur such as the package becoming displaced or not fixed on the surface. Care is particularly required when lead-free materials or processes are being handled. 1. The land pattern does not have left-right symmetry. 2. The amount of solder cream applied is not uniform. 3. The soldered parts are not all heated at the same time. 4. If some parts are in the shadow of neighboring components, the left-right temperature difference of the soldered section can become large. 5. The ratio of flux contained fluctuates.
Countermeasure/ Method of verifying		Check for the problems listed above.
Reference item		Diode Package Data Book and Renesas Surface Mount Package User's Manual

6.5 Preventing Malfunction

There are several types of semiconductor malfunction. The semiconductor itself can become damaged or degraded, making normal operation permanently impossible. In other cases, even though a semiconductor has a slight defect, it will operate normally until a change in the conditions of use and/or environmental conditions causes the latent defect to become critical. In the former case, there is nothing to do except replace the damaged part, so quality is expressed in terms of MTTF (Mean Time To Failure). In the latter case quality is expressed by a measure of the frequency with which malfunction occurs, MTBF (Mean Time Between Failures).

MTBF expresses the frequency of malfunction in the environment in which the device is actually used. If the mechanism of malfunction and the conditions in which it occurs become clear, it is possible for the operation to become 100% defective under those conditions. In this section we explain mainly the latter case.

6.5.1 Precautions with Respect to Hardware

In our company's 100% inspection procedure, a component's electrical characteristics are efficiently and rigorously tested by a tester. However, for economic reasons there is a limit as to how much time can be spent testing one component, so the test is conducted under what are expected to be the worst case conditions. Because of the difference between the conditions of the tester test and the conditions under which the component is used in practice, there are cases in which malfunction occurs. Here we give specific examples of troubles that have been experienced in the past, in the hope that this experience can be applied in the final evaluation of products.

6.5.2 Precautions in Circuit Design

Circuits are classified into two categories, analog circuits and digital circuits.

Analog circuits, typified by PLL circuits, sacrifice gain to obtain accurate amplification factor by means of a feedback circuit between the input signal and the output signal. They can also generate a variety of functions. They can also compare, detect, and integrate the phase difference between input signals, and use a voltage-frequency conversion circuit to tune the phase difference. In all cases small differences between input signals are greatly amplified for use, so it is easy for noise that accompanies the input signal to have a considerable effect, and the output is very sensitive to fluctuations in the electrical characteristics of constituent elements. Consequently, small changes in leakage current and changes in gain can develop into a malfunctioning condition. Therefore it is necessary to design the circuit while comprehending the worst case conditions among the electrical characteristic specifications in sensitive parts of the circuit.

In contrast, in a digital circuit, the levels of the input signal and the output signal are standardized, and a noise margin between the two signals is set, which is advantageous with respect to fluctuations in the characteristics of constituent elements. On the other hand, if a malfunction does occur, it has the potential to grow into a very serious malfunction, depending on the meaning of the signal that is affected. Recently, in devices which contain programs such as microcontrollers, once the content of the program is changed, even if the immediate cause of the malfunction is removed the original operation cannot be restored, so that the damage caused is greater than in the case of an analog circuit. When malfunction occurs in a digital circuit, whether the input level, output level and timing margin are being observed correctly are important points. In addition, particularly during transient periods such as when the power is turned ON or OFF, one important precaution is to design the circuit so that the effect of environmental conditions under which correct operation is not guaranteed does not remain after regular operation starts.

- Example 29
  TTL-CMOS Interface

No. 29	Example	TTL-CMOS interface
Type of device		TTL, CMOS IC
Point		Undershoot and overshoot must be within the specified range.
Summary of example/ phenomenon/ cause		When CMOS LSIs are driven by TTL ICs, a malfunction may occur due to undershoot noise or insufficient input level. Undershoot is caused by reflection due to the imbalance between the low output impedance of the TTL IC and the extremely high input impedance of the CMOS LSI. Insufficient input level is also caused by the significant difference in the input level between TTL and CMOS. Particularly, the TTL level output does not rise to Vcc level, which will cause a problem.
		1. Insert a resistor at output pins of TTL IC to prevent undershoot. 2. Attach a pull-up resistor to input pins of CMOS IC. 3. Use a special interfacing IC.
Reference items		

- Example 30

  Malfunction of Power-On Reset Circuit

No. 30	Example	Malfunction of power-on reset circuit
Type of device		IC, LSI
Point		An appropriate type of power-on reset circuit must be used for the power-up waveform.
Summary of example/ phenomenon/ cause		There are two types of power-on reset circuits, integral and differential. The integral type is vulnerable to short-time power supply interruption, whereas the differential type is vulnerable to slow rises in voltage. Due to this, circuits may malfunction as shown in the figure below. 1. Malfunction of integral circuit If t is too short after power is turned off, the potential at point Ⓐ will not fall and a pulse will not be generated (dotted line). 2. Malfunction of differential circuit If the rise of the power supply is too slow, the waveform will not reach the reset operation potential and a reset will not be effected (dotted line).
Countermeasure/ measure of checking		Replace the current power-on reset circuit with the power-supply-voltage monitoring IC shown in the figure below.
Reference items		

- Example 31

  Malfunction during Measurement

No. 31 Example	Malfunction during measurement
Type of device	MOS LSI
Point	The impedance of measurement systems must be appropriate.
Summary of example/ phenomenon/ cause	During measurement, resistors were connected to the measurement system (see figure below) to prevent damage. This caused cross-talk between adjacent input and output pins, thus resulting in a defective input voltage margin. A single measurement system was shared for testing products with different pin layouts, with a resistor connected not only to the output pin but also to the input pin during measurement. LSI Output Input Measurement system R Ω R Ω Input/output crosstalk
Countermeasure/ measure of checking	Modify the system so that the appropriate resistor for protecting the measurement system can be selected by a relay depending on the pin specifications (input/output) to allow selecting the 0-Ω resistor for input and R-Ω resistor for output.
Reference items	

6.5.3 Precautions for Board Mounting

Semiconductor devices are not used alone; they are mounted and used on various boards such as printed-circuit boards, on which other devices are also mounted. Therefore, semiconductor devices share a power-supply line with other devices and are subject to influence by extraneous signals used for the circuits located near the semiconductor devices. Special consideration is thus necessary regarding positioning of the signal lines that are likely to be affected by subtle signal waveforms.

- Example 32

  Linear IC Oscillation

No. 32	Example	Linear IC oscillation
Type of device		Linear IC
Point		Oscillation must be checked.
Summary of example/ phenomenon/ cause		If a long line is connected to an input pin of a linear IC, equivalent inductive (L) load is generated on the input pin, causing oscillation. If a small signal line runs parallel to a large-current output line, mutual induction is generated, also causing oscillation of the output waveform. Wiring is long ("L" load). Input Output GND Oscillates. C_i C_L R Example of 3-pin regulator
Countermeasures/ measure of checking		1. Make input lines as short as possible to reduce inductive (L) load on the input. 2. If input lines are inevitably long, monitor the waveform on the input pins while varying the capacitance of input capacitor C_i and output capacitive load C_L. 3. Separate large-current lines from small signal lines. 4. In a printed-circuit board, insert a GND pattern between the signal line patterns.
Reference items		

RENESAS

- Example 33

  Malfunction due to Design Changes of Terminal Equipment

No. 33	Example	Malfunction due to design modification of terminal equipment
Type of device		MOS LSI
Point		LSIs must not be operated under high voltage.
Summary of example/ phenomenon/cause		After the design of CRT display equipment had been changed, a non-repeatable runaway failure occurred abruptly. It recovered from the failure after temporarily being left turned off. By reviewing the changes, it was found that the cause was a shift in a threshold voltage due to a high electric field (anode voltage was 20 kV). Before design modification (operates correctly.) After design modification (mulfunction occurred.)
Countermeasures/ measure of checking		1. Modify the CRT connection manner to prevent high electric field application. 2. Shield the LSI from electric charge.
Reference items		

- Example 34

  Reset Malfunction due to Hazardous Noise

No. 34 Example	Reset malfunction due to hazardous noise
Type of device	IC, LSI
Point	Anti-noise measures must be taken for mechanical switches.
Summary of example/ phenomenon/ cause	With set 1 connected to set 2, when the reset switch of the application circuit was pressed, the application circuit was not reset, and instead malfunctioned. Specifically, the reset signal of set 2 fell so slowly that hazardous noise was generated in the reset-input circuit in set 1, thus disabling correct reset function.
Countermeasure/ measure of checking	Modify set 1 to prevent generation of hazardous noise.
Reference items	

- Example 35

  Oscillation Circuit and Patterns on a Board

No. 35	Example	Oscillation circuit and patterns on a board
Type of device		Microcontroller
Point		Oscillation-start time must be constant.
Summary of example/ phenomenon/ cause		An intermittent failure occurred in microcontrollers. The failure-occurrence ratio depended on the product model despite the fact that the products were assembled by the same manufacturer. By analyzing the oscillation waveforms of the products presenting the high failure-occurrence ratio, it was found that it sometimes took so long for oscillation to start that the reset signal was cancelled before oscillation became stabilized, thus causing malfunction. It was also found that the difference in the failure-occurrence ratio between product models was caused by the difference in oscillation circuit patterns. That is, the products presenting the high malfunction ratio had no shield for the input pattern of the oscillation pin, and a high-speed signal line crossed the pattern. This signal line generated cross-talk, thus preventing stable oscillation.
Countermeasures/ measure checking		1. Oscillation circuit patterns were modified to the standard patterns recommended by the supplier. 2. Eliminating distortion of oscillation waveforms was confirmed by monitoring the waveforms. 3. Series resistors were inserted into the input to stabilize the oscillation circuit. Adequate margin was then confirmed.
Reference items		

6.5.4 Precautions against Malfunction due to Noise

Accompanying the increased speed of semiconductor device operations, the devices now generate more noise and have become more sensitive to noise that leads to malfunction. Extraneous noise, for example, was eliminated by conventional low-speed devices acting as noise filters, thus preventing malfunction of the subsequent devices, whereas the same noise is amplified by recent high-speed devices, thus sometimes increasing the incidence of malfunction.

Currently, CMOS devices capable of high-speed operation while at low power, have significantly higher signal impedance and higher noise sensitivity. Furthermore, as CMOS circuits are inevitably accompanied by large current changes synchronized with clock pulses on the power supply line, this large current change coupled with print circuit patterns, may generate a lot of noise. Specifically, sine-wave signals generate relevant frequency noise only, whereas square-wave signals generate various harmonics as noise.

Particular components of harmonic waves can be determined by performing Fourier analysis on the square waves.

When the original oscillation frequency is f_0 and a frequency that depends on the rise/fall gradient of waveforms is f_1, harmonic noise spectrum is attenuated at a rate of –10 dB/decade within the frequency domain between f_0–f_1 and –20 dB/decade above f_1. If harmonic signal waveforms are further superposed on square waveforms, still more noise in the form of harmonics will be generated.

- Example 36
  Malfunction due to Cross-Talk Noise from NC Pins

No. 36	Example	Malfunction due to cross-talk noise from NC pins
Type of device		IC, LSI
Point		NC pins adjacent to noise-sensitive pins must be appropriately handled.
Summary of example/ phenomenon/ cause		The user system malfunctioned in noise-tolerance testing during development. The noise level was found to be high and several anti-noise measures were tried. Grounding the NC pin was shown to be effective. After investigation, it was found that the open NC pin was near the high-frequency signal pattern on the printed circuit board, and the resulting cross-talk noise was input to the adjacent pin through the stray capacitance, thus causing malfunction.
Countermeasures/ measure of checking		1. NC pins must be grounded with an appropriate value of impedance, or connected to the power supply. 2. NC pins must be handled carefully because they may serve as internal test pins.
Reference items		

- Example 37

  Noise Generation

No. 37	Example	Noise generation (electrical)
Type of device		Microcontroller
Point		The capacitance and layout of the bypass capacitor must be appropriate. The clock waveforms must be appropriately shaped.
Summary of example/ phenomenon/ cause		Noise generated by digital circuits such as microcontrollers may cause malfunction of peripheral devices. The noise depends on various factors such as the clock waveforms and power supply current waveforms of the LSI, and the positioning of the bypass capacitor and routing of both the power and the GND lines on the printed circuit board.
Countermeasures/ measure of checking		An LSI generates only a small electric waveform by itself. Power-supply-related electric waveforms can be eliminated using a bypass capacitor effectively to suppress the power supply current loop, and clock-related electric waveforms can be eliminated by shaping the rising and falling waveforms. In other words, monitoring the clock waveforms and power-supply waveforms of the LSI mounted on the board using a spectrum analyzer provides the means of preventing noise generation. 1. Shape the rising and falling waveforms of the clock (t_r,t_f) and reduce the speed to accelerate attenuation of the harmonic waveforms. The harmonic waveforms will be attenuated at a rate of 10 dB/decade within the frequency range between the original oscillation frequency and t_r (f_f) and at 20 dB/decade above this. 2. Absorb harmonic spectrum component using the bypass capacitor. Selecting an appropriate capacitor that has excellent frequency characteristics and is capable of absorbing the harmonic spectrum component is important, and appropriate positioning of the bypass capacitor, which determines magnitude of the power supply loop, is also important.
Reference items		

6.5.5 Precautions on Signal Waveforms

Along with the speed-up of semiconductor device operations, noise and distorted waveforms, which did not cause problems previously, have become likely to affect basic LSI operations. It becomes increasingly difficult to test the stability of device operations. This is because not only finding the conditions that most affect the operations is extremely difficult but also finding the combination of good samples and samples that adversely affects the operations in an evaluation and testing phase is also very difficult.

The best approach to effectively find and solve these issues is analyzing waveforms in detail. Recently, advanced waveform monitors incorporating glitch-detection function are available, and abnormal waveforms that were previously difficult to find can be quickly found today. However, even when abnormal waveforms are found, it is often difficult to determine how much the abnormal waveforms can affect the LSI. In such cases, please direct inquiries to the technical support department of our company.

- Example 38

  Malfunction due to Distorted Input Waveforms

No. 38	Example	Malfunction due to distorted input waveforms
Type of device		IC, LSI
Point		Distortion of signals must be monitored.
Summary of example/ phenomenon/ cause		When operating an IC, depending on the input waveform, distortion near the threshold voltage may cause unstable IC operation leading to malfunction. A certain logic product exhibited a significant propagation delay of the input waveform shown below. Specifically, the input waveform was distorted near the threshold voltage, which changed the input level and disturbed multi-gate operation, thus causing the delay.
Countermeasure/ measure of checking		Add a buffer gate and shape the waveform to eliminate distorted input waveforms.
Reference items		

- Example 39
  DRAM Malfunction due to Noise in Address Signals

No. 39	Example	DRAM malfunction due to noise in address signals
Type of device		DRAM
Point		Signal waveform of DRAM must be appropriate.
Summary of example/ phenomenon/ cause		DRAM internal circuits are designed to be triggered when the voltage level of the address signals becomes stable. If a large noise above the specifications is applied to these signals, access time starts at the time of noise generation, thus causing malfunction. Particularly, special care for the waveforms of these signals must be taken because they change depending on the retained data, and the word line selected immediately before.
Countermeasure/ measure of checking		1. Find a large noise in the waveforms of various signals using the glitch-detection function and determine the worst pattern based on the characteristics. 2. Shape the waveform by improving the impedance matching with the driver, power-supply patterns, positioning of bypass capacitors.
Reference items		

In some cases, the operational margin for a circuit can be confirmed by analyzing signal waveforms in detail. For analog circuits such as oscillation circuits and PLL circuits in particular, waveform monitoring is one of the most effective means. If the phase difference between input and output signals, amplitude, distortion, noise level, and other factors are strictly measured and the waveforms are shaped to what it should be, malfunction frequency can be reduced and the reliability can be improved greatly.

- Example 40

  Evaluation of Oscillation Circuit Stability

No. 40	Example	Evaluation of oscillation circuit stability
Type of device		Microcontroller
Point		Stability of oscillation circuits must be carefully confirmed.
Summary of example/ phenomenon/ cause		Oscillation circuits are very difficult to handle and often cause intermittent failures. This is particularly because they depend on the compatibility between the LSI and the oscillator, the pattern routing on the printed circuit board, and the combination of external capacitors, resistors, and other elements. Therefore, the stability of oscillation circuits must be carefully confirmed regarding temperature, power supply rising waveform, oscillation stabilization time, phase difference between input and output, and input/output waveforms.
Countermeasure/ measure of checking		1. Confirm the temperature characteristics of the oscillation circuit because the circuit gain may vary depending on the temperature. 2. Test the oscillation waveform while varying the power-supply rising waveform and confirm that the waveform is perfect and that extraordinarily slow rise of the power-supply waveform does not affect the oscillation waveform. 3. Create the distribution of oscillation stabilization time and infer the probability that oscillation will be stabilized after reset cancellation. 4. Find the limit regarding the stability of oscillation start by inserting series resistors into the feedback circuit. 5. If oscillation is not obtained, check for distortion in the input/output waveforms. 6. Oscillation stability can be predicted from the phase difference between input and output waveforms.
Reference items		

6.5.6 Precautions with Regard to the Environmental Conditions in which the Device is Used

There is a hidden danger lurking in the event of unexpected malfunction. If enough consideration of the actual environmental conditions in which the device will be used in practice is not made, trouble can occur as a result of differing perceptions between the party that supplies the device and the party that uses it. It is difficult to detect this type of problem in advance. In particular, since this kind of problem is difficult to classify, only a general discussion that applies to various cases will be given here.

The case of illumination is an example of an environmental condition which can reduce the temperature margin due to the generation of photoelectrons when the LSI is illuminated by intense light, a process that becomes more active as the package becomes slimmer. The case of natural rubber in close proximity to the LSI in a hot and humid environment is another. In this case, leakage currents are increased if a buffer component has sulfur as its main component. The case of a malfunction when the power is initially supplied, due to the system having been started up without determining the conditions required by the device, provides a further example.

- Example 41
  Decrease of the Operation Margin by Light Illumination

No. 41	Example	Decrease of the operation margin by light illumination
Type of device		Microcontroller
Point		For an application in which strong light is to be used, measure under the actual conditions of use.
Summary of example/ phenomenon/ cause		When strong light is applied on a semiconductor, photoelectrons are produced. If there is a possibility that strong light will be incident on the LSI during use, exercise caution. Caution is particularly necessary when the package is thin and/or chips are purchased and assembled.
Countermeasure/ measure of checking		1. When the electric characteristics of a bare chip are measured, shut off the incoming light. 2. For an application in which strong light is to be applied to a packaged product, measure the electric characteristics while applying light.
Reference items		

- Example 42

  Leakage Defect Caused by Sulphide Gas Emitted by Natural Rubber

No. 42	Example	Leakage defect caused by sulphide gas emitted by natural rubber
Type of device		IC, LSI
Point		A substance of which sulphur is the main constituent, such as rubber, should not be in close proximity to the IC.
Summary of example/ phenomenon/ cause		Malfunction of unknown origin occurred in the market; as the result of an investigation it was judged that a sulphide substance had crystallized between LSI pins, amplifying the leakage current and causing malfunction. The result of the investigation further revealed that there was a buffer component made of a substance that had sulphur as its main constituent, such as rubber, in close proximity to the LSI; sulphide gas emitted from that substance cause dew in high humidity, causing the foreign chemical substance to be formed between the LSI leads. In an experiment conducted to reproduce the phenomenon in a high temperature, high humidity tank, it could not be reproduced, but when an identical rubber component was inserted into a desiccator and a test was conducted at high temperature and high humidity, it was reproduced. (This defect does not occur in a well-ventilated location.)
Countermeasure/ measure of checking		Do not place or mount any substance having sulphur as its principal constituent, such as rubber, in close proximity to an IC.
Reference items		

- Example 43

  Malfunction Caused by Surge Current when Power is Turned ON

No. 43	Example	Malfunction caused by surge current when power is turned ON
Type of device		Microcontroller
Point		The power-supply current is OK between the time the power is turned ON and the start of oscillations.
Summary of example/ phenomenon/ cause		After power is turned ON, until clock input, there was an indeterminate section in the internal logic, and a current exceeding the current rating flowed in the power supply. Part of the users system had internal circuits to detect excess current flow; this current caused the device to malfunction.
Countermeasure/ measure of checking		In an application in which it is necessary to detect excess current, the peak power-supply current, as well as the average power-supply current, should be specified.
Reference items		

6.6 Software Precautions

The number of products in which microcontrollers are used has increased considerably in recent years. In most cases it has become possible for the user to customize the functions with software; this is very convenient, but is also a source of problems. If a problem occurs infrequently in the final product and is difficult to reproduce, it can be extremely difficult to determine whether the problem is in the LSI or in the user's program.

Typical examples include malfunctions that sometimes occur and sometimes do not depending on the internal RAM data pattern at power on.

From the viewpoint of security maintenance, many functions have come to be realized in software. We are entering an age in which functions such as error logging and the load-and-go execution of small programs in RAM are handled by combinations of hardware and software. When a failure occurs, confirm that software programs written for the system do not include an error.

- Example 44

  Program Malfunction in Referring to an Indeterminate RAM Area

No. 44	Example	Program malfunction in referring to an indeterminate RAM area
Type of device		Microcontroller
Point		Contents of indeterminate RAM must not be used in a program.
Summary of example/ phenomenon/ cause		In a user's pre-production, small percentage of operation defects occurred when power was turned ON. When only a short time elapsed between turning power OFF and turning it ON again, reproducibility of the defects was very poor. When the smoothing capacitor was shorted and completely discharged after power was turned OFF, the defect became easy to reproduce. As a result of analyzing the user's program, it was found that uninitialized RAM content at a certain address was used as a branch in the program; it was judged that sometimes when power was turned ON this RAM data was inverted, causing the malfunction.
Countermeasure/ measure of checking		1. RAM contents that are not initialized must not be used as a branch statement. 2. When developing a program, check operation after the RAM content is initialized to set or reset state.
Reference items		

6.7 Being Prepared for Possible Malfunction

In order to achieve zero defects in LSI production, strenuous efforts have continued day and night, but unfortunately this goal has not yet been achieved. Under conditions in which it is not possible to obtain 100 % good products as the concept of yield represents, the failure to achieve a 100 % testing rate means that the final product cannot be made fail-safe with respect to the possibility of malfunction of the semiconductor components. Such product as a relay that has certain characteristics as to how it behaves when it is destroyed. When the natural phenomenon of gravity could be utilized, that characteristic could be used in system design, but unfortunately the characteristics of semiconductor failure are not that simple. Types of failures include broken or shorted wires, and open low stack or high stack. This fact can be used to judge that the output of a high or low-level signal (not a fixed level) is evidence of normal operation. In addition, by using this type of judgment together with the watchdog function, much higher fail-safe operation can be obtained than with a relay circuit. Considering these, the end user should make the necessary adjustments in the user system.

- Example 45

  Watchdog and Fail Safe

No. 45	Example	Watchdog and fail safe
Type of device		Microcontroller
Point		The division of labor between hardware and software in the watchdog function is important.
Summary of example/ phenomenon/ cause		The watchdog function is effective in maintaining the safety of a system. The watchdog function uses both hardware and software to reverse the output at certain pins at regular intervals; if an interval deviates from the design value, the problem can be detected from a separate monitoring circuit and the system adjusted in the direction of safety to prevent the worst from happening. In this case, it is important that the reversal of output at regular intervals not be achieved with hardware alone. If this were done, it would no longer be possible to verify that software operation is normal.
Countermeasure/ measure of checking		1. Let the program run away to test the cooperative protective functions. 2. Degenerate the hardware signal to test the cooperative protective functions.
Reference items		

With the development of digital processing technology including microcontrollers, it has become possible to let this technology perform very sophisticated judgments. At the same time, the number of cases of completely unexpected types of malfunction has been increasing. Between the hardware component manufacturer and the user who develops a system and software, great difficulties occur when malfunction is intermittent. In systems in which a high degree of reliability is required, it must be considered that not only in cases of frequent occurrence of a fault but also in case of a fault that occurs infrequently and might be difficult to reproduce it in a test, an error logging function should be built into the system. In the case of a microcontroller with a stored program, electronic components such as the register and memory can change the flow of the program. A function should be included in the system so that when abnormal operation is detected, the data from these important parts will be stored and can be investigated later. This will greatly contribute to finding leads that can be followed up to solve the problem. If possible, if, in addition, there is also a Data Load and Go function to access the RAM area, greater analysis power will be obtained.

- Example 46

  Microcontroller Intermittent Failure Analysis

No. 46	Example	Analysis of intermittent failures in microcontrollers
Type of device		Microcontroller
Point		In analysis of intermittent defects, search for the cause starting from differences in the contents of RAM and registers during normal and erroneous operation.
Summary of example/ phenomenon/ cause		In a product that used a microcontroller, the program ran away intermittently, but the cause could not be determined and efforts to solve the problem took a long time. Since the device was being used in single-chip mode, the history of data changes on the address and data lines during the malfunction could not be ascertained; it was not possible to determine the reason for the microcontroller going into runaway execution from the data on the output pins alone.
Countermeasure/ measure of checking		If it is confirmed that a problem has occurred but the failure is an intermittent one that occurs very infrequently, information regarding the problem will always remain in variable data areas. These data can also be used effectively as the information indicating that the logic of some parts operated correctly by elimination method. In applications that require high reliability, consideration should be given to incorporating an error logging function from the beginning of development, and the system designed so that the cause of malfunction can be determined logically and appropriate action taken.
Reference items		

6.8 Failure-Detection Ratio during Test

As LSIs become faster and more complex, it becomes increasingly difficult to test the performance of the LSI. Generally, as far as memory devices are concerned, 100% of failures can be easily detected during test. However, it is difficult to prepare a perfect test pattern and test conditions that accurately simulate all on-board memory device operations. The difficulty arises from the fact that the test pattern and test conditions depend on various factors such as input signal waveform, timing, data patterns, and address patterns.

Typical memory test patterns are as follows:

1. All-1 or all-0 pattern
2. Checker or checker-bar pattern
3. Diagonal pattern
4. Address-decode pattern
5. Data retention test pattern
6. Marching pattern
7. Long-cycle test pattern
8. Walking pattern
9. Galloping pattern
10. Ping-pong pattern

Typical points to note are as follows:

1. Influence of adjacent bits
2. Interference between data lines
3. Interference between word lines
4. Output noise
5. Sense-amplifier switching timing and timing of input signals
6. Stability of potentials of internal signal lines
7. Switching timings of the ATD circuit and other signals
8. Input-noise sensitivity
9. Input-signal undershoot

Unlike memory devices, it is virtually impossible to test all the internal signals of microcontroller ICs and application-specific digital-signal processor logic ICs because of their complex logic. In particular, since memory circuits have pattern dependency as described above, and devices such as microcontrollers are combinations of large-scale logic circuits, it is impossible to eliminate manufacture-related failures effectively unless systematic measures for achieving satisfying detection ratios are taken as early as possible in the phase of testing circuit design. When the logic is highly complex, the device logic must be configured such that it allows the internal RAM to be externally and directly tested in the test mode.

- Example 47

  Testing Design of Devices with Internal RAM

No. 47	Example	Testing design of devices with internal RAM
Type of device		SoC
Point		RAM and registers must be able to be tested independently.
Summary of example/ phenomenon/ cause		Malfunction occurred frequently in an SoC/LSI with incorporated memory elements such as RAM due to an unknown cause. It was difficult to eliminate failures using the test program. By failure analysis, it was found that the malfunction was caused by an internal RAM failure dependent on the data pattern. However, the RAM module was difficult to test because the relevant SoC/LSI allowed the internal RAM to be accessed only through logic paths. Although specific measures were taken by adding patterns against each failure, effective RAM testing was impossible and thus data-dependent manufacture-related failures could not be eliminated completely using the test program. Therefore, an on-board RAM test had to be implemented.
Countermeasure/ measure of checking		1. Internal RAM circuits must be externally and directly accessed. 2. Failures of the devices with the internal RAM that can only be internally accessed can be eliminated during an on-board test.
Reference items		

Dielectric breakdown is one of the inevitable failure modes of MOS devices. This failure mode requires burn-in, that is, a highly costly screening method, to obtain high-quality products. As a 100% failure-detection ratio can be easily achieved for memory devices, the burn-in saturation is directly connected to the expectant product quality on the market. However, logic ICs, for which a 100% failure-detection ratio cannot be achieved due to the mechanisms involved and for economic reasons, are shipped with some logic circuits remaining to be burnt in because of the low detection ratio obtained by the burn-in pattern. In order to systematically eliminate from the market the failures that were not detected by the test pattern, product quality must be controlled while identifying and relating such conditions statistically and rationally.

- Example 48

  Burn-in Saturation and Detection Ratio

No. 48	Example	Burn-in saturation and detection ratio
Type of device		Microcontroller
Point		The appropriate burn-in pattern must be used.
Summary of example/ phenomenon/ cause		Appropriate burn-in has a positive affect on device lifetime in the future. In the Weibull distribution approximation, the virtual shape parameter *m* approaches 1 with the increasing numbers of burn-ins. If the user should encounter any initial failure with exceptionally small *m*, the likely causes are as follows: 1. The manufacturer did not perform burn-in. 2. The sections that were not subject to burn-in operation by the manufacturer caused the failures. 3. Some novel causes of initial failures have been generated (causing breakdown).
Countermeasure/ measure of checking		1. Analyze failures and see whether or not the failed sections can be detected by the test program. 2. Analyze failures and see whether or not the failed sections can be operated by the burn-in pattern.
Reference items		

If the scale of logic complexity increases further despite the limited failure-detection ratio by testing, the number of untested lines would also increase. As the undetected failure rate is proportional to the number of untested lines, it seems that only unacceptably low quality products will be manufactured in the near future. However, this is not the case. Specifically, if the yield in production processes is maintained at the appropriate level, the current undetected failure rate can be retained even if the logic scale increases. If the yield cannot be maintained at the appropriate level and defect-repairing circuits or equivalents are not used to improve the yield, the untested failure rate will be so high that it can no longer be ignored. In short, improving the yield is very effective in maintaining product quality.

- Example 49

  Logic Scale and Undetected Failures

No. 49	Example	Logic scale and undetected failures
Type of device		SoC
Point		The fraction defective in the untested sections by the test program must be estimated.
Summary of example/ phenomenon/ cause		It is anticipated that the increasing logic scale will lead to an increased failure rate in the untested sections because the fraction defective in the untested sections by the test program is simply proportional to the number of untested patterns. However, the fraction defective in the untested sections will be the same in spite of the increasing logic scale if the yield-related production quality (production quality) and the test-detection-ratio-related design quality (design quality) are maintained at the current level. This is because the defect density itself decreases in spite of the increasing logic scale as long as the yield is maintained at the same level. It must be noted that this is true only when defects are random, and does not hold for non-random defects such as specific layout, circuit function, and performance faults, which are not tested.
Countermeasure/ measure of checking		1. Estimate the fraction defective in the untested sections based on the random-defect ratio. 2. Improve the production process to eliminate non-random defects.
Reference items		

The yield usually does not correspond well to the undetected failure rate. This may be because many multiple defects are contained in yield-defective products. As multiple defects exhibit multiple failures simultaneously, the detection ratio will be exceptionally high, thus allowing the products to be screened out. The undetected failure rate can be controlled by effectively selecting single defects from yield-defective products and exclusively controlling these single defects.

- Example 50

  Single Defects, Multiple Defects, and Undetected Failures

<table>
<tr><td>No. 50</td><td>Example</td><td>Single defects, multiple defects, and undetected failures</td></tr>
<tr><td colspan="2">Type of device</td><td>SoC</td></tr>
<tr><td colspan="2">Point</td><td>Single defects must be separated from multiple defects.</td></tr>
<tr><td colspan="2">Summary of example/ phenomenon/ cause</td><td>It is anticipated that the increasing logic scale would lead to the increased yield failure rate in the undetected sections. If the same ratio of single defects and multiple defects are detected, fraction defectives are different if they are missed by the test program. It must be noted that almost all undetected failures are from single-defect products when the detection ratio is high.</td></tr>
<tr><td colspan="2">Countermeasure/ measure of checking</td><td>1. A single-defect ratio is estimated by burn-in failure rate.
2. The undetected failure rate is estimated by the single-defect ratio.</td></tr>
<tr><td colspan="2">Reference items</td><td></td></tr>
</table>

6.9 Precautions in Packaging

General precautions in storage and transport of electronic components can be applied directly to semiconductor devices, but there are additional points that require caution. An explanation of some relevant general items is given below.

Recent semiconductor devices are of high quality and high reliability, but depending on such factors as handling by the user, mounting and the conditions of use, there are many factors that can lead to damage of the device (electrostatic discharge, mechanical destruction, moist gas, etc.). First, let us discuss precautions with regard to possible damage of devices in the storage case and during packaging.

(1) The Storage Case

(a) Semiconductor manufacturers use storage cases of materials and construction that will maintain the initial quality even under the worst environmental conditions, so use the storage case specified by the manufacturer as much as possible.

(b) If the storage case specified by the manufacturer cannot be used, use a storage case that satisfies the following conditions.

- The material will not trigger a chemical reaction or emit a harmful gas.
- The construction protects the device from damage by vibrations and shocks.
- The case material that leads of the device will contact is either electrically conductive or ESD safe.

(c) When removing a device that is vulnerable to destruction by static electricity, such as a high frequency device or an MOS device, from its storage case, discharge any electrical charge on the body and clothing through electrostatic high-resistance (about 1 MΩ to the ground), then remove it from the storage case using electrically conducting finger stole or gloves.

(2) Packaging

A semiconductor device in a storage case must be further packaged to protect it from outside effects such as a shock, rain water and soiling. The packages used for some common products are shown in figure 6.22.

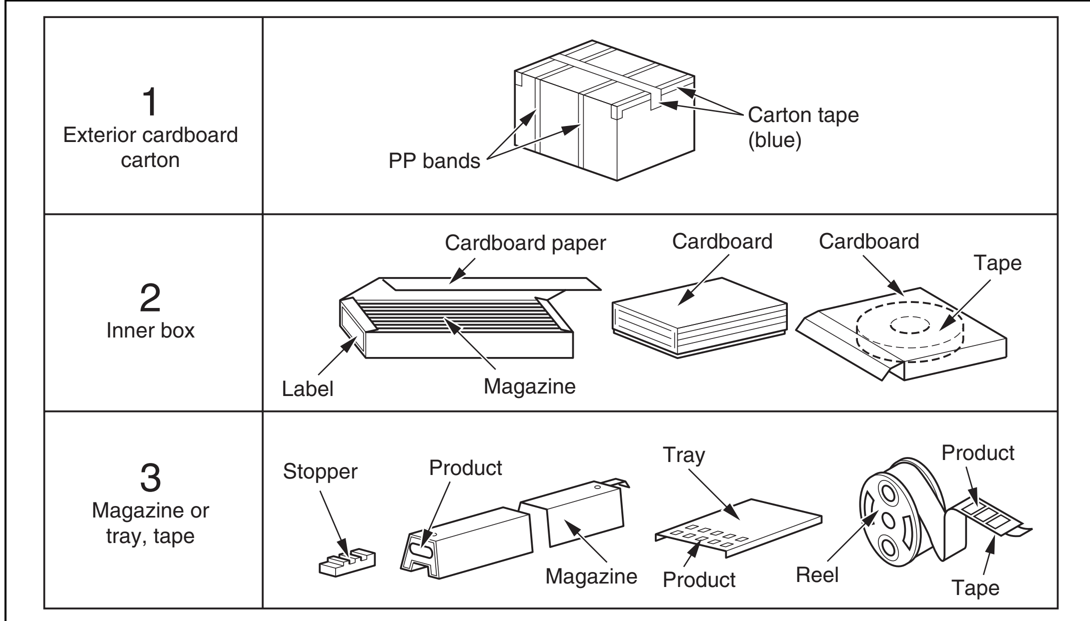


Figure 6.22 Example of Packaging

Opening the exterior cardboard carton reveals an inner box or boxes, inside of which is the storage case (magazine, tray or tape and reel), inside which the ICs reside. In the case of plastic surface-mount packages which have large chips, there is also moisture-proof packaging to prevent moisture absorption. Next, we give some precautions in packaging.

(a) To keep the shock, vibrations and moisture to which the semiconductor device is subjected to a minimum, it is necessary to give serious consideration to using packaging that has sufficient mechanical strength, ability to withstand vibrations and ability to block moisture to meet the requirements of the transport method to be used. In general, the storage case is securely wrapped in polyurethane foam or vinyl, which in turn is put into a cardboard carton with sufficient packaging material to prevent vibrations, then the carton is closed with gummed tape. Depending on the transport conditions, more secure packaging may become necessary.

(b) The outside of the cardboard carton should be labeled to indicate that the contents are fragile, must not be allowed to become wet and which direction is up.

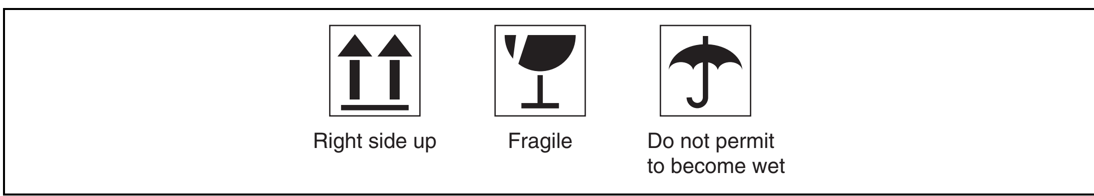


Figure 6.23 Examples of Exterior Labeling

(c) If poor environmental conditions are anticipated, as in transport by sea, it is necessary to use vacuum packaging and sealed packaging.

(d) The surfaces of transparent plastic magazines are treated to prevent them from becoming electrically charged, but this surface treatment wears off over time, so these magazines should not be used for storage for more than six months. Never reuse the magazines.

6.10 Storage Precautions

When storing semiconductor devices, it is necessary to protect them from environmental dangers including temperature, humidity, ultraviolet rays, poisonous or contaminating gases such as hydrogen sulphide, radiation including X-rays, static electricity and strong electromagnetic fields.

(1) Storage environment

(a) Ambient temperature and humidity

The storage location should be kept at normal temperature and humidity, that is 25 to 35°C and 45 to 75% relative humidity (some products have special restrictions on storage conditions, which should be observed). Care must be taken to avoid storage under temperature and humidity conditions that are significantly different from these. When it is very dry, such as during winter, it is necessary to use a humidifier. If tap water is used in the humidifier the chlorine in it can corrode leads of devices, so purified or distilled water should be used.

(b) Atmosphere and cleanliness

Avoid storage in a location with corrosive gas or a large amount of dust.

(c) Temperature variations

Sudden temperature variations can cause condensation to form on devices and/or packing material, so avoid such an environment, and store devices in a location where temperature variations are small and slow (and away from direct sunlight or other strong light).

(d) Electrical and electromagnetic environment

Store devices in a location with free of radiation, static electricity and strong electromagnetic fields.

(2) Storage Conditions

(a) In storing semiconductor devices, it is necessary to make sure that they are not subjected to heavy loads. In particular, when boxes are stacked, it is possible to subject the semiconductors to excessive loads without realizing it. Of course it is also necessary to avoid placing heavy objects on top of them.

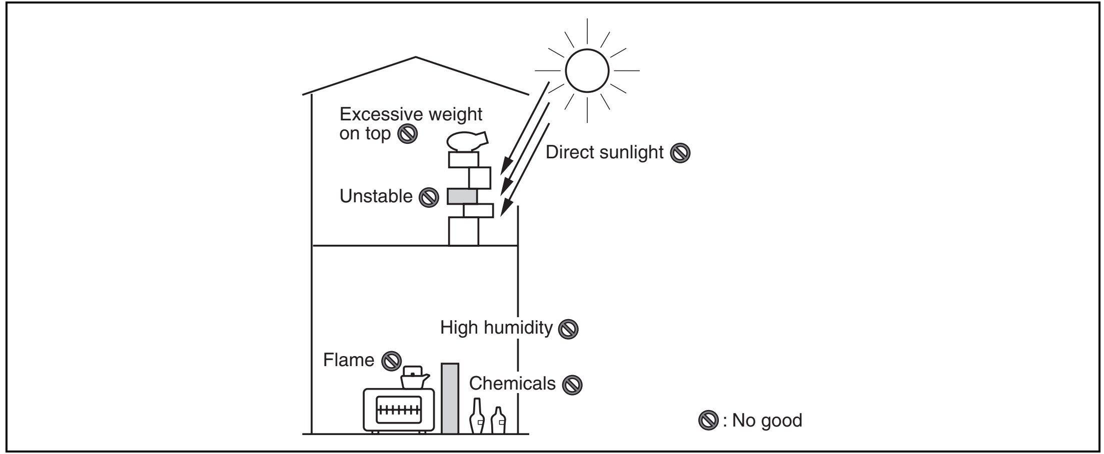


Figure 6.24 Examples of Poor Storage Locations and Practices

(b) Store semiconductor devices without processing their external leads. This is to avoid degrading the adherence of solder during mounting due, for example, to rust.

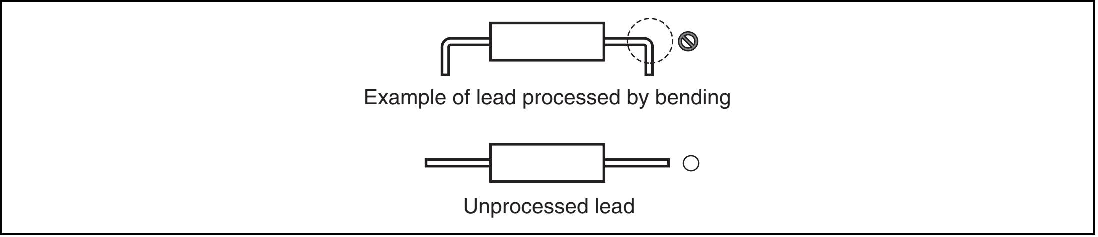


Figure 6.25 Storage Condition

(c) Place semiconductor devices only in containers that do not readily become electrostatic-charged.

(3) Long-term Storage

If a semiconductor device is stored for a long time (1 year or more), there is danger that the lead terminals can become difficult to solder, perhaps even rust, and/or can suffer deterioration of electrical characteristics. In particular, the following precautions are necessary.

(a) Storage environment: See (1) above.

(b) If long-term (1 year or more) storage is envisioned from the beginning, take such precautions as using vacuum packaging or a sealed container into which silica gel is inserted.

(c) If a semiconductor device is stored under ordinary storage conditions and for a long time (1 to 8 years) has elapsed, before using the device it is necessary to determine if it can still be easily soldered and if it has rusted.

(d) Storage in a poor environment, or long-term storage under ordinary storage conditions

Devices that have been placed in an extremely poor environment or stored under normal conditions for one year or more must be examined for solderability, including rusting of the leads, and electrical characteristics (packages for surface mounting are covered in section 6.4.2). Use TAB products within three months of their manufacture.

(e) Although products in moisture-proof packaging can be stored for 10 or more years, this does not guarantee the quality. If the package is opened and then resealed within this period, we recommend the use of a fresh desiccant.

If a semiconductor device is stored in a very poor environment, or is stored under ordinary storage conditions and 1 year or more has elapsed, it is necessary to determine whether it can still be easily soldered, if it has rusted, and if there has been any change in its electrical characteristics (for surface-mount packages, see section 6.4.2). Use TAB products within 3 months.

(4) Storage of Chips and Wafers

Semiconductor chips and wafers must be stored under more strictly controlled conditions than package products. Absolutely avoid storing chips and wafers in conditions in which they are exposed to the outside air.

(a) Storage of chips and wafers

Store chips and wafers in the designated types of containers, and do not open and close the containers any more than necessary. Normally, chip storage containers are airtight sealed to protect chips and wafers from temperature, humidity and corrosive gases, and from vibrations and shock during transport.

(b) Do not store chips and wafers in opened containers. This is to prevent the chips and wafers from being oxidized or corroded due to changes in temperature and humidity, and the presence of gases, dust and chemicals.

(c) Store chips and wafers in an atmosphere at 5 to 30ºC and 45% to 75% RH, where they will not be affected by chemicals or volatile substances.

(d) When putting a chip into or taking it out of a storage container, handle it gently using vacuum tweezers or a vacuum collet so that the surface will not be scratched.

(e) The chip should be mounted within 5 days after the sealed storage container is opened. When work is not being performed, as at night, the component should be stored in a dried nitrogen atmosphere. If the sealed storage container has been opened, the component should be stored in dried nitrogen (with the dew point of –30ºC or below) for not more than 20 days; if the storage container is still sealed, it should be stored for no longer than three months.

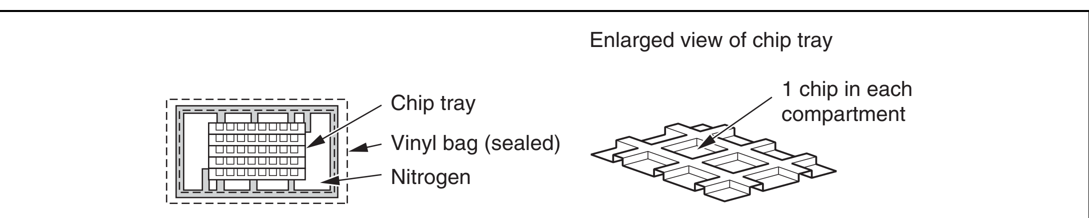


Figure 6.26 Examples of Chip Storage Containers

- Example 51

  Solderability Defects that can Develop during Storage

No. 51	Example	Solderability defects that can develop during storage
Type of device		IC
Outline of example		Magazines made of cardboard paper and black rubber were used for IC storage, causing the device lead wires to become discolored and leading to solderability defects. The lead surface material was converted to sulphide by sulphur compounds contained in the storage magazines.
Countermeasure		Storage cases and magazines made of material that does not react with the lead wires should be used. In particular, sulphur compounds must be avoided.

6.11 Precautions in Transport

In transport of semiconductor devices and of units and subsystems which incorporate semiconductor devices, the same precautions must be observed that are necessary for other electronic components; in addition, the points listed below must be considered.

1. Handle the cardboard cartons used as the exterior packaging carefully. In particular, be careful not to subject them to shocks or drop them as this can damage the products inside.
2. Be particularly careful in handling the interior boxes.

   If these are dropped, stoppers can fall out of the magazines inside allowing the products to fall out and causing the leads to become deformed. Ceramic packages can be damaged, causing leakage defects.
3. It is necessary to make sure that the products do not become wet. Be particularly careful when transporting them through rain and/or snow (Do not permit products to become a wet).
4. Transport containers and jigs must not be easily charged and not generate electrostatic charge when subjected to vibrations. One effective measure is to use conducting containers or aluminum foil.
5. To prevent components from being destroyed by electrostatic charge on the body and/or clothing, ground the body through a high resistance to discharge static electricity when handling semiconductor devices. The resistance should be about 1 MΩ. It is necessary for the resistor to be inserted into the connection between body and ground at a position relatively close to the body to prevent danger of electrical shock.
6. In transporting a printed circuit board with semiconductor devices mounted on it, it is necessary to take a measure, such as shorting the lead terminals to keep them at the same potential, to prevent them from becoming charged with static electricity. If a printed circuit board is transported on a belt conveyor, take an appropriate measure to prevent electrical charging by the belt rubber.
7. When transporting a semiconductor device or printed circuit board, keep mechanical vibrations and shocks to an absolute minimum.
8. Wafer shipments particularly must be handled very carefully to prevent vibration and shock during transport and movement.

6.12 Product Safety

(1) Efforts to Ensure Product Safety

Since July 1995 the Product Liability (PL) Law has been in effect in Japan, but even before that our company considered safety an integral element of product quality and has promoted safety of semiconductor products as part of our efforts to improve them.

Our company's basic philosophy on product safety and efforts to improve it are as follows.

The product safety of our company's products is the normal level of safety required of the semiconductor products themselves; the user must assume full responsibility for meeting safety requirements connected with the way these products are used and the environment in which they are used.

(a) Product safety measures from the beginning

In the flow of, for example, the reliability program examples and quality certification flow, requirements for product safety are specified; safety considerations form an integral part of the decision to use a product, development and design. The principal safety measures that are taken in the major steps from product development through shipment are listed in table 6.11.

Table 6.11 Principal Product Safety Measures

Principal Categories	Considerations (main points)
Product Development	On the way the user uses the product
Determination of Specifications	On the environment in which the product is used
Design	On destruction mode On malfunction mode
Manufacture	Observance and clarification of manufacturing rules
Quality Assurance	Quality assurance and evaluation checks at each stage of production
Sales	Issuance of documents

(b) Documentation

In order for semiconductor products to be used safely, there are a number of documents including data sheets that indicate the product performance. We also issue a number of documents specifically related to product safety so that the maximum utilization can be taken of the product specifications.

Table 6.12 Documents Concerning Product Safety

Category	Examples of Specific Documents
Documents that give product specifications	Data sheets, Data books, Technical information, Delivery specifications (Purchase specifications), etc.
Documents that give precautions in use	Reliability hand Book, Renesas Surface Mount Package User's Manual, etc.
Other documents (documents prepared for individual users)	Sale agreements, Quality agreements, etc.

(c) Consultations on specifications and quality

Quality consultations are held to assist the user in using the products under conditions that are appropriate for the product specifications. As stated above, these conditions are announced in a variety of documents, but discussion are held in order to give more detailed conditions for use and help the user to select the most suitable product for each application.

6.13 Examples of Other Categories of Problems

Finally, we introduce several examples that do not fit into any of the categories that have been presented thus far.

- Example 52

  Tape Peeling Off Caused by High-Speed Peeling in the Case of Tape and Reel Products

No. 52	Example	Tape peeling off caused by high-speed peeling in the case of tape and reel products
Type of device		Embossed taping products
Point		The strength of embossed tape to being peeled off should be measured at the actual speed to be used.
Outline of example/ phenomenon/ cause		Even though no problem occurred in the embossed taping certification test, the tape frequently peeled off during the users mounting process. An investigation revealed that, in the line in which the defect occurred, the most recent model of high speed mounting machine was being used, and the tape peel-off speed was faster than the previous speed in order to increase the component mounting index time. In a test in which the tape peel-off speed was increased, the defect was reproduced.
Countermeasures/ checking methods		1. In the embossed tape peel-off test, attention must be paid to the peel-off speed. 2. In the embossed tape peel-off test, one must not forget to apply the stress of storage as preprocessing.
Reference item		

- Example 53

  Changes in Characteristics Caused by X-ray Irradiation

No. 53	Example	Changes in characteristics caused by X-ray irradiation
Type of device		MOS IC (plastic sealed)
Outline of example		In an X-ray penetration test, the device was irradiated with X-rays for a long time, and the IC came to have defective characteristics. The IC's MOS parameter (Vth) fluctuated, causing deterioration of characteristics.
Countermeasure		The X-rays with which the device is irradiated should be kept as weak as possible.

- Example 54

  Lifetime Curve Using Cp and Cpk

No. 54	Example	Lifetime curve using Cp and Cpk
Type of device		All semiconductors
Point		The Cp and Cpk fraction defective is given and used effectively in predicting the lifetime.
Outline of example/ phenomenon/ cause		Cp and Cpk provide an effective means not only for PQC but also for testing the product lifetime. When Cp and Cpk are used, it is possible to determine the fraction defective of products which do not meet the standards at that time. That is interpreted as the defect rate at that time. If a Weibull plot of the fraction defective is prepared together with the time duration of the lifetime test, then the shape parameter *m* and the scale parameter η can be determined even if the occurrence of defects is zero. If data are taken under the diversified conditions, then it is even possible to find the acceleration coefficient. Always select items to measure that are correlated with the failure mode.
Countermeasures/ checking methods		1. Cp and Cpk indicate the fraction defectives. 2. The ability to approximate the distribution by a normal distribution is the starting point for using Cp and Cpk.
Reference item		

- Example 55

  Cp, Cpk and Screening

No. 55	Example	Cp, Cpk and screening
Type of device		All semiconductors
Point		Cp and Cpk provide a means of assuring quality without having to test every single device.
Outline of example/ phenomenon/ cause		The concept of Cp and Cpk is convenient, but caution is particularly necessary when making a judgment on an item on which screening has been performed. Trying to predict the fraction defective from data after every single device has been tested and defective devices removed is meaningless. If defective devices are removed, the devices that were removed contain important elements. Between the values that are announced outside the company and the values used in the final test, the following indeterminate factors are included. 1. Measurement tolerances 2. Temperature corrections 3. Deterioration of reliability
Countermeasure/ checking method		When screening is performed, look carefully into the margin between the external standards applied outside the company and the classification standards.
Reference item		

- Example 56

  Bonding Stress in Mounting Chips that Have Been Shipped

No. 56	Example	Bonding stress in mounting chips that have been shipped
Type of device		Power MOS FET
Point		The oxide film below the bonding pad is destroyed by the stress of bonding.
Outline of example/ phenomenon/ cause		When the characteristics of chips that had been shipped (power MOS FETs) were tested after mounting by the user, the breakdown voltage between source and gate was insufficient. As a result of analysis, it was judged that the oxide film below the gate bonding was cracked, causing the breakdown voltage to deteriorate. The cause was inadequate checking of the conditions at the time of mounting.
Countermeasure/ checking method		After the bonding conditions are set, the characteristics need to be checked, and, at the same time, the aluminum film below the bonded section should be removed and the silicon oxide film should be checked for cracking.
Reference item		

- Example 57

  Leakage from Airtight Seal due to Electrolytic Corrosion

No. 57	Example	Leakage from airtight seal due to electrolytic corrosion
Type of device		Glass diode
Point		A voltage must not be applied to a product to which moisture is adhering.
Outline of example/ phenomenon/ cause		Copper oxide (Cu_2O) that forms on the surface of the copper layer of a Dumet line diffuses into the glass, bonding to form an airtight construction. While a reverse bias is applied, water that adheres to the diode surface is decomposed electrolytically by reverse bias, and hydrogen (H_2) is generated on the anode side. This hydrogen reduces the cuprous oxide; water penetrates where the reduction took place, producing a cavity and destroying the airtightness. Destruction of the airtightness in turn permits more moisture to penetrate into the cavity. Moisture penetration produces a leakage current on the surface of the chip, increasing the reverse current (IR). If the reverse bias continues to be applied while the reverse current is flowing, migration of the silver (Ag) electrode of a chip occurs.
Countermeasure/ checking method		The IR becomes large due to fluctuations in the electrical characteristics. View the inside from the glass package.
Reference item		Renesas Diode Data Book

- Example 58

  Signal Data Collision

No. 58	Example	Signal data collision
Type of device		IC, LSI
Outline of example		For memory ICs having common input/output terminals, when data is at output state and an input signal with the opposite direction is applied, data collision will occur and generate excessive current flow. The resulting supply voltage variation may cause malfunction or device destruction.
Countermeasures		1. Timing Design should be made to prevent data collision. 2. Timing should be changed using latch.

- Example 59

  Destruction of Device due to Condensation

No.59	Example	Destruction of device due to condensation
Type of device		Power MOS FET
Outline of example		Although we knew that products already on the market were regularly being destroyed by condensation, we had difficulty determining the cause of the defect from destroyed devices. In fact, however, the problem was occurring only with the same model of a product purchased by particular customers. Our investigation into seasonal occurrence revealed that the problem worsened during the summer season. When we checked the customer's operating environment, we found that the customer had installed a system near the nozzle of an air conditioner. As a result, cold air from the air conditioner caused condensation, leading to leakage between terminals and destruction of the device. Once the system was relocated away from the air conditioner nozzle, the products were no longer being destroyed.
Countermeasures		Check the environment where the product will be used to make sure that it is not a particular kind of environment.

Section 7 Standards and Certification Schemes for the Quality System, Safety, and Reliability of Semiconductor Devices

7.1 Quality System Standards

7.1.1 Overview of the ISO 9000 Series

- The ISO 9000 series are international standards for quality assurance and quality management, which were established in 1987 by ISO (the International Organization for Standardization) based on British BS5750 and U.S. ANSI/ASQC Z1-15. The ISO 9000 series are adopted in more than 50 countries (22 in Europe, 9 in Asia, 4 in North and South America, and the rest in the other regions) as a national standard. In Japan also, the JIS (Japanese Industrial Standards) Z 9900 series, based on the ISO 9000 series, was established in October 1991.
- At one time, the ISO 9000 series was divided into three major parts: ISO 9000, ISO 9001-9003, and ISO 9004. In 2000, however, the series was reorganized as the ISO 9000/2000 version, which is explained below.

7.1.2 ISO 9000 Family Standards (Standards of the Year 2000)

- ISO 9000 (Quality Management System - Basics and Terminology)

  This standard explains the basics of a quality management system and defines the terms used in a quality management system.
- ISO 9001 (Quality Management System - Requirements)

  This standard provides the requirements for a quality management system when an organization needs to demonstrate that it has the capability of providing products that meet customer requirements as well as satisfying any applicable restrictions or when an organization wishes to achieve a higher level of customer satisfaction.
- ISO 9004 (Quality Management System - Guidelines for Performance Improvement)

  This standard provides guidelines that consider both the efficacy and efficiency of a quality management system.

  The purpose of this family of standards is to help an organization improve its performance and satisfy its customers and other interested parities.

(1) Principle of quality management

No organization can be successfully led or managed unless it employs systematic, transparent methods. An organization can become successful only if it implements and maintains a management system designed to allow it to address the needs of all interested parties and constantly improve its performance.

Of the various management norms, quality management should be the top priority in managing an organization. There are eight clear-cut principles in quality management that can be used by an organization's top management when it attempts to improve the organization's performance:

1. Focus on the customer
2. Leadership
3. Participation by people
4. Process approach
5. Systematic approach to management
6. Continual improvement
7. Approach based on decision-making
8. Reciprocal relationship with suppliers

7.1.3 Registration Systems for the ISO 9000 Series

A third party certification registration system is implemented to certify ISO 9000-based company quality systems. This system is established in more than 30 foreign countries (14 in Europe, 7 in Asia, 2 in North America, and the rest in the other regions). The Japanese accreditation body (The Japan Accreditation Board for Quality System Registration) was founded on November 1, 1993. Before this system, Japanese companies were certified by foreign bodies (BSIQA, LRQA, BVQI, etc.) or JQA (Japan Quality Assurance Organization) which is a representative of BSIQA. Owing to the establishment of the Japanese registration system, it became possible for Japanese companies to be certified being accredited by the national government. Figure 7.1 shows a scheme of the system.

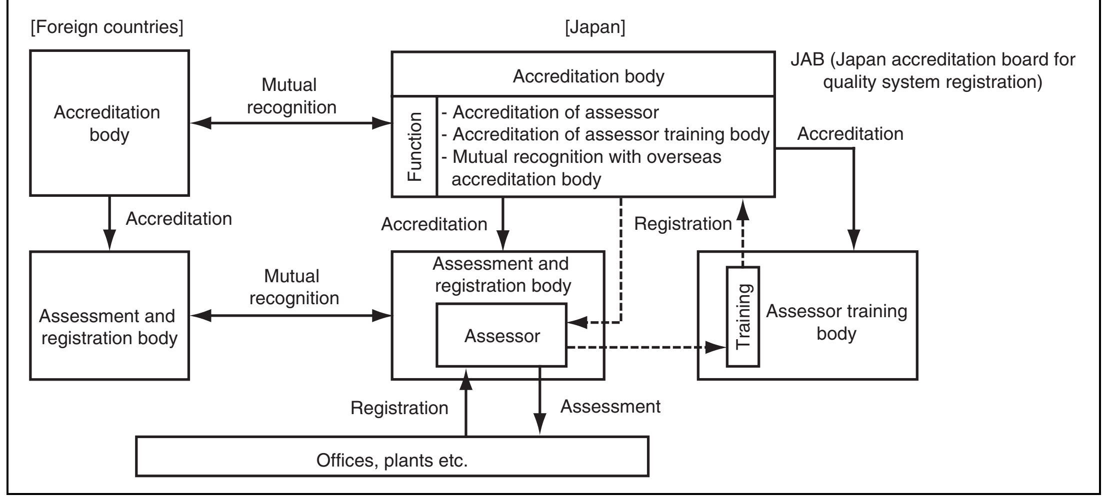


Figure 7.1 A Scheme of the Registration System for Quality Systems

7.2 Safety-Related Standards

7.2.1 Introduction

To ensure the safety of electronic and electric equipment, safe materials and components must be used to construct them. For this reason, standards have been established to prevent hazards such as fire and electric shock.

Some of them are covered by the Electrical Appliance and Material Control Law in Japan. IECQ has IEC Publication 695 (1982) which sets forth implementation methods and guidance for fire resistance tests. In the United States, UL (Underwriters Laboratories) has UL 94 (testing methods for flammability), UL 746 (Insulation Materials), and other standards established for verification and assurance of the safety of electrical appliances, components, materials, etc. Although private standards, UL standards are indeed applied to products designed for US markets. EN (European Standards) are used in Europe, which are duly applied to products shipped for European markets.

These are safety standards established to prevent fire and electric shocks. Product safety in a broader sense is called for today, however. Applicable standards include ISO 9004 (quality management guidelines) and ISO 14000 (Environmental Management Systems). The applicable law in Japan is the product liability law, which was promulgated on July 1, 1994 and enforced on July 1, 1995.

It is expected that various safety standards will be established in the future. Accordingly, product safety should be promoted as a company policy.

7.2.2 CE Marking System

Since the twelve European countries unified their markets and formed the single EU (former EC) market on January 1, 1993, people, goods, services, and capitals have been moving freely in the region. For safe unification of the EU market, regulative barriers should be removed and at the same time minimum regulations should be enforced in terms of safety and consumer protection.

EC Directives include Low Voltage (73/23/EEC), Simple Pressure Vessels (87/404/EEC), Safety of Toys (88/378/EEC), Construction Machinery (89/106/EEC), Electromagnetic Compatibility (89/336/EEC), Machinery (89/392/EEC), Personal Protective Equipment (89/686/EEC), Active Implantable Medical Devices (90/385/EEC), Non-automatic Weighing Instruments (90/384/EEC), Gas Appliances (90/396/EEC), Telecommunication terminal equipment (91/293/EEC), Medical Devices (93/42/EEC), Machinery in Explosive Atmospheres (94/9/EC), etc.

Manufacturers of final products (products that can be used as they are) are required to issue an "EC declaration of conformity" to indicate conformity to standards, prepare and preserve evidences (technical documents and engineering files) verifying conformity to standards, establish quality systems to ensure maintenance of quality and continued production, and develop an organization for submitting evidences. In the final stage, "CE Marking" should be indicated on the product itself or box to prove that the product fulfills the unified standards. This is known as the "CE Marking" system.

Among these directives, the EMC Directive enforced on January 1, 1996 has a significant impact on semiconductor devices.

Along with increasing use of radio waves and diffusion of electronic equipment, there has arisen a great concern over electromagnetic interference with equipment and systems caused by other equipment and systems. Not only to take EMI measures for controlling the source of interference, but also to make improvements in immunity on the interfered part is necessary to minimize deterioration of performance in the above-mentioned electromagnetic environment.

The EMC Directive regulates equipment and system capability taking both into consideration.

7.3 Reliability-Related Standards

7.3.1 Introduction

The MIL standards governing the reliability of semiconductor devices are authoritative and well recognized. Recently, the Japanese Industrial Standards (JIS) have been undergoing a process of revamping in response to the registration of the JEDEC standard under the EIA in the U.S. and formation of IEC (International Electrotechnical Commission) Quality Certification.

International bodies publicly issuing reliability standards include CECC (CENELEC Electronic Components Committee) in addition to JEDEC and IEC. Domestically, in addition to the Japanese Standards Association, the body issuing JIS, we have EIAJ (Electronic Industries Association of Japan) and RCJ (Reliability Center for Electronic Components of Japan). Standards and specifications of these bodies are used as basic data for establishing and revising JIS.

This section provides an overview of JIS, JEITA, JEDEC, IEC, CECC, and MIL standards and specifications as they relate to the reliability of semiconductor devices. Table 7.1 lists principle standards and specifications available from these bodies.

7.3.2 JIS Standards

JIS C5700 provides general rules for reliability assured electronic components including common necessary elements in such areas as reliability assurance programs, approval testing, quality assurance inspections, and periodic certification maintenance testing. It is basically intended to be in accord with the IEC "General Rules and Specification Standards to Be Applied to Quality Certification for Electronic Components."

There has arisen a need for filing as domestic standards the standards established by the IEC electronic components quality assurance system. JIS C 0010, 0022, and similar standards are based on IEC standards and modified for Japanese conditions. Testing methods pertaining to environmental factors (Publication 68) are laid down.

7.3.3 JEITA (EIAJ) Standards

The EIAJ ED-4701 standard was created from a review and merging of the contents of SD-121 (discrete semiconductors) and IC-121 (integrated circuits). The first version of SD-121 was published in December 1971 and the second version in March 1984. The EIAJ ED-4701 standard has also standardized the vapor pressure test, pressure reduction test, and other new testing methods for which there are no JIS counterparts.

It also covers the electrostatic discharge test, high-temperature/high-humidity bias test, and other tests, and has added a method for testing special packages. The method for electrostatic discharge testing was revised in 1988, when a standard for current waveforms was also added. In November 2000, the Japan Electronics and Information Technology Industries Association (JEITA) was formed through a merger of the Electronic Industries Association of Japan (EIAJ) and the Japan Electronic Industries Development Association (JEIDA). In August 2001, the JEITA published a new set of standards (consisting of six volumes) as the EIAJ ED-4701 series, including the supplementary Version 4. Since then, these standards have been adopted by a large number of Japanese domestic semiconductor manufacturers as the basis of their own reliability test standards.

7.3.4 JEDEC Standards

JESD22 is a set of standards covering reliability testing of individual semiconductor electronics components. J-STD, which is a set of joint standards established by the Joint Electron Device Engineering Council (JEDEC) and the Institute of Interconnecting and Packaging Electronic Circuits (IPC), provides a set of standards mainly covering reliability testing for mounting and connecting components on boards. In 1960, the JEDEC itself was formed under the umbrella of the Electronic Industries Alliance (EIA) in the United States for the primary purposes of standardizing semiconductor products, presenting the results of surveys and statistics related to the electronics industry, standardizing a variety of technologies, and making proposals to the U.S. government. At present, these standards have essentially replaced the MIL specifications, which used to be the de-facto standard for semiconductor testing, as standard specifications not only in the United States but also throughout the world.

7.3.5 IEC Standards

IEC Publication 68 covers environmental testing methods for electronic equipment and components and was established as an IEC recommended document in 1954. It consisted of Part 1 (General), Part 2 (Tests), and Part 3 (Background Information), and for each test category, was revised and appended. Publications 747 (Discrete Semiconductors), 748 (Integrated Circuits), and 749 (Environmental Testing) were issued in 1982, completely revising Publications 147-0 to 147-5, 148, and others. Devices that had been classified according to their rating, characteristics, and methods of measurement were rearranged by their models for ease of understanding. Publication 747 consists of 747-1 through 747-10. These include general rules (747-1), rectifier diodes (747-2), signal diodes (737-3), and other types of devices up to 747-9. Section 747-10 contains common specifications. Publication 748 comprises 748-1 through 748-4, and includes general rules, digital, analog, and interface specifications. Publication 749 sets down mechanical and weatherability testing methods for discrete semiconductor devices and integrated circuits. This publication is based on former Publications 147-5 and 147-5A.

7.3.6 CECC Standards

CECC 50000 and CECC 90000 are the common specifications for discrete semiconductor devices and integrated circuits of CENELEC (Comite European des Normalisation Electrotechnique). CECC 50000 contains general rules for various categories corresponding to JIS C 7210. CECC 50001 to CECC 50007 correspond to JIS standards for these categories. For each category, reliability assurance requirements and individual standard specifications are stipulated.

7.3.7 MIL Standards

MIL-S-19500 is the general specification for discrete semiconductor devices. It covers common requirements for procurement by the U.S. military, including the accreditation procedure, items and conditions for screening and type identification, and rules for preparing individual specifications.

MIL-STD-202 specifies mechanical and environmental testing methods for electronic and electrical components and corresponds to IEC Publication 68.

MIL-STD-750 specifies mechanical, environmental and durability testing methods and conditions for discrete semiconductor devices. This standard applies to test methods and conditions required in MIL-S-19500. Corresponding standards include JIS C 7201 and EIAJ SD-121.

MIL-STD-883 establishes test methods and other procedures for integrated circuits. It provides general requirements, mechanical, environmental, durability and electrical test methods, and quality assurance methods and procedures for procurement by the U.S. Military. This standard applies to test methods and conditions required in MIL-M-38510.

7.4 Certification Systems

7.4.1 Mutual Relationships of Certification Systems in the World

Recently, internationally harmonized certification systems are increasingly established and use of certifications in many regions is promoted to cope with trade liberalization. With regard to international harmonization of standards and certification systems, the World Trade Organization (WTO, former GATT) indicated guidelines in the TBT Agreement (an agreement on technical barriers to trade) in 1980.

The EU (European Union) adopted a comprehensive product certification system compatible with the guidelines. Since 1995, the EU has been implementing the CE Marking system according to new rules.

International standardization bodies such as ISO and IEC are also undertaking development of standards and guidelines for supporting the TBT Agreement. (ISO 9000S quality systems etc.)

Figure 7.2 shows the conformity assessment system indicated in the TBT Agreement.

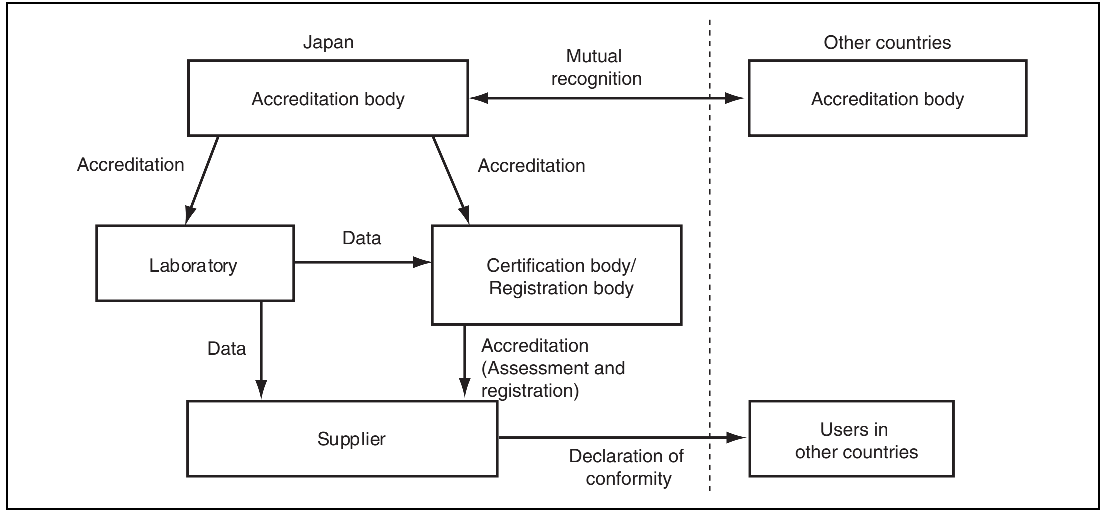


Figure 7.2 Conformity Assessment System Indicated in the TBT Agreement

To sign an MRA (Mutual Recognition Agreement) recommended in the TBT Agreement, it is necessary between countries concerned to make consistent to a certain degree laws governing companies' responsibilities. Similar conformity assessment systems and technology levels should also be maintained.

Accordingly, MRAs are signed in each area where consistency is ensured. If, however, different standards are used in countries concerned, conformity assessment should as a rule be conducted according to the other country's standards. Therefore, an MRA cannot be expected to be practically effective if the countries concerned use substantially different standards.

ISO/IEC Guides set out guidelines in this respect. The EU has developed EN standards following these guidelines. Internationalization of JIS standards will also be promoted in Japan.

7.4.2 Reliability Certification Systems for Semiconductor Devices

In 1970, the "Certification System for Electronic Components (CECC)" was established under CENEL (Comite Europeen de Cordination des Normes Electrotechniques) in Europe as a semiconductor device certification system. Later, this system was adopted by IEC to promote it on a global scale as its own system.

With regard to electronic component certification systems in IEC, PMC (Preparatory Managing Committee) was established in 1971 to study the feasibility of mutual certification of electronic components. A quality certification system was established in IEC in 1976. This led to the founding of CMC (Control Managing Committee) in the same year, and tentative ICC (Inspection Control Committee) in 1977. Thereafter, rules for the operation of systems were established and mutual inspections of systems among member countries were conducted. In January 1982, the IEC Quality Assessment System for Electronic Components, namely, the IECQ system commenced formally. Basic rules and enforcement regulations were promulgated along with the inauguration of certification activities. CECC certification systems have transferred to this system step by step.

The Japanese Industrial Standards Committee is the national agency in Japan (NAI). Approval is granted by the Reliability Center for Electronic Components of Japan as the supervision and inspection body (NSI).

Table 7.1 Major Standards for Reliability and Quality Management of Semiconductor Devices And ICs

(1) JIS standards

Number	Title	Established
JIS C 60068-1	Environmental testing Part 1: General and guidance	1993
JIS C 60068-2-1	Environmental testing procedures Part 2: Tests, Tests A: Cold	1995
JIS C 60068-2-2	Basic environmental testing procedures Part 2: Tests, Test B: Dry heat	1995
JIS C 60068-2-3	Basic environmental testing procedures Part 2: Tests, Test Ca: Damp heat, steady state	1987
JIS C 60068-2-11	Basic environmental testing procedures Part 2: Tests -- Test Ka: Salt mist	1989
JIS C 60068-2-52	Environmental testing -- Part 2: Tests -- Test Kb: Salt mist, cyclic (sodium, chloride solution)	2000
JIS C 0025	Basic environmental testing procedures Part 2: Tests Test N: Change of temperature	1988
JIS C 0027	Basic environmental testing procedures Part 2: Tests Test Db: Damp heat, cyclic (12 + 12-Hour cycle)	1988
JIS C 60068-2-13	Basic environmental testing procedures Part 2: Tests, Test M: Low air pressure	1989
JIS C 60068-2-6	Environmental testing Part 2: Tests -- Test Fc: Vibration (sinusoidal)	1999
JIS C 60068-2-27	Basic environmental testing procedures Part 2: Tests, Test Ea and guidance: Shock	1995
JIS C 60068-2-29	Basic environmental testing procedures Part 2: Tests Test Eb and guidance: Bump	1995
JIS C 60068-2-21	Environmental testing -- Part 2-21: Tests -- Test U: Robustness of termination and integral mounting devices	2002
JIS C 5003	General test procedure of failure rate for electronic components	1974
JIS C 7032	General Rules for Transistors	1993
JIS C 7030	Measuring methods for transistors	1993
JIS C 7031	Measuring methods for small signal diodes	1993
JIS Z 8115	Glossary of terms used in dependability	2000

(2) JEDEC standards

Number	Title	Established
J-STD-	Joint IPC/JEDEC Standard	1999-2003
JESD22-	JEDEC Standard	1997-2005

- J-STD-(Joint IPC/JEDEC Standard) individual standards

Number	Title	Established
J-STD-002B	SOLDERBILITY TESTS FOR COMPONENT LEADS, TERMINATIONS, LUGS, TERMINALS AND WIRES	2003
J-STD-020C	JOINT IPC/JEDEC STANDARD FOR MOISTURE/REFLOW SENSITIVITY CLASSFICATION FOR NONHERMETIC SOLID STATE SURFACE-MOUNT DEVICE	2004
J-STD-033A	JOINT IPC/JEDEC STANDARD FOR HANDLING, PACKING, SHIPPING AND USE OF MOISTURE/REFLOW SENSITIVE SURFACE-MOUNT DEVICES	2002
J-STD-035	JOINT IPC/JEDEC STANDARD FOR ACCOUSTIC MICROSCOPY FOR NONHERMETRIC ENCAPSULATED ELECTRIC COMPONENT	1999

- JESD22-(JEDEC Standard) individual standards

Number	Title	Established
JESD22-A100-B	CYCLED TEMPERATURE HUMIDITY BIAS LIFE TEST	2000
JESD22-A101-B	STEADY-STATE TEMPERATURE HUMIDITY BIAS LIFE TEST	1997
JESD22-A102-C	ACCELERATED MOISTURE RESISTANCE—UNBIASWS AUTOCLAVE	2000
JESD22-A103-C	HIGH TEMPERATURE STORAGE LIFE	2004
JESD22-A104C	TEMPERATURE CYCLING	2005
JESD22-A105C	POWER AND TEMPERATURE CYCLING	2004
JESD22-A106B	THERMAL SHOCK	2004
JESD22-A107B	SALT ATOMOSPHERE	2004
JESD22-A108C	TEMPERATURE, BIAS, AND OPERATING LIFE	2005
JESD22-A109A	HERMETICITY	2001

Number	Title	Established
JESD22-A110-B	HIGHLY ACCELERATED TEMPERATURE AND HUMIDITY STRESS TEST (HAST)	1999
JESD22-A111	EVALUATION PROCEDURE FOR DETERMINING CAPABILITY TO BOTTOM SIDE BOARD ATTACH BY FULL BODY SOLDER IMMERSION OF SMALL SURFACE MOUNT SOLID STATE DEVICES	2004
JESD22-A113D	PRECONDITIONING OF PLASTIC SURFACE MOUNT DEVICES PRIOR TO RELIABILITY TESTING	2003
JESD22-A114C.01	ELECTROSTATIC DISCHARGE (ESD) SENSITIVETY TESTING HUMAN BODY MODEL (HBM)	2005
JESD22-A115-A	ELECTROSTATIC DISCHARGE (ESD) SENSITIVITY TESTING MACHINE MODEL (MM)	1997
JESD22-A117	ELECTRICALLY ERASBLE PROGRAMMABLE ROM (EEPROM) PROGRAM/ERASE ENDURANCE AND DATA RETENTION TEST	2000
JESD22-A118	ACCELERATED MOISTURE RESISTANCE—UNBIASED HAST	2000
JESD22-A119	LOW TEMPERATURE STRAGE LIFE	2004
JESD22-A120.01	TEST METHOD FOR THE MEASUREMENT OF MOISTURE DIFFUSIVITY AND WATER SOLUBILITY IN ORGANIC MATERIALS USED IN INTEGRATED CIRCUITS	2001
JESD22-A121	Measuring Whisker Growth on Ti and Tin Alloy Surface fishes	2005
JESD22-B	SUPERSEDED BY THE TEST METHODS INDICATED BY "JESD22-"	2000
JESD22-B100B	PHYSICAL DIMENTION	2003
JESD22-B101A	EXTERNAL VISUAL	2004
JESD22-B102D	SOLDERBILITY	2004
JESD22-B103-B	VIBRATION, VARIABLE FREQUENCY	2002
JESD22-B104C	MECHANICAL SHOCK	2004
JESD22-B105C	LEAD INTEGRITY	2003
JESD22-B106C	RESISTANCE TO SOLDERING TEMPERATURE FOR THROUGH-HOLE MOUTED DEVICE	2005
JESD22-B107C	MARKING PERMANENCY	2004
JESD22-B108A	COPLANARITY TEST FOR SURFACE-MOUNT SEMICONDUCTOR DEVICES	2003
JESD22-B109	FLIP CHIP TENSILE PULL	2002

Number	Title	Established
JESD22-B110A	SUBASEMBLY MECHANICAL SHOCK	2004
JESD22-B111	BOARD LEVEL DROP TEST METHOD OF COMPONENTS FOR HANDHELD ELECTRONIC PRODUCTS	2003
JESD22-B112	High Temperature Package Warpage Measurement Methodology	2005
JESD22-B116	WIRE BOND SHEAR TEST	1998
JESD22-B117	BALL GRID ARRAY (BGA) BALL SHAER	2000
JESD22-C100-A	HIGH TEMPERATURE CONTINUITY—RESCINDED, November 1999	1990
JESD22-C101C	FILED-INDUCED CHARGED-DEVICE MODEL TEST METHOD FOR ELECTROSTATIC DISCHARGE WITHSTAND THRESHOLDS OF MICROELECTRONIC COMPONENTS	2004
JESD35-A	Procedure for the Wafer-Level Testing of Thin Dielectrics	2001
JESD671-A	Component Quality Problem Analysis and Corrective Action Requirements	1999
JESD46-B	Customer Notification of Product/Process Changes by Semiconductor Suppliers	2001
JESD47D	Stress-Test-Driven Qualification of Integrated Circuits	2003
JESD48B	Product Discontinuance	2005
JESD50A	Special Requirements for Maverick Product Elimination	2004
JESD61	Isothermal Electromigration Test Procedure	1997
JESD69	Information Requirements for the Qualification of Silicon Devices	2000
JESD74	Early Life Failure Rate Calculation Procedure for Electronic Components	2000
JESD78A	IC Latch-Up Test	1997
JESD85	Methods for Calculating Failure Rates in Units of FITs	2001
JESD87	Standard Test Structures for Reliability Assessment of AlCu Metallizations with Barrier Materials	2001
JESD89	Measurement and Reporting of Alpha Particles and Terrestrial Cosmic Ray-Induced Soft Errors in Semiconductor Devices	2001
JESD90	A Procedure for Measuring P-Channel MOSFET Negative Bias Temperature Instabilities	2004

Number	Title	Established
JESD91A	Method for Developing Acceleration Models for Electronic Component Failure Mechanisms	2003
JESD94	Application Specific Qualification Using Knowledge Based Test Methodology	2004
JESD659-A	Failure-Mechanism-Driven Reliability Monitoring	1999

(3) IEC standards

Number	Established	Title	Part
Publication 68	1969-95	Environmental testing	Parts 1 to 5
Publication 747	1983-95	Semiconductor devices, —Discrete devices and integrated circuits	Parts 1 to 12
Publication 748	1984-95	Semiconductor devices, Integrated circuit	Parts 1 to 22
Publication 749	1984	Semiconductor Devices, Mechanical and climatic test methods	Parts 1 to 36
IEC-60749-xx	2002-2004	Semiconductor devices —Mechanical and climatic test methods	Parts 1 to 36

- Publication 68 individual standards

Number	Title	Established
68-1	Environmental testing, Part 1: General and guidance	1988
68-2	Part 2: Test Series	1973
68-2-1	Test A: Cold. Amendment No. 1 (1983), No. 2 (1994)	1990
68-2-2	Test B: Dry heat. Amendment No. 1 (1993), No. 2 (1994)	1974
68-2-3	Test Ca: Damp heat, steady state	1969
68-2-5	Test Sa: Simulated solar radiation at ground level	1975
68-2-6	Test Fc: Vibration (sinusoidal)	1995
68-2-7	Test Ga and guidance: Acceleration, steady state. Amendment No. 1 (1986)	1983
68-2-9	Guidance for solar radiation testing. Amendment No. 1 (1984)	1975
68-2-10	Part 2: Test—Test J and guidance: Mould growth	1988
68-2-11	Test Ka: Salt mist	1981
68-2-13	Test M: Low air pressure	1983

Number	Title	Established
68-2-14	Test N: Change of temperature. Amendment No. 1 (1986)	1984
68-2-17	Test Q: Sealing	1994
68-2-20	Test T: Soldering. Amendment No. 2 (1987)	1979
68-2-21	Test U: Robustness of terminations and integral mounting devices. Amendment No. 2 (1991), No. 3 (1992)	1983
68-2-27	Part 2: Tests. Test Ea and Guidance: Shock	1987
68-2-28	Guidance for damp heat tests	1990
68-2-29	Part 2: Tests. Test Eb and Guidance: Bump	1987
68-2-30	Test Db and guidance: Damp heat, cyclic (12+12-hour cycle). Amendment No. 1 (1985)	1980
68-2-31	Test Ec: Drop and topple, primarily for equipment type specimens. Amendment No. 1 (1982)	1969
68-2-32	Test Ed: Free fall. Amendment No. 2 (1990)	1975
68-2-33	Guidance on change of temperature tests. Amendment No. 1 (1978)	1971
68-2-34	Test Fd: Random vibration wide band—General requirements. Amendment No. 1 (1983)	1973
68-2-35	Test Fda: Random vibration wide band—Reproducibility High. Amendment No. 1 (1983)	1973
68-2-36	Test Fdb: Random vibration wide band—Reproducibility Medium. Amendment No. 1 (1983)	1973
68-2-37	Test Fdc: Random vibration wide band—Reproducibility Low. Amendment No. 1 (1983)	1973
68-2-38	Test Z/AD: Composite temperature/humidity cycle test	1974
68-2-39	Test Z/AMD: Combined sequential cold, low air pressure, and damp heat test	1976
68-2-40	Test Z/AMD: Combined cold/low air pressure tests. Amendment No. 1 (1983)	1976
68-2-41	Test Z/BM: Combined dry heat/low air pressure tests. Amendment No. 1 (1983)	1976
68-2-42	Test Kc: Sulphur dioxide test for contacts and connections	1982
68-2-43	Test Kd: Hydrogen sulphide test for contacts and connections	1976
68-2-44	Guidance on Test T: Soldering	1995

Number	Title	Established
68-2-45	Test XA and guidance: Immersion in cleaning solvents. Amendment No. 1 (1993)	1980
68-2-46	Guidance to Test Kd: Hydrogen sulphide test for contacts and connections	1982
68-2-47	Mounting of components, equipment and other articles for dynamic tests including shock (Ea), bump (Eb), vibration (Fc and Fd) and steady-state acceleration (Ga) and guidance	1982
68-2-48	Guidance on the application of the tests of IEC 68 to simulate the effects of storage	1982
68-2-49	Guidance to Test Kc: Sulphur dioxide test for contacts and connections	1983
68-2-50	Test Z/AFc: Combined cold/vibration (sinusoidal) tests for both heat-dissipating and non-heat-dissipating specimens	1983
68-2-51	Test Z/BFc: Combined dry heat/vibration (sinusoidal) tests for both heat-dissipating and non-heat-dissipating specimens	1983
68-2-52	Test Kb: Salt mist, cyclic (sodium chloride solution)	1984
68-2-53	Guidance to test Z/AFc and Z/BFc: Combined temperature (cold and dry heat) and vibration (sinusoidal) tests	1984
68-2-54	Test Ta: Soldering. Solderbility testing by the wetting balance method	1985
68-2-55	Test Ee and Guidance: Bounce	1987
68-2-56	Part 2: Tests. Test Cb: Damp heat, steady state, primarily for equipment	1988
68-2-57	Test Ff: Vibration. Time-history method	1989
68-2-58	Test Td: Solderbility, resistance to dissolution of metallization and to soldering heat of Surface Mounting Devices (SMD)	1989
68-2-59	Test Fe: Vibration—Sine-beat method	1990
68-2-60	Part 2: Tests—Test Ke: Flowing mixed gas corrosion test	1995
68-2-61	Test Z/ABDM: Climatic sequence	1991
68-2-62	Test Ef: Impact, pendulum hammer	1991
68-2-63	Test Eg: Impact, spring hammer	1991
68-2-64	Part 2: Test methods—Test Fh: Vibration broad-band random (digital control) and guidance	1993
68-2-65	Part 2: Tests—Test Fg: Vibration, acoustically induced	1993

Number	Title	Established
68-2-66	Part 2: Test methods—Test Cx: Damp heat, steady state (unsaturated pressurized vapor)	1994
68-2-67	Part 2: Tests—Test Cy: Damp heat, steady state, accelerated test primarily intended for components	1995
68-2-68	Part 2: Tests—Test L: Dust and sand	1994
68-2-69	Part 2: Tests—Test Te: Solderability testing of electronic components for surface mount technology by the wetting balance method	1995
68-2-70	Part 2: Tests—Test Xb: abrasion of markings and letterings caused by rubbing of fingers and hands	1995
68-3-1	Part 3: Background information Section One—Cold and dry heat tests	1974
68-3-1A	First supplement	1978
68-3-2	Section Two—Combined temperature/low air pressure tests	1976
68-3-3	Part 3: Guidance. Seismic test methods for equipments	1991
68-4	Part 4: Information for specification writers—Test summaries. Amendment No. 1 (1992). Amendment No. 2 (1994)	1987
68-5-1	Part 5: Guide to drafting of test methods—General principles	1991
68-5-2	Part 5: Guide to drafting of test methods—Terms and definitions	1990

- IEC-60749-xx individual standards

Number	Title	Established
IEC-60749-1	General	2003
IEC-60749-2	Low air pressure	2003
IEC-60749-3	External Visual examination	2003
IEC-60749-4	Damp heat, steady state, highly accelerated test (HAST)	2003
IEC-60749-5	Steady state temperature humidity bias life test	2003
IEC-60749-6	Storage at high temperature	2003
IEC-60749-8	Sealing	2003
IEC-60749-9	Permanence of marking	2003
IEC-60749-10	Mechanical Shock	2003
IEC-60749-11	Rapid change of temperature—Two-fluid-bath method	2003
IEC-60749-12	Vibration, variable frequency	2003

Number	Title	Established
IEC-60749-13	Salt atmosphere	2003
IEC-60749-14	Robustness of terminations (lead integrity)	2003
IEC-60749-15	Resistance to soldering temperature for through-hole mounted device	2003
IEC-60749-16	Particle impact noise detection (PIND)	2003
IEC-60749-17	Neutron irradiation	2003
IEC-60749-18	Ionizing radiation (total dose)	2002
IEC-60749-19	Die shear strength	2003
IEC-60749-20	Resistance of plastic-encapsulated SMDs to the combined effect of moisture and soldering heat	2003
IEC-60749-21	Solderbility	2004
IEC-60749-22	Bond strength	2003
IEC-60749-23	High temperature operating life	2004
IEC-60749-24	Accelerated moisture resistance—Unbiased HAST	2004
IEC-60749-25	Temperature cycling	2003
IEC-60749-26	Electrostatic discharge (ESD) sensitivity testing—Human body model (HBM)	2003
IEC-60749-27	Electrostatic discharge (ESD) sensitivity testing—Machine model (MM)	2003
IEC-60749-29	Latch-up test	2003
IEC-60749-31	Flammability of plastic-encapsulated device (internally induced)	2003
IEC-60749-32	Flammability of plastic-encapsulated device (externally induced)	2003
IEC-60749-33	Accelerated moisture resistance—Unbiased autoclave	2004
IEC-60749-34	Power cycling	2004
IEC-60749-36	Acceleration, steady state	2003

(4) MIL standards

Number	Title	Established
MIL-STD-202	Test Methods for Electronic and Electrical Component Parts	1980
MIL-STD-690	Failure Rate Sampling Plans and Procedures	1968
MIL-STD-750	Test Methods for Semiconductor Devices	1983
MIL-STD-790	Reliability Assurance Program for Electronic Parts Specifications	1968
MIL-STD-883	Test Methods and Procedures for Microelectronics	1983
MIL-M-38510	Microcircuits, General Specification	1981
MIL-M-55565	Microcircuits, Preparation for Delivery	1978
MIL-S-19500	Semiconductor Devices, General Specification	1977

Appendix

A. Attached Tables

A.1 AQL Sampling Table (SOURCE: JIS Z 9015)

- Sample size code letters

	Special Inspection Level				Normal Inspection Level		
Lot Size	**S-1**	**S-2**	**S-3**	**S-4**	**I**	**II**	**III**
1 to 8	A	A	A	A	A	A	B
9 to 15	A	A	A	A	A	B	C
16 to 25	A	A	B	B	B	C	D
26 to 50	A	B	B	C	C	D	E
51 to 90	B	B	C	C	C	E	F
91 to 150	B	B	C	D	D	F	G
151 to 280	B	C	D	E	E	G	H
281 to 500	B	C	D	E	F	H	J
501 to 1200	C	C	E	F	G	J	K
1201 to 3200	C	D	E	G	H	K	L
3201 to 10000	C	D	F	G	J	L	M
10001 to 35000	C	D	F	H	K	M	N
35001 to 150000	D	E	G	J	L	N	P
150001 to 500000	D	E	G	J	M	P	Q
500001 up	D	E	H	K	N	Q	R

Specify suitable AQLs selecting from 16 levels in a range from 0.010 to 10 for inspections using percent defective (%); or 26 levels from 0.010 to 1,000 for inspections using defectives per 100 units. Unless otherwise specified, use Inspection Standard II.

Table A.1 AQL Sampling Table

Single Sampling Plans for Normal Inspection (Master Table)

Sample Size Code Letter	Sample Size	Acceptable Quality Level (AQL) (Normal Inspection)																									
		0.010	0.015	0.025	0.040	0.065	0.10	0.15	0.25	0.40	0.65	1.0	1.5	2.5	4.0	6.5	10	15	25	40	65	100	150	250	400	650	1000
		Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re
A	2	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	0 1	↓	↓	2 3	2 4	3 5	5 6	7 8	10 11	14 15	21 22	30 31
B	3	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	0 1	↑	↓	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22	30 31	44 45
C	5	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	0 1	↑	↓	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22	30 31	44 45	↑
D	8	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	0 1	↑	↓	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22	30 31	44 45	↑	↑
E	13	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	0 1	↑	↓	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22	30 31	44 45	↑	↑	↑
F	20	↓	↓	↓	↓	↓	↓	↓	↓	↓	0 1	↑	↓	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22	↑	↑	↑	↑	↑	↑
G	32	↓	↓	↓	↓	↓	↓	↓	↓	0 1	↑	↓	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22	↑	↑	↑	↑	↑	↑	↑
H	50	↓	↓	↓	↓	↓	↓	↓	0 1	↑	↓	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22	↑	↑	↑	↑	↑	↑	↑	↑
J	80	↓	↓	↓	↓	↓	↓	0 1	↑	↓	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22	↑	↑	↑	↑	↑	↑	↑	↑	↑
K	125	↓	↓	↓	↓	↓	0 1	↑	↓	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
L	200	↓	↓	↓	↓	0 1	↑	↓	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
M	315	↓	↓	↓	0 1	↑	↓	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
N	500	↓	↓	0 1	↑	↓	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
P	800	↓	0 1	↑	↓	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
Q	1250	0 1	↑	↓	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
R	2000	↑	↑	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑

↓ : Use first sampling plan below arrow. If sample size equals or exceeds lot size do 100% inspection.
↑ : Use first sampling plan above arrow.

Ac: Number of pieces accepted.
Re: Number of pieces rejected.

Single Sampling Plans for Severe Inspection (Master Table)

Sample Size Code Letter	Sample Size	Acceptable Quality Level (AQL) (Tightened Inspection)																									
		0.010	0.015	0.025	0.040	0.065	0.10	0.15	0.25	0.40	0.65	1.0	1.5	2.5	4.0	6.5	10	15	25	40	65	100	150	250	400	650	1000
		Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re
A	2	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	1 2	2 3	3 4	5 6	8 9	12 13	18 19	27 28
B	3	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	0 1	↓	↓	1 2	2 3	3 4	5 6	8 9	12 13	18 19	27 28	41 42
C	5	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	0 1	↓	↓	1 2	2 3	3 4	5 6	8 9	12 13	18 19	27 28	41 42	↑
D	8	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	0 1	↓	↓	1 2	2 3	3 4	5 6	8 9	12 13	18 19	27 28	41 42	↑	↑
E	13	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	0 1	↓	↓	1 2	2 3	3 4	5 6	8 9	12 13	18 19	27 28	41 42	↑	↑	↑
F	20	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	0 1	↓	↓	1 2	2 3	3 4	5 6	8 9	12 13	18 19	↑	↑	↑	↑	↑	↑
G	32	↓	↓	↓	↓	↓	↓	↓	↓	↓	0 1	↓	↓	1 2	2 3	3 4	5 6	8 9	12 13	18 19	↑	↑	↑	↑	↑	↑	↑
H	50	↓	↓	↓	↓	↓	↓	↓	↓	0 1	↓	↓	1 2	2 3	3 4	5 6	8 9	12 13	18 19	↑	↑	↑	↑	↑	↑	↑	↑
J	80	↓	↓	↓	↓	↓	↓	↓	0 1	↓	↓	1 2	2 3	3 4	5 6	8 9	12 13	18 19	↑	↑	↑	↑	↑	↑	↑	↑	↑
K	125	↓	↓	↓	↓	↓	↓	0 1	↓	↓	1 2	2 3	3 4	5 6	8 9	12 13	18 19	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
L	200	↓	↓	↓	↓	↓	0 1	↓	↓	1 2	2 3	3 4	5 6	8 9	12 13	18 19	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
M	315	↓	↓	↓	↓	0 1	↓	↓	1 2	2 3	3 4	5 6	8 9	12 13	18 19	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
N	500	↓	↓	↓	0 1	↓	↓	1 2	2 3	3 4	5 6	8 9	12 13	18 19	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
P	800	↓	↓	0 1	↓	↓	1 2	2 3	3 4	5 6	8 9	12 13	18 19	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
Q	1250	↓	0 1	↓	↓	1 2	2 3	3 4	5 6	8 9	12 13	18 19	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
R	2000	0 1	↑	↓	1 2	2 3	3 4	5 6	8 9	12 13	18 19	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
S	3150			1 2																							

↓ : Use first sampling plan below arrow. If sample size equals or exceeds lot size do 100% inspection.
↑ : Use first sampling plan above arrow.

Ac: Number of pieces accepted.
Re: Number of pieces rejected.

Single Sampling Plans for Slack Inspection (Master Table)

Sample Size Code Letter	Sample Size	Acceptable Quality Level (AQL) (Reduced Inspection)*																									
		0.010	0.015	0.025	0.040	0.065	0.10	0.15	0.25	0.40	0.65	1.0	1.5	2.5	4.0	6.5	10	15	25	40	65	100	150	250	400	650	1000
		Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re
A	2	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	1 2	↓	↓	2 3	2 4	3 5	5 6	7 8	10 11	14 15	21 22	30 31
B	2	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	0 2	↑	↓	1 3	2 3	2 4	3 5	5 6	7 8	10 11	14 15	21 22	30 31
C	2	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	0 1	↑	↓	1 2	1 3	2 4	2 5	3 6	5 8	7 10	10 13	14 17	21 24	↑
D	3	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	0 1	↑	↓	1 2	1 3	2 4	2 5	3 6	5 8	7 10	10 13	14 17	21 24	↑	↑
E	5	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	0 1	↑	↓	1 2	1 3	2 4	2 5	3 6	5 8	7 10	10 13	14 17	21 24	↑	↑	↑
F	8	↓	↓	↓	↓	↓	↓	↓	↓	↓	0 1	↑	↓	1 2	1 3	2 4	2 5	3 6	5 8	7 10	10 13	↑	↑	↑	↑	↑	↑
G	13	↓	↓	↓	↓	↓	↓	↓	↓	0 1	↑	↓	1 2	1 3	2 4	2 5	3 6	5 8	7 10	10 13	↑	↑	↑	↑	↑	↑	↑
H	20	↓	↓	↓	↓	↓	↓	↓	0 1	↑	↓	1 2	1 3	2 4	2 5	3 6	5 8	7 10	10 13	↑	↑	↑	↑	↑	↑	↑	↑
J	32	↓	↓	↓	↓	↓	↓	0 1	↑	↓	1 2	1 3	2 4	2 5	3 6	5 8	7 10	10 13	↑	↑	↑	↑	↑	↑	↑	↑	↑
K	50	↓	↓	↓	↓	↓	0 1	↑	↓	1 2	1 3	2 4	2 5	3 6	5 8	7 10	10 13	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
L	80	↓	↓	↓	↓	0 1	↑	↓	1 2	1 3	2 4	2 5	3 6	5 8	7 10	10 13	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
M	125	↓	↓	↓	0 1	↑	↓	1 2	1 3	2 4	2 5	3 6	5 8	7 10	10 13	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
N	200	↓	↓	0 1	↑	↓	1 2	1 3	2 4	2 5	3 6	5 8	7 10	10 13	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
P	315	↓	0 1	↑	↓	1 2	1 3	2 4	2 5	3 6	5 8	7 10	10 13	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
Q	500	0 1	↑	↓	1 2	1 3	2 4	2 5	3 6	5 8	7 10	10 13	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
R	800	↑	↑	1 2	1 3	2 4	2 5	3 6	5 8	7 10	10 13	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑

↓ : Use first sampling plan below arrow. If sample size equals or exceeds lot size do 100% inspection.
↑ : Use first sampling plan above arrow.

Ac: Number of pieces accepted.
Re: Number of pieces rejected.
* : The lot is acccepted when failures are grater than Ac but less then Re. Subsequent lots are, however, subject to normal inspection.

A.2 LTPD Sampling Table (Source: MIL-S-19500, sampling inspection tables)

The minimum required sample size to obtain a 90% confidence level that a lot of the same fraction defective as that of the specified LTPD

Lot Tolerance Percent Defective (LTPD) or λ	50	30	20	15	10	7	5	3
Number of failures allowed (C) (r = C + 1) Minimum sample size (× 1,000 for elements required in life test × time)								
0	5 (1.03)	8 (0.64)	11 (0.46)	15 (0.34)	22 (0.23)	32 (0.16)	45 (0.11)	76 (0.07)
1	8 (4.4)	13 (2.7)	18 (2.0)	25 (1.4)	38 (0.94)	55 (0.65)	77 (0.46)	129 (0.28)
2	11 (7.4)	18 (4.5)	25 (3.4)	34 (2.24)	52 (1.6)	75 (1.1)	105 (0.78)	176 (0.47)
3	13 (10.5)	22 (6.2)	32 (4.4)	43 (3.2)	65 (2.1)	94 (1.5)	132 (1.0)	221 (0.62)
4	16 (12.3)	27 (7.3)	38 (5.3)	52 (3.9)	78 (2.6)	113 (1.8)	158 (1.3)	265 (0.75)
5	19 (13.8)	31 (8.4)	45 (6.0)	60 (4.4)	91 (2.9)	131 (2.0)	184 (1.4)	308 (0.85)
6	21 (15.6)	35 (9.4)	51 (6.6)	68 (4.9)	104 (3.2)	149 (2.2)	209 (1.6)	349 (0.94)
7	24 (16.6)	39 (10.2)	57 (7.2)	77 (5.3)	116 (3.5)	166 (2.4)	234 (1.7)	390 (1.0)
8	26 (18.1)	43 (10.9)	63 (7.7)	85 (5.6)	128 (3.7)	184 (2.6)	258 (1.8)	431 (1.1)
9	28 (19.4)	47 (11.5)	69 (8.1)	93 (6.0)	140 (3.9)	201 (2.7)	282 (1.9)	471 (1.2)
10	31 (19.9)	51 (12.1)	75 (8.4)	100 (6.3)	152 (4.1)	218 (2.9)	306 (2.0)	511 (1.2)
11	33 (21.0)	54 (12.8)	83 (8.3)	111 (6.2)	166 (4.2)	238 (2.9)	332 (2.1)	555 (1.2)
12	36 (21.4)	59 (13.0)	89 (8.6)	119 (6.5)	178 (4.3)	254 (3.0)	356 (2.2)	594 (1.3)
13	38 (22.3)	63 (13.4)	95 (8.9)	126 (6.7)	190 (4.5)	271 (3.1)	379 (2.26)	632 (1.3)
14	40 (23.1)	67 (13.8)	101 (9.2)	134 (6.9)	201 (4.6)	288 (3.2)	403 (2.3)	672 (1.4)
15	43 (23.3)	71 (14.1)	107 (9.4)	142 (7.1)	213 (4.7)	305 (3.3)	426 (2.36)	711 (1.41)
16	45 (24.1)	74 (14.6)	112 (9.7)	150 (7.2)	225 (4.8)	321 (3.37)	450 (2.41)	750 (1.44)
17	47 (24.7)	79 (14.7)	118 (9.86)	158 (7.36)	236 (4.93)	338 (3.44)	473 (2.46)	788 (1.48)
18	50 (24.9)	83 (15.0)	124 (10.0)	165 (7.54)	248 (5.02)	354 (3.51)	496 (2.51)	826 (1.51)
19	52 (25.5)	86 (15.4)	130 (10.2)	173 (7.76)	259 (5.12)	370 (3.58)	518 (2.56)	864 (1.53)
20	54 (26.1)	90 (15.6)	135 (10.4)	180 (7.82)	271 (5.19)	386 (3.65)	541 (2.60)	902 (1.56)
25	65 (27.0)	109 (16.1)	163 (10.8)	217 (8.08)	326 (5.38)	466 (3.76)	652 (2.69)	1,086(1.61)

Notes: 1. The number of samples is determined according to the limits of the binomial distribution indexes.

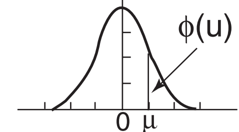
2. Values in parentheses indicate the minimum quality required to have 19 out of 20 lots pass (on average). This approximates AQL values.

Will not be passed. (Single sampling)

2	1.5	1	0.7	0.5	0.3	0.2	0.15	0.1
116 (0.04)	153 (0.03)	231 (0.02)	328 (0.02)	461 (0.01)	767 (0.007)	1152 (0.005)	1534 (0.003)	2303 (0.002)
195 (0.18)	258 (0.14)	390 (0.09)	555 (0.06)	778 (0.045)	1296 (0.027)	1946 (0.018)	2592 (0.013)	3891 (0.009)
266 (0.31)	354 (0.23)	533 (0.15)	759 (0.11)	1065 (0.08)	1773 (0.045)	2662 (0.031)	3547 (0.022)	5323 (0.015)
333 (0.41)	444 (0.32)	668 (0.20)	953 (0.14)	1337 (0.10)	2226 (0.062)	3341 (0.041)	4452 (0.031)	6681 (0.018)
398 (0.51)	531 (0.37)	798 (0.52)	1140 (0.17)	1599 (0.12)	2663 (0.074)	3997 (0.049)	5327 (0.037)	7994 (0.025)
462 (0.57)	617 (0.42)	927 (0.28)	1323 (0.20)	1855 (0.14)	3090 (0.085)	4638 (0.056)	6181 (0.042)	9275 (0.028)
528 (0.62)	700 (0.47)	1054 (0.31)	1503 (0.22)	2107 (0.155)	3509 (0.093)	5267 (0.052)	7019 (0.074)	10533 (0.031)
589 (0.67)	783 (0.51)	1178 (0.34)	1680 (0.24)	2355 (0.17)	3922 (0.101)	5886 (0.067)	7845 (0.051)	11771 (0.034)
648 (0.72)	864 (0.54)	1300 (0.36)	1854 (0.25)	2599 (0.18)	4329 (0.108)	6498 (0.072)	8660 (0.054)	12995 (0.036)
709 (0.77)	945 (0.58)	1421 (0.38)	2027 (0.27)	2842 (0.19)	4733 (0.114)	7103 (0.077)	9468 (0.057)	14206 (0.038)
770 (0.80)	1025 (0.60)	1541 (0.40)	2199 (0.28)	3082 (0.20)	5133 (0.120)	7704 (0.080)	10268 (0.060)	15407 (0.040)
832 (0.83)	1109 (0.62)	1664 (0.42)	2378 (0.29)	3323 (0.21)	5546 (0.12)	8319 (0.083)	11092 (0.062)	16638 (0.042)
890 (0.86)	1187 (0.65)	1781 (0.43)	2544 (0.3)	3562 (0.22)	5936 (0.13)	8904 (0.086)	11872 (0.065)	17808 (0.043)
948 (0.89)	1264 (0.67)	1896 (0.44)	2709 (0.31)	3793 (0.22)	6321 (0.134)	9482 (0.089)	12643 (0.067)	18964 (0.045)
1007 (0.92)	1343 (0.69)	2015 (0.46)	2878 (0.32)	4029 (0.23)	6716 (0.138)	10073 (0.092)	13431 (0.069)	20146 (0.046)
1066 (0.94)	1422 (0.71)	2133 (0.47)	3046 (0.33)	4265 (0.235)	7108 (0.141)	10662 (0.094)	14216 (0.070)	21324 (0.047)
1124 (0.96)	1499 (0.72)	2249 (0.48)	3212 (0.337)	4497 (0.241)	7496 (0.144)	11244 (0.096)	14992 (0.072)	22487 (0.048)
1182 (0.98)	1576 (0.74)	2364 (0.49)	3377 (0.344)	4728 (0.246)	7880 (0.148)	11819 (0.098)	15759 (0.074)	23639 (0.049)
1239 (1.0)	1652 (0.75)	2478 (0.50)	3540 (0.351)	4956 (0.251)	8260 (0.151)	12390 (0.100)	16520 (0.075)	24780 (0.050)
1296 (1.02)	1728 (0.77)	2591 (0.52)	3702 (0.358)	5183 (0.256)	8638 (0.153)	12957 (0.102)	17276 (0.077)	25914 (0.051)
1353 (1.04)	1803 (0.78)	2705 (0.52)	3864 (0.364)	5410 (0.260)	9017 (0.156)	13526 (0.104)	18034 (0.078)	27051 (0.052)
1629 (1.08)	2173 (0.807)	3259 (0.538)	4656 (0.376)	6518 (0.259)	10863 (0.161)	16295 (0.108)	21726 (0.081)	32589 (0.054)

A.3 Probability Density of Normal Distribution

$$\phi(u) = \frac{1}{\sqrt{2\pi}} e^{-\frac{u^2}{2}}$$



U	.00	.01	.02	.03	.04	.05	.06	.07	.08	.09
.0	.39894	.39892	.39886	.39876	.39862	.39844	.39822	.39797	.39767	.39733
.1	.39695	.39654	.39608	.39559	.39505	.39448	.39387	.39322	.39253	.39181
.2	.39104	.39024	.38940	.38853	.38762	.38667	.38568	.38466	.38361	.38251
.3	.38139	.38023	.37903	.37780	.37654	.37524	.37391	.37255	.37115	.36973
.4	.36827	.36678	.36526	.36371	.36213	.36053	.35889	.35723	.35553	.35381
.5	.35207	.35029	.34849	.34667	.34482	.34294	.34105	.33912	.33718	.33521
.6	.33322	.33121	.32918	.32713	.32506	.32297	.32086	.31874	.31659	.31443
.7	.31225	.31006	.30785	.30563	.30339	.30114	.29887	.29659	.29431	.29200
.8	.28969	.28737	.28504	.28269	.28034	.27798	.27562	.27324	.27086	.26848
.9	.26609	.26369	.26129	.25888	.25647	.25406	.25164	.24923	.24681	.24439
1.0	.24197	.23955	.23713	.23471	.23230	.22988	.22747	.22506	.22265	.22025
1.1	.21785	.21546	.21307	.21069	.20831	.20594	.20357	.20121	.19886	.19652
1.2	.19419	.19186	.18954	.18724	.18494	.18265	.18037	.17810	.17585	.17360
1.3	.17137	.16915	.16694	.16474	.16256	.16038	.15822	.15608	.15395	.15183
1.4	.14973	.14764	.14556	.14350	.14146	.13943	.13742	.13542	.13344	.13147
1.5	.12952	.12758	.12566	.12376	.12188	.12001	.11816	.11632	.11450	.11270
1.6	.11092	.10915	.10741	.10567	.10396	.10226	.10059	.098925	.097282	.095657
1.7	.094049	.092459	.090887	.089333	.087796	.086277	.084776	.083293	.081828	.080380
1.8	.078950	.077538	.076143	.074766	.073407	.072065	.070740	.069433	.068144	.066871
1.9	.065616	.064378	.063157	.061952	.060765	.059595	.058441	.057304	.056183	.055079
2.0	.053991	.052919	.051864	.050824	.049800	.048792	.047800	.046823	.045861	.044915

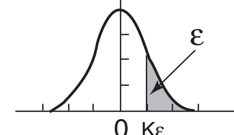
U	.00	.01	.02	.03	.04	.05	.06	.07	.08	.09
2.1	.043984	.043067	.042166	.041280	.040408	.039550	.038707	.037878	.037063	.036262
2.2	.035475	.034701	.033941	.033194	.032460	.031740	.031032	.030337	.029655	.028985
2.3	.028327	.027682	.027048	.026426	.025817	.025218	.024631	.024056	.023491	.022937
2.4	.022395	.021862	.021341	.020829	.020328	.019837	.019356	.018885	.018423	.017971
2.5	.017528	.017095	.016670	.016254	.015848	.015449	.015060	.014678	.014305	.013940
2.6	.013583	.013234	.012892	.012558	.012232	.011912	.011600	.011295	.010997	.010706
2.7	.010421	.010143	$.0^{2}98712$	$.0^{2}96058$	$.0^{2}93466$	$.0^{2}90936$	$.0^{2}88465$	$.0^{2}86052$	$.0^{2}83697$	$.0^{2}81398$
2.8	$.0^{2}79155$	$.0^{2}76965$	$.0^{2}74829$	$.0^{2}72744$	$.0^{2}70711$	$.0^{2}68728$	$.0^{2}66793$	$.0^{2}64907$	$.0^{2}63067$	$.0^{2}61274$
2.9	$.0^{2}59525$	$.0^{2}57821$	$.0^{2}56160$	$.0^{2}54541$	$.0^{2}52963$	$.0^{2}51426$	$.0^{2}49929$	$.0^{2}48470$	$.0^{2}47050$	$.0^{2}45666$
3.0	$.0^{2}44318$	$.0^{2}43007$	$.0^{2}41729$	$.0^{2}40486$	$.0^{2}39276$	$.0^{2}38098$	$.0^{2}36951$	$.0^{2}35836$	$.0^{2}34751$	$.0^{2}33695$
3.1	$.0^{2}32668$	$.0^{2}31669$	$.0^{2}30698$	$.0^{2}29754$	$.0^{2}28835$	$.0^{2}27943$	$.0^{2}27075$	$.0^{2}26231$	$.0^{2}25412$	$.0^{2}24615$
3.2	$.0^{2}23841$	$.0^{2}23089$	$.0^{2}22358$	$.0^{2}21649$	$.0^{2}20960$	$.0^{2}20290$	$.0^{2}19641$	$.0^{2}19010$	$.0^{2}18397$	$.0^{2}17803$
3.3	$.0^{2}17226$	$.0^{2}16666$	$.0^{2}16122$	$.0^{2}15595$	$.0^{2}15084$	$.0^{2}14587$	$.0^{2}14106$	$.0^{2}13639$	$.0^{2}13187$	$.0^{2}12748$
3.4	$.0^{2}12322$	$.0^{2}11910$	$.0^{2}11510$	$.0^{2}11122$	$.0^{2}10747$	$.0^{2}10383$	$.0^{2}10030$	$.0^{3}96886$	$.0^{3}93557$	$.0^{3}90372$
3.5	$.0^{3}87268$	$.0^{3}84263$	$.0^{3}81352$	$.0^{3}78534$	$.0^{3}75807$	$.0^{3}73166$	$.0^{3}70611$	$.0^{3}68138$	$.0^{3}65745$	$.0^{3}63430$
3.6	$.0^{3}61190$	$.0^{3}59024$	$.0^{3}56928$	$.0^{3}54901$	$.0^{3}52941$	$.0^{3}51046$	$.0^{3}49214$	$.0^{3}47443$	$.0^{3}45731$	$.0^{3}44077$
3.7	$.0^{3}42478$	$.0^{3}40933$	$.0^{3}39440$	$.0^{3}37998$	$.0^{3}36605$	$.0^{3}35260$	$.0^{3}33960$	$.0^{3}32705$	$.0^{3}31494$	$.0^{3}30324$
3.8	$.0^{3}29195$	$.0^{3}28105$	$.0^{3}27053$	$.0^{3}26037$	$.0^{3}25058$	$.0^{3}24113$	$.0^{3}23201$	$.0^{3}22321$	$.0^{3}21473$	$.0^{3}20655$
3.9	$.0^{3}19866$	$.0^{3}19105$	$.0^{3}18371$	$.0^{3}17664$	$.0^{3}16983$	$.0^{3}16326$	$.0^{3}15693$	$.0^{3}15083$	$.0^{3}14495$	$.0^{3}13928$
4.0	$.0^{3}13383$	$.0^{3}12858$	$.0^{3}12352$	$.0^{3}11864$	$.0^{3}11395$	$.0^{3}10943$	$.0^{3}10509$	$.0^{3}10090$	$.0^{4}96870$	$.0^{4}92993$
4.1	$.0^{4}89262$	$.0^{4}85672$	$.0^{4}82218$	$.0^{4}78895$	$.0^{4}75700$	$.0^{4}72626$	$.0^{4}69670$	$.0^{4}66828$	$.0^{4}64095$	$.0^{4}61468$
4.2	$.0^{4}58943$	$.0^{4}56516$	$.0^{4}54183$	$.0^{4}51942$	$.0^{4}49788$	$.0^{4}47719$	$.0^{4}45731$	$.0^{4}43821$	$.0^{4}41988$	$.0^{4}40226$
4.3	$.0^{4}38535$	$.0^{4}36911$	$.0^{4}35353$	$.0^{4}33856$	$.0^{4}32420$	$.0^{4}31041$	$.0^{4}29719$	$.0^{4}28499$	$.0^{4}27231$	$.0^{4}26063$
4.4	$.0^{4}24942$	$.0^{4}23868$	$.0^{4}22837$	$.0^{4}21848$	$.0^{4}20900$	$.0^{4}19992$	$.0^{4}19121$	$.0^{4}18286$	$.0^{4}17486$	$.0^{4}16719$
4.5	$.0^{4}15984$	$.0^{4}15280$	$.0^{4}14605$	$.0^{4}13959$	$.0^{4}13340$	$.0^{4}12747$	$.0^{4}12180$	$.0^{4}11636$	$.0^{4}11116$	$.0^{4}10618$
4.6	$.0^{4}10141$	$.0^{5}96845$	$.0^{5}92477$	$.0^{5}88297$	$.0^{5}84298$	$.0^{5}80472$	$.0^{5}76812$	$.0^{5}73311$	$.0^{5}69962$	$.0^{5}66760$
4.7	$.0^{5}63698$	$.0^{5}60771$	$.0^{5}57972$	$.0^{5}55296$	$.0^{5}52739$	$.0^{5}50295$	$.0^{5}47960$	$.0^{5}45728$	$.0^{5}43596$	$.0^{5}41559$
4.8	$.0^{5}39613$	$.0^{5}37755$	$.0^{5}35980$	$.0^{5}34285$	$.0^{5}32667$	$.0^{5}31122$	$.0^{5}29647$	$.0^{5}28239$	$.0^{5}26895$	$.0^{5}25613$
4.9	$.0^{5}24390$	$.0^{5}23222$	$.0^{5}22108$	$.0^{5}21046$	$.0^{5}20033$	$.0^{5}19066$	$.0^{5}18144$	$.0^{5}17265$	$.0^{5}16428$	$.0^{5}15629$

The left-hand and top values are used to identify the value of the deviation u. The table value listed at the intersection of these two values is the probability density ϕ (u) at this value of u.

Example: For u = 2.96, find the value located at the intersection of 2.9 on the left and .06 on the top. This value, $.0^{2}49929$ (= 0.0049929) is the value of ϕ (u) for u = 2.96.

A.4 Upper Probability of Normal Distribution

$$\varepsilon(K\varepsilon):\ \varepsilon = \int_{K\varepsilon}^{\infty} \phi(u)\,du$$



Kε	.00	.01	.02	.03	.04	.05	.06	.07	.08	.09
.0	.50000	.49601	.49202	.48803	.48405	.48006	.47608	.47210	.46812	.46414
.1	.46017	.45620	.45224	.44828	.44433	.44038	.43644	.43251	.42858	.42465
.2	.42074	.41683	.41294	.40905	.40517	.40129	.39743	.39358	.38974	.38591
.3	.38209	.37828	.37448	.37070	.36693	.36317	.35942	.35569	.35197	.34827
.4	.34458	.34090	.33724	.33360	.32997	.32636	.32276	.31918	.31561	.31207
.5	.30854	.30503	.30153	.29806	.29460	.29116	.28774	.28434	.28096	.27760
.6	.27425	.27093	.26763	.26435	.26109	.25785	.25463	.25143	.24825	.24510
.7	.24196	.23885	.23576	.23270	.22965	.22663	.22363	.22065	.21770	.21476
.8	.21186	.20897	.20611	.20327	.20045	.19766	.19489	.19215	.18943	.18673
.9	.18406	.18141	.17879	.17619	.17361	.17106	.16853	.16602	.16354	.16109
1.0	.15866	.15625	.15386	.15151	.14917	.14686	.14457	.14231	.14007	.13786
1.1	.13567	.13350	.13136	.12924	.12714	.12507	.12302	.12100	.11900	.11702
1.2	.11507	.11314	.11123	.10935	.10749	.10565	.10383	.10204	.10027	.098525
1.3	.096800	.095098	.093418	.091759	.090123	.088508	.086915	.085343	.083793	.082264
1.4	.080757	.079270	.077804	.076359	.074934	.073529	.072145	.070781	.069437	.068112
1.5	.066807	.065522	.064255	.063008	.061780	.060571	.059380	.058208	.057053	.055917
1.6	.054799	.053699	.052616	.051551	.050503	.049471	.048457	.047460	.046479	.045514
1.7	.044565	.043683	.042716	.041815	.040930	.040059	.039204	.038364	.037538	.036727
1.8	.035930	.035148	.034380	.033625	.032884	.032157	.031443	.030742	.030054	.029379
1.9	.028717	.028067	.027429	.026803	.026190	.025588	.024998	.024419	.023852	.023295
2.0	.022750	.022216	.021692	.021178	.020675	.020182	.019699	.019226	.018763	.018309

Kε	.00	.01	.02	.03	.04	.05	.06	.07	.08	.09
2.1	.017864	.017429	.017003	.016586	.016177	.015778	.015386	.015003	.014629	.014262
2.2	.013903	.013553	.013209	.012874	.012545	.012224	.011911	.011604	.011304	.011011
2.3	.010724	.010444	.010170	$.0^{2}99031$	$.0^{2}96419$	$.0^{2}93867$	$.0^{2}91375$	$.0^{2}88940$	$.0^{2}86563$	$.0^{2}84242$
2.4	$.0^{2}81975$	$.0^{2}79763$	$.0^{2}77603$	$.0^{2}75494$	$.0^{2}73436$	$.0^{2}71428$	$.0^{2}99469$	$.0^{2}67557$	$.0^{2}65691$	$.0^{2}63872$
2.5	$.0^{2}62097$	$.0^{2}60366$	$.0^{2}58677$	$.0^{2}57031$	$.0^{2}55426$	$.0^{2}53861$	$.0^{2}52336$	$.0^{2}50849$	$.0^{2}49400$	$.0^{2}47988$
2.6	$.0^{2}46612$	$.0^{2}45271$	$.0^{2}43965$	$.0^{2}42692$	$.0^{2}41453$	$.0^{2}40246$	$.0^{2}39070$	$.0^{2}37926$	$.0^{2}36811$	$.0^{2}35726$
2.7	$.0^{2}34670$	$.0^{2}33642$	$.0^{2}32641$	$.0^{2}31667$	$.0^{2}30720$	$.0^{2}29798$	$.0^{2}28901$	$.0^{2}28028$	$.0^{2}27179$	$.0^{2}26354$
2.8	$.0^{2}25551$	$.0^{2}24771$	$.0^{2}24012$	$.0^{2}23274$	$.0^{2}22557$	$.0^{2}21860$	$.0^{2}21182$	$.0^{2}20524$	$.0^{2}19884$	$.0^{2}19262$
2.9	$.0^{2}18658$	$.0^{2}18071$	$.0^{2}17502$	$.0^{2}16948$	$.0^{2}16411$	$.0^{2}15889$	$.0^{2}15382$	$.0^{2}14890$	$.0^{2}14412$	$.0^{2}13949$
3.0	$.0^{2}13499$	$.0^{2}13062$	$.0^{2}12639$	$.0^{2}12228$	$.0^{2}11829$	$.0^{2}11442$	$.0^{2}11067$	$.0^{2}10703$	$.0^{2}10350$	$.0^{2}10008$
3.1	$.0^{3}96760$	$.0^{3}93544$	$.0^{3}90426$	$.0^{3}87403$	$.0^{3}84474$	$.0^{3}81635$	$.0^{3}78885$	$.0^{3}76219$	$.0^{3}73638$	$.0^{3}71136$
3.2	$.0^{3}68714$	$.0^{3}66367$	$.0^{3}64095$	$.0^{3}61895$	$.0^{3}59765$	$.0^{3}57703$	$.0^{3}55706$	$.0^{3}53774$	$.0^{3}51904$	$.0^{3}50094$
3.3	$.0^{3}48342$	$.0^{3}46648$	$.0^{3}45009$	$.0^{3}43423$	$.0^{3}41889$	$.0^{3}40406$	$.0^{3}38971$	$.0^{3}37584$	$.0^{3}36243$	$.0^{3}34946$
3.4	$.0^{3}33693$	$.0^{3}32481$	$.0^{3}31311$	$.0^{3}30179$	$.0^{3}29086$	$.0^{3}28029$	$.0^{3}27009$	$.0^{3}26023$	$.0^{3}25071$	$.0^{3}24151$
3.5	$.0^{3}23263$	$.0^{3}22405$	$.0^{3}21577$	$.0^{3}20778$	$.0^{3}20006$	$.0^{3}19262$	$.0^{3}18543$	$.0^{3}17849$	$.0^{3}17180$	$.0^{3}16534$
3.6	$.0^{3}15911$	$.0^{3}15310$	$.0^{3}14730$	$.0^{3}14171$	$.0^{3}13632$	$.0^{3}13112$	$.0^{3}12611$	$.0^{3}12128$	$.0^{3}11662$	$.0^{3}11213$
3.7	$.0^{3}10780$	$.0^{3}10363$	$.0^{4}99611$	$.0^{4}95740$	$.0^{4}92010$	$.0^{4}88417$	$.0^{4}84957$	$.0^{4}81624$	$.0^{4}78414$	$.0^{4}75324$
3.8	$.0^{4}72348$	$.0^{4}69483$	$.0^{4}66726$	$.0^{4}64072$	$.0^{4}61517$	$.0^{4}59059$	$.0^{4}56694$	$.0^{4}54418$	$.0^{4}52228$	$.0^{4}50122$
3.9	$.0^{4}48096$	$.0^{4}46148$	$.0^{4}44274$	$.0^{4}42473$	$.0^{4}40741$	$.0^{4}39076$	$.0^{4}37475$	$.0^{4}35936$	$.0^{4}34458$	$.0^{4}33037$
4.0	$.0^{4}31671$	$.0^{4}30359$	$.0^{4}29099$	$.0^{4}27888$	$.0^{4}26726$	$.0^{4}25609$	$.0^{4}24536$	$.0^{4}23507$	$.0^{4}22518$	$.0^{4}21569$
4.1	$.0^{4}20658$	$.0^{4}19783$	$.0^{4}18944$	$.0^{4}18138$	$.0^{4}17365$	$.0^{4}16624$	$.0^{4}15912$	$.0^{4}15230$	$.0^{4}14575$	$.0^{4}13948$
4.2	$.0^{4}13346$	$.0^{4}12769$	$.0^{4}12215$	$.0^{4}11685$	$.0^{4}11176$	$.0^{4}10689$	$.0^{4}10221$	$.0^{5}97736$	$.0^{5}93447$	$.0^{5}89337$
4.3	$.0^{5}85399$	$.0^{5}81627$	$.0^{5}78015$	$.0^{5}74555$	$.0^{5}71241$	$.0^{5}68069$	$.0^{5}65031$	$.0^{5}62123$	$.0^{5}59340$	$.0^{5}56675$
4.4	$.0^{5}54125$	$.0^{5}51685$	$.0^{5}49350$	$.0^{5}47117$	$.0^{5}44979$	$.0^{5}42935$	$.0^{5}40980$	$.0^{5}39110$	$.0^{5}37322$	$.0^{5}35612$
4.5	$.0^{5}33977$	$.0^{5}32414$	$.0^{5}30920$	$.0^{5}29492$	$.0^{5}28127$	$.0^{5}26823$	$.0^{5}25577$	$.0^{5}24386$	$.0^{5}23249$	$.0^{5}22162$

Kε	.00	.01	.02	.03	.04	.05	.06	.07	.08	.09
4.6	$.0^{5}21125$	$.0^{5}20133$	$.0^{5}19187$	$.0^{5}18283$	$.0^{5}17420$	$.0^{5}16597$	$.0^{5}15810$	$.0^{5}15060$	$.0^{5}14344$	$.0^{5}13660$
4.7	$.0^{5}13008$	$.0^{5}12386$	$.0^{5}11792$	$.0^{5}11226$	$.0^{5}10686$	$.0^{5}10171$	$.0^{6}96796$	$.0^{6}92113$	$.0^{6}87648$	$.0^{6}83391$
4.8	$.0^{6}79333$	$.0^{6}75465$	$.0^{6}71779$	$.0^{6}68267$	$.0^{6}64920$	$.0^{6}61731$	$.0^{6}58693$	$.0^{6}55799$	$.0^{6}53043$	$.0^{6}50418$
4.9	$.0^{6}47918$	$.0^{6}45538$	$.0^{6}43272$	$.0^{6}41115$	$.0^{6}39061$	$.0^{6}37107$	$.0^{6}35247$	$.0^{6}33476$	$.0^{6}31792$	$.0^{6}30190$

The above table gives the upper probability for a normal distribution for the values of Kε = 0.00 to 4.99.

Example : For Kε = 3.18, find the value located at the intersection of 3.1 on the left and .08 on the top.

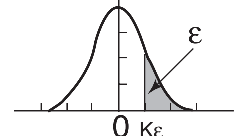
The value $\varepsilon = .0^{3}73638 = 0.00073638$ is the value of the upper probability for Kε = 3.18.

Similarly, for Kε = 1.96, ε = .024998, and for Kε = 2.58, $\varepsilon = .0^{2}49400 = 0.0049400$.

If two-sided probability of distribution is considered, then the above values, respectively, correspond to $2.\varepsilon = 0.049996 \geq 0.05$ and $0.00988 \cong 0.01$.

A.5 Percent Points of Normal Distribution

$$K\varepsilon(\varepsilon): \varepsilon = \int_{K\varepsilon}^{\infty} \phi(u)\, du$$



ε	.000	.001	.002	.003	.004	.005	.006	.007	.008	.009
.00	∞	3.09023	2.87816	2.74778	2.65207	2.57583	2.51214	2.45726	2.40892	2.36562
.01	2.32635	2.29037	2.25713	2.22621	2.19729	2.17009	2.14441	2.12007	2.09693	2.07485
.02	2.05375	2.03352	2.01409	1.99539	1.97737	1.95996	1.94313	1.92684	1.91104	1.89570
.03	1.88079	1.86630	1.85218	1.83842	1.82501	1.81191	1.79912	1.78661	1.77438	1.76241
.04	1.75069	1.73920	1.72793	1.71689	1.70604	1.69540	1.68494	1.67466	1.66456	1.65463
.05	1.64485	1.63523	1.62576	1.61644	1.60725	1.59819	1.58927	1.58047	1.57179	1.56322
.06	1.55477	1.54643	1.53820	1.53007	1.52204	1.51410	1.50626	1.49851	1.49085	1.48328
.07	1.47579	1.46838	1.46106	1.45381	1.44663	1.43953	1.43250	1.42554	1.41865	1.41183
.08	1.40507	1.39838	1.39174	1.38517	1.37866	1.37220	1.36581	1.35946	1.35317	1.34694
.09	1.34076	1.33462	1.32854	1.32251	1.31652	1.31058	1.30469	1.29884	1.29303	1.28727
.10	1.28155	1.27587	1.27024	1.26464	1.25908	1.25357	1.24808	1.24264	1.23723	1.23186
.11	1.22653	1.22123	1.21596	1.21073	1.20553	1.20036	1.19522	1.19012	1.18504	1.18000
.12	1.17499	1.17000	1.16505	1.16012	1.15522	1.15035	1.14551	1.14069	1.13590	1.13113
.13	1.12639	1.12168	1.11699	1.11232	1.10768	1.10306	1.09847	1.09390	1.08935	1.08482
.14	1.08032	1.07584	1.07138	1.06694	1.06252	1.05812	1.05374	1.04939	1.04505	1.04073
.15	1.03643	1.03215	1.02789	1.02365	1.01943	1.01522	1.01103	1.00686	1.00271	.99858
.16	.99446	.99036	.98627	.98220	.97815	.97411	.97009	.96609	.96210	.95812
.17	.95417	.95022	.94629	.94238	.93848	.93459	.93072	.92686	.92301	.91918
.18	.91537	.91156	.90777	.90399	.90023	.89647	.89273	.88901	.88529	.83159
.19	.87790	.87422	.87055	.86689	.86325	.85962	.85600	.85239	.84879	.84520
.20	.84162	.83805	.83450	.83095	.82742	.82389	.82038	.81687	.81338	.80990

ε	.000	.001	.002	.003	.004	.005	.006	.007	.008	.009
.21	.80642	.80296	.79950	.79606	.79262	.78919	.78577	.78237	.77897	.77557
.22	.77219	.76882	.76546	.76210	.75875	.75542	.75208	.74876	.74545	.74214
.23	.73885	.73556	.73228	.72900	.72574	.72248	.71923	.71599	.71275	.70952
.24	.70630	.70309	.69988	.69668	.69349	.69031	.68713	.68396	.68080	.67764
.25	.67449	.67135	.66821	.66508	.66196	.65884	.65573	.65262	.64952	.64643
.26	.64335	.64027	.63719	.63412	.63106	.62801	.62496	.62191	.61887	.61584
.27	.61281	.60979	.60678	.60376	.60076	.59776	.59477	.59178	.58879	.58581
.28	.58284	.57987	.57691	.57395	.57100	.56805	.56511	.56217	.55924	.55631
.29	.55338	.55047	.54755	.54464	.54174	.53884	.53594	.53305	.53016	.52728
.30	.52440	.52153	.51866	.51579	.51293	.51007	.50722	.50437	.50153	.49869
.31	.49585	.49032	.49019	.48736	.48454	.48173	.47891	.47610	.47330	.47050
.32	.46770	.46490	.46211	.45933	.45654	.45376	.45099	.44821	.44544	.44268
.33	.43991	.43715	.43440	.43164	.42889	.42615	.42340	.42066	.41793	.41519
.34	.41246	.40974	.40701	.40429	.40157	.39886	.39614	.39343	.39073	.38802
.35	.38532	.38262	.37993	.37723	.37454	.37186	.36917	.36649	.36381	.36113
.36	.35846	.35579	.35312	.35045	.34779	.34513	.34247	.33981	.33716	.33450
.37	.33185	.32921	.32656	.32392	.32128	.31864	.31600	.31337	.31074	.30811
.38	.30548	.30286	.30023	.29761	.29499	.29237	.28976	.28715	.28454	.28193
.39	.27932	.27671	.27411	.27151	.26891	.26631	.26371	.26112	.25853	.25594
.40	.25335	.25076	.24817	.24559	.24301	.24043	.23785	.23527	.23269	.23012
.41	.22754	.22497	.22240	.21983	.21727	.21470	.21214	.20957	.20701	.20445
.42	.28189	.19934	.19678	.19422	.19167	.18912	.18657	.18402	.18147	.17892
.43	.17637	.17383	.17128	.16874	.16620	.16366	.16112	.15858	.15604	.15351
.44	.15097	.14843	.14590	.14337	.14084	.13830	.13577	.13324	.13072	.12819
.45	.12566	.12314	.12061	.11809	.11556	.11304	.11052	.10799	.10547	.10295

ε	.000	.001	.002	.003	.004	.005	.006	.007	.008	.009
.46	.10043	.09791	.09540	.09288	.09036	.08784	.08533	.08281	.08030	.07778
.47	.07527	.07276	.07024	.06773	.06522	.06271	.06020	.05768	.05517	.05766
.48	.05015	.04764	.04513	.04263	.04012	.03761	.03510	.03259	.03008	.02758
.49	.02507	.02256	.02005	.01755	.01504	.01253	.01003	.00752	.00501	.00251

The above table gives the value of Kε for the upper probability of normal distribution ε = 0.000 to 0.499.

The Kε value is known as 100 ε percent point.

Example: For ε = 0.200 we find the value at the intersection of .20 on the left side and the .000 on the top.

The value is Kε = .84162. This is referred to as (upper) 20 percent point.

The 2.5% point is represented by the value of ε = 0.025 for which Kε = 1.95996 ≅ 1.96 and the 0.5% point by the value of ε = 0.005, for which Kε = 2.57583 ≅ 2.58.

A.6 Poisson Distribution (Probability)

	m									
x	**0.1**	**0.2**	**0.3**	**0.4**	**0.5**	**0.6**	**0.7**	**0.8**	**0.9**	**1.0**
0	.9048	.8187	.7408	.6703	.6065	.5488	.4966	.4493	.4066	.3679
1	.0905	.1637	.2222	.2681	.3033	.3293	.3476	.3595	.3659	.3679
2	.0045	.0164	.0333	.0536	.0758	.0988	.1217	.1438	.1647	.1839
3	.0002	.0010	.0033	.0072	.0126	.0198	.0284	.0383	.0494	.0613
4	.0000	.0001	.0002	.0007	.0016	.0030	.0050	.0077	.0111	.0153
5	.0000	.0000	.0000	.0001	.0002	.0004	.0007	.0012	.0020	.0031
6	.0000	.0000	.0000	.0000	.0000	.0000	.0001	.0002	.0003	.0005
7	.0000	.0000	.0000	.0000	.0000	.0000	.0000	.0000	.0000	.0001

	m									
x	**1.1**	**1.2**	**1.3**	**1.4**	**1.5**	**1.6**	**1.7**	**1.8**	**1.9**	**2.0**
0	.3329	.3012	.2725	.2466	.2231	.2019	.1827	.1653	.1496	.1353
1	.3662	.3614	.3543	.3452	.3347	.3230	.3106	.2975	.2842	.2707
2	.2014	.2169	.2303	.2417	.2510	.2584	.2640	.2678	.2700	.2707
3	.0738	.0867	.0998	.1128	.1255	.1378	.1496	.1607	.1710	.1804
4	.0203	.0260	.0324	.0395	.0471	.0551	.0636	.0723	.0812	.0902
5	.0045	.0062	.0084	.0111	.0141	.0176	.0216	.0260	.0309	.0361
6	.0008	.0012	.0018	.0026	.0035	.0047	.0061	.0078	.0098	.0120
7	.0001	.0002	.0003	.0005	.0008	.0011	.0015	.0020	.0027	.0034
8	.0000	.0000	.0001	.0001	.0001	.0002	.0003	.0005	.0006	.0009
9	.0000	.0000	.0000	.0000	.0000	.0000	.0001	.0001	.0001	.0002

x	m 2.1	2.2	2.3	2.4	2.5	2.6	2.7	2.8	2.9	3.0
0	.1225	.1108	.1003	.0907	.0821	.0743	.0672	.0608	.0550	.0498
1	.2572	.2438	.2306	.2177	.2052	.1931	.1815	.1703	.1596	.1494
2	.2700	.2681	.2652	.2613	.2565	.2510	.2450	.2384	.2314	.2240
3	.1890	.1966	.2033	.2090	.2138	.2176	.2205	.2225	.2237	.2240
4	.0992	.1082	.1169	.1254	.1336	.1414	.1488	.1557	.1622	.1680
5	.0417	.0476	.0538	.0602	.0668	.0735	.0804	.0872	.0940	.1008
6	.0146	.0174	.0206	.0241	.0278	.0319	.0362	.0407	.0455	.0504
7	.0044	.0055	.0068	.0083	.0099	.0118	.0139	.0163	.0188	.0216
8	.0011	.0015	.0019	.0025	.0031	.0038	.0047	.0057	.0068	.0081
9	.0003	.0004	.0005	.0007	.0009	.0011	.0014	.0018	.0022	.0027
10	.0001	.0001	.0001	.0002	.0002	.0003	.0004	.0005	.0006	.0008
11	.0000	.0000	.0000	.0000	.0000	.0001	.0001	.0001	.0002	.0002
12	.0000	.0000	.0000	.0000	.0000	.0000	.0000	.0000	.0000	.0001

x	m 3.1	3.2	3.3	3.4	3.5	3.6	3.7	3.8	3.9	4.0
0	.0450	.0408	.0369	.0334	.0302	.0273	.0247	.0224	.0202	.0183
1	.1397	.1304	.1217	.1135	.1057	.0984	.0915	.0850	.0789	.0733
2	.2165	.2087	.2008	.1929	.1850	.0771	.1692	.1615	.1539	.1465
3	.2237	.2226	.2209	.2186	.2158	.2125	.2087	.2046	.2001	.1954
4	.1734	.1781	.1823	.1858	.1888	.1912	.1931	.1944	.1951	.1954
5	.1075	.1140	.1203	.1264	.1322	.1377	.1429	.1477	.1522	.1563
6	.0555	.0608	.0662	.0716	.0711	.0826	.0881	.0936	.0989	.1042
7	.0246	.0278	.0312	.0348	.0385	.0425	.0466	.0508	.0551	.0595
8	.0095	.0111	.0129	.0148	.0169	.0191	.0215	.0241	.0269	.0298
9	.0033	.0040	.0047	.0056	.0066	.0076	.0089	.0102	.0116	.0132
10	.0010	.0013	.0016	.0019	.0023	.0028	.0033	.0039	.0045	.0053
11	.0003	.0004	.0005	.0006	.0007	.0009	.0011	.0013	.0016	.0019
12	.0001	.0001	.0001	.0002	.0002	.0003	.0003	.0004	.0005	.0006
13	.0000	.0000	.0000	.0000	.0001	.0001	.0001	.0001	.0002	.0002
14	.0000	.0000	.0000	.0000	.0000	.0000	.0000	.0000	.0000	.0001

x : number of failures detected (percent defective)

m : number of expected failures (number of defective items)

	m									
x	**4.1**	**4.2**	**4.3**	**4.4**	**4.5**	**4.6**	**4.7**	**4.8**	**4.9**	**5.0**
0	.0166	.0150	.0136	.0123	.0111	.0101	.0091	.0082	.0074	.0067
1	.0679	.0630	.0583	.0540	.0500	.0462	.0427	.0395	.0365	.0337
2	.1393	.1323	.1254	.1188	.1125	.1063	.1005	.0948	.0894	.0842
3	.1904	.1852	.1798	.1743	.1687	.1631	.1574	.1517	.1460	.1404
4	.1951	.1944	.1933	.1917	.1898	.1875	.1849	.1820	.1789	.1755
5	.1600	.1633	.1662	.1687	.1708	.1725	.1738	.1747	.1753	.1755
6	.1093	.1143	.1191	.1237	.1281	.1323	.1362	.1398	.1432	.1462
7	.0640	.0686	.0732	.0778	.0824	.0869	.0914	.0959	.1002	.1044
8	.0328	.0360	.0393	.0428	.0463	.0500	.0537	.0575	.0614	.0653
9	.0150	.0168	.0188	.0209	.0232	.0255	.0280	.0307	.0334	.0363
10	.0061	.0071	.0081	.0092	.0104	.0118	.0132	.0147	.0164	.0181
11	.0023	.0027	.0032	.0037	.0043	.0049	.0056	.0064	.0073	.0082
12	.0008	.0009	.0011	.0014	.0016	.0019	.0022	.0026	.0030	.0034
13	.0002	.0003	.0004	.0005	.0006	.0007	.0008	.0009	.0011	.0013
14	.0001	.0001	.0001	.0001	.0002	.0002	.0003	.0003	.0004	.0005
15	.0000	.0000	.0000	.0000	.0001	.0001	.0001	.0001	.0001	.0002

	m									
x	**5.1**	**5.2**	**5.3**	**5.4**	**5.5**	**5.6**	**5.7**	**5.8**	**5.9**	**6.0**
0	.0061	.0055	.0050	.0045	.0041	.0037	.0033	.0030	.0027	.0025
1	.0311	.0287	.0265	.0244	.0225	.0207	.0191	.0176	.0162	.0149
2	.0793	.0746	.0701	.0659	.0618	.0580	.0544	.0509	.0477	.0446
3	.1348	.1293	.1239	.1185	.1133	.1082	.1033	.0985	.0938	.0892
4	.1719	.1681	.1641	.1600	.1558	.1515	.1472	.1428	.1383	.1339
5	.1753	.1748	.1740	.1728	.1714	.1697	.1678	.1656	.1632	.1606
6	.1490	.1515	.1537	.1555	.1571	.1584	.1594	.1601	.1605	.1606
7	.1086	.1125	.1163	.1200	.1234	.1267	.1298	.1326	.1353	.1377
8	.0692	.0731	.0771	.0810	.0849	.0887	.0925	.0962	.0998	.1033
9	.0392	.0423	.0454	.0486	.0519	.0552	.0586	.0620	.0654	.0688
10	.0200	.0220	.0241	.0262	.0285	.0309	.0334	.0359	.0386	.0413
11	.0093	.0104	.0116	.0129	.0143	.0157	.0173	.0190	.0207	.0225
12	.0039	.0045	.0051	.0058	.0065	.0073	.0082	.0092	.0102	.0113
13	.0015	.0018	.0021	.0024	.0028	.0032	.0036	.0041	.0046	.0052
14	.0006	.0007	.0008	.0009	.0011	.0013	.0015	.0017	.0019	.0022
15	.0002	.0002	.0003	.0003	.0004	.0005	.0006	.0007	.0008	.0009
16	.0001	.0001	.0001	.0001	.0001	.0002	.0002	.0002	.0003	.0003
17	.0001	.0000	.0000	.0000	.0000	.0001	.0001	.0001	.0001	.0001

	m									
x	**6.1**	**6.2**	**6.3**	**6.4**	**6.5**	**6.6**	**6.7**	**6.8**	**6.9**	**7.0**
0	.0022	.0020	.0018	.0017	.0015	.0014	.0012	.0011	.0010	.0009
1	.0137	.0126	.0116	.0106	.0098	.0090	.0082	.0076	.0070	.0064
2	.0417	.0390	.0364	.0340	.0318	.0296	.0276	.0258	.0240	.0223
3	.0848	.0806	.0765	.0726	.0688	.0652	.0617	.0584	.0552	.0521
4	.1294	.1249	.1205	.1162	.1118	.1076	.1034	.0992	.0952	.0912
5	.1579	.1549	.1519	.1487	.1454	.1420	.1385	.1349	.1314	.1277
6	.1605	.1601	.1595	.1586	.1575	.1562	.1546	.1529	.1511	.1490
7	.1399	.1418	.1435	.1450	.1462	.1472	.1480	.1486	.1489	.1490
8	.1066	.1099	.1130	.1160	.1188	.1215	.1240	.1263	.1284	.1304
9	.0723	.0757	.0791	.0825	.0858	.0891	.0923	.0954	.0985	.1014
10	.0441	.0469	.0498	.0528	.0558	.0588	.0618	.0649	.0679	.0710
11	.0245	.0265	.0285	.0307	.0330	.0353	.0377	.0401	.0426	.0452
12	.0124	.0137	.0150	.0164	.0179	.0194	.0210	.0227	.0246	.0264
13	.0058	.0065	.0073	.0081	.0089	.0098	.0108	.0119	.0130	.0142
14	.0025	.0029	.0033	.0037	.0041	.0046	.0052	.0058	.0064	.0071
15	.0010	.0012	.0014	.0016	.0018	.0020	.0023	.0026	.0029	.0033
16	.0004	.0005	.0005	.0006	.0007	.0008	.0010	.0011	.0013	.0014
17	.0001	.0002	.0002	.0002	.0003	.0003	.0004	.0004	.0005	.0006
18	.0000	.0001	.0001	.0001	.0001	.0001	.0001	.0002	.0002	.0002
19	.0000	.0000	.0000	.0000	.0000	.0000	.0000	.0001	.0001	.0001

x	m									
	7.1	**7.2**	**7.3**	**7.4**	**7.5**	**7.6**	**7.7**	**7.8**	**7.9**	**8.0**
0	.0008	.0007	.0007	.0006	.0006	.0005	.0005	.0004	.0004	.0003
1	.0059	.0054	.0049	.0045	.0041	.0038	.0035	.0032	.0029	.0027
2	.0208	.0194	.0180	.0167	.0156	.0145	.0134	.0125	.0116	.0107
3	.0492	.0464	.0438	.0413	.0389	.0366	.0345	.0324	.0305	.0286
4	.0874	.0836	.0799	.0764	.0729	.0696	.0663	.0632	.0602	.0573
5	.1241	.1204	.1167	.1130	.1094	.1057	.1021	.0986	.0951	.0916
6	.1468	.1445	.1420	.1394	.1367	.1339	.1311	.1282	.1252	.1221
7	.1489	.1486	.1481	.1474	.1465	.1454	.1442	.1428	.1413	.1396
8	.1321	.1337	.1351	.1363	.1373	.1382	.1388	.1392	.1395	.1396
9	.1042	.1070	.1096	.1121	.1144	.1167	.1187	.1207	.1224	.1241
10	.0740	.0770	.0800	.0829	.0858	.0887	.0914	.0941	.0967	.0993
11	.0478	.0504	.0531	.0558	.0585	.0613	.0640	.0667	.0695	.0722
12	.0283	.0303	.0323	.0344	.0366	.0388	.0411	.0434	.0457	.0481
13	.0154	.0168	.0181	.0196	.0211	.0227	.0243	.0260	.0278	.0296
14	.0078	.0086	.0095	.0104	.0113	.0123	.0134	.0145	.0157	.0169
15	.0037	.0041	.0046	.0051	.0057	.0062	.0069	.0075	.0083	.0090
16	.0016	.0019	.0021	.0024	.0026	.0030	.0033	.0037	.0041	.0045
17	.0007	.0008	.0009	.0010	.0012	.0013	.0015	.0017	.0019	.0021
18	.0003	.0003	.0004	.0004	.0005	.0006	.0006	.0007	.0008	.0009
19	.0001	.0001	.0001	.0002	.0002	.0002	.0003	.0003	.0003	.0004
20	.0000	.0000	.0001	.0001	.0001	.0001	.0001	.0001	.0001	.0002
21	.0000	.0000	.0000	.0000	.0000	.0000	.0000	.0000	.0001	.0001

	m									
x	**8.1**	**8.2**	**8.3**	**8.4**	**8.5**	**8.6**	**8.7**	**8.8**	**8.9**	**9.0**
0	.0003	.0003	.0002	.0002	.0002	.0002	.0002	.0002	.0001	.0001
1	.0025	.0023	.0021	.0019	.0017	.0016	.0014	.0013	.0012	.0011
2	.0100	.0092	.0086	.0079	.0074	.0068	.0063	.0058	.0054	.0050
3	.0269	.0252	.0237	.0222	.0208	.0195	.0183	.0171	.0160	.0150
4	.0544	.0517	.0491	.0466	.0443	.0420	.0398	.0377	.0357	.0337
5	.0882	.0849	.0816	.0784	.0752	.0722	.0692	.0663	.0635	.0607
6	.1191	.1160	.1128	.1097	.1066	.1034	.1003	.0972	.0941	.0911
7	.1378	.1358	.1338	.1317	.1294	.1271	.1247	.1222	.1197	.1171
8	.1395	.1392	.1388	.1382	.1375	.1366	.1356	.1344	.1332	.1318
9	.1256	.1269	.1280	.1290	.1299	.1306	.1311	.1315	.1317	.1318
10	.1017	.1040	.0163	.1084	.1104	.1123	.1140	.1157	.1172	.1186
11	.0749	.0776	.0802	.0828	.0853	.0878	.0902	.0925	.0948	.0970
12	.0505	.0530	.0555	.0579	.0604	.0629	.0654	.0679	.0703	.0728
13	.0315	.0334	.0354	.0374	.0395	.0416	.0438	.0459	.0481	.0504
14	.0182	.0196	.0210	.0225	.0240	.0256	.0272	.0289	.0306	.0324
15	.0098	.0107	.0116	.0126	.0136	.0147	.0158	.0169	.0182	.0194
16	.0050	.0055	.0060	.0066	.0072	.0079	.0086	.0093	.0101	.0109
17	.0024	.0026	.0029	.0033	.0036	.0040	.0044	.0048	.0053	.0058
18	.0011	.0012	.0014	.0015	.0017	.0019	.0021	.0024	.0026	.0029
19	.0005	.0005	.0006	.0007	.0008	.0009	.0010	.0011	.0012	.0014
20	.0002	.0002	.0002	.0003	.0003	.0004	.0004	.0005	.0005	.0006
21	.0001	.0001	.0001	.0001	.0001	.0002	.0002	.0002	.0002	.0003
22	.0000	.0000	.0000	.0000	.0001	.0001	.0001	.0001	.0001	.0001

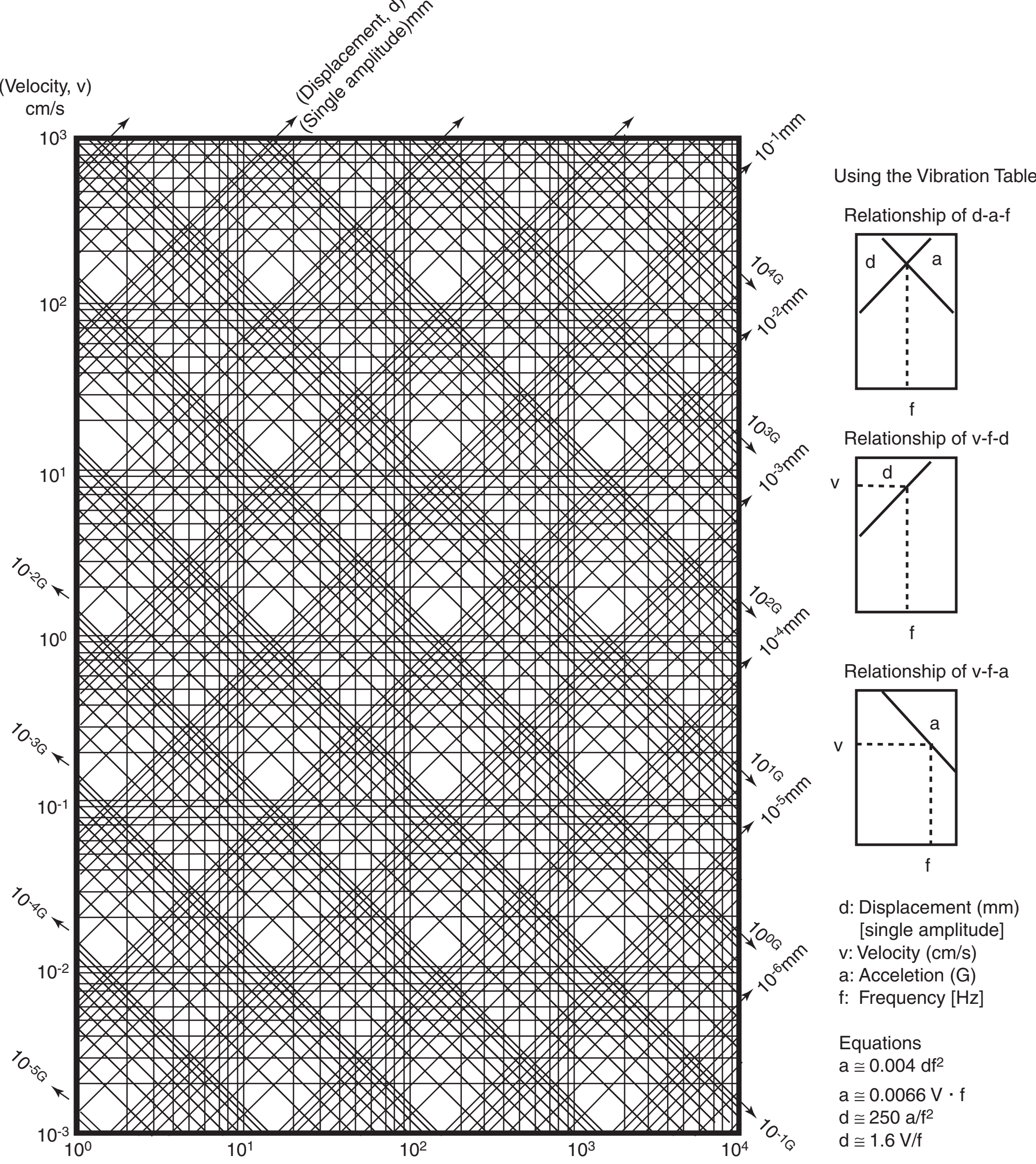
	m									
x	**9.1**	**9.2**	**9.3**	**9.4**	**9.5**	**9.6**	**9.7**	**9.8**	**9.9**	**10**
0	.0001	.0001	.0001	.0001	.0001	.0001	.0001	.0001	.0001	.0000
1	.0010	.0009	.0009	.0008	.0007	.0007	.0006	.0005	.0005	.0005
2	.0046	.0043	.0040	.0037	.0034	.0031	.0029	.0027	.0025	.0023
3	.0140	.0131	.0123	.0115	.0107	.0100	.0093	.0087	.0081	.0076
4	.0319	.0302	.0285	.0269	.0254	.0240	.0226	.0213	.0201	.0189
5	.0581	.0005	.0530	.0506	.0483	.0460	.0439	.0418	.0398	.0378
6	.0881	.0851	.0822	.0793	.0764	.0736	.0709	.0682	.0656	.0631
7	.1145	.1118	.1091	.1064	.1037	.1010	.0982	.0955	.0928	.0901
8	.1302	.1286	.1269	.1251	.1232	.1212	.1191	.1170	.1148	.1126
9	.1317	.1315	.1311	.1306	.1300	.1293	.1284	.1274	.1263	.1251
10	.1198	.1210	.1219	.1228	.1235	.1241	.1245	.1249	.1250	.1251
11	.0991	.1012	.1031	.1049	.1067	.1083	.1098	.1112	.1125	.1137
12	.0752	.0776	.0799	.0822	.0844	.0866	.0888	.0908	.0928	.0948
13	.0526	.0549	.0572	.0594	.0617	.0640	.0662	.0685	.0707	.0729
14	.0342	.0361	.0380	.0399	.0419	.0439	.0459	.0479	.0500	.0521
15	.0208	.0221	.0235	.0250	.0265	.0281	.0297	.0313	.0330	.0347
16	.0118	.0127	.0137	.0147	.0157	.0168	.0180	.0192	.0204	.0217
17	.0063	.0069	.0075	.0081	.0088	.0095	.0103	.0111	.0119	.0128
18	.0032	.0035	.0039	.0042	.0046	.0051	.0055	.0060	.0065	.0071
19	.0015	.0017	.0019	.0021	.0023	.0026	.0028	.0031	.0034	.0037
20	.0007	.0008	.0009	.0010	.0011	.0012	.0014	.0051	.0017	.0019
21	.0003	.0003	.0004	.0004	.0005	.0006	.0006	.0007	.0008	.0009
22	.0001	.0001	.0002	.0002	.0002	.0002	.0003	.0003	.0004	.0004
23	.0000	.0001	.0001	.0001	.0001	.0001	.0001	.0001	.0002	.0002
24	.0000	.0000	.0000	.0000	.0000	.0000	.0000	.0001	.0001	.0001

	m									
x	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**
0	.0000	.0000	.0000	.0000	.0000	.0000	.0000	.0000	.0000	.0000
1	.0002	.0001	.0000	.0000	.0000	.0000	.0000	.0000	.0000	.0000
2	.0010	.0004	.0002	.0001	.0000	.0000	.0000	.0000	.0000	.0000
3	.0037	.0018	.0008	.0004	.0002	.0001	.0000	.0000	.0000	.0000
4	.0102	.0053	.0027	.0013	.0006	.0003	.0001	.0001	.0000	.0000
5	.0224	.0127	.0070	.0037	.0019	.0010	.0005	.0002	.0001	.0001
6	.0411	.0255	.0152	.0087	.0048	.0026	.0014	.0007	.0004	.0002
7	.0646	.0437	.0281	.0174	.0104	.0060	.0034	.0018	.0010	.0005
8	.0888	.0655	.0457	.0304	.0194	.0120	.0072	.0042	.0024	.0013
9	.1085	.0874	.0661	.0473	.0324	.0213	.0135	.0083	.0050	.0029
10	.1194	.1048	.0859	.0663	.0486	.0341	.0230	.0150	.0095	.0058
11	.1194	.1144	.1015	.0884	.0663	.0496	.0355	.0245	.0164	.0106
12	.1094	.1144	.1099	.0984	.0829	.0661	.0504	.0368	.0259	.0176
13	.0926	.1056	.1099	.1060	.0956	.0814	.0658	.0509	.0378	.0271
14	.0728	.0905	.1021	.1060	.1024	.0930	.0800	.0655	.0514	.0387
15	.0534	.0724	.0885	.0989	.1024	.0992	.0906	.0786	.0650	.0516
16	.0367	.0543	.0719	.0866	.0960	.0992	.0963	.0884	.0772	.0646
17	.0237	.0383	.0550	.0713	.0847	.0934	.0963	.0936	.0863	.0760
18	.0145	.0256	.0397	.0554	.0706	.0830	.0909	.0936	.0911	.0844
19	.0084	.0161	.0272	.0409	.0557	.0699	.0814	.0887	.0911	.0888
20	.0046	.0097	.0177	.0286	.0418	.0559	.0692	.0798	.0866	.0888
21	.0024	.0055	.0109	.0191	.0299	.0426	.0560	.0684	.0783	.0846
22	.0012	.0030	.0065	.0121	.0204	.0310	.0433	.0560	.0676	.0769
23	.0006	.0016	.0037	.0074	.0133	.0216	.0320	.0438	.0559	.0669
24	.0003	.0008	.0020	.0043	.0083	.0144	.0226	.0328	.0442	.0557

x	m 11	12	13	14	15	16	17	18	19	20
25	.0001	.0004	.0010	.0024	.0050	.0092	.0154	.0237	.0336	.0446
26	.0000	.0002	.0005	.0013	.0029	.0057	.0101	.0164	.0246	.0343
27	.0000	.0001	.0002	.0007	.0016	.0034	.0063	.0109	.0173	.0254
28	.0000	.0000	.0001	.0003	.0009	.0019	.0038	.0070	.0117	.0181
29	.0000	.0000	.0001	.0002	.0004	.0011	.0023	.0044	.0077	.0125
30	.0000	.0000	.0000	.0001	.0002	.0006	.0013	.0026	.0049	.0083
31	.0000	.0000	.0000	.0000	.0001	.0003	.0007	.0015	.0030	.0054
32	.0000	.0000	.0000	.0000	.0001	.0001	.0004	.0009	.0018	.0034
33	.0000	.0000	.0000	.0000	.0000	.0001	.0002	.0005	.0010	.0020
34	.0000	.0000	.0000	.0000	.0000	.0000	.0001	.0002	.0006	.0012
35	.0000	.0000	.0000	.0000	.0000	.0000	.0000	.0001	.0003	.0007
36	.0000	.0000	.0000	.0000	.0000	.0000	.0000	.0001	.0002	.0004
37	.0000	.0000	.0000	.0000	.0000	.0000	.0000	.0000	.0001	.0002
38	.0000	.0000	.0000	.0000	.0000	.0000	.0000	.0000	.0000	.0001
39	.0000	.0000	.0000	.0000	.0000	.0000	.0000	.0000	.0000	.0001

A.7 Vibration Tables (Amplitude, Velocity, and Acceleration vs. Frequency)

The relationship between amplitude, velocity, and acceleration vs. frequency is shown blow.



A.8 Water Vapor Pressure Tables

- Saturated water vapor table (by temperature)

Temperature °C t	Saturation Pressure Kg/cm^2 P_s	Temperature °C t	Saturation Pressure Kg/cm^2 P_s
0	0.006228	125	2.3666
5	0.008891	130	2.7544
10	0.012513	135	3.1923
15	0.017378	140	3.6848
20	0.023830	145	4.2369
25	0.032291	150	4.8535
30	0.043261	155	5.5401
35	0.057387	160	6.3021
40	0.075220	165	7.1454
45	0.097729	170	8.0759
50	0.12581	175	9.1000
55	0.16054	180	10.224
60	0.20316	185	11.455
65	0.25506	190	12.799
70	0.31780	195	14.263
75	0.39313	200	15.856
80	0.48297	210	19.456
85	0.58947	220	23.660
90	0.71493	230	28.534
95	0.86193	240	34.144
100	1.03323	250	40.564
105	1.2318	260	47.868
110	1.4609	270	56.137
115	1.7239	280	65.456
120	2.0245	290	75.915
		300	87.611

(Source: The Japan society of machinery water vapor tables (new edition))

Note: 1 kg/cm^2 = 0.9678 atm

- Saturated water vapor table (by pressure)

Pressure Kg/cm^2 P	Saturation Temperature °C t_a	Pressure Kg/cm^2 P	Saturation Temperature °C t_a
0.1	45.45	3.6	139.18
0.2	59.66	3.8	141.09
0.3	68.67	4.0	142.92
0.4	75.41	4.2	146.38
0.5	80.86	5.0	151.11
0.6	85.45	6	158.08
0.7	89.45	7	164.17
0.8	92.99	8	169.61
0.9	96.18	9	174.53
1.0	99.09	10	179.04
1.1	101.76	11	183.20
1.2	104.25	12	187.08
1.3	106.56	13	190.71
1.4	108.74	14	194.13
1.5	110.79	15	197.36
1.6	112.73	16	200.43
1.8	116.33	17	203.36
2.0	119.62	18	206.15
2.2	122.64	19	208.82
2.4	125.46	20	211.38
2.6	128.08	25	222.90
2.8	130.55	30	232.75
3.0	132.88	35	241.41
3.2	135.08	40	249.17
3.4	137.18	45	256.22
		50	262.70

(Source: The Japan society of machinery water vapor tables (new edition))

Note: 1 kg/cm^2 = 0.9678 atm

B. Reliability Theory

B.1 Reliability Criteria

B.1.1 Failure Rate and Reliability Function

If we observe a sample of n devices at fixed time intervals h, we obtain a frequency distribution of the number of failures as shown in figure B.1. In this analysis, ri devices fail in the period ti – ti – 1 = h, with all devices failing before the time tn.

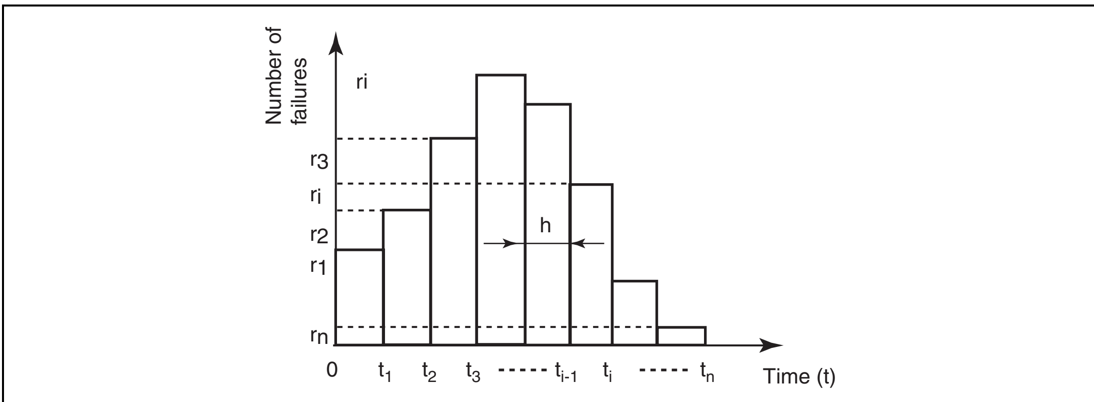


Figure B.1 Discrete Failure Distribution

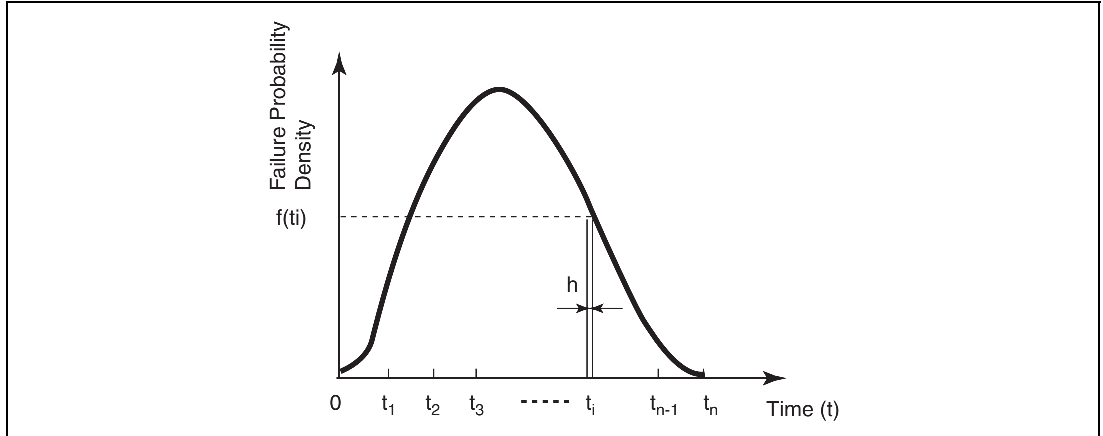


Figure B.2 Continuous Failure Distribution

The number of devices left after the i-th measurement period is given as $n_i = n - \sum_{i=1}^{i} r_i$. The average failure rate $\hat{\lambda}(t_i - 1, t_i)$ in the period between ti-1 and ti is given by the expression

$$\hat{\lambda}(t_i - 1, t_i) = \frac{r_i}{n_i - 1} \bullet \frac{1}{h} \quad \text{(IX-1)}$$

If we make the time interval h increasingly small and use the failure rate density function f(t), the instantaneous failure rate λ (ti, ti + h) in the interval from ti to ti + h, shown in figure B.2, is given by

$$\lambda(t_i, t_i + h) = \frac{f(t_i) \bullet h}{\int_{ti}^{\infty} f(t)dt} \bullet \frac{1}{h} = \frac{f(t_i)}{\int_{ti}^{\infty} f(t)dt} \quad \text{(IX-2)}$$

Equation IX-2 is the generalization of the model in figure B.2 with tn as infinity.

The probability that a device will fail before the time ti is known as the failure (or non-reliability) distribution function f(ti). Also, the probability that a device will not fail before time ti is the reliability function R(ti). These functions are shown in figure B.3.

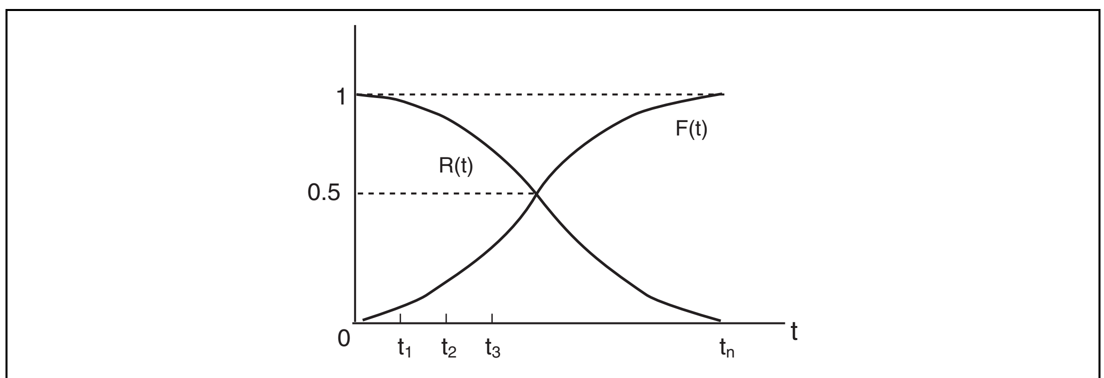


Figure B.3 Failure Distribution Function F(t) and Reliability Function R(t)

$$F(t_i) = \int_0^{t_i} f(t)dt \qquad \text{(IX-3)}$$

$$R(t_i) = 1 - F(t_i) = \int_{t_i}^{\infty} f(t)dt \qquad \text{(IX-4)}$$

The probability P that a given semiconductor device will fail in the period between t and t + dt is the product of the probability R(t) that it will not fail before t and the instantaneous failure rate λ(t)dt in the period t to t + dt.

$$P = f(t)dt = R(t) \cdot \lambda(t)dt$$

$$\therefore \lambda(t) = \frac{f(t)}{R(t)} \qquad \text{(IX-5)}$$

For the failure rate λ(t), using the relationship of equation IX-4 we have

$$\lambda(t) = -\frac{1}{R(t)}\frac{d}{dt}R(t) = \frac{d}{dt} 1nR(t) \qquad \text{(IX-6)}$$

$$R(t) = \exp\left(-\int_0^t \lambda(t)dt\right) \qquad \text{(IX-7)}$$

B.1.2 Definition of Reliability Index

Mean value (or expected value) μ and variance σ^2 (where σ is the standard deviation) are defined as characteristics of the distributions of figures B.1 and B.2 by the following expressions:

$$\left.\begin{aligned} \mu &= \int_0^\infty t f(t)\,dt \\ \sigma^2 &= \int_0^\infty (t-\mu)^2 f(t)dt = \int_0^\infty t^2 f(t)dt - \mu^2 \end{aligned}\right\} \text{(Continuous distribution)} \qquad \text{(IX-8)}$$

$$\left.\begin{aligned} \mu &= \sum_{i=0}^{\infty} t_i f(t_i) \\ \sigma^2 &= \sum_{i=0}^{\infty} (t_i - \mu)^2 f(t_i) = \sum_{i=0}^{\infty} t_i^2 f(t_i) - \mu^2 \end{aligned}\right\} \text{(Discrete distribution)} \qquad \text{(IX-9)}$$

The expected lifetime (remaining lifetime) L(t) of a device which has been operated for time t is given by the following expressions:

$$\left.\begin{aligned} L(t) &= \frac{1}{R(\gamma)}\left\{\gamma - t + \int_\gamma^\infty R(t)dt\right\} && (t \le \gamma) \\ L(t) &= \frac{1}{R(t)}\int_\gamma^\infty R(x)dx = \frac{1}{R(t)}\int_0^\infty R(t+y)dy && (\gamma \le t) \end{aligned}\right\} \qquad \text{(IX-10)}$$

Note that the device failure distribution function (equation IX-3) takes on the constant g in the range $0 \le t \le \gamma$, that is,

$$F(t) = 0 \ (0 \le t \le \gamma)$$

and that after the passage of time g it assumes a value (g is the order of position).

When equipment can be repaired by renewing a failed device, the mean value of the interval that operation is possible between occurrences of failures is know as the MTBF (Mean Time Between Failures).

If the operating time between subsequent failures of a device throughout its life until discarded is given by t1, t2, ..., tn, the MTBF is given by

$$MTBF = \frac{t_1 + t_2 + \ldots + t_n}{n} \qquad \text{(IX-11)}$$

Since we are dealing with the measure of the entire operating life of the device, we will call (t1, t2, ..., tn) a complete sample. MTBF known after the life of equipment is of no practical use. Therefore, the MTBF for a truncated portion of the life of the equipment up to the time T0 is estimated using the following expression:

$$MTBF = \frac{t1 + t2 + \cdots + tr + (n - r)\, To}{n} \qquad \text{(IX-12)}$$

In equation IX-12, r is the number of failures occurring until the time T0.

We can also estimate the MTBF truncated after the number of failures = r.

$$MTBF = \frac{t1 + t2 + \cdots + tr + (n - r)\, tr}{r} \qquad \text{(IX-13)}$$

In equations IX-12 and IX-13, the value n is determined by the type of failures for the device being considered (including such factors as the total number of semiconductor devices used and maximum number of failures before the equipment is disposed of).

In general, once a semiconductor device has failed, it cannot be repaired and used again. That is, it is a non-maintainable component. For this type of device, the mean time to the occurrence of a failure is know as the MTTF (Mean Time to Failure). As can be seen from equation IX-10, the remaining expected life L(t) is not equal to the MTTF minus the actual operating time. This is analogous to the fact that the remaining life of an adult is not necessarily equal to the expected lifetime of a new born child minus the adult's actual age.

In the period that failure rate λ (t) is time-independent and is constant, taking the value λ, we can use equation IX-7 to obtain

$$MTTF = \int_0^{\infty} R(t)dt = \int_0^{\infty} e^{-\lambda t}\, dt = \frac{1}{\lambda} \qquad \text{(IX-14)}$$

As a unit for the measure of failure rate,

$$1 \times 10^{9} \text{ (failures/(number of operating devices} \times \text{operating time))} = 1\text{FIT} \qquad \text{(IX-15)}$$

is used. For example, if we say that a given semiconductor device has a failure rate of 10 FIT, this means that one device fails for every 10^8 component hours. This, however, is not equivalent to saying the device lifetime is 10^8 hours. This is because the denominator of the defining expression equation IX-15 (component hours) does not refer to any particular device.

B.2 Reliability of Composite Devices

B.2.1 Parallel and Series Models

Assume that we have n semiconductor devices used in series, and one device failure will result in the total group of devices failing. Such a system is known as a series system of redundancy of 0 (figure B.4). If all the individual devices have failure mechanisms that are mutually independent, and the reliability function of the i-th device is given by the expression Ri(t) (where i = 1, 2, ..., n), the reliability function R (t) of this series system is

$$R(t) = \prod_{i=1}^{n} Ri(t) \qquad \text{(IX-16)}$$

Equation IX-3 used for integrated circuit models in Section 3.2.2 can be modified to

$$\lambda p = C_1\pi_1 + C_2\pi_2$$

Where $\pi_1 = \pi_Q \times \pi_T \times \pi_V \times \pi_L$

$\pi_2 = \pi_Q \times \pi_E \times \pi_L$

Then the reliability function equation IX-7 for integrated circuits can be expressed as follows using equation IX-16.

$$R(t) = e^{-\lambda pt} = e^{-C1\pi1t} \cdot e^{-C2\pi2t} = R_1(t) \cdot R_2(t)$$

Where $R_1(t) = e^{-C1\pi1t}$

$R_2(t) = e^{-C2\pi2t}$

Hence equation IX-3 is an equation derived by applying a series model of redundancy of 0 (figure B.4) involving a failure factor (C_1) attributable to circuit complexity and a failure factor (C_2) caused by package complexity to integrated circuits.

There are other systems that n semiconductor devices are used in parallel, and as long as at least one of the devices is operating, the overall multiple device still functions. This is a parallel system with a redundancy of n -1 (figure B.5). In this case as well, the failures of individual devices are taken to be mutually independent. If the failure distribution function for the i-th device is Fi(t) (where i = 1, 2, ..., n), the failure distribution probability function F(t) for the parallel system is

$$F(t) = \prod_{i=1}^{n} Fi(t) \quad \text{(IX-17)}$$

$$R(t) = 1 - F(t) \quad \text{(IX-18)}$$

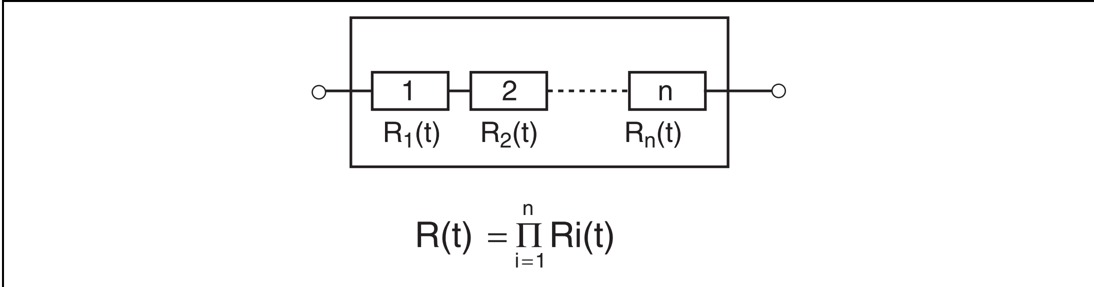


Figure B.4 Reliability Function for Series Model

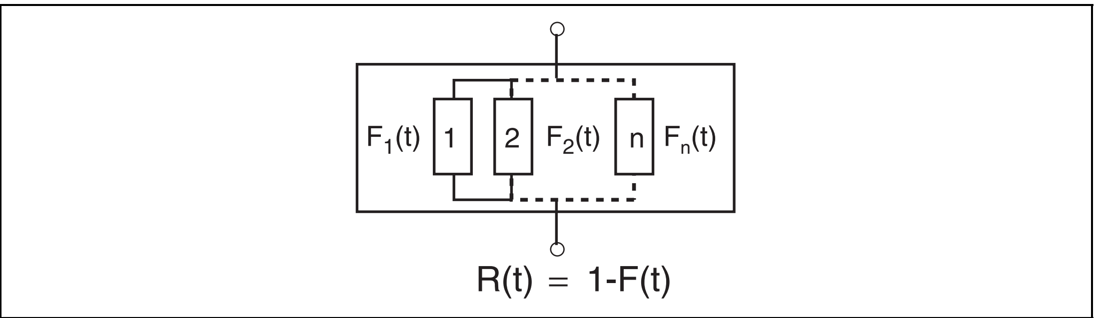


Figure B.5 Reliability Function for Parallel Model

B.2.2 Application Example

Let us consider the reliability function of the system in figure B.6. This model consists of m units connected in series, which i-th unit has ni devices connected in parallel. Moreover, we consider the system in figure B.7, in which units of m series connected devices are connected in parallel up to n units. For the system in figure B.6, let us assume that the reliability function for devices in the i-th unit is the same, which is Ri(t). In figure B.7, we assume that the reliability function for the i-th series connected devices Rij (where j = 1, 2, ..., m) is the same and is Ri(t). For the system in figure B.6 we have

$$R(t) = \prod_{i-1}^{m} \{1 - (Ri(t))^{n}\} \qquad \text{(IX-19)}$$

and for the system in figure B.7 we have

$$R(t) = 1 - (1 - \prod_{i=1}^{m} Ri(t))^{n} \qquad \text{(IX-20)}$$

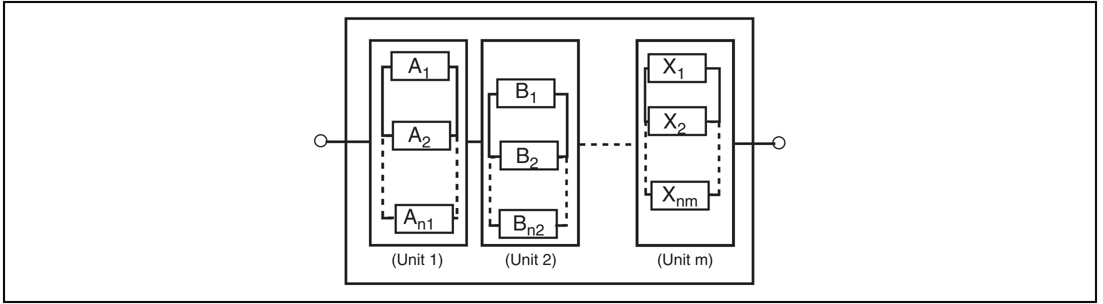


Figure B.6 Series-Parallel Composite Model (1)

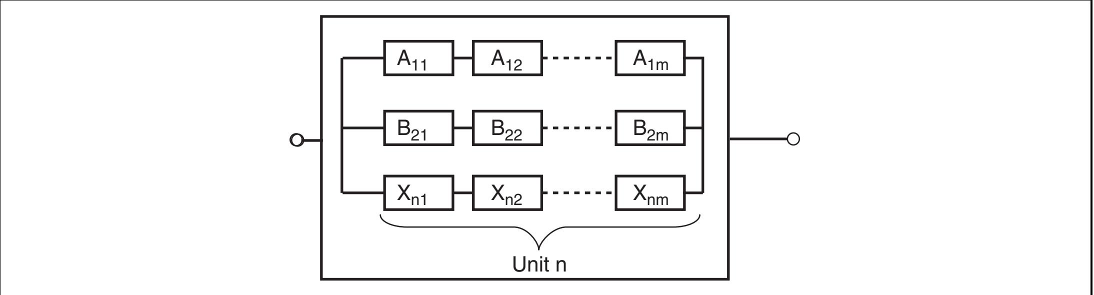


Figure B.7 Series-Parallel Composite Model (2)

B.2.3 Stand-by Redundancy System

If we attach a selector switch to n devices in the parallel model shown in figure B.5, we can select another device should one particular device experience a failure (figure B.8).

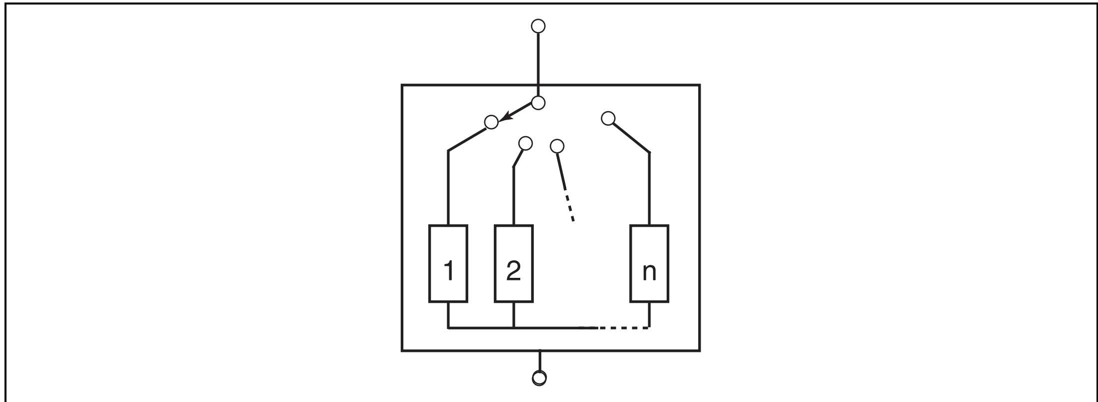


Figure B.8 Stand-by Redundancy Model

We will assume for simplicity that the switch does not fail and that the failure rates for the n devices are all equal to l. The reliability function R(t) for this system is given by the Poisson partial sum.

$$R(t) = e^{-\lambda t} \sum_{i=0}^{n-1} \frac{(\lambda t)^i}{i!} \qquad \text{(IX-21)}$$

An explanation of this equation will be given in B.4.9, Poisson Distribution.

If we now assume that the failure rate of the switch is equal to lk for any tap, the overall reliability function becomes

$$R(t) = e^{-\{\lambda + (n-1)\lambda_k\}t} \sum_{i=0}^{n-1} \frac{(\lambda t)^i}{i!} \qquad \text{(IX-22)}$$

B.3 Failure Models for Accelerated Life Testing

B.3.1 Reaction Theory Model

A particular characteristic of a device has the value X. Let us assume that the device will fail when the characteristic value changes to X_L. If the amount of change in the characteristic value is found to be accelerated by thermal stress, in many cases the Arrhenius chemical reaction kinetics model can be applied to this phenomenon.

In chemical reactions, if molecules reach the temperature above which they may react (the activation energy), a reaction occurs. The higher the temperature of the molecules, the higher becomes their energies, and so increasing the temperature quickens reactions. Arrhenius expressed the chemical reaction rate, K, experimentally as follows:

$$K = \Lambda e^{-\frac{\Delta E}{kT}} \qquad \text{(IX-23)}$$

where

Λ: experimentally derived constant

k: Boltzmann's constant

ΔE: activation energy (kcal/mol)

T: absolute temperature (K).

When considering the reliability of semiconductor devices, the activation energy is usually expressed in units of electron volts (eV), so that the Arrhenius relationship becomes

$$K = \Lambda e^{-\frac{\Delta E}{kT}} = \Lambda e^{11606 \times \left(-\frac{B}{T}\right)} \qquad \text{(IX-24)}$$

where

B: activation energy (eV).

1eV is equivalent to 23.05 kcal/mol or 11,606 K.

B.3.2 Eyring Model

The Eyring model is an extension of the Arrhenius model, and takes into consideration both mechanical stress and voltage stress as well as thermal stress. The reaction rate K using this model is given by the following expression:

$$K = A\left(\frac{kT}{h}\right) \cdot e^{-\frac{\Delta E}{kT}} \cdot e^{\left\{f(s) \cdot \left(C + \frac{D}{kT}\right)\right\}} \qquad \text{(IX-25)}$$

where

A, C, and D: constants

ΔE: activation energy

k: Boltzmann's constant

T: absolute temperature (K)

h: Planck's constant

f(s): stress function representing non-thermal stresses s

Here

$$f(s) = 1ns, \quad C + \frac{D}{kT} = F$$

so that for small ranges of T, an approximation of equation IX-25 becomes

$$K = \Lambda T e^{-\frac{B}{T}} s^{F} \qquad \text{(IX-26)}$$

B.3.3 Acceleration Factor

Let us assume that an intermittent operation life test performed on a semiconductor device detected, as a result of the stress placed on the device, a leakage current which increases with time. As the device is subjected to more and more cycles of intermittent operation (n), as shown in figure B.9, the leakage current increases. The level of degradation of the device can be expressed as a function of the leakage current i. If we take this current i as the device characteristic X discussed in B.3.1, we can say that there is a failure criterion current iR MAX which corresponds to the device failure point XL. That is,

$$f = f(i) \qquad \text{(IX-27)}$$

Since the reaction rate K in the accelerated life test is basically defined as the rate of degradation of the device, we have

$$K = \frac{df(i)}{dt} \qquad \text{(IX-28)}$$

$$\therefore f(i) = Kt \qquad \text{(IX-29)}$$

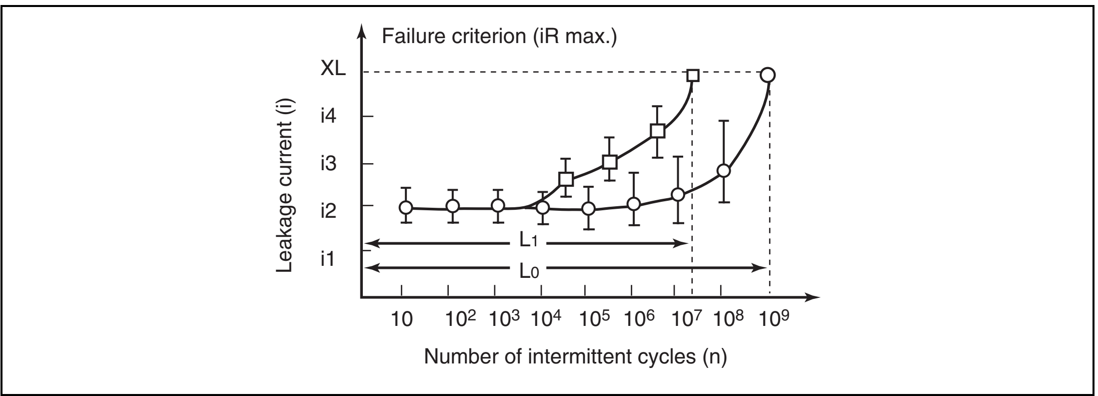


Figure B.9 Data Example for Intermittent Operation Life Test

The pattern of degradation f caused by the intermittent test varies depending upon the current flowing in the device. In figure B.9 the curve marked with circles represents such test performed at the rated current of the device, while that marked with squares shows the results of operating the device intermittently at 1.5 times the rated current. Since in either case the device fails when i = iR MAX, if we use the subscripts 0 and 1 to represent test conditions for these two cases, we have

$$L_0 = \frac{f(i_R\ MAX)}{K0},\ L_1 = \frac{f(i_R\ MAX)}{K1} \quad \text{(IX-30)}$$

In this case, the current acceleration factor $\alpha 1$ is

$$\alpha_1 = \frac{L_0}{L_1} = \frac{K_1}{K_0} \quad \text{(where the subscript 0 represents operation at the rated current)} \quad \text{(IX-31)}$$

For the purposes of the explanation we have used an actual example, as shown in figure B.9. We can, however, make a generalization about the state function f(X) and the characteristic value X that defines the state. If we use the relationship in equation IX-29 in the Arrhenius equation of equation IX-24, we have

$$K = \Lambda e^{-\frac{\Delta E}{kT}} = \frac{f(X)}{X} \quad \text{(IX-32)}$$

If we assume that the device reaches the end of its life when the characteristic value X = XL, as discussed in B.3.1, equation IX-32 will be

$$K = \frac{f(X_L)}{L} \quad \text{(IX-32')}$$

Then we have the relationship between temperature and life as

$$1nL = 1nf\,(X_L) - 1n\Lambda + \frac{\Delta E}{kT} \quad \text{(IX-33)}$$

Life tests using temperature as a dominant factor are verified by a logarithmic normal distribution. This is based on equation IX-33. If we let T0 and L0 be the reference conditions (such as the standard operating conditions) for temperature and life, and T1 and L1 be the corresponding temperature and life for accelerated conditions, the temperature acceleration factor aT is referring to equation IX-32,

$$\alpha_T = \frac{L_0}{L_1} = e^{\frac{\Delta E}{k}\left(\frac{1}{T0} - \frac{1}{T1}\right)} \quad \text{(IX-34)}$$

As can be seen by equation IX-34, acceleration caused by heat varies depending on the activation energy ΔE. The relationship between activation energy and the acceleration factor is shown in figure B.10.

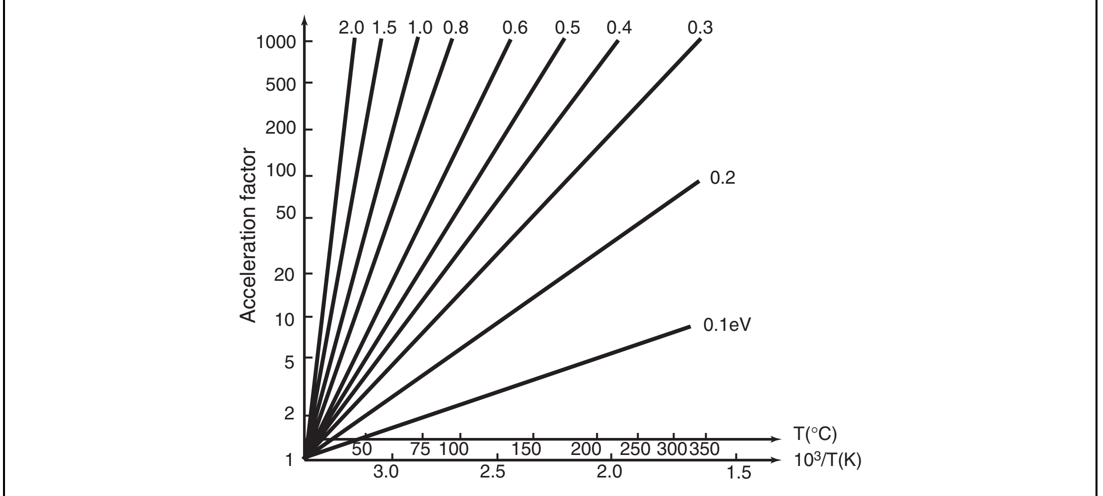


Figure B.10 Activation Energy Versus Acceleration Factor

B.4 Probability Models Used in Reliability Analysis

B.4.1 Bernoulli Trial

From a given population of semiconductor devices a single device is sampled and tested. The possible test results are limited to either (1) "failure or defect"or (2) "no failure or acceptance," with no possibility of such results as "pending decision" or "exception acceptance" allowed. This cycle of sampling, testing, and rejection/acceptance is repeated n times. In a single such test the probability of (1) "failure" is p and the probability of (2) "no failure" is q (p + q = 1). The values of p and q will be uniform for all test results. Each test result is independent from one another. This discrete model is termed the Bernoulli trial or sampling. For ease of understanding we have chosen "failure" and "no failure" for results (1) and (2), respectively. The fundamental condition of the Bernoulli trial is that results are only two types and they are definitely identified.

B.4.2 Binomial Distribution: fBin(x, n, p)

In the Bernoulli trial, assume that x of n tests result in (1) and n - x tests result in (2). Such a phenomenon occurs with some probability. This probability is described by the binomial probability distribution fBin(x, n, p).

$$\left.\begin{aligned} & f_{Bin}(x, n, p) = \binom{n}{x} p^x q^{n-x} = \frac{n!}{x!(n-x)!} p^x q^{n-x} \\ & \mu = np, \ \sigma^2 = npq \end{aligned}\right\} \qquad \text{(IX-35)}$$

A sample lot comprising n devices randomly selected from a large population whose average fraction defective is p, contains x defective devices with some probability. Such a probability is a typical example of the binomial probability distribution.

B.4.3 Negative Binomial Distribution: fneg – bin(x, n, p) and Multinomial Distribution: fmulti-bin(x1, x2, ..., xm, n, p1, p2, ..., pm)

Let us consider the number of tests n required before we encounter (1) "failure" x times in the Bernoulli trial. By the (n – 1) th test there have been x - 1 times of (1) and (n – 1) – (x – 1) = n – x times of (2), and the x-th failure occurs on the n-th test. The probability of this, fneg-bin(x, n, p) is

$$f\text{neg} - \text{bin}(x, n, p) = \binom{n-1}{x-1} p^{x-1} \cdot q^{(n-1)-(x-1)} \cdot p = \binom{n-1}{n-x} p^x q^{n-x} \qquad \text{(IX-36)}$$

Using the characteristics of binomial coefficients, we have

$$\binom{-x}{x-1} = (-1)^{n-x} \binom{n-1}{n-x}$$

Hence from equation IX-36,

$$\sum_{n=x}^{\infty} f\text{neg} - \text{bin}(x, n, p) = \sum_{n=x}^{\infty} \binom{n-1}{n-x} p^x q^{n-x} = p^x \sum_{n=x}^{\infty} (-1)^{n-x} \binom{-x}{n-x} q^{n-x}$$

$$= p^x \sum_{r=0}^{\infty} \binom{-x}{r} (-q)^r = p^x (1-q)^{-x} = 1 \qquad \text{(IX-37)}$$

Since fneg – bin (x, n, p) ≥ 0, we have, from equation IX-37

$$\left.\begin{aligned} &\text{fneg} - \text{bin}(x, n, p) = \binom{n-1}{n-x} p^x q^{n-x} = \binom{-x}{n-x} p^x q^{n-x} \\ &\mu = \frac{xq}{p}, \quad \sigma^2 = \frac{xq}{p2} \end{aligned}\right\} \qquad \text{(IX-38)}$$

There is a case that test results are not limited to two possible results of acceptance and rejection but fall into m classes (E1, E2, ..., Em). Let us examine the probability fmulti – bin(x1, x2, ..., xm, n, p1, p2, ..., pm) with which tested devices fall into these classes. After n times of tests, any one of the results is E1, E2, ..., or Em. The result Ei occurs with the probability pi. The result Ei is observed xi times ($\sum_{i=1} xi = n, n \geq xi \geq 0$) during n tests. Hence, results fall into m classes (E1, E2, ..., Em) numbering x1, x2, ..., xm with the probability fmulti – bin(x1, x2, ..., xm, n, p1, p2, ..., pm). This is known as the multinomial distribution.

$$f\text{multi} - \text{bin}(x1, x2, \ldots xm, n, p1, p2 \ldots pm) = \frac{n!}{x1!\,x2! \ldots xm!} p1^{x1} p2^{x2} \ldots pm^{xm} \qquad \text{(IX-39)}$$

The multinomial distribution is an extended binomial distribution with m variables.

B.4.4 Geometric Distribution: fGeo(n, p)

In the Bernoulli trial, the first 1 "failure" is encountered on the n-th test. The probability of this phenomenon is expressed by the geometric distribution fGeo(n, p)

$$\left.\begin{array}{l} f_{Geo}(n,\ p) = q^{n-1}p\ \ (n = 1,2,\ \dots) \\ \mu = \dfrac{q}{p},\ \sigma^2 = \dfrac{q}{p^2} \end{array}\right\} \qquad \text{(IX-40)}$$

The geometric distribution is a case of equation IX-38 for the negative binomial distribution where x = 1. The mean value of the geometric distribution μ is the expected value for the number of tests in Bernoulli trial before the first occurrence of 1. The failure distribution function of the geometric distribution is

$$F_{Geo}(N,\ p) = \sum_{n=1}^{N} f_{Geo}(n,\ p) = p + qp + q^2 p + \dots + q^{N-1}p = 1 - q^N$$

which indicates that even if the acceptance rate q on any particular test is high (q 1), a failure will eventually occur $(\lim_{N\to\infty} F_{Geo}(N, p) = 1)$ with a larger number of tests N.

B.4.5 Hypergeometric Distribution: fH - geo(N, R, n, x)

In the mass production of semiconductor devices a widely used technique is the sampling of a small number of devices n from a large population of N devices and making decision on the total population based on observation of the sample alone. An overall population of N devices has R defective devices (R is not known unless 100% inspection is performed). By inspecting n randomly sampled devices, x defective devices are detected with the probability fH - geo (N, R, n, x). If min (R, n) represents the smaller of R and n, we have

$$\left.\begin{array}{l} f_{H-geo}\ (N, R, n, x) = \dfrac{\dbinom{R}{x}\dbinom{N-R}{n-x}}{\dbinom{N}{n}}\ (0 \le x \le \min(R, n)) \\ \mu = n\dfrac{R}{N} = np,\quad \sigma^2 = \dfrac{N-n}{N-1}npq \end{array}\right\} \qquad \text{(IX-41)}$$

This is referred to as the probability function of hypergeometric distribution. Different ways are available for sampling n devices from N devices. If the sampled device is returned each time to choose a device from N constantly, or using replacement operations in other words, we will obtain a binomial distribution. If the sampled device is not returned (non-replacement), we will have a hypergeometric distribution. If the original population is large, however, the fraction defective obtained through a sampling inspection can be approximated by the binomial distribution. By expanding equation IX-41 and reordering the product terms, we have

$$f_{H-geo}(N, R, n, x) = \binom{n}{x} \prod_{j=0}^{x-1} \frac{R-i}{N-i} \prod_{j=0}^{n-x-1} \left(1 - \frac{R-x}{N-x-j}\right) \tag{IX-42}$$

If N and R increase to infinity while maintaining $\frac{R}{N} = p$ constant, for finite n (and therefore finite x) we have

$$\lim_{N,R\to\infty} \prod_{i=0}^{x-1} \frac{R-i}{N-i} = \left(\frac{R}{N}\right)^x = p^x, \quad \lim_{N,R\to\infty} \prod_{j=0}^{n-x-1} \left(1 - \frac{R-x}{N-x-j}\right) = \left(1 - \frac{R}{N}\right)^{n-x} = (1-p)^{n-x}$$

Using this relation and letting N and R approach infinity to the limit, from equation IX-42 we obtain

$$f_{H-geo}(N, R, n, x) \to \binom{n}{x} p^x (1-p)^{n-x} = f_{Bin}(x, n, p) \tag{IX-43}$$

An actual sampling plan sets a rejection criterion number c. If the number of defective devices x detected in a sample of n devices does not exceed c, the entire lot is considered to have passed inspection. When n devices are sampled from a population with fraction defective ($p\left(=\frac{R}{N}\right)$) the number of defective devices x will not exceed c with some probability. This probability ψ with which the lot is judged to be accepted (the lot acceptance rate) is given by equation IX-44.

$$\Psi = \sum_{x=0}^{c} f_{H-geo}(N, Np, n, x) = \sum_{x=0}^{c} \frac{\binom{Np}{x}\binom{Nq}{n-x}}{\binom{N}{Np}} \tag{IX-44}$$

The lot acceptance rate ψ varies depending on how the values of n and c are chosen for populations of the same quality level (i.e., p being the same value), as is clearly indicated by equation IX-44. How the lot acceptance rate changes is illustrated by the operation characteristic curve (OC curve) in figure B.11. The fraction defective ($p\left(=\frac{R}{N}\right)$) with which the population contains defective devices is plotted on the horizontal axis. The probability ψ with which the lot is judged to be accepted through sampling inspection is plotted on the vertical axis.

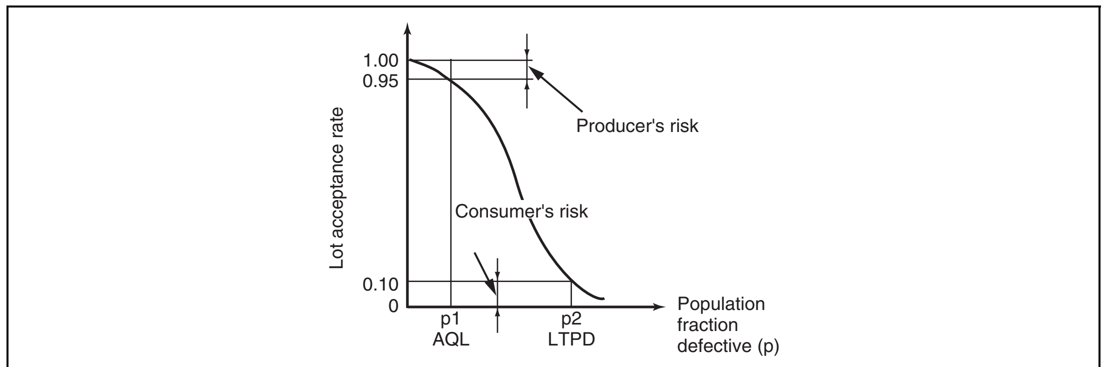


Figure B.11 OC Curve

In some sampling plans, the fraction defective p1 is set to control the lot acceptance rate to, for example, 95%. This plan is known as the AQL (Acceptable Quality Level) plan. In this case, 5% of lots whose quality level could be accepted (fraction defective p1) are rejected by sampling inspection. The producer gives up shipping the 5%. The risk of this rejection implies the producer's loss, so the risk is referred to as producer's risk.

In some other inspection plans, lots whose fraction defective is p2 are accepted with a probability of, for example, 10%. Such an inspection plan is known as the LTPD (Lot Tolerance Percent Defective) plan. This implies that the consumer takes a risk of purchasing a lot whose fraction defective is p2 with a probability of 10%. This is known as consumer's risk.

The AQL plan measures the lot whose fraction defective is p1 as having the lowest acceptable quality level. In contrast, the LTPD plan verifies that the fraction defective is no more than p2 with 90% probability.

B.4.6 Exponential Distribution: fexp(t)

The failure rate is constant with time in the random failure period. Therefore, from equation IX-7, we have

$$\left.\begin{aligned} R(t) &= e^{-\lambda t} \\ f_{exp}(t) &= \lambda e^{-\lambda t} \end{aligned}\right\} \quad \text{(IX-45)}$$

$$\mu = \frac{1}{\lambda} = \text{MTTF (or MTBF)}, \quad \sigma^2 = \frac{1}{\lambda^2} \quad \text{(IX-46)}$$

Observation of a model with a constant failure rate may be either continuous or discrete at fixed intervals. By considering the probability of detecting the first failure at time t, the relation of exponential and geometric distributions can be identified.

Let us assume that floating dust causes an average of r mask defects on the surfaces of silicon wafers of a given lot. The area of the wafer surface S is divided into many portions. From one end of the wafer, each portion is inspected with a microscope. Since the location of the dust particles on the wafer surface is unpredictable, we can assume that mask defects occur completely at random. Therefore, the failure rate λ is uniform over the wafer's entire surface, so $\lambda = \frac{r}{S}$, the probability p of a mask defect existing in a divided portion is

$$p = C\lambda \quad \text{(IX-47)}$$

where C is the area of the portion.

If the first detection of a mask defect is in the x-th portion, that is, the first detection occurs when the inspected area reaches t (t = Cx), the probability that this phenomenon will occur is expressed by the geometric distribution $pq^{x-1} = p(1-p)^{x-1}$ on the average in the portion C that includes t. A mask defect can be detected at the same level of expectation at the inspection area t and at the number of inspection cycles x (figure B.12).

$$\text{Mask defect expectation} = \lambda t = xp \quad \text{(IX-48)}$$

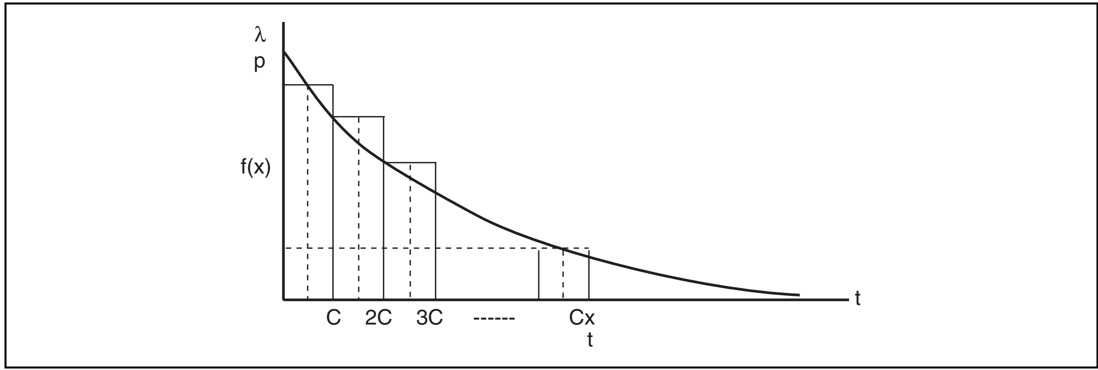


Figure B.12 Relation between Geometric and Exponential Distributions

Incidentally, continuous observation is in this case equivalent to reduction of the area C to the limit. The average probability of finding a mask defect within the area C approaches the probability that a mask defect exists on a point on the surface of the wafer. Noting the relations expressed by equations IX-47 and IX-48, we have

$$\lim_{C\to 0}\frac{1}{C}pq^{x-1} = \lim_{C\to 0}\frac{P}{C}(1-p)^{x-1} = \lambda \lim_{p\to 0}\left[(1-p)^{\frac{1}{p}}\right]^{\lambda t}\cdot\frac{1}{1-p} = \lambda e^{-\lambda t} \qquad \text{(IX-49)}$$

This implies that the exponential distribution is equivalent to the limit of the geometric distribution.

B.4.7 Pascal Distribution: fPas(x, y, p)

In a Bernoulli trial comprising n = x + y tests, there may be a case that the last n-th test result is (1) "failure" after x times of (1) "failure" and y times of (2) "no failure." The probability that this phenomenon occurs is expressed by the Pascal probability distribution fPas(x, y, p).

$$\left.\begin{aligned} f_{Pas}(x, y, p) &= \binom{x+y-1}{y} P^x q^y \\ \mu = \frac{qy}{p}&,\ \sigma^2 = \frac{qy}{p^2} \end{aligned}\right\} \qquad \text{(IX-50)}$$

If x = 1 in a specific case, the Pascal distribution is the same as the geometric distribution.

$$f_{Pas}(1, y, p) = pq^y = f_{Geo}(y+1, p) \qquad \text{(IX-51)}$$

Consider that products are randomly sampled from a flow process in a production line for the purpose of intermediate inspection. The probability of defective items produced in the manufacturing process is p. For a sampling inspection of n = x + r items, the probability that the r-th failed product is detected is expressed by the Pascal distribution.

We can find a relation between the Pascal distribution and the binomial distribution if we interpret the Pascal distribution as a Bernoulli trial comprising n - 1 tests with phenomenon 1 invariably occurring at the last n-th time after x - 1 times of phenomenon 1.

$$f_{Pas}(x, y, p) = p\, f_{Bin}(x-1, n-1, p) \qquad \text{Where} \quad n = x + y \tag{IX-52}$$

B.4.8 Gamma Distribution: $f\Gamma(t, \alpha, \beta)$

We can derive the relation below from equation IX-50 representing the Pascal distribution.

$$f_{Pas}(x, y, p) = \frac{p(n-1)}{x-1} f_{Pas}(x-1, y, p), \qquad \text{Where } n = x + y \tag{IX-53}$$

From equations IX-51 and IX-49, we have

$$f_{Pas}(1, y, p) = f_{Geo}(y+1, p) \rightarrow f_{exp}(\lambda t) = \lambda e^{-\lambda t} \tag{IX-54}$$

In equation IX-54, the arrow → denotes the operation $\lim_{C \to 0}$ used to reduce the divided portion C for discrete observation, which is the relation shown by equation IX-49. Noting the relation expressed by Eqs. IX-53 and IX-54, we can obtain Pascal probability distribution functions respectively for x = 1, 2, 3, ...

$$x = 1: f_{Pas}(1, y, p) \rightarrow \lambda e^{-\lambda t} \tag{IX-55}$$

$$x = 2: f_{Pas}(2, y, p) = \frac{p(n-1)}{1} f_{Pas}(1, y, p) = \frac{\lambda t}{1} f_{Pas}(1, y, p) \rightarrow \frac{\lambda t}{1} \lambda e^{-\lambda t} \tag{IX-56}$$

In equation IX-56, we used the relation represented by equation IX-48. Similarly we have

$$x = 3: f_{Pas}(3, y, p) = \frac{\lambda t}{1} \cdot \frac{\lambda t}{2} f_{Pas}(1, y, p) \rightarrow \frac{(\lambda t)^2}{2!} \lambda e^{-\lambda t}$$

Its generalized equation is

$$f_{Pas}(x, y, p) \rightarrow \lambda \frac{(\lambda t)^{x-1}}{(x-1)!} e^{-\lambda t} \equiv f\Gamma(t, x, \lambda) \tag{IX-57}$$

The function $f\Gamma(t, x, \lambda)$ derived by equation IX-57 from $fPas(x, y, p)$ is known as the Gamma probability function. By calculating the normalized constant of $\int_0^\infty dt$ for equation IX-57, we obtain the generalized expression of the Gamma distribution.

$$f\,\Gamma(t,\ \alpha,\ \beta) = \frac{\alpha}{\Gamma(\beta)}(\alpha t)^{\beta-1} e^{-\alpha t} \qquad \text{(IX-58)}$$

In equation IX-58 expressing the Gamma distribution, β is the shape parameter and α, the scale parameter. Figure B.13 shows graphs of equation IX-57 where $\lambda = 1$.

$$f\,\Gamma(t,\ x,\ 1) = \frac{1}{(x-1)!} t^{x-1} e^{-1} \qquad \text{(IX-59)}$$

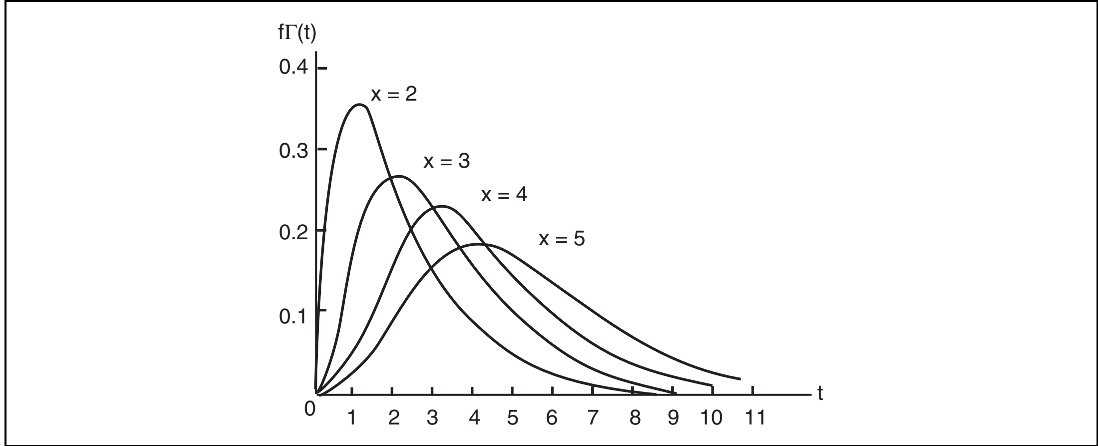


Figure B.13 Gamma Probability Density Functions $f\Gamma(t, x, 1)$

As can be seen from the derivation of the Gamma distribution given by equations. IX-55 through IX-57, the Pascal and Gamma distributions are the discrete and continuous probability distributions for the same probability model.
In particular, for the case of $x = 1$, the Gamma distribution (IX-57) reduces to the exponential distribution (IX-46). The Pascal distribution, if $x = 1$, becomes the geometric distribution (IX-51). This is consistent with the fact that the geometric and exponential distributions are discrete and continuous distributions, respectively (IX-49). The Gamma distribution is a failure probability density function if failure occurrence is considered to follow the Poisson process. We deal with this issue in B.4.9, Poisson Distribution.

B.4.9 Poisson Distribution: fPois(x)

Cosmic rays collide with semiconductor devices used in an artificial satellite completely at random. We cannot expect that there will be no collision for some time since one has just occurred. Similarly, we cannot say that a cosmic ray will soon collide with a semiconductor device because there have been no collisions for a moment.

This is an example of cases in which we can consider that a rare phenomenon will occur with some expectation if the period of observation is sufficiently long or the population to be observed is sufficiently large. Here we assume that the phenomenon does not occur twice or more at the same instant, and further that the probability of the phenomenon occurring is constant. In other words, the MTTF of the phenomenon = θ (or the instantaneous failure rate = λ) is constant. Such a probability process is known as the Poisson process.

If a phenomenon occurs in accordance with the Poisson process with the expectation x, the probability of the phenomenon occurring n times within the time interval $0 < T \leq t1$ is described by the Poisson distribution. Detailed discussions of the Poisson distribution are given below.

Let us determine the probability that the phenomenon occurs in a short moment dt in the time $0 < T \leq t1$. Using reliability functions applicable to times $0 < T \leq t1$ and $0 < T \leq t1 - t$ before and after dt, we obtain

$$R(t) \cdot \frac{dt}{\theta} \cdot R(t_1 - t) \tag{IX-60}$$

Hence the probability $P_1\left(\frac{t1}{\theta}\right)$ of the phenomenon occurring once in the time $0 < T \leq t1$ is

$$P_1\left(\frac{t1}{\theta}\right) = \int_0^{t1} R(t)\,\frac{dt}{\theta}\,(t_1 - t) = \int_0^{t_1} e^{-\frac{t}{\theta}} \cdot \frac{dt}{\theta} \cdot e^{-\frac{t_1 - t}{\theta}} = \frac{1}{\theta} e^{-\frac{t_1}{\theta}} \cdot t_1 \tag{IX-61}$$

The probability $P_n\left(\frac{t_1}{\theta}\right)$ that the phenomenon occurs n times within $0 < T \leq t1$ is obtained through repeated calculations of equation

$$P_n\left(\frac{t_1}{\theta}\right) = \int_0^{t_1} R(t)\,\frac{dt}{\theta} P_{n-1}\left(\frac{t_1}{\theta}\right) = \frac{1}{n!}\left(\frac{t_1}{\theta}\right)^n e^{-\frac{t_1}{\theta}} \tag{IX-62}$$

Eventually, when the expectation $x = \frac{t_1}{\theta}$, the Poisson probability density function fPois(x) is

$$\left.\begin{aligned} f_{Pois}(x) &= \frac{1}{n!} x^n e^{-x} \\ \mu = x, &\quad \sigma^2 = x^2 \end{aligned}\right\} \qquad \text{(IX-63)}$$

A three-dimensional representation of equation IX-64 is shown in figure B.14 within the range of $1 \le n \le 6$ and $0 \le x \le 6$. The values of f(x) for representative values in the range of

$0 \le n \le 39$, and $0.1 \le x \le 20$

are shown in the attached table.

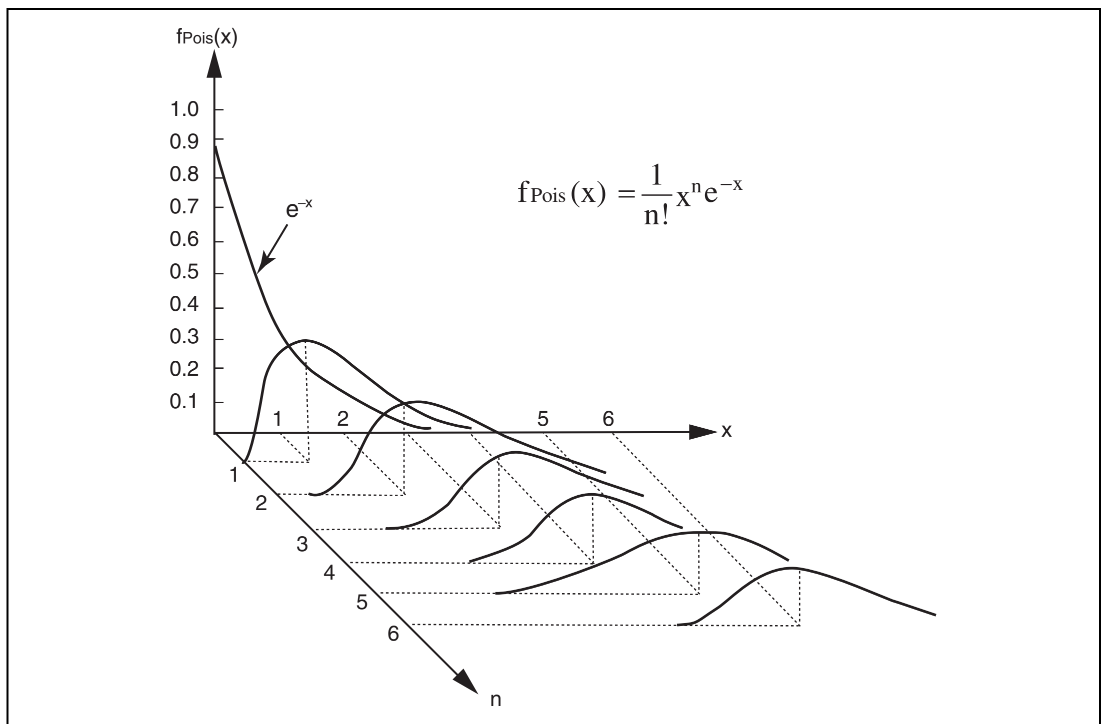


Figure B.14 Three-Dimensional Representation of Poisson Distributions

Let us determine the probability F(t1, k) that failures occur at least k times or more within the time $0 < T \leq t1$ in a Poisson process. This probability is expressed as follows using equation IX-62 for the Poisson distribution.

$$F(t1, k) = 1 - \sum_{n=0}^{k-1} P_n\left(\frac{t1}{\theta}\right) = 1 - \sum_{n=0}^{k-1} \frac{1}{n!}\left(\frac{t1}{\theta}\right)^n e^{-\frac{t1}{\theta}} \tag{IX-64}$$

In B.2.3, the stand-by redundancy system in figure B.8 will not fail unless the n switches all fail. Therefore, based on equation IX-64, the reliability function R(t) of this stand-by redundancy system is

$$R(t)=1 - F(t, k)$$

This equation leads to equation IX-21.

If damage causing failure occurs randomly in accordance with the Poisson process, the failure distribution function of the device is equation IX-64 assuming that the device breaks from k times or more of damage in the operating time $0 < T \leq t1$. In this case, the failure probability density function becomes equation IX-57 for the Gamma distribution. This is explained as follows.

Using a fixed value, in equation IX-64, for the number of damages k received before failure, consider the failure distribution function F(t1, k) as a function of time t1. Based on equation IX-3, the failure probability density function f(t1) is

$$f(t1) = \frac{\alpha}{\alpha t1} F(t1, k) = \frac{1}{(k-1)!}\left(\frac{t1}{\theta}\right)^{k-1} e^{-\frac{t1}{\theta}} = f\Gamma\left(t1, x, \frac{1}{\theta}\right) \tag{IX-65}$$

If, on the other hand, only a single damage (n = 1) is fatal to the device, the failure probability density function becomes equation IX-46 of the exponential distribution.

The Poisson distribution approximates the binomial probability distribution if the population is large and the phenomenon occurs with a low probability.

The binomial probability distribution should deal with Bernoulli samples, for which the probability p = constant is a premise. In contrast, the Poisson distribution handles phenomenons that the expectation x = Np = constant. It is important to note that N no longer denotes the number of tests of Bernoulli trial due to the approximation of the binomial probability distribution to the Poisson distribution. This process is explained in detail as follows.

$$f_{Bin}(n, N, P) = \frac{N!}{n!(N-n)!} p^n q^{N-n} = \frac{\left(1-\frac{1}{N}\right)\left(1-\frac{2}{N}\right)\cdots\left(1-\frac{n-1}{N}\right)}{n!} (Np)^n q^{N-n} \quad \text{(IX-66)}$$

and,

$$\log q^{N-n} = (N-n)\log(1-p) = -(N-n)\sum_{k=1}^{\infty}\frac{p^k}{k} = -\left(1-\frac{n}{N}\right)\left(x + \frac{1}{2}\frac{x^2}{N} + \frac{1}{3}\frac{x^3}{N^2} + \cdots\right) \quad \text{(IX-67)}$$

$$\therefore \lim_{N\to\infty} \log q^{N-n} = -x, \lim_{N\to\infty} q^{N-n} = e^{-x} \quad \text{(IX-68)}$$

N in these equations is not the number of tests of Bernoulli trial, but serves to indicate that the population size is expanded. Through these steps we obtain

$$\lim_{N\to\infty} f_{Bin}(n, N, P) = \frac{1}{n!} x^n e^{-x} \quad \text{(IX-69)}$$

Thus understanding the Poisson distribution in different ways we can clarify its relations with other probability distributions. This will be illustrated later in section C, "Relations of Probability Distributions."

B.4.10 Normal Distribution: fNorm(x)

The general character of a population comprising numerous, uniform, and random independent phenomena is expressed by the normal distribution fNorm (x). A typical example of this is the movement of molecules of a classical, ideal gas. (We will not discuss the correctness of this in a strict mathematical sense.)

Expected characteristics of the function fNorm (x) are these: the mean value μ is also the maximum value; the value smoothly decreases from the maximum value in a symmetrical manner; the broadening of the curve about the peak is proportional to the standard deviation σ. Wear-out-failures which almost suddenly outbreak after a certain period approximate the normal distribution.

Let us first examine a simple binomial distribution model to know concretely what the normal distribution expresses.

In the Bernoulli trial, the result of observation is either (1) $+\sigma/\sqrt{N}$ or (2) $-\sigma/\sqrt{N}$. The probability of (1) or (2) occurring is equally 1/2. The initial value for starting the trial is 0 and we perform N tests. We obtain n times of 1 and N - n times of (2), then the value x after N tests is

$$x = \frac{\sigma(2n - N)}{\sqrt{N}} \qquad \text{(IX-70)}$$

This type of binomial distribution model approaches the normal distribution as we make the number of tests N sufficiently large.

$$f_{Bin}(n) = \frac{N!\left(\frac{1}{2}\right)^N}{n!(N-n)!} = \frac{N!\left(\frac{1}{2}\right)^N}{\left(\frac{1}{2}N + \frac{x}{2\sigma}\sqrt{N}\right)! \times \left(\frac{1}{2}N - \frac{x}{2\sigma}\sqrt{N}\right)!} \qquad \text{(IX-71)}$$

If N is sufficiently large we can consider that x is a continuous variable. Hence

$$f_{Bin}(n)\,dn \to \phi(x)dx,\ dn \to \frac{\sqrt{N}}{2\sigma}dx \quad (N \to \infty) \qquad \text{(IX-72)}$$

Here, ϕ (x) is given by

$$\phi(x) = \lim_{N\to\infty} \frac{\sqrt{N}}{2\sigma} f_{Bin}(n) = \lim_{N\to\infty} \left\{ \frac{\frac{\sqrt{N}}{2\sigma} \cdot ! \cdot \left(\frac{1}{2}\right)^N}{\left(\frac{1}{2}N + \frac{x}{2\sigma}\sqrt{N}\right)! \times \left(\frac{1}{2}N - \frac{x}{2\sigma}\sqrt{N}\right)!} \right\} \quad \text{(IX-73)}$$

Using Sterling's formula we can write

$$N! \approx \sqrt{2\pi N}\, N^N e^{-N} \qquad N > 10$$

$$\therefore \quad \phi(x) = \lim_{N\to\infty} \left\{ \frac{1}{\sigma\sqrt{2\pi}} \frac{1}{\sqrt{1 - \frac{x^2}{\sigma^2 N}}} \left(1 + \frac{x}{\sigma\sqrt{N}}\right)^{-\frac{N}{2} - \frac{x}{2\sigma}\sqrt{N}} \cdot \left(1 - \frac{x}{\sigma\sqrt{N}}\right)^{-\frac{N}{2} + \frac{x}{2\sigma}\sqrt{N}} \right\}$$

$$= \lim_{N\to\infty} \left\{ \frac{1}{\sigma\sqrt{2\pi}} \left(1 - \frac{x^2}{\sigma^2 N}\right)^{-\frac{N}{2} - \frac{1}{2}} \cdot \left(1 + \frac{x}{\sigma\sqrt{N}}\right)^{\frac{x}{2\sigma}\sqrt{N}} \cdot \left(1 - \frac{x}{\sigma\sqrt{N}}\right)^{-\frac{x}{2\sigma}\sqrt{N}} \right\} \quad \text{(IX-74)}$$

Here, using the exponential function

$$e^Z = \lim_{n\to\infty} \left(1 + \frac{Z}{n}\right)^n$$

We obtain

$$\phi(x) = \frac{1}{\sqrt{2\pi}} \exp\left(-\frac{x^2}{2}\right) \quad \text{(IX-75)}$$

ϕ (x) is known as the standard normal distribution. The general form of the normal probability density function is

$$f_{Norm}(x) = \frac{1}{\sigma\sqrt{2\pi}} \exp\left(-\frac{(x-\mu)^2}{2\sigma^2}\right) \quad \text{(IX-76)}$$

By applying Equation IX-76 to Equation IX-8, we can calculate the mean value and the variance, which, we can confirm, will be μ and σ^2. The variable y used to convert fNorm (x) to Equation IX-76 is

$$y = \frac{x - \mu}{\sigma} \qquad \text{(IX-77)}$$

This is known as the standard normal variable. Figure B.15 shows the typical characteristics of fNorm(x) and ϕ (y). In Figure B.15, the following calculations can be made.

$$\int_{\mu-\sigma}^{\mu+\sigma} f_{Norm}(x)\,dx \cong 0.6826 \,, \int_{\mu-2\sigma}^{\mu+2\sigma} f_{Norm}(x)\,dx \cong 0.9545 \,, \int_{\mu-3\sigma}^{\mu+3\sigma} f_{Norm}(x)\,dx \cong 0.9973$$

When the value InX rather than X behaves according to the normal distribution, we have a logarithmic normal distribution. To serve as an example, consider the life L in equation IX-33. Let us assume that a given lot of semiconductor devices are storage tested at temperature T. As long as there is no great variation in the quality of this lot, the distribution of the life L as caused by the stress placed on the devices by the temperature T is expressed as a logarithmic normal distribution and should be analyzed as such. Moreover, the logarithmic normal distribution is also used for the analysis of oxide film life by TDDB

$$f_{log-Norm}(x) = \frac{1}{\sigma x\sqrt{2\pi}} \exp\left(-\frac{(InX - InX0)^2}{2\sigma^2}\right) \qquad X > 0 \qquad \text{(IX-78)}$$

$$\text{Mean value} = e^{InX_0 + \frac{\sigma^2}{2}}, \quad \text{Variance} = e^{2InX_0 + \sigma^2} \times (e^{\sigma^2} - 1)$$

where X0 is the median value of the probability distribution: $\int_0^{X0} f_{log-Norm}(X)dX = \int_{X0}^{\infty} f_{log-Norm}(X)dX$

σ^2 is the variance of the normal distribution.

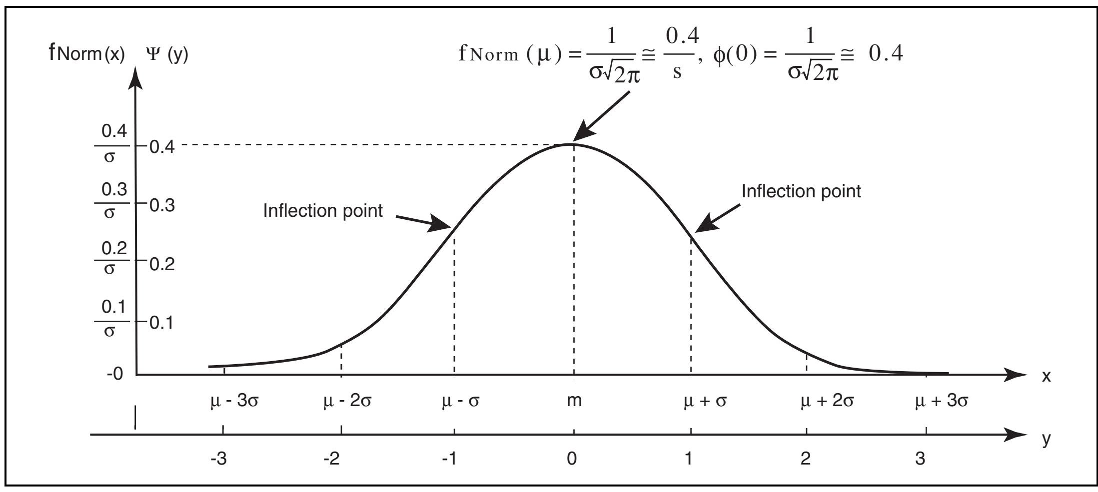


Figure B.15 Probability Density Function of Normal Distribution

B.4.11 Weibull Distribution: fWbl(t)

A set of n semiconductor devices is subjected to operation life test all together. As time t passes, the failure rate of these semiconductor devices changes. For studying the change, in this model, probabilities of individual devices failing by the time t are uniformly p(t), and the probability that at least one of the n devices will fail is F(t). Reversely the probability that none of the n devices will fail by the time t is R(t), which is, from equation IX-4

$$R(t) = 1 - F(t) = \{1 - p(t)\}^{n} \qquad \text{(IX-79)}$$

The Weibull distribution characteristically assumes that the n devices are as a lot expressed by the following reliability function.

$$R(t) = \{1 - p(t)\}^{n} = e^{-\phi(t)} \qquad \text{(IX-80)}$$

Let us make arrangements to express properly the failure distribution trends that we know through experience in the function form of equation IX-80.

We know through experience that no failures occur before a given test time γ and after γ the total number of failed devices increases with time t (or more correctly, maintains a non-decreasing trend). To express this empirically observed fact, ϕ (t) should have the characteristics below.

$$\phi(t) = 0 \quad (0 < t \leq \gamma)$$

$$\phi(t) \geq 0, \ \frac{d}{dt}\phi(t) \geq 0 \ (\gamma < t)$$

Hence we choose the following form of function.

$$\left.\begin{aligned} \phi(t) &= 0 \ (0 < t \le \gamma) \\ \phi(t) &= \frac{(t-\gamma)^m}{t0} \ (\gamma < t) \end{aligned}\right\} \qquad \text{(IX-81)}$$

Therefore,

$$F_{Wb1}(t) = 1 - \{1 - p(t)\}^n = 1 - e^{-\phi(t)} = 1 - \exp\left\{-\frac{(t-\gamma)^m}{t\,0}\right\} \qquad \text{(IX-82)}$$

Equation IX-82 is referred to as the Weibull failure distribution function.

Equation IX-83 of the Weibull distribution has three parameters, m, γ, and t0, which are the shape parameter, position parameter, and scale parameter, respectively. The position parameter $\gamma = 0$ if we assume that the probability of failure is already above 0 immediately before testing. From equation IX-82 and according to equations. IX-3 and IX-8

$$\left.\begin{aligned} F_{Wb1}(t) &= \frac{m(t-\gamma)^{m-1}}{t0} \exp\left\{-\frac{(t-\gamma)^m}{t0}\right\} \\ \mu &= t0^{\frac{1}{m}}\,\Gamma\left(1+\frac{1}{m}\right), \quad \sigma^2 = t0^{\frac{2}{m}}\left\{\Gamma\left(1+\frac{2}{m}\right) - \Gamma^2\left(1+\frac{1}{m}\right)\right\} \\ \lambda_{Wb1}(t) &= \frac{m}{t0}(t-\gamma)^{m-1} \end{aligned}\right\} \qquad \text{(IX-83)}$$

If m = 1, Wbl = 1/ t0 = constant, so the distribution is exponential.

If m > 1, Wbl (t) monotonically increases, representing a wear-out failure mode.

If m < 1, Wbl (t) monotonically decreases, representing an initial failure mode.

The function form of the Weibull distribution is capable of representing different failure modes depending on the value of the parameter m. Figure B.16 shows how the form of $f_{Wb1}(t)$ changes with various values of m under conditions of $\gamma = 0$ and $t_0 = 1$.

When the position parameter $\gamma = 0$, equation IX-79 of the Weibull reliability function becomes

$$R_{Wb1}(t) = \int_t^\infty f_{Wb1}(t)\,dt = \int_t^\infty \frac{m}{t_0} t^{m-1} e - \frac{tm}{t_0} dt = e - \frac{t^m}{t_0} \qquad \text{(IX-84)}$$

If we take the natural logarithm of equation IX-84 twice we obtain

$$1n\ 1n \frac{1}{R_{Wb1}(t)} = 1n\ 1n \frac{1}{1 - F_{Wb1}(t)} = m\,1n\ t - 1n\ t_0 \qquad \text{(IX-85)}$$

Here we rewrite as

$$1n\ 1n \frac{1}{1 - F_{Wb1}(t)} = Y,\ 1n\,t = X,\ 1n\,t_0 = h$$

Then equation IX-85 becomes

$$Y = mX - h \qquad \text{(IX-86)}$$

The Weibull chart is a chart in which the value of $F_{Wbl}(t)$ being converted into the length $1n\ 1n \frac{1}{1 - F_{Wb1}(t)}$ is plotted on the vertical axis and time t is plotted on the horizontal axis on a logarithmic scale. The cumulative failure rate $F_{Wbl}(t)$ determined from observed data is described by the Weibull distribution. It is represented by a straight line according to the relation expressed by equation IX-86. The Weibull chart is useful for analysis of failure mode since observed data are graphed on the Weibull chart in the shape of an linear expression.

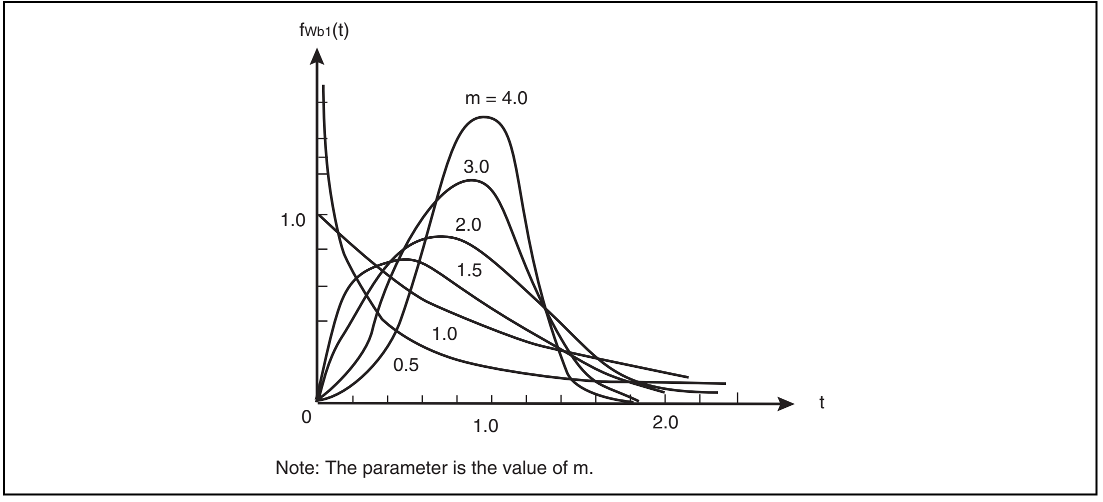


Figure B.16 Weibull Distribution

B.4.12 Double Exponential Distribution: fd-exp(x)

If $\gamma = 0$ in equation IX-84 of the Weibull distribution

$$f_{Wb1}(t) = \frac{m}{t_0} t^{m-1} e^{-\frac{t^m}{t_0}} \qquad \text{(IX-87)}$$

in which, if we perform logarithmic transformation of t so that x = ln t and $t = e^x$, we have

$$f_{Wb1}(t)\,dt = \frac{m}{t_0} e^{mx} \cdot e - \frac{e^{mx}}{t_0} dx = me^{mx - \ln t_0} \cdot \exp(-e^{(mx - \ln t_0)})\,dx \qquad \text{(IX-88)}$$

This is the logarithmic transformation of the original distribution. Here we restate

$m = \lambda$, $\ln t_0 = \alpha$

$$f_d - \exp(x) = \lambda e^{\lambda x - \alpha} \bullet e^{-e\lambda x - \alpha} \qquad \text{(IX-89)}$$

Equation IX-89 is known as the double exponential (or extreme value) distribution. Here λ and α are the scale and position parameters, respectively.

$$\mu = \frac{\alpha - \gamma}{\lambda}, \quad \sigma^2 = \frac{\varepsilon^2}{\lambda^2}$$

where γ = Euler's constant = 0.577 ⋯ $\quad \varepsilon = \frac{\pi}{\sqrt{6}} = 1.283 \cdots$

When performing reliability tests on devices and subjecting them to stress, the damage incurred by all parts of the device is not necessarily equal. The part of the device which is most susceptible to the applied stress will be the most damaged and will eventually fail. It becomes the determining factor in the life of the device. This occurs in the case of a surge pulse withstand or mechanical impact test. In such a case, stress is applied locally to the device and the life or the withstanding limit of the device depends on its weak point. The double exponential distribution is suitable for analysis of such kinds of phenomena. To simplify equation IX-89 we use

$$-y = \lambda x - \alpha \qquad \text{(IX-90)}$$

to yield

$$f_{d-\exp}(y) = \lambda e^{-y} e^{-e-y} \qquad \text{(IX-91)}$$

$$F_{d-\exp}(y) = e^{-e-y} \qquad \text{(IX-92)}$$

If we take the natural logarithm of this twice, we have

$$1n \ 1n \frac{1}{F_{d-\exp}(y)} = y = \lambda x - \alpha \qquad \text{(IX-93)}$$

As seen by equation equation IX-87 related to the Weibull chart, the observed data can be plotted on extremal probability paper in the shape of a linear expression derived from equation IX-93. Thus it is possible to determine the scale parameter λ and position parameter α.

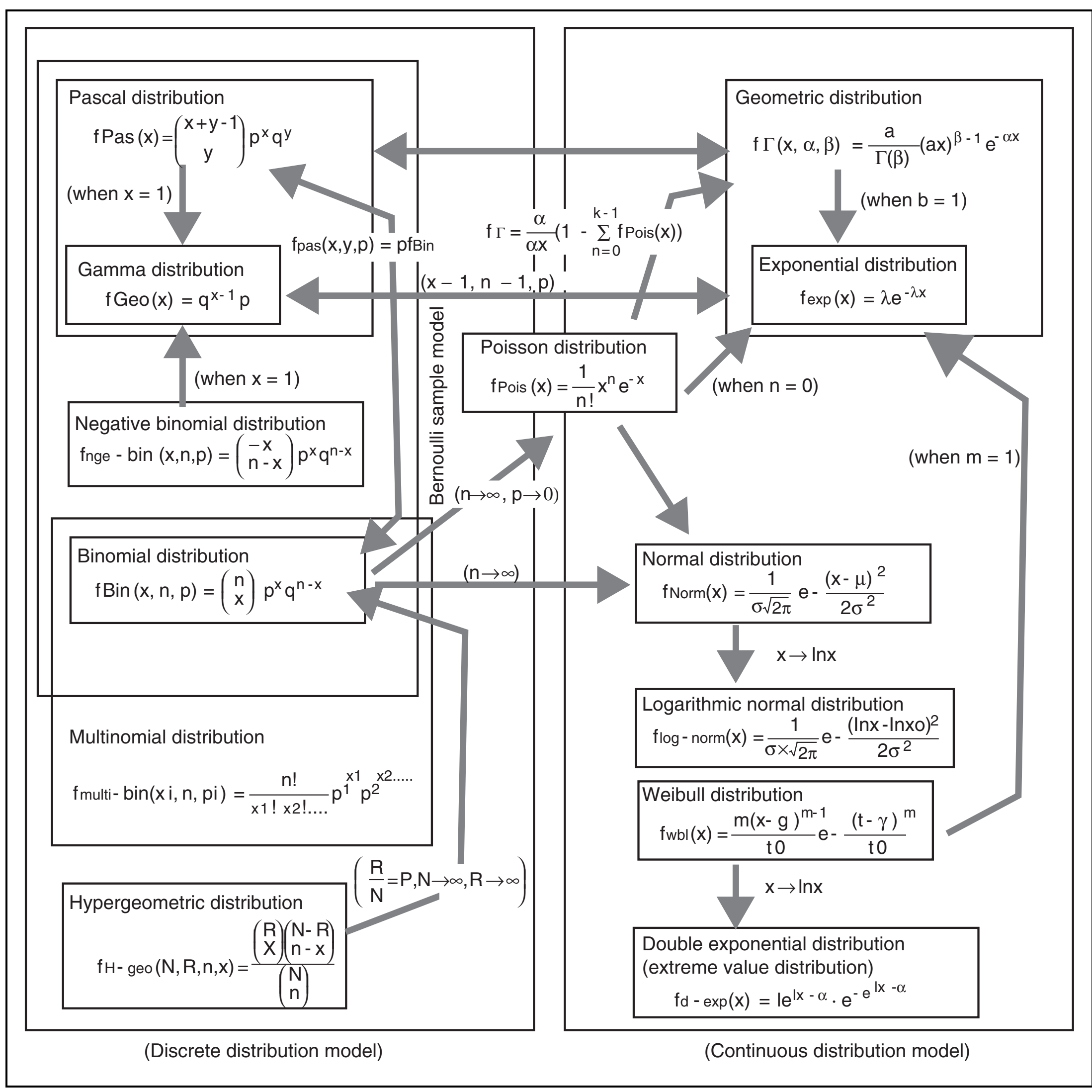
REFERENCES:

[1] Misao Mikami: Statistical Predictions (Mathematic Lecture 6), Chikuma Shobo, 1969 (In Japanese)

[2] Hiroshi Shiomi: 3rd edition of Introduction to Reliability Engineering. Maruzen. 1995 (In Japanese)

[3] Quality Control, New Edition, Japan Industrial Standards: 1977 (In Japanese)

C. Relations of Probability Distributions



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D. Probability Functions

Probability Distribution	Probability density function f(x)	Reliability function R(x)	Failure Rate $\lambda(x)$	Mean Value μ	Variance σ^2	Remark
Binomial distribution	$f_{Bin}(x,n,p)=\binom{n}{x}p^x q^{n-x}$	$R_{Bin}(x)=\sum_{i=x+1}^{n}\binom{n}{1}p^i q^{n-i}$		np	npn	
Geometric distribution	$f_{Geo}(x) = q^x p$	$R_{Geo}(x) = q^{x+1}$	$\lambda_{Geo} = \frac{p}{q} = const$	$\frac{q}{p}$	$\frac{q}{p^2}$	
Exponential distribution	$f_{exp}(x) = \lambda e^{-\lambda x}$	$R_{exp}(x) = e^{-\lambda x}$	$\lambda_{exp} = \lambda = const$	$\frac{1}{\lambda}$	$\frac{1}{\lambda^2}$	
Pascal distribution	$f_{Pas}(x)=\binom{x+y-1}{y}p^x q^y$	$R_{Pas}(x)=\sum_{i=x}^{n-1}\binom{n-1}{i}p^{n-i}q^i$	$\lambda_{Pas} = \frac{f_{Pas}}{R_{Pas}}$	$\frac{qy}{p}$	$\frac{qy}{p^2}$	
Gamma distribution	(x, α, β)	$R_{\Gamma}(x)= \frac{\alpha}{\Gamma(\beta)}\int_x^{\infty}(\alpha t)^{\beta-1}e^{-\alpha t}dt$	$\lambda_{\Gamma} = \frac{f_{\Gamma}}{R_{\Gamma}}$	$\frac{\beta}{\alpha}$	$\frac{\beta}{\alpha^2}$	α: Scale palameter β: Shape palameter Refer to Figure B.13

Probability Distribution	Probability density function f(x)	Reliability function R(x)	Failure Rate λ(x)	Mean Value μ	Variance σ^2	Remark
Poisson distribution	$f_{pois}(x) = \frac{1}{n!}x^n e^{-x}$	$R_{pois}(x) = \frac{1}{n!}\int_x^\infty t^n e^{-t}dt$	$\lambda_{Pois} = \frac{f_{Pois}}{R_{Pois}}$	x	x^2	Refer to Figure B.14
Weibull distribution	$f_{wbl}(x) = \frac{m(x-\gamma)^{m-1}}{t_0} \bullet e^{-\frac{(x-\gamma)^m}{t_0}}$	$R_{wbl}(x) = e^{-\frac{(x-\gamma)^m}{t_0}}$	$\lambda_{Wdl}(x) = \frac{m}{t_0}(x-\gamma)^{m-1}$	$t_0^{\frac{1}{m}}\Gamma(1+\frac{1}{m})$	$t_0^{\frac{2}{m}}\{\Gamma(1+\frac{2}{m}) - \Gamma^2(1+\frac{1}{m})\}$	m: Shape palameter γ: Position palameter t0: Scale palameter Refer to Figure B.16
Normal distribution	$f_{Norm}(x) = \frac{1}{\sigma\sqrt{2\pi}} e^{-\frac{(x-\mu)^2}{2\sigma^2}}$	$R_{Norm}(x) = \frac{1}{\sigma\sqrt{2\pi}}\int_x^\infty e^{-\frac{(t-\mu)^2}{2\sigma^2}}dt$	$\lambda_{Norm} = \frac{f_{Nom}}{R_{Norm}}$	μ	σ^2	Refer to Figure B.15
Logarithmic normal distribution	$f_{log-norm}(x) = \frac{1}{\sigma x\sqrt{2\pi}} e^{-\frac{(lix - ln xo)^2}{2\sigma^2}}$	$R_{log-norm}(x) = \int_x^\infty f_{log-norm}(t)dt$	$\lambda_{log-norm} = \frac{fl_{-norm}}{Rl_{-norm}}$	$e - (\ln x0 + \frac{\sigma^2}{2})$	$e^{2\ln x0+\sigma^2} \times (e^{\sigma^2} - 1)$	σ^2: Variance of normal distribution X0: median value of probability distribution

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Colophon 6.0

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