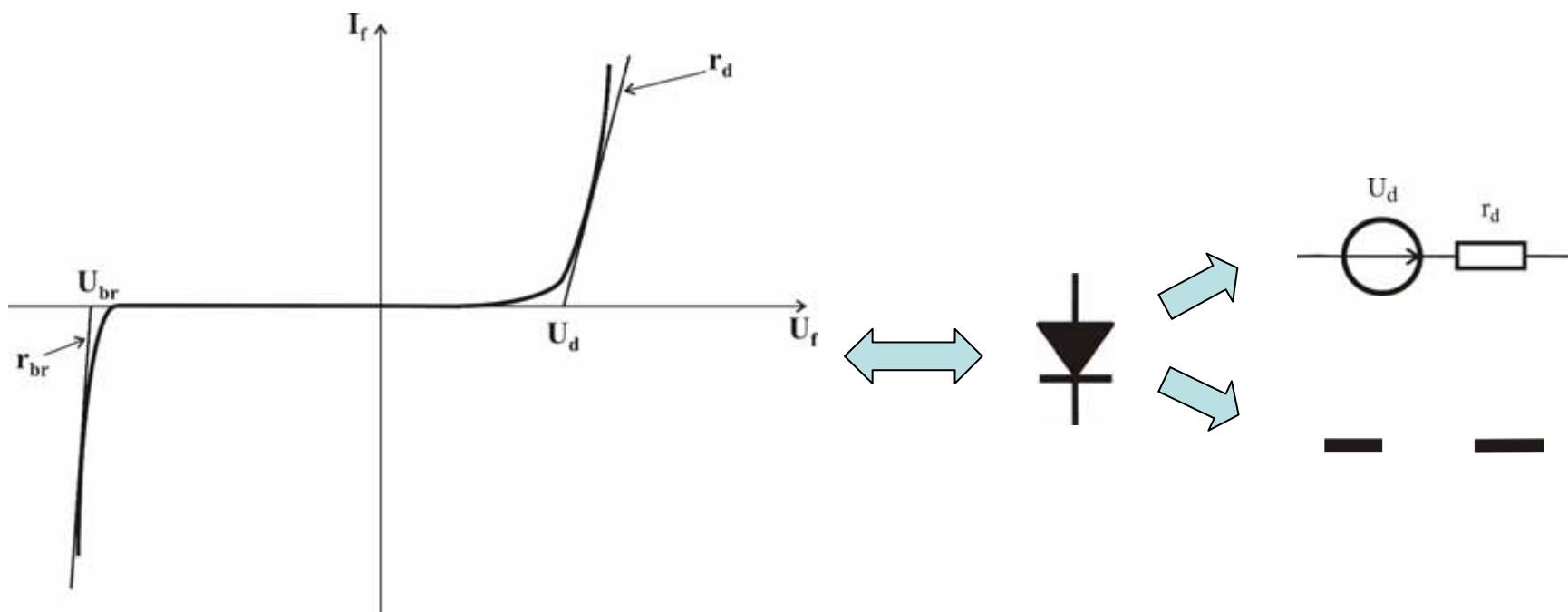


## **Семинарно занятие №: 3**

### **ПАСИВНИ ДИОДНИ ОГРАНИЧИТЕЛИ**

#### **Цел на занятието:**

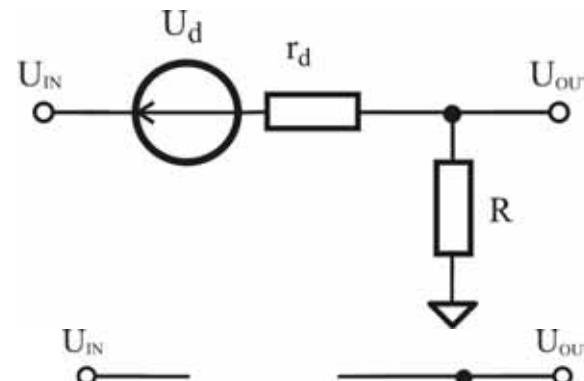
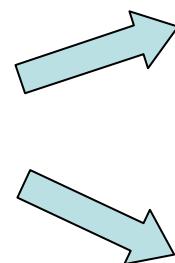
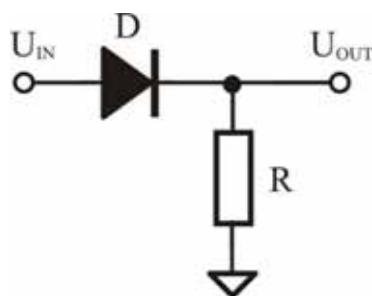
Дефиниране, определяне, математически и логически анализ на предавателните функции в нелинейните пасивни вериги, взаимната връзка в развитието на процесите между входа и изхода във времето, както и преходните процеси в тях .



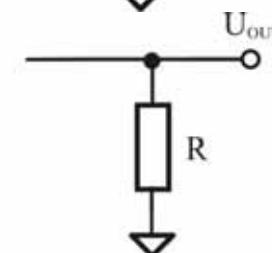
## ПОСЛЕДОВАТЕЛНИ ПАСИВНИ ДИОДНИ ОГРАНИЧИТЕЛИ

**!!! Във всички схеми на едностранините последователни пасивни диодни ограничители работят в режим на предаване, когато входният сигнал се предава на изхода през отпущен диод или са в режим на ограничение, когато диодът е запущен.**

## Еквивалентни схеми

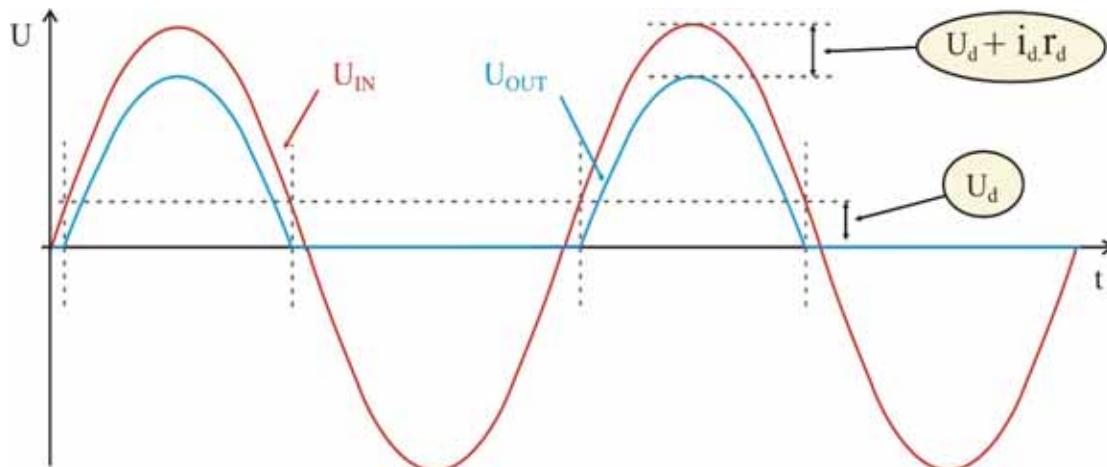
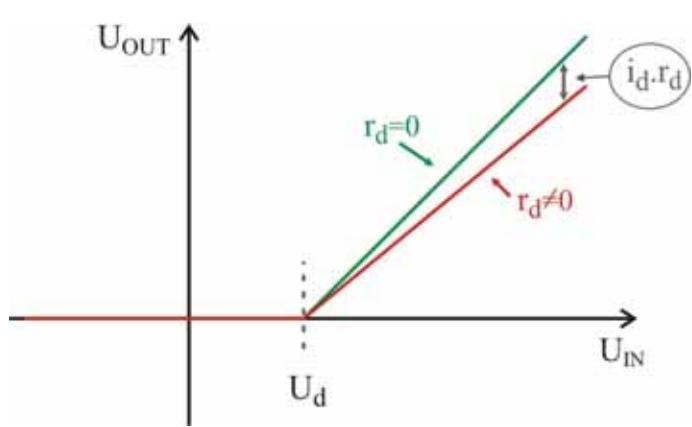


$$U_{IN} > U_d$$

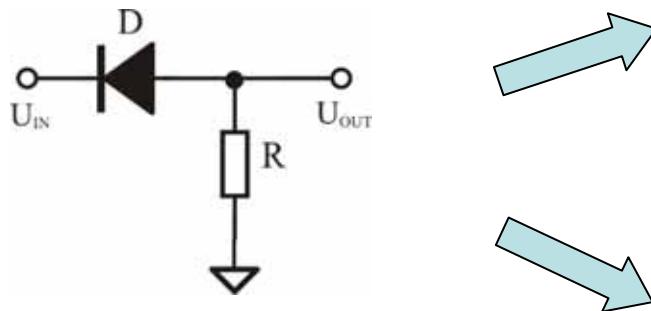


$$U_{IN} \leq U_d$$

$$U_{OUT} = \begin{cases} 0 & \text{за } U_{INP} < U_d \\ (U_{INP} - U_d) \cdot \frac{R}{R + r_d} & \text{за } U_{INP} \geq U_d \end{cases}$$



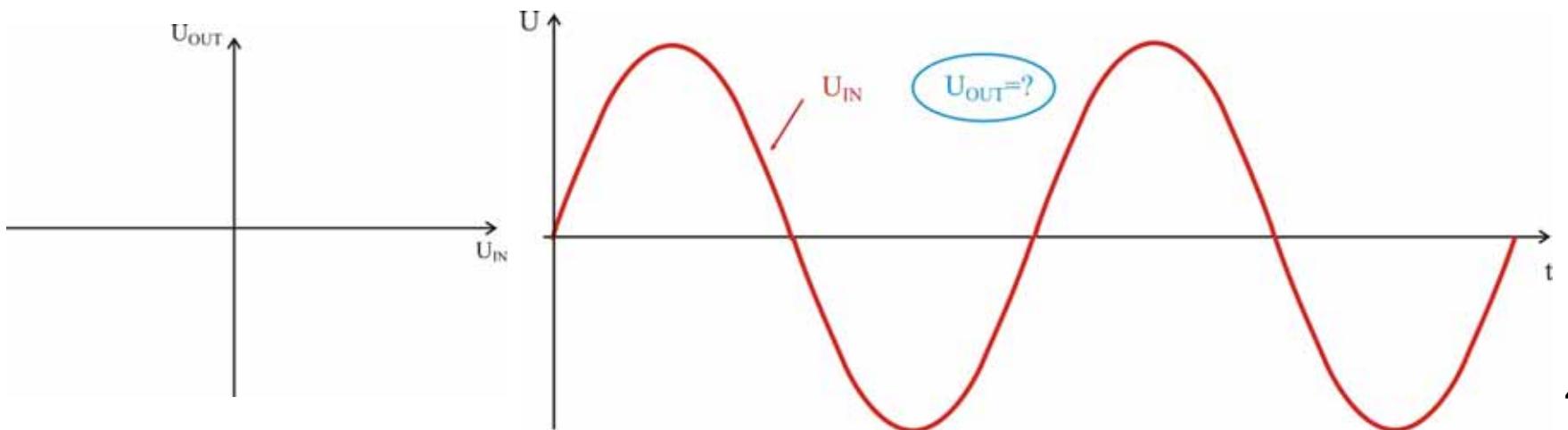
## Еквивалентни схеми



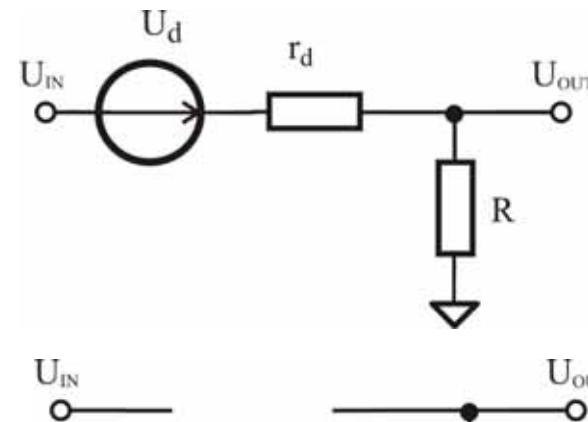
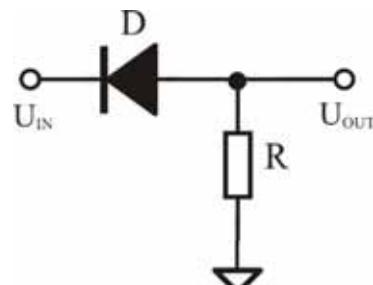
$U_{IN} \Leftrightarrow ?$

$U_{IN} \Leftrightarrow ?$

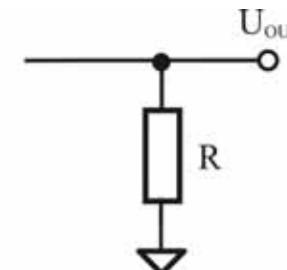
$$U_{out} = \begin{cases} ? & \text{за } ? \\ ? & \text{за } ? \end{cases}$$



## Еквивалентни схеми

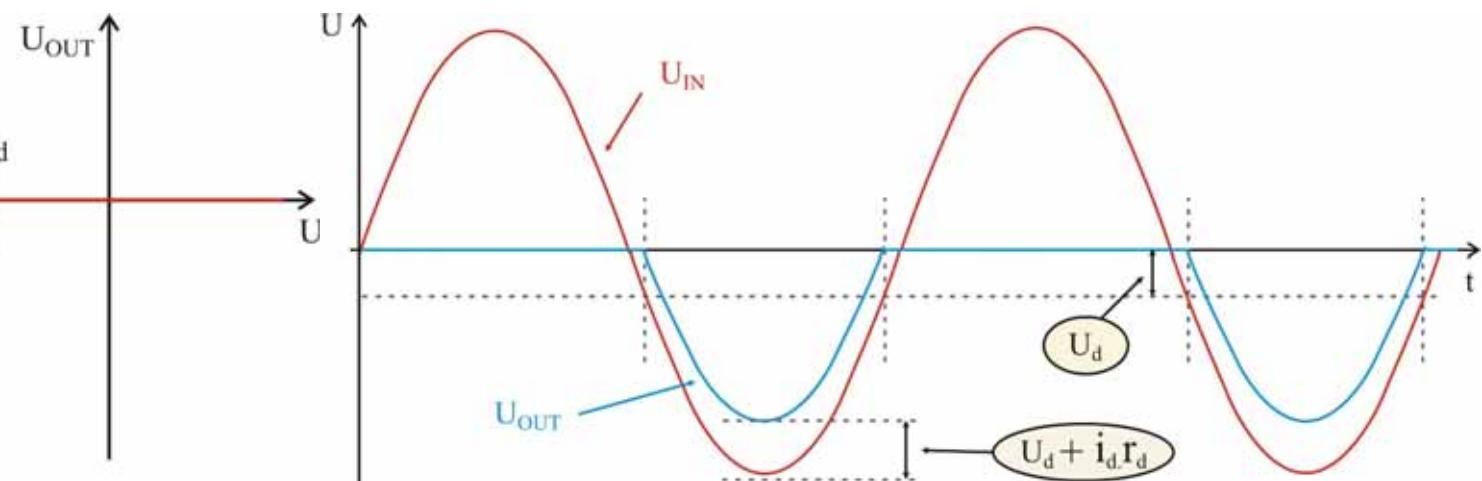
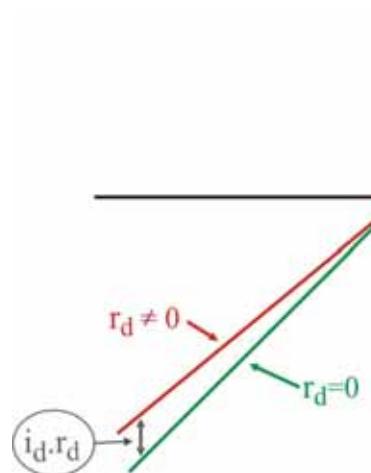


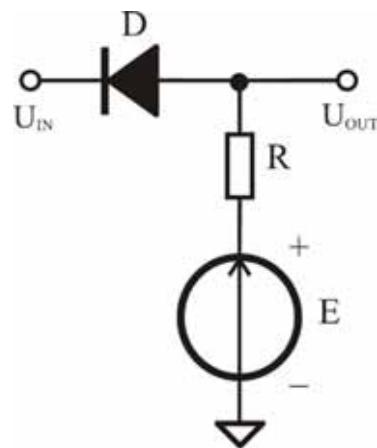
$$U_{IN} \leq -U_d$$



$$U_{IN} > -U_d$$

$$U_{OUT} = \begin{cases} 0 & \text{за } U_{INP} \geq -U_d \\ (U_{INP} - U_d) \frac{R_1}{R_1 + r_d} & \text{за } U_{INP} < -U_d \end{cases}$$



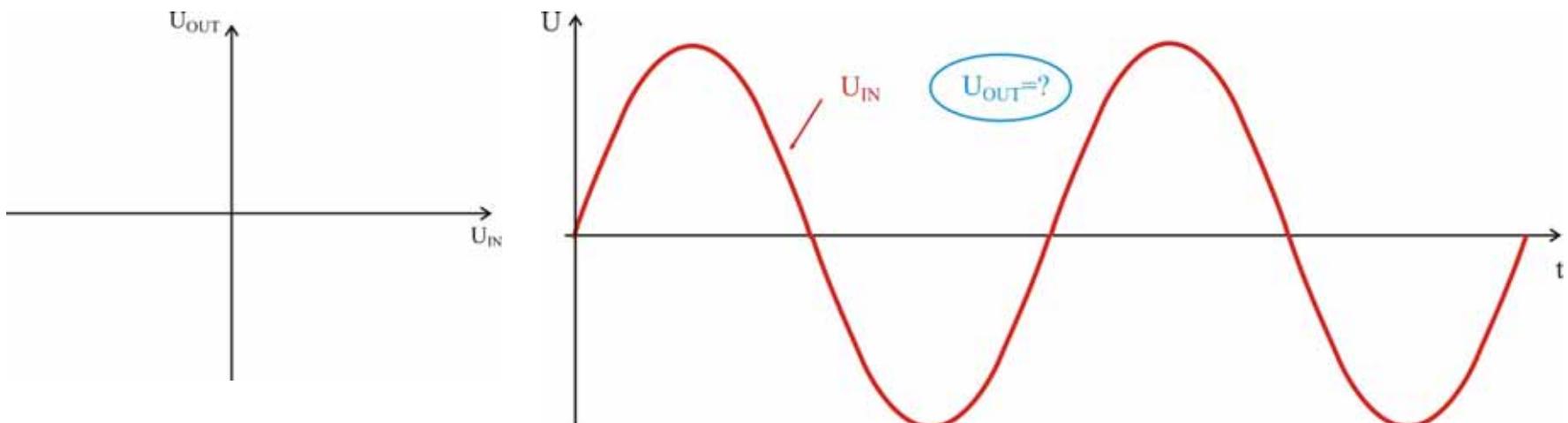


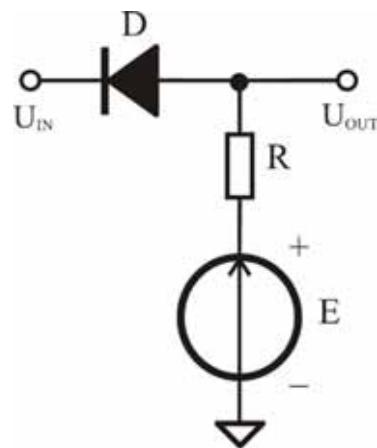
Еквивалентни схеми

$U_{IN} \Leftrightarrow ?$

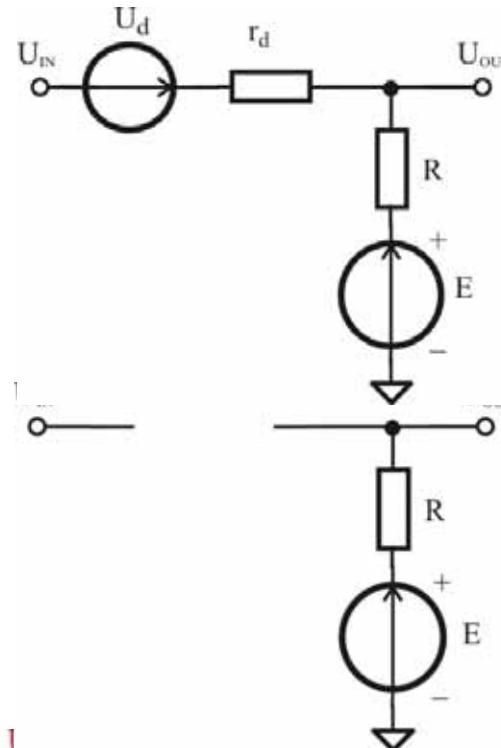
$U_{IN} \Leftrightarrow ?$

$$U_{out} = \begin{cases} ? & \text{за } ? \\ ? & \text{за } ? \end{cases}$$





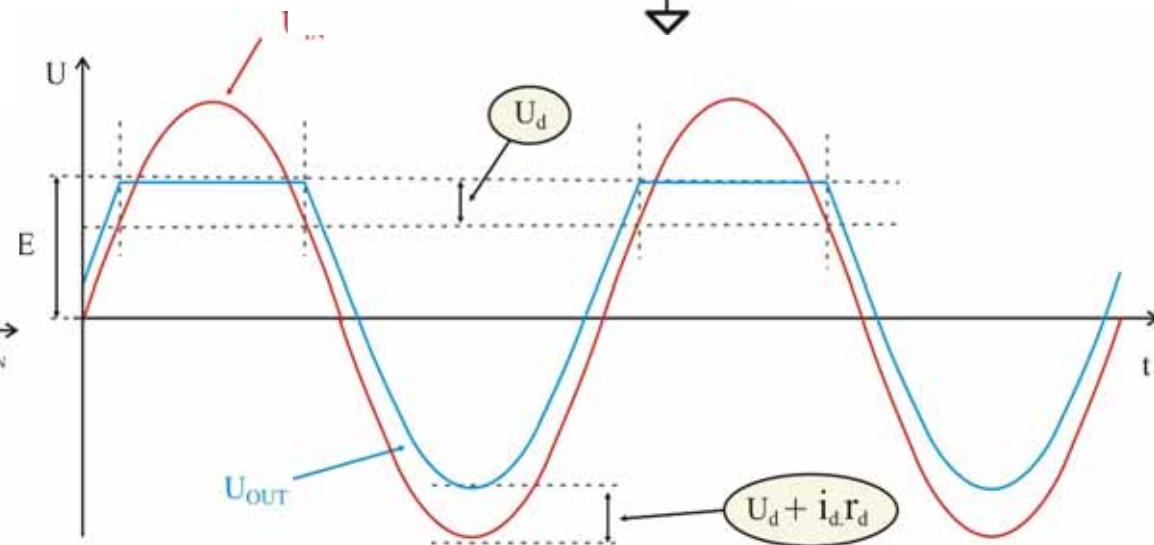
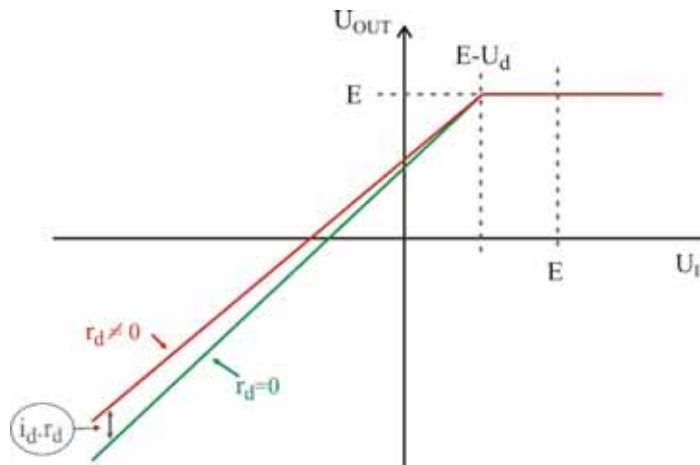
## Еквивалентни схеми



$$U_{IN} \leq E$$

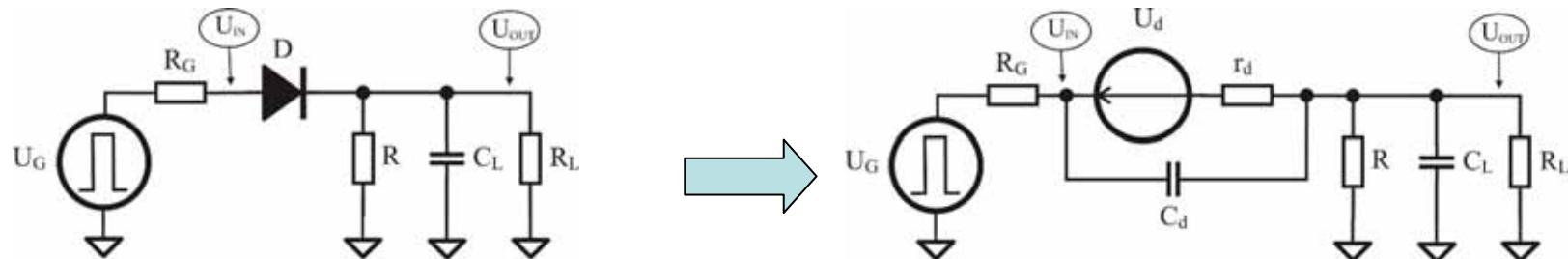
$$U_{IN} > E$$

$$U_{OUT} = \begin{cases} E & \text{за } U_{IN} \geq E \\ (U_{IN} + U_d + i_d \cdot r_d) & \text{за } U_{IN} < E \end{cases}$$

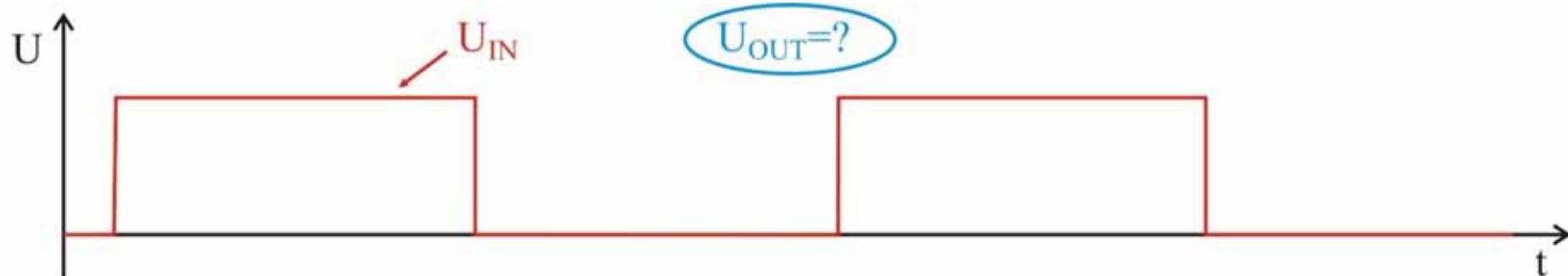


## Преходни процеси в еднострани последователни диодни ограничители

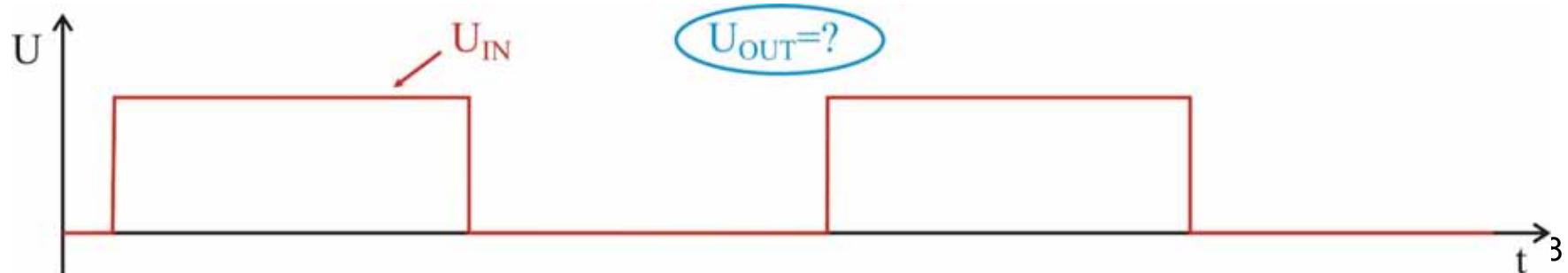
Еквивалентна схема



Влияние на  $C_L$   $C_L \gg C_d$

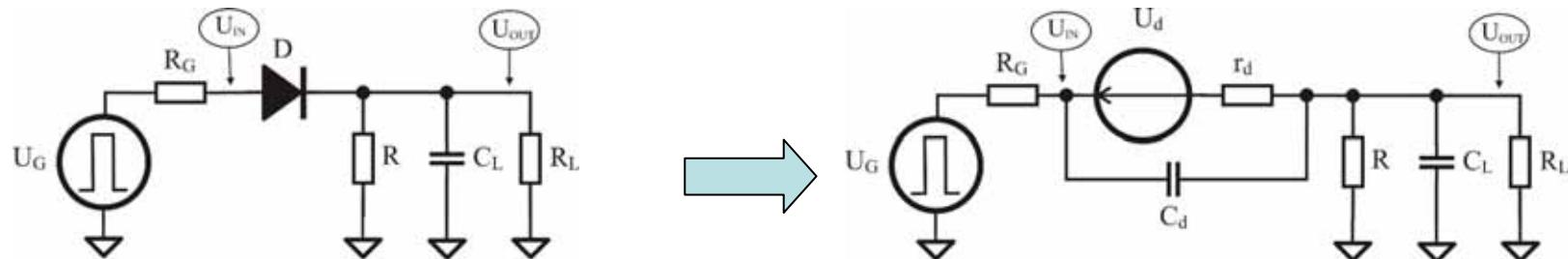


Влияние на  $C_d$   $C_d \gg C_L$

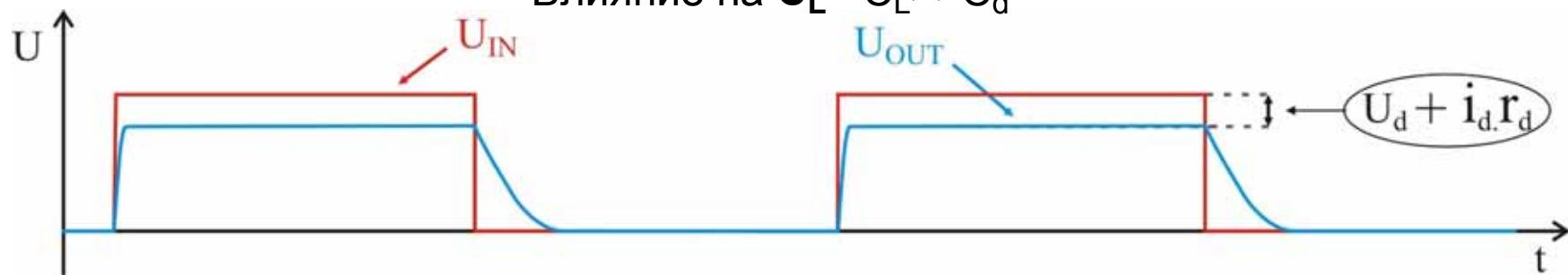


## Преходни процеси в еднострани последователни диодни ограничители

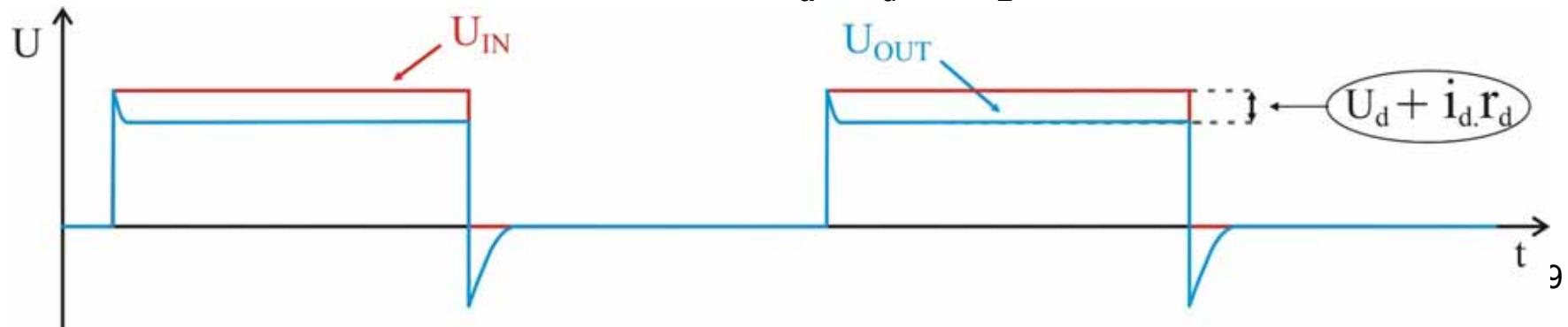
Еквивалентна схема



Влияние на  $C_L$   $C_L \gg C_d$

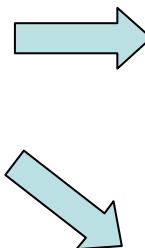
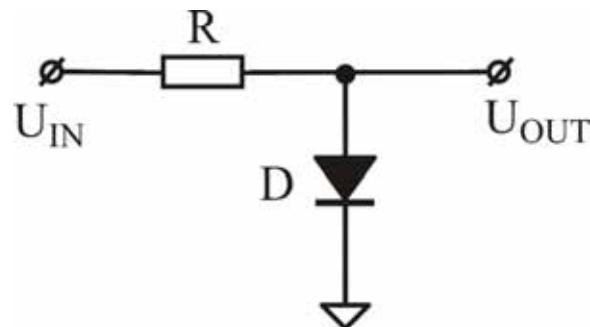


Влияние на  $C_d$   $C_d \gg C_L$



## ПАРАЛЕЛНИ ПАСИВНИ ДИОДНИ ОГРАНИЧИТЕЛИ

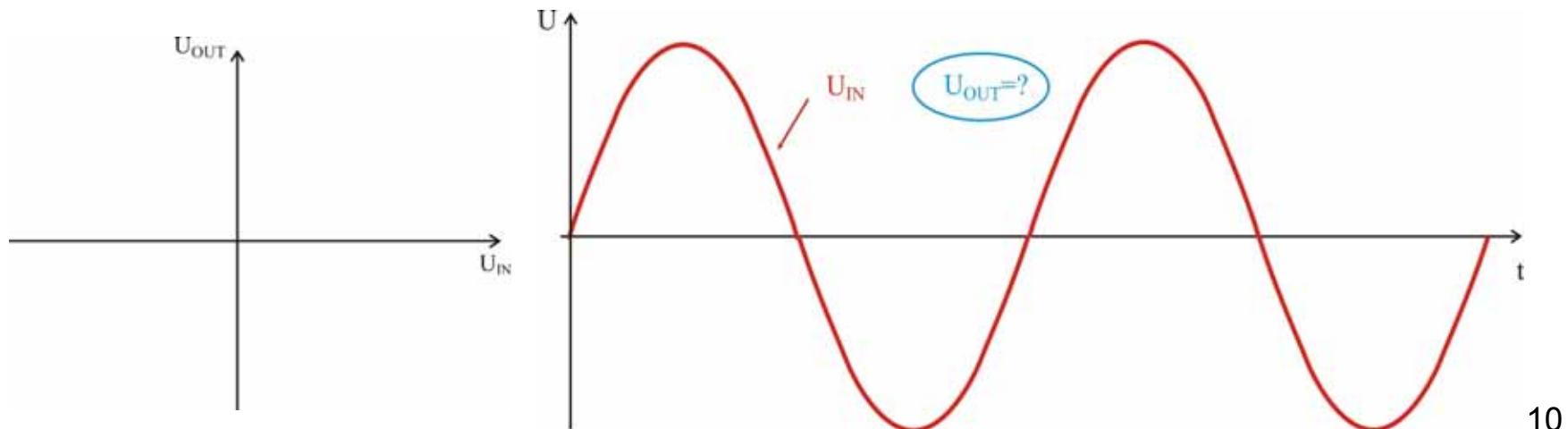
Еквивалентни схеми



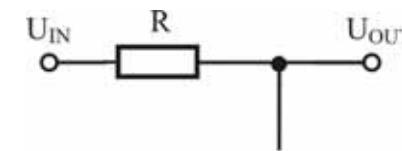
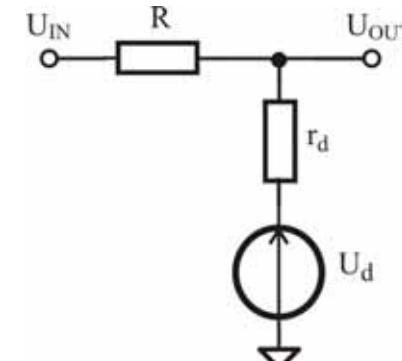
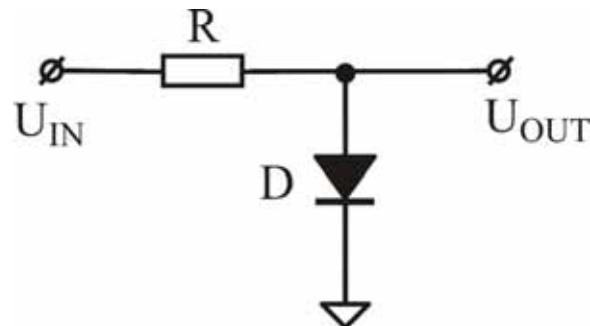
$$U_{IN} \Leftrightarrow ?$$

$$U_{OUT} = \begin{cases} ? & \text{за } ? \\ ? & \text{за } ? \end{cases}$$

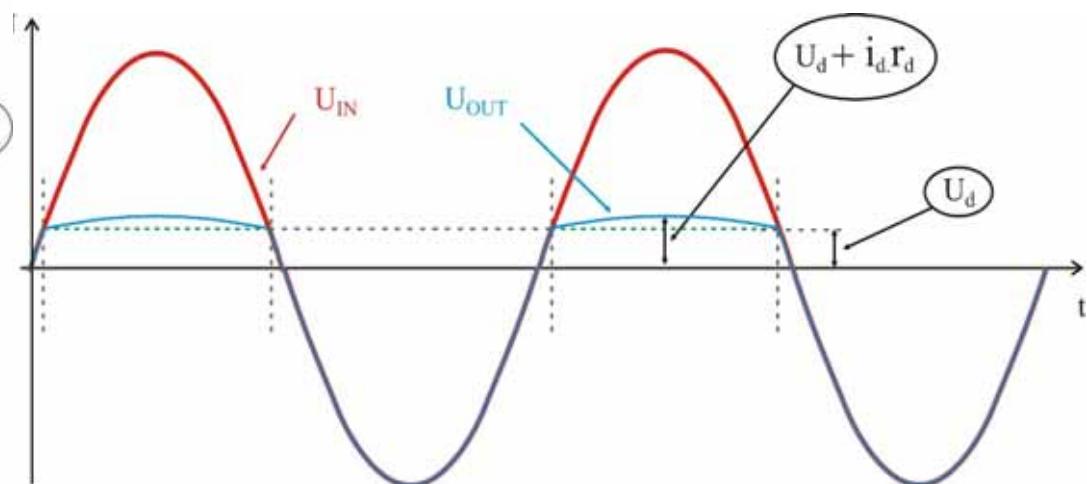
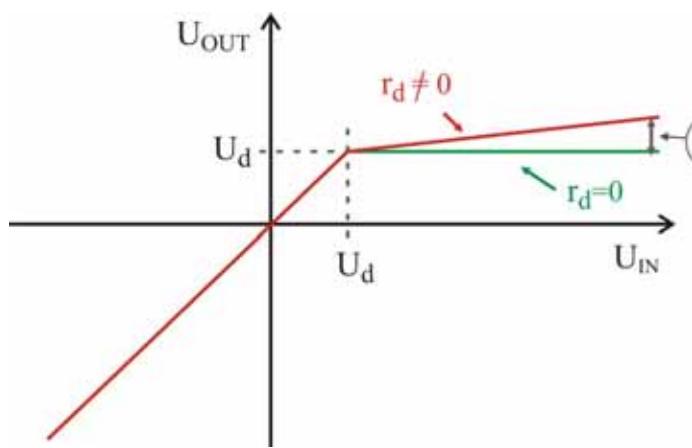
$$U_{IN} \Leftrightarrow ?$$



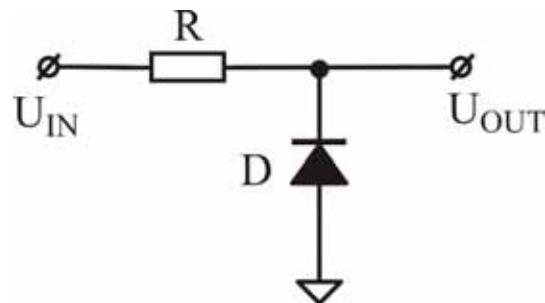
## Еквивалентни схеми



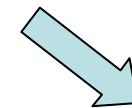
$$U_{OUT} = \begin{cases} U_{IN} & \text{за } U_{IN} \leq U_d \\ (U_d + i_d \cdot r_d) & \text{за } U_{IN} > U_d \end{cases}$$



## Еквивалентни схеми

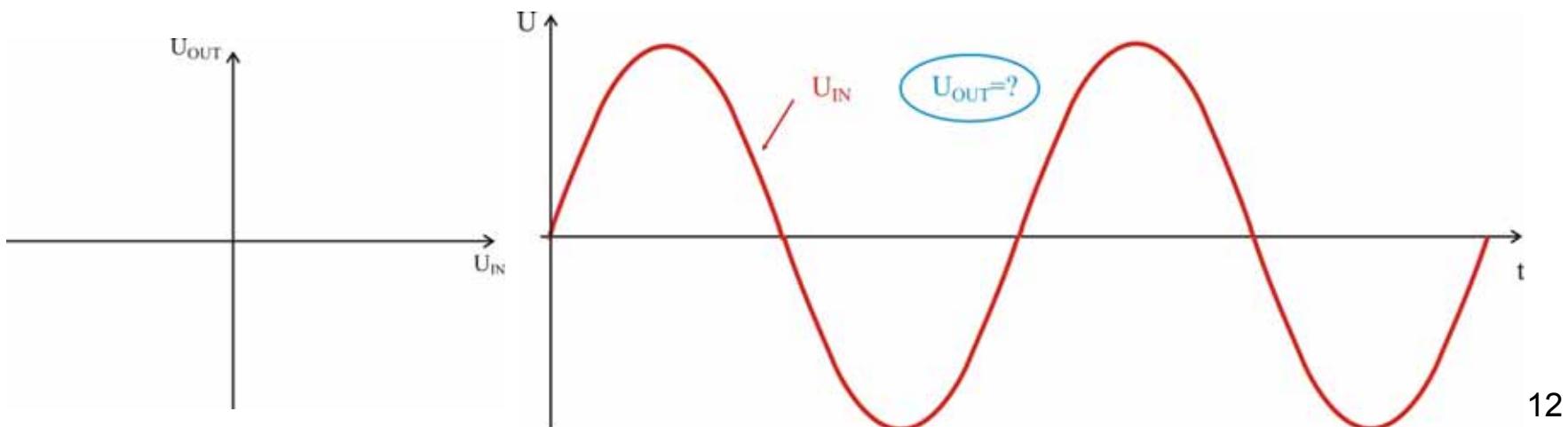


$U_{IN} \Leftrightarrow ?$

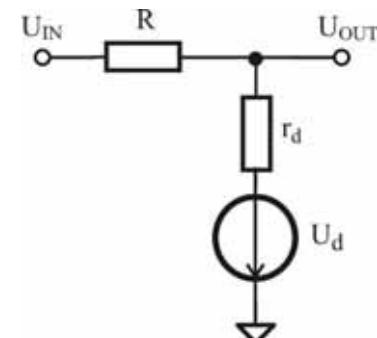
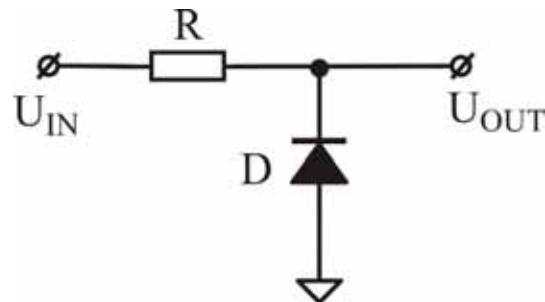


$U_{IN} \Leftrightarrow ?$

$$U_{OUT} = \begin{vmatrix} ? & \text{за} & ? \\ ? & \text{за} & ? \end{vmatrix}$$



## Еквивалентни схеми

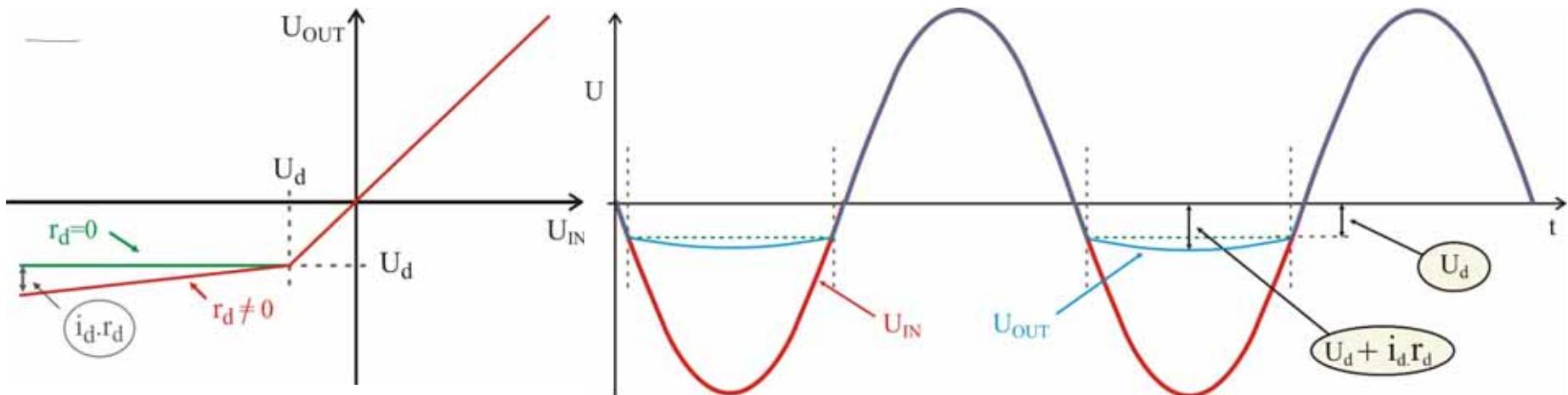


$$U_{IN} \leq -U_d$$

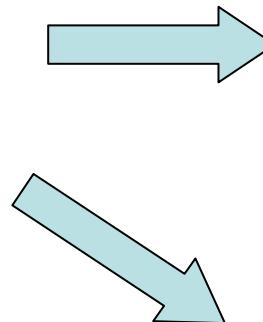
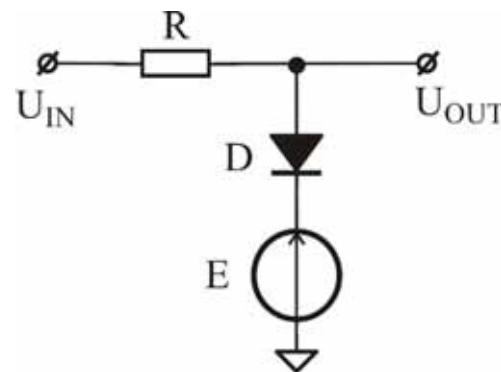


$$U_{IN} > -U_d$$

$$U_{OUT} = \begin{cases} U_{IN} & \text{за } U_{IN} > -U_d \\ -U_d - i_d \cdot r_d & \text{за } U_{IN} \leq -U_d \end{cases}$$



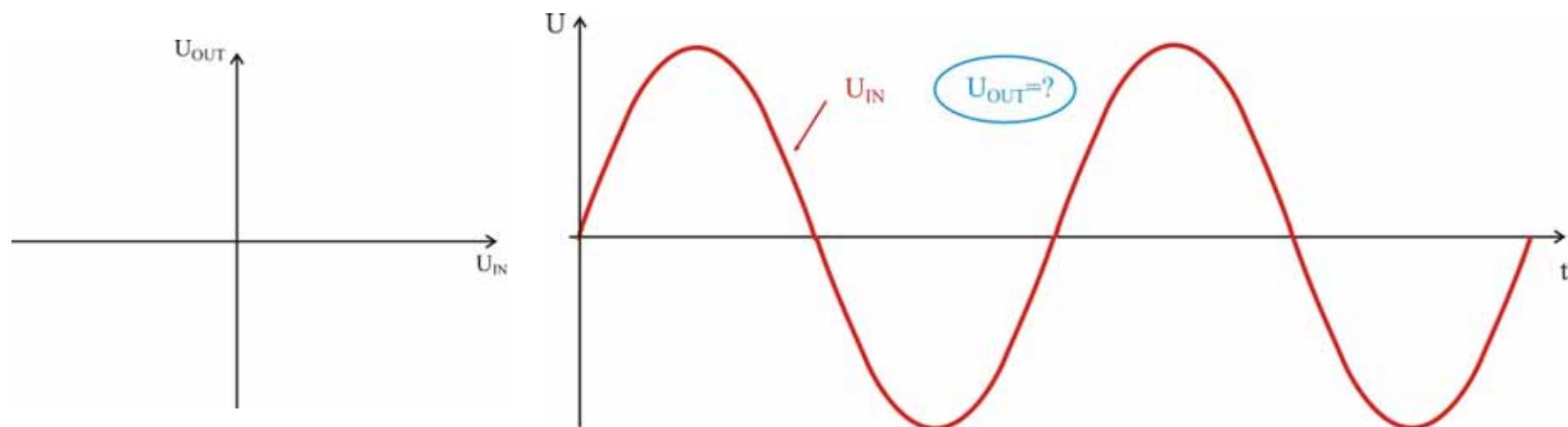
## Еквивалентни схеми



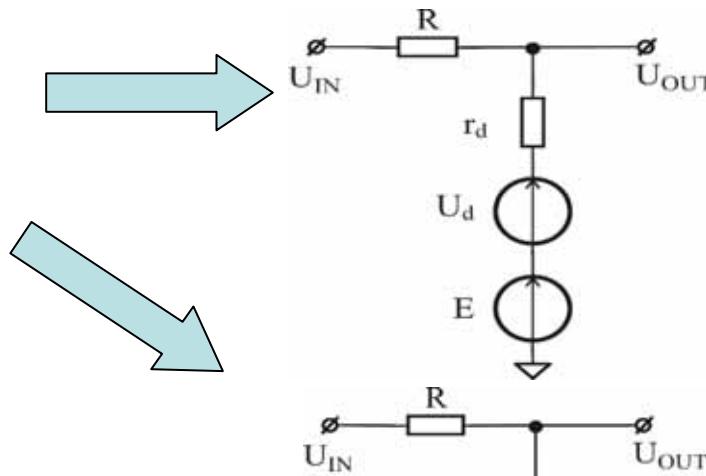
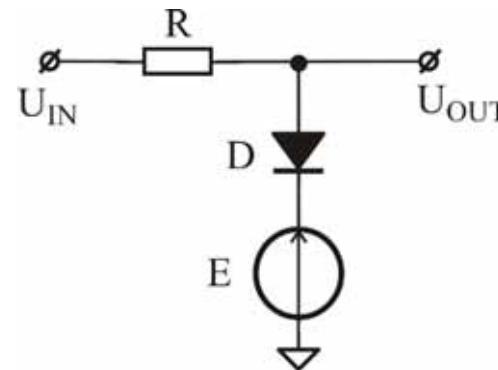
$U_{IN} \Leftrightarrow ?$

$$U_{OUT} = \begin{vmatrix} ? & \text{за} & ? \\ ? & \text{за} & ? \end{vmatrix}$$

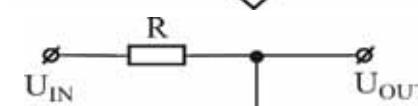
$U_{IN} \Leftrightarrow ?$



## Еквивалентни схеми

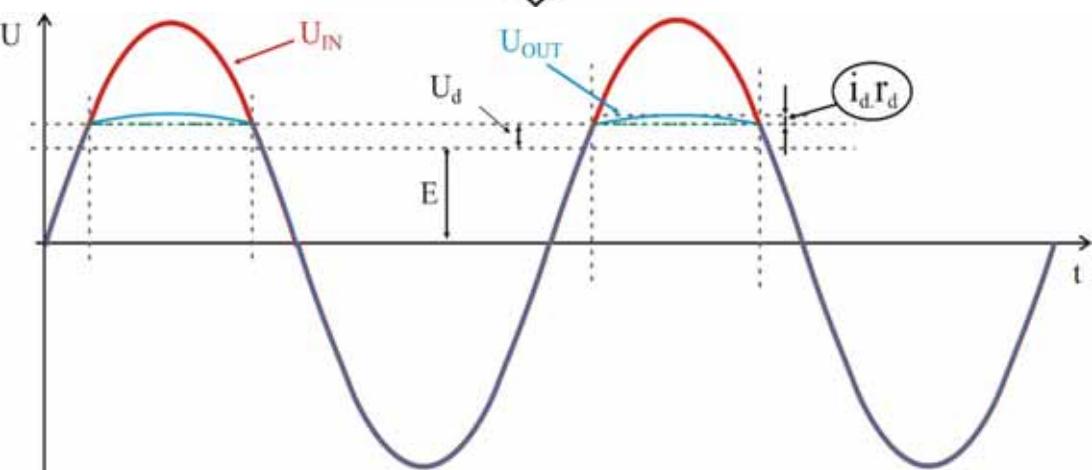
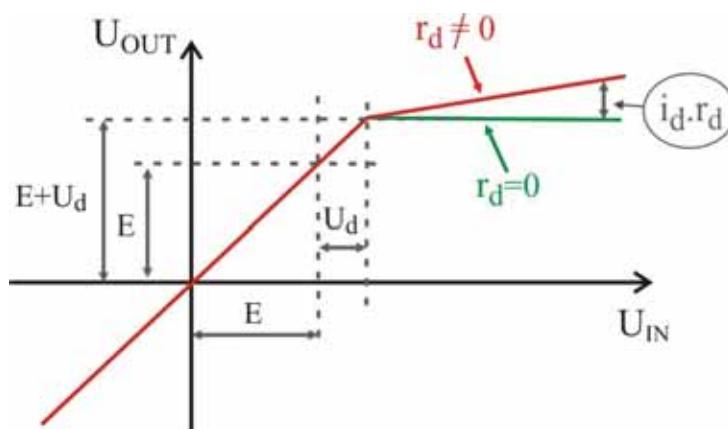


$$U_{IN} > E + U_d$$



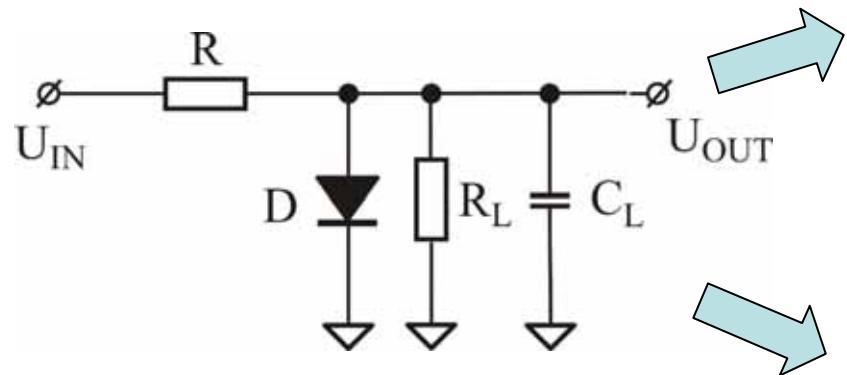
$$U_{IN} \leq E + U_d$$

$$U_{OUT} = \begin{cases} U_{IN} & \text{за } U_{IN} \leq (E + U_d) \\ (E + U_d) + i_d \cdot r_d & \text{за } U_{IN} > (E + U_d) \end{cases}$$



## Преходни процеси в едностранни паралелни диодни ограничители

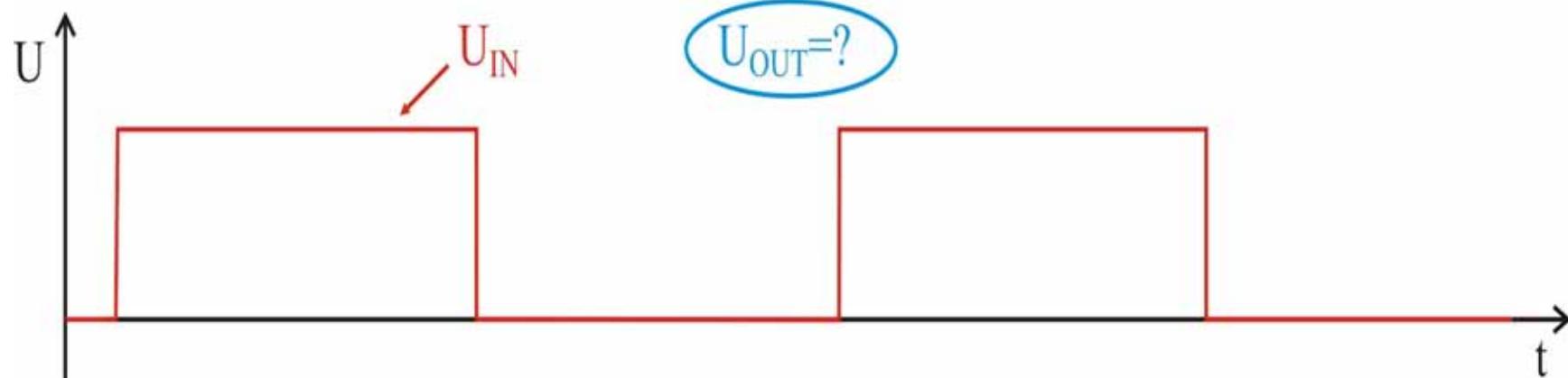
### Еквивалентни схеми



$$\tau_r = ?$$

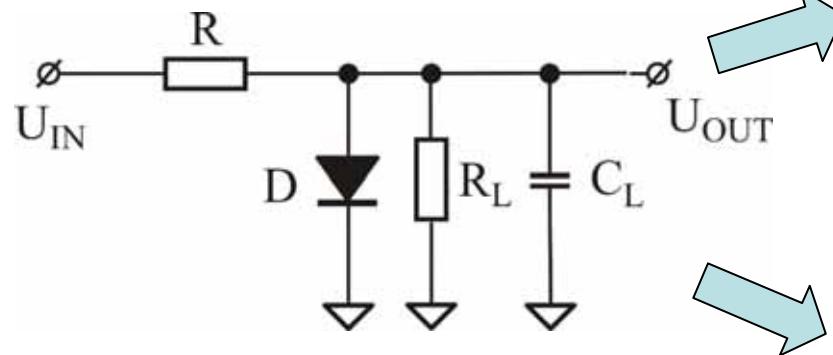
$$R_L \gg R \gg r_d$$

$$\tau_f = ?$$

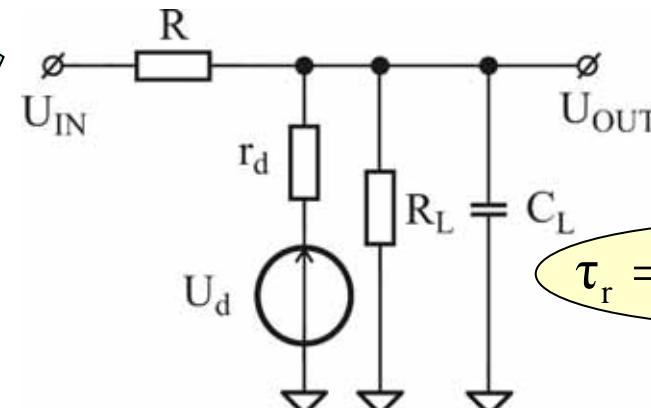


## Преходни процеси в еднострани паралелни диодни ограничители

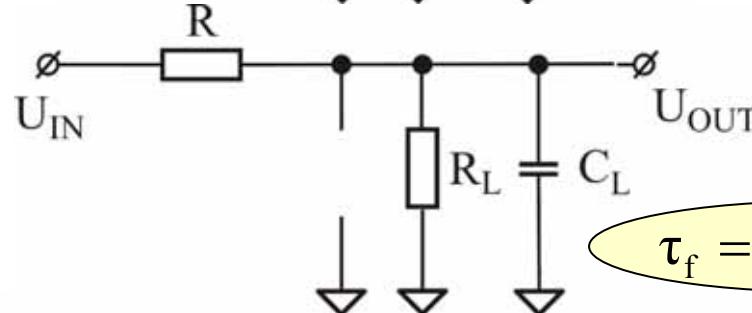
### Еквивалентни схеми



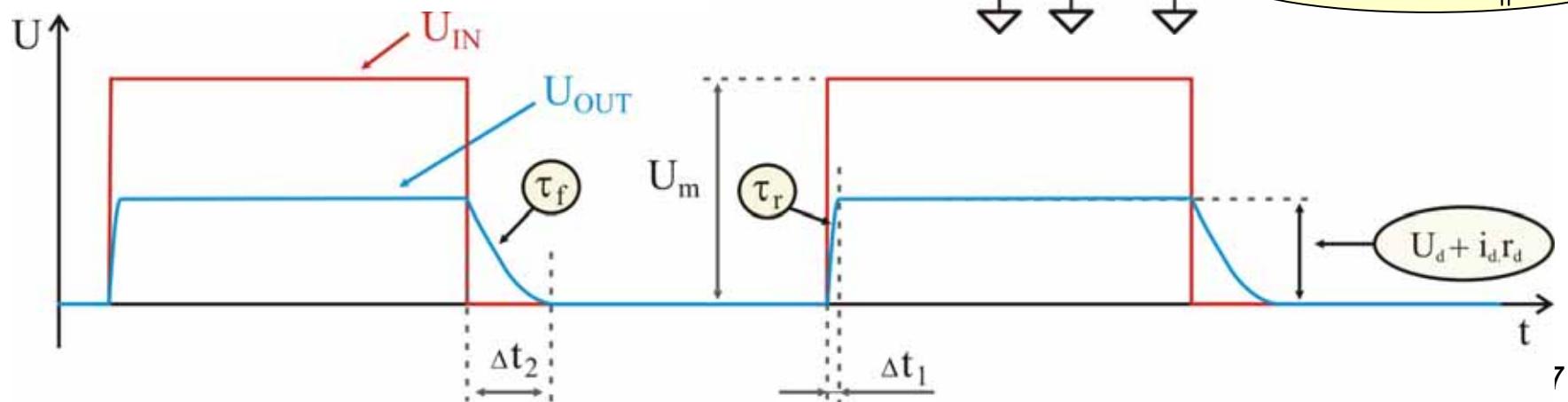
$$R_L \gg R \gg r_d$$



$$\tau_r = C \cdot (R_L \parallel r_d \parallel R)$$

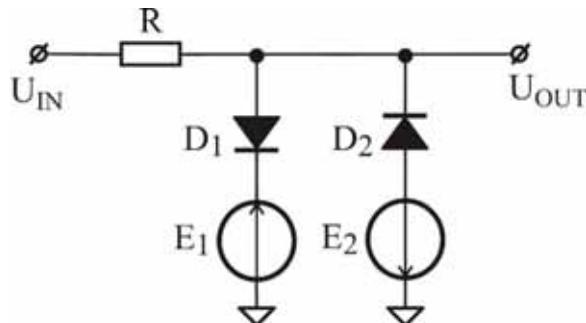


$$\tau_f = C \cdot (R_L \parallel R)$$



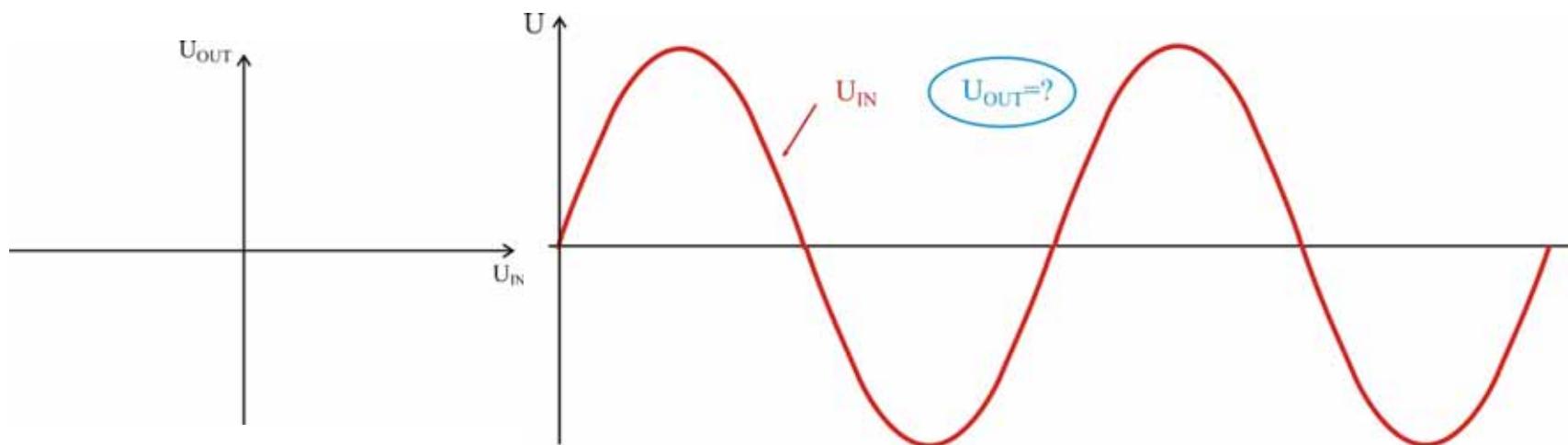
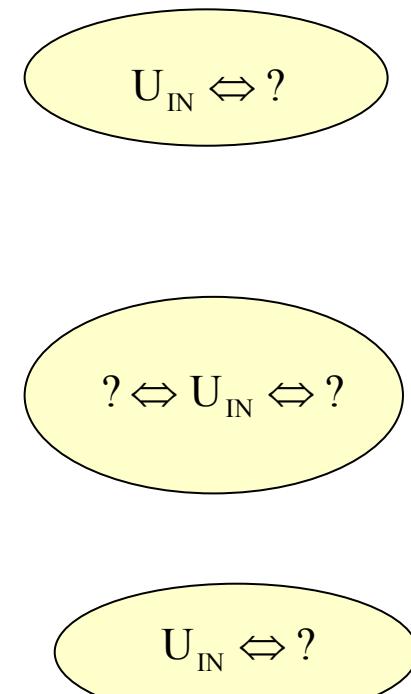
7

## ДВУСТРАННИ ПАРАЛЕЛНИ ДИОДНИ ОГРАНИЧИТЕЛИ

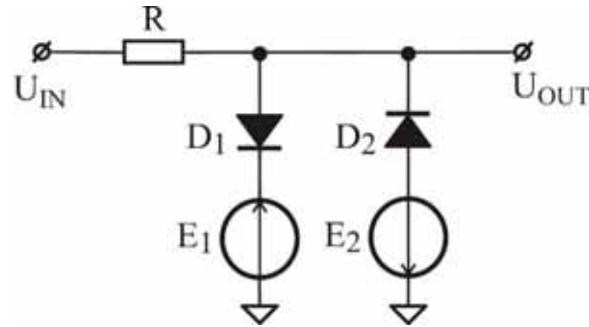


$$U_{\text{OUT}} = \begin{cases} ? & \text{за } ? \\ ? & \text{за } ? \\ ? & \text{за } ? \end{cases}$$

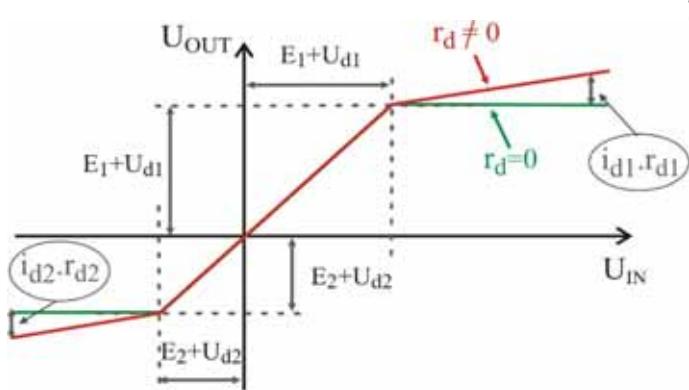
Еквивалентни схеми



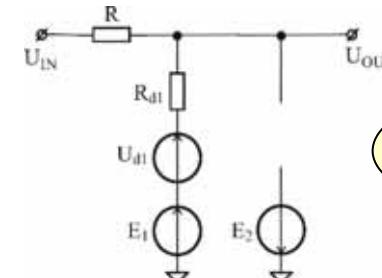
## ДВУСТРАННИ ПАРАЛЕЛНИ ДИОДНИ ОГРАНИЧИТЕЛИ



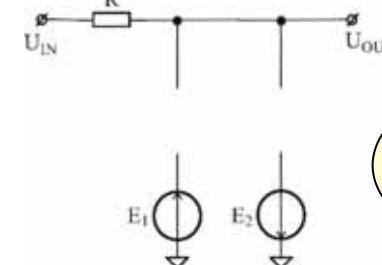
$$U_{OUT} = \begin{cases} (E_1 + U_{d1}) + i_{d1} \cdot r_{d1} & \text{за } U_{IN} > (E_1 + U_{d1}) \\ U_{IN} & \text{за } (E_2 - U_{d2}) \leq U_{IN} \leq (E_1 + U_{d1}) \\ (E_2 - U_{d2}) - i_{d2} \cdot r_{d2} & \text{за } U_{IN} < (E_2 - U_{d2}) \end{cases}$$



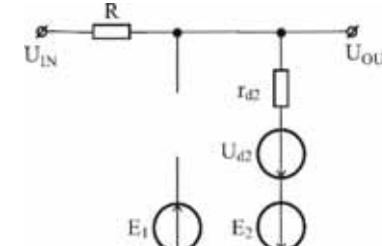
## Еквивалентни схеми



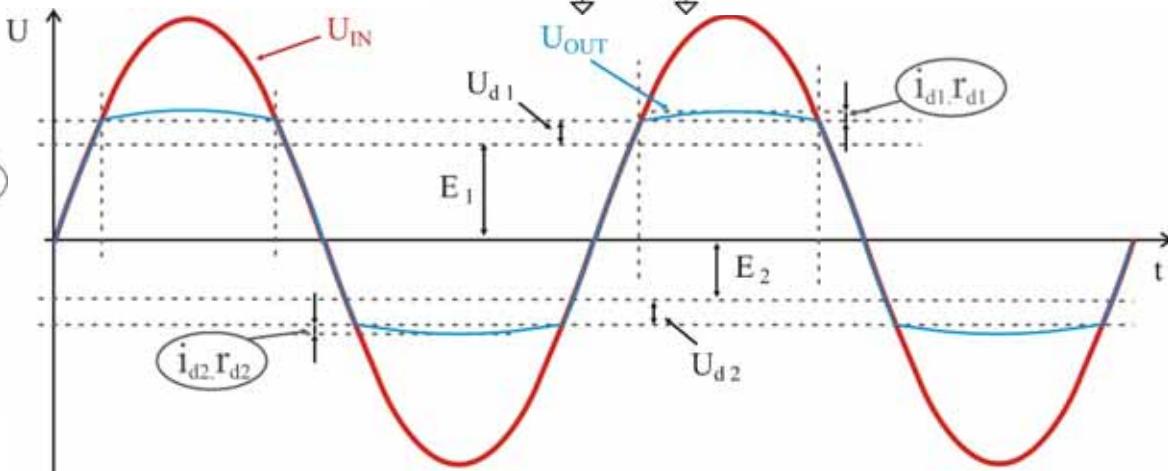
$$U_{IN} > (E_1 - U_{d1})$$



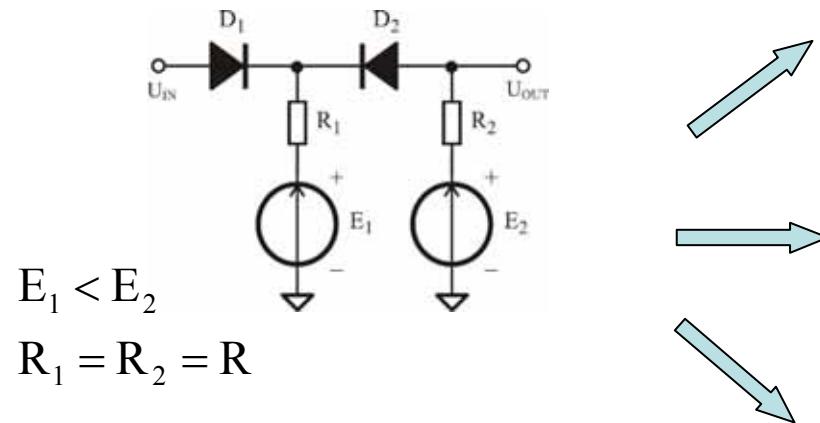
$$(E_1 + U_{d1}) \leq U_{IN} \\ U_{IN} \leq (E_2 - U_{d2})$$



$$U_{IN} < (E_2 - U_{d2})$$



## ДВУСТРАННИ ПОСЛЕДОВАТЕЛНИ ДИОДНИ ОГРАНИЧИТЕЛИ



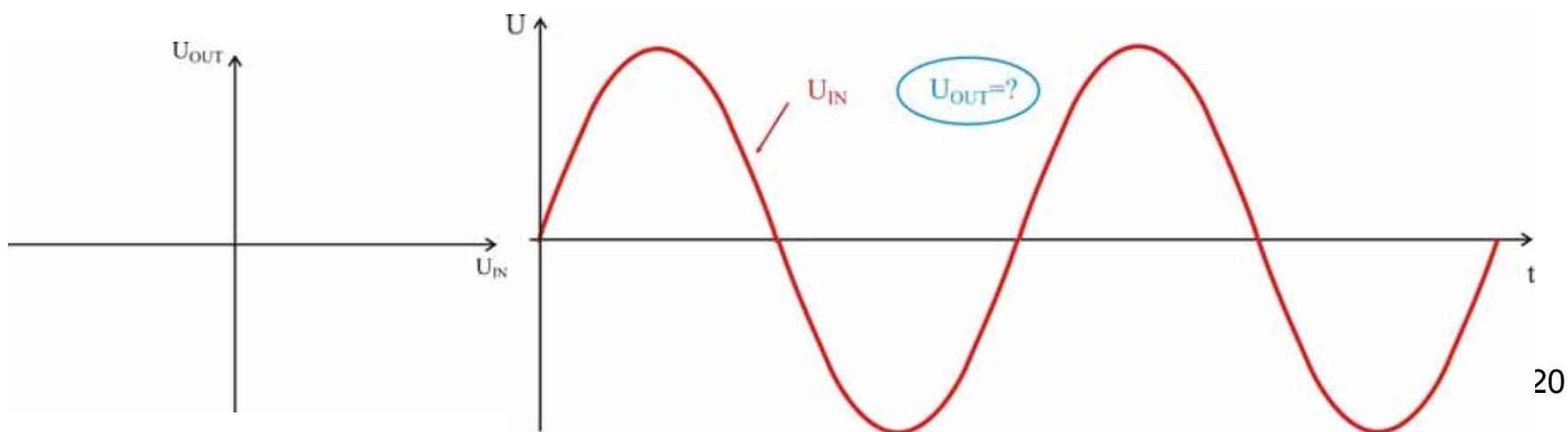
Еквивалентни схеми

$$U_{IN} \Leftrightarrow ?$$

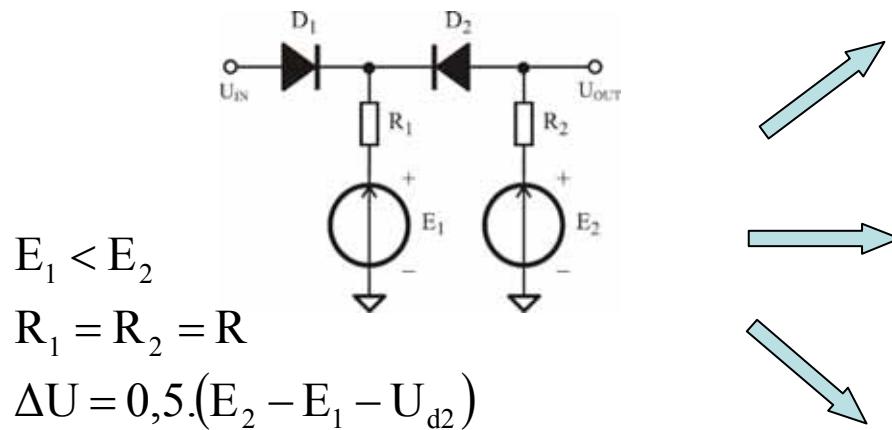
$$? \Leftrightarrow U_{IN} \Leftrightarrow ?$$

$$U_{IN} \Leftrightarrow ?$$

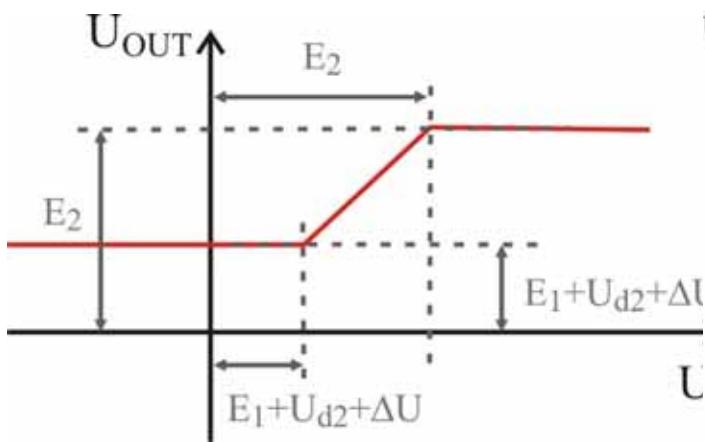
$$U_{OUT} \cong \begin{vmatrix} ? & \text{за} & ? \\ ? & \text{за} & ? \\ ? & \text{за} & ? \end{vmatrix}$$



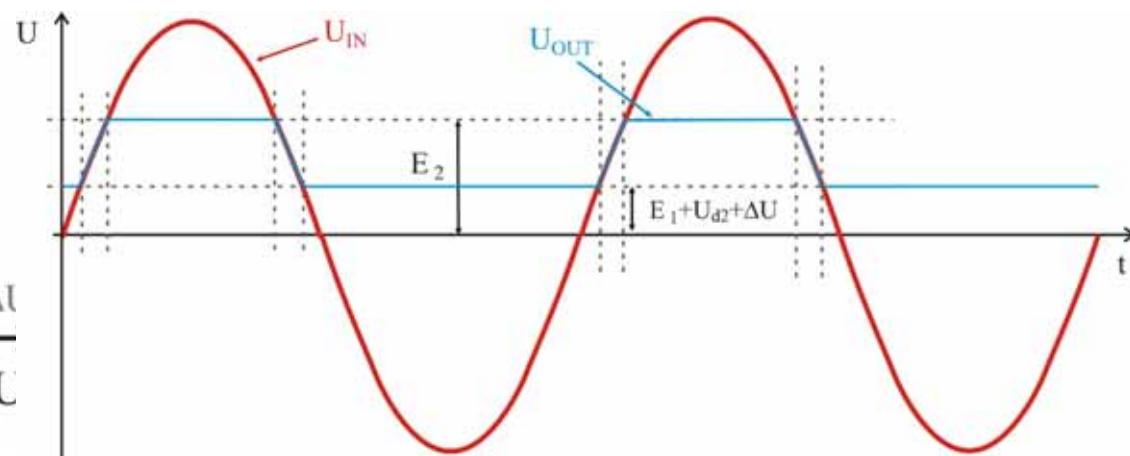
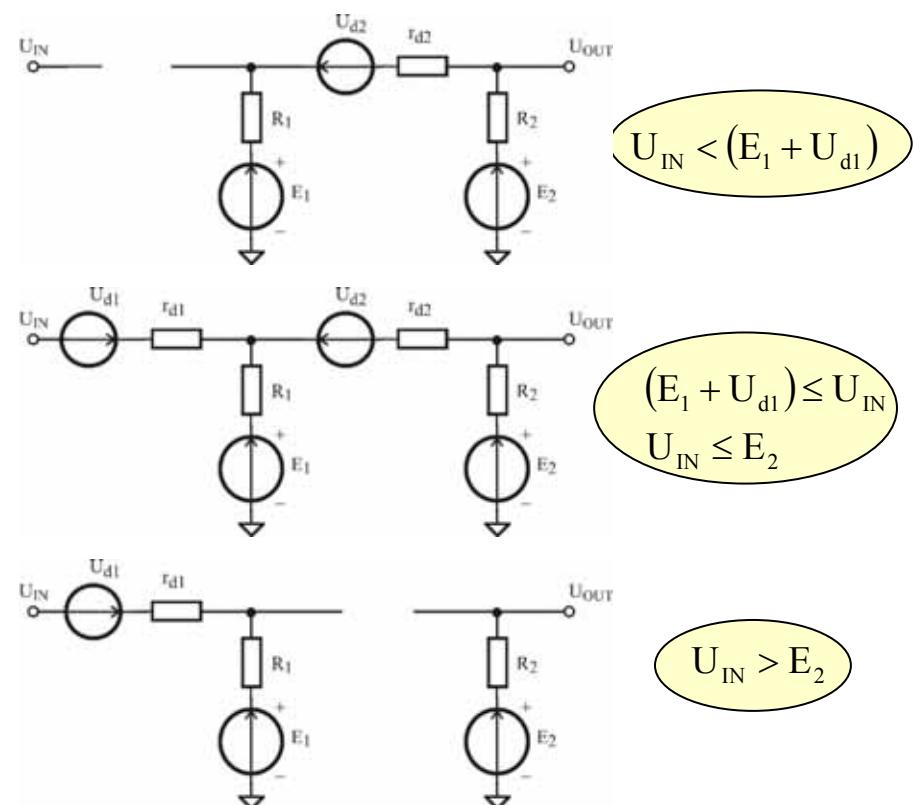
## ДВУСТРАННИ ПОСЛЕДОВАТЕЛНИ ДИОДНИ ОГРАНИЧИТЕЛИ

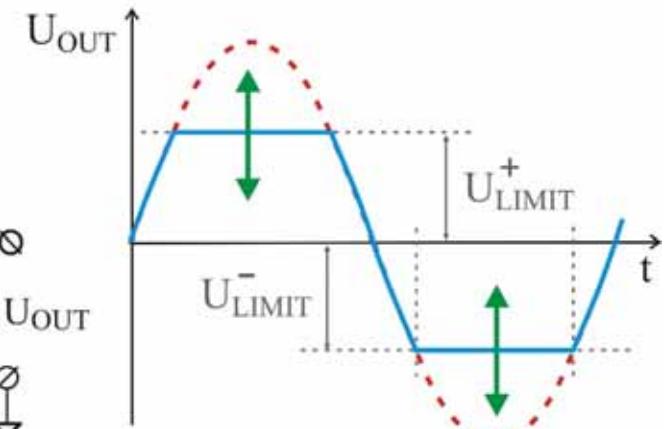
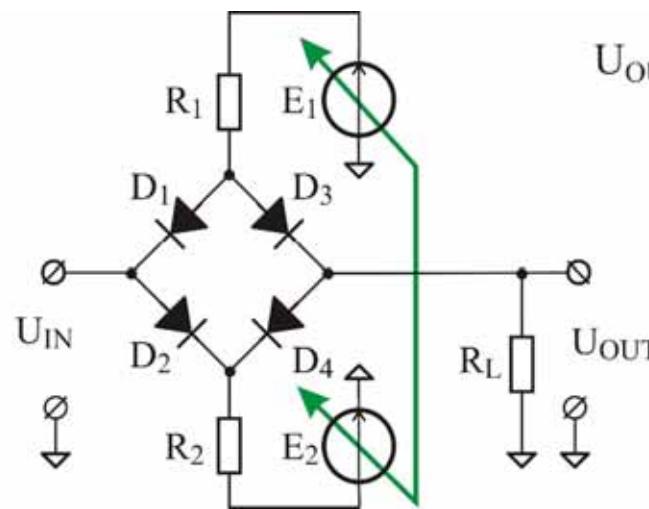
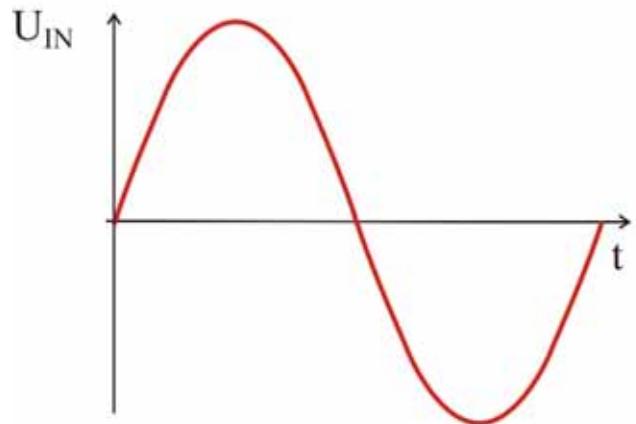
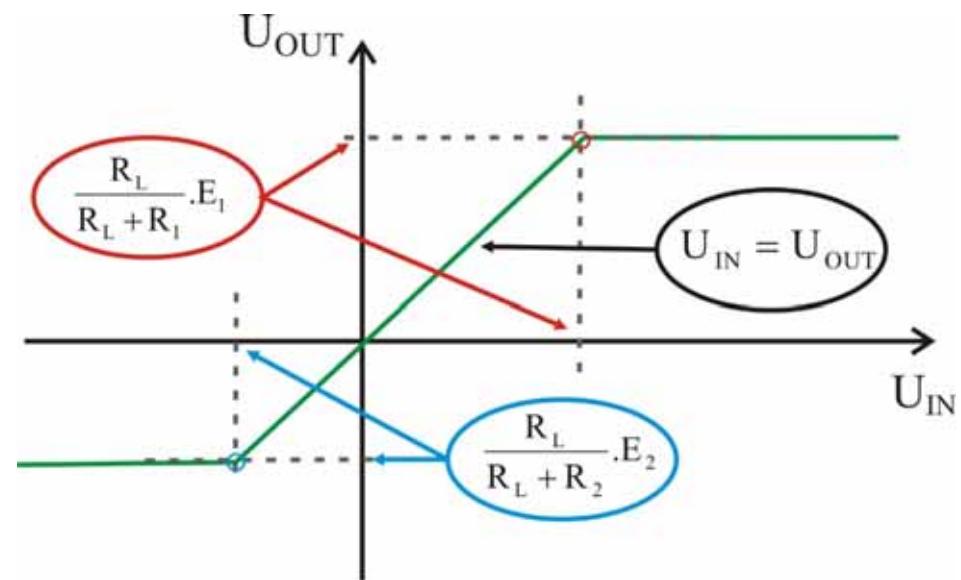
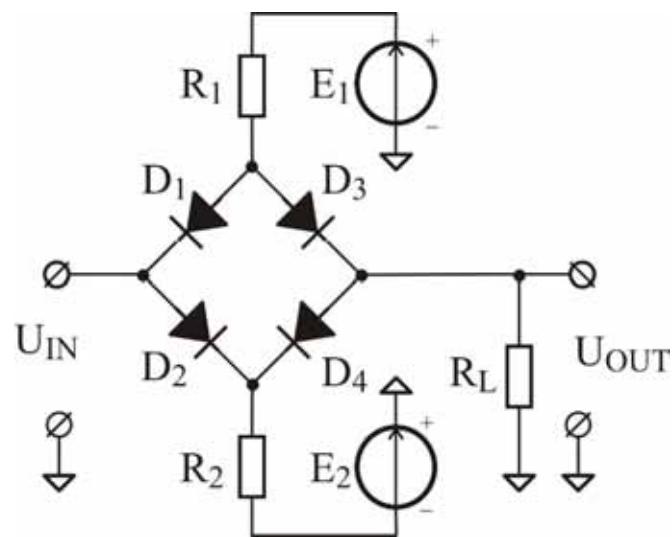


$$U_{\text{OUT}} \cong \begin{cases} E_1 + U_{d2} + \Delta U & \text{за } U_{\text{IN}} < (E_1 + U_{d1}) \\ U_{\text{IN}} & \text{за } (E_1 + U_{d1}) \leq U_{\text{IN}} \leq E_2 \\ E_2 & \text{за } U_{\text{IN}} > E_2 \end{cases}$$



## Еквивалентни схеми





## **ЛИТЕРАТУРА**

1. Попов А. Импулсна схемотехника – Технически Университет - София, 2016
2. Димитрова, М., И. Ванков. Импулсни схеми и устройства. С., Техника, 1987.
3. Rabaey J., A. Chandrakasan, B. Nikolic, Digital Integrated Circuits. A Design Perspective, Second Edition, Prentice Hall, 2003.
4. Оренхайм А., А. Уилски, Я. Йънг, Сигнали и системи, С., Техника, 1993
5. Nonlinear Circuits Handbook, Analog Devices Inc., 1974
6. Manuel des Circuits Integres Analogiques, Texas Instrument Inc. France, 1974
7. Rutkowski, Georgge B. "Handbook of integrated circuit"; Prebtice Hall, New Jersey

## **Internet адреси**

1. <http://www.ittc.ku.edu/~jstiles/312/handouts/Diode%20Limiters.pdf>
2. <https://wiki.analog.com/university/courses/electronics/text/chapter-7>
3. [staff.iium.edu.my/adah510/L8%20clipper\\_clamper.ppt](http://staff.iium.edu.my/adah510/L8%20clipper_clamper.ppt)
4. [https://www.researchgate.net/post/What\\_is\\_a\\_proper\\_Analysis\\_of\\_this\\_Variant\\_OPA\\_Diode\\_Limiter](https://www.researchgate.net/post/What_is_a_proper_Analysis_of_this_Variant_OPA_Diode_Limiter)
5. [http://people.seas.harvard.edu/~jones/es154/lectures/lecture\\_2/diode\\_circuits/diode\\_appl.html](http://people.seas.harvard.edu/~jones/es154/lectures/lecture_2/diode_circuits/diode_appl.html)
6. <http://www.kluniversity.in/elearn/materials/ozyewohcli61376ozyewohcli.pdf>
7. <https://www.coursehero.com/file/p1nve9j/TYPICAL-DIODES-Diode-Limiting-and-Clamping-Circuits-%C3%98-Diode-Limiters-%C3%98-Diode/%C3%98-Diode-Limiters-%C3%98-Diode/>