ON-CHIP SPIRAL INDUCTOR/TRANSFORMER DESIGN AND MODELING FOR RF APPLICATIONS

by

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ABSTRACT

Passive components are indispensable in the design and development of microchips for high-frequency applications. Inductors in particular are used frequently in radio frequency (RF) IC's such as low-noise amplifiers and oscillators. High performance inductor has become one of the critical components for voltage controlled oscillator (VCO) design, for its quality factor (Q) value directly affects the VCO phase noise. The optimization of inductor layout can improve its performance, but the improvement is limited by selected technology. Inductor performance is bounded by the thin routing metal and small distance from lossy substrate. On the other hand, the in-accurate inductor modeling further limits the optimization process.

The on-chip inductor has been an important research topic since it was first proposed in early 1990's. Significant amount of study has been accomplished and reported in literature; whereas some methods have been used in industry, but not released to public. It is of no doubt that a comprehensive solution is not exist yet. A comprehensive study of previous will be first address. Later author will point out the in-adequacy of skin effect and proximity effect as cause of current crowding in the inductor metal. A model method embedded with new explanation of current crowding is proposed and its applicability in differential inductor and balun is validated. This study leads to a robust optimization routine to improve inductor performance without any addition technology cost and development.

ACKNOWLEDGMENTS

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TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

LIST OF ACRONYMS/ABBREVIATIONS

EM	Electro-magnetic
IC	Integrated Circuit
MEMS	Micro Electron-Mechanical System
Q	Quality Factor
RF	Radio Frequency
VCO	voltage controlled oscillator

CHAPTER ONE: INTRODUCTION

1.1 Motivation

1.1.1 Need for Inductors

In contrast with digital circuits which use mainly active devices, on-chip passive components are necessary and imperative adjuncts to most RF electronics [1-2]. These components, which include inductors, capacitors, varactors, and resistors, have been known as performance as well as cost limiting elements of radio frequency (RF) integrated circuits. While all of these components can be realized using MOS technology, their specific designs necessitate special consideration due to the requirement of high quality factor Q at relatively high frequencies. Inductors in particular are critical components in oscillators and other tuned circuits. For low-frequency applications, passive devices can be connected externally, but as the frequency increases, the characteristics of the passive devices would be overwhelmed by parasitic effect [3]. For instance, a voltage-controlled oscillator (VCO) of 10 MHz needs a tank inductance on the order of several μH, whereas at 10 GHz the inductance is around 1 nH. It's impossible to access such a small inductance externally, since the inductance associated with the package pin and bond wire can exceed 1 nH. As a result, on-chip passive components are commonly used in RF applications.

This chapter will focus on the on-chip inductors. Basically there are three types of on-chip inductors. The most widely used type is the planar spiral inductor, and a square shaped spiral inductor is shown in Figure 1 [4]. Although a circular shaped inductor may be more efficient and yield better performance, the shape of inductor is often limited to the availability of fabrication

processes. Most processes restrict all spiral angles to be 90°, and a rectangular/square pattern (hereafter called square pattern) is a nature choice, but a polygon spiral inductor can serve as a compromise between the square and circular shaped inductors. Structural parameters such as the outer dimension, number of turns, the distance between the centers of lines (or pitch), and substrate property are all important factors in determining the performance of on-chip inductors.

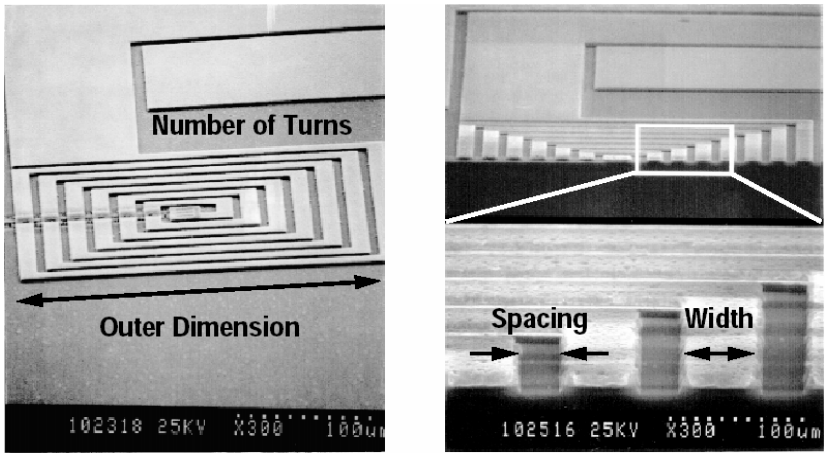


Figure 1 Topology and cross section of a typical on-chip square shaped spiral inductor. (after [4]).

Besides the spiral inductor, two other kinds of on-chip inductors have been used. Gyrator, or active inductor, utilizes active components (i.e., transistors) to transform the impedance of a capacitor to inductance [5]. Figure 2 shows the basic gyrator circuit. The active device and capacitor required in the gyrator can be easily fabricated and occupy minimal space, but they consume relatively large power and introduce additional noise. The third on-chip inductor type is constructed with the bond wire [6], as shown in Figure 3. It can offer a very high quality factor (30~60, typically), but

such an approach is likely to cause unwanted coupling to other devices and may not be sufficiently robust for some RF applications. Only spiral inductors are covered in this dissertation.

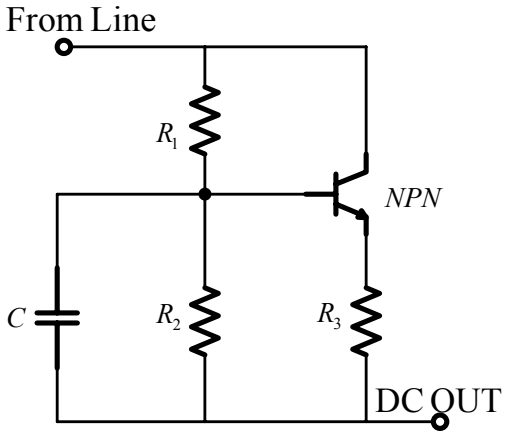


Figure 2 Equivalent circuit of a basic gyrator.

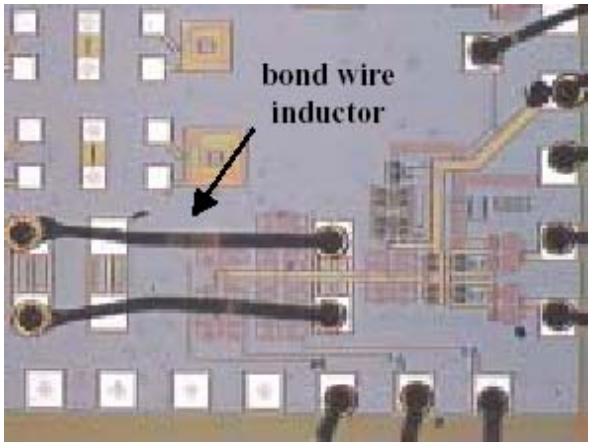
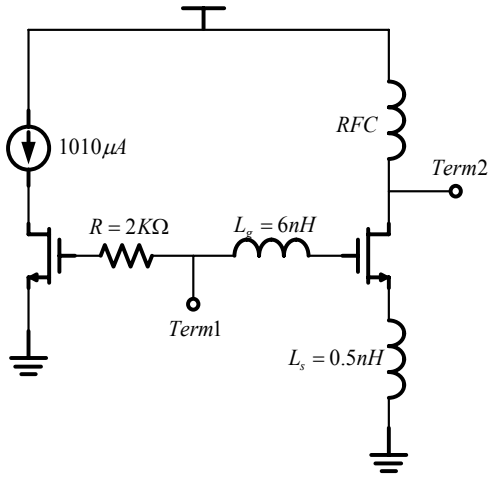


Figure 3 Schematic of a bond wire inductor (after [6]).

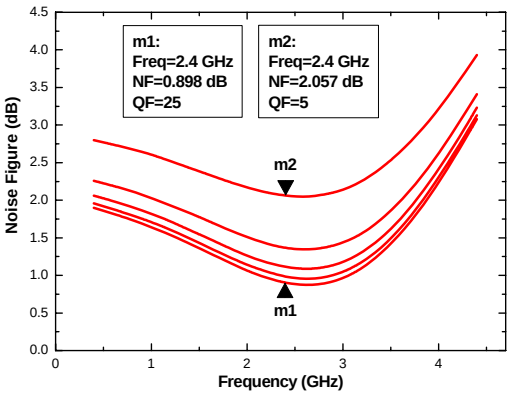
1.1.2 The Effect of Inductor Quality Factor

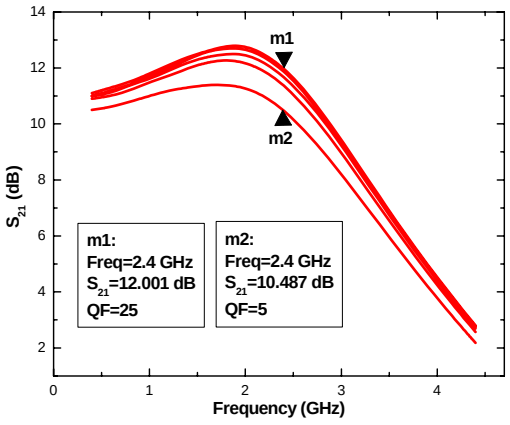
One of most frequently mentioned figure of merit of the on-chip inductor is its Q (quality factor). It has be often questioned what is quality factor and how it relates with the performance of an inductor.

Although describing the roll of an inductor in a RF circuit is not the purpose of this dissertation, two example circuits below, with simulation results, explain the importance of Q factor. Figs. 4(a) shows a typical low-noise amplifier (LNA) with two active inductors and an ideal inductor with infinite inductance serving as RF choke (RFC). Figs. 4(b) and (c) show the simulated noise figure and current gain, respectively, for the LNA when the Q factors of the two inductors are assumed equal and changed from 5 to 25. Clearly, the RF performances of the LNA are degraded when the inductors' Q factor is reduced. Figure 5(a) shows an RF oscillator circuit having one inductor, and the simulation results given in Figure 5(b) indicate that the phase noise of the circuit is again degraded as the Q factor of the inductor is reduced.



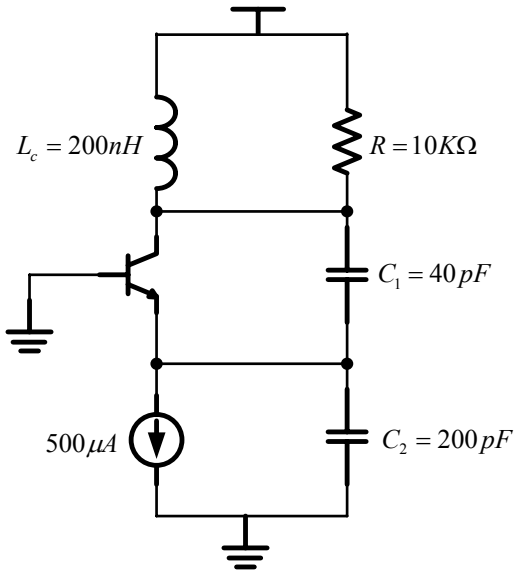
(a)



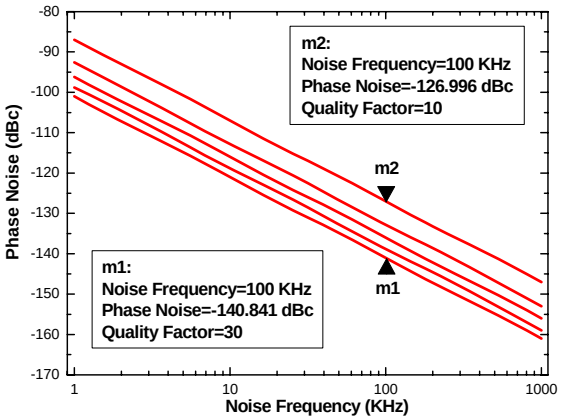


(b) (c)

Figure 4(a) A typical low-noise amplifier, (b) simulated noise figures, and (c) simulated small-signal current gains. In the simulations, the two active inductors were assumed having the same Q factors and the Q factors were increased from 5 to 25.



(a)



(b)

Figure 5(a) An RF oscillator circuit, and (b) simulated phase noises of the circuit with the inductor's Q factor increasing from 10 to 30.

1.2 Description of Problems

As studied in the previous section, inductance quality factor is a limiting factor of RF front end circuits. High performance on-chip magnetic device design method is highly demanded for both academic study and industrial development.

This dissertation is constructed with six chapters. The first chapter introduces the application of inductor and describes the aim of this dissertation. The second chapter reviews significant amount of most updated literatures related to the topic, and offers a clear clue about on-chip inductor physics and modeling. Chapter three discovers the current crowding phenomena from a new angle of view, and proposes a new model structure to address this discovery. Chapter four further fulfill the proposed model in differential inductor and balun, and chapter five proposed an algorithm in optimizing inductor layout without any additional technology modification. Silicon data is measured and presented in the related chapters. At last, chapter six concludes the dissertation, and lead to the future work.

CHAPTER TWO: LITERATURE REVIEW

2.1 Modeling Concept and Design Guideline

Traditionally, spiral inductors are made in square shape due to its ease of design and support from drawing tools [7]. From the performance point of view, however, the most optimum pattern is a circular spiral because it suffers less resistive and capacitive losses. But the circular inductor is not widely used because only a few commercial layout tools support such a pattern. Hexagonal and octagonal structures are good alternatives, as they resemble closely to the circular structure and are easier to construct and supported by most computer-aided design tools. It has been reported that the series resistance of the octagonal and circular shaped inductors is 10% smaller than that of a square shaped spiral inductor with the same inductance value [8].

In 1990, Nguyen and Meyer [9] first developed a planar inductor on silicon using the interconnect technology, and they proposed a simple π model to describe the inductor's behavior (see Figure 6(a)), which can be considered as a section of the ladder model for interconnects. An improved model, shown in Figure 4(b), was later developed by Ashby et al. [10]. This model accounts for more physical mechanisms taking place in the inductor. However, the model parameters need to be extracted from empirical curve fitting rather than physical means. More recently, Yue and Wong [11] reported an inductor model similar to that in Figure 6(b), as shown in Figure 6(c), but with models parameters more relevant to inductor geometry and processing.

In the following subsections, we will consider the square shaped spiral inductor and use the model in Figure 6(c) as a benchmark to discuss the important issues associated with such a device,

including the series inductance (LS), resistances (RS and RSi), capacitances (CS, CSi, and COX), and quality factor and substrate loss. Note that these issues strongly correlate with the components in the equivalent circuit given in Figure 6(c) for modeling the on-chip inductor.

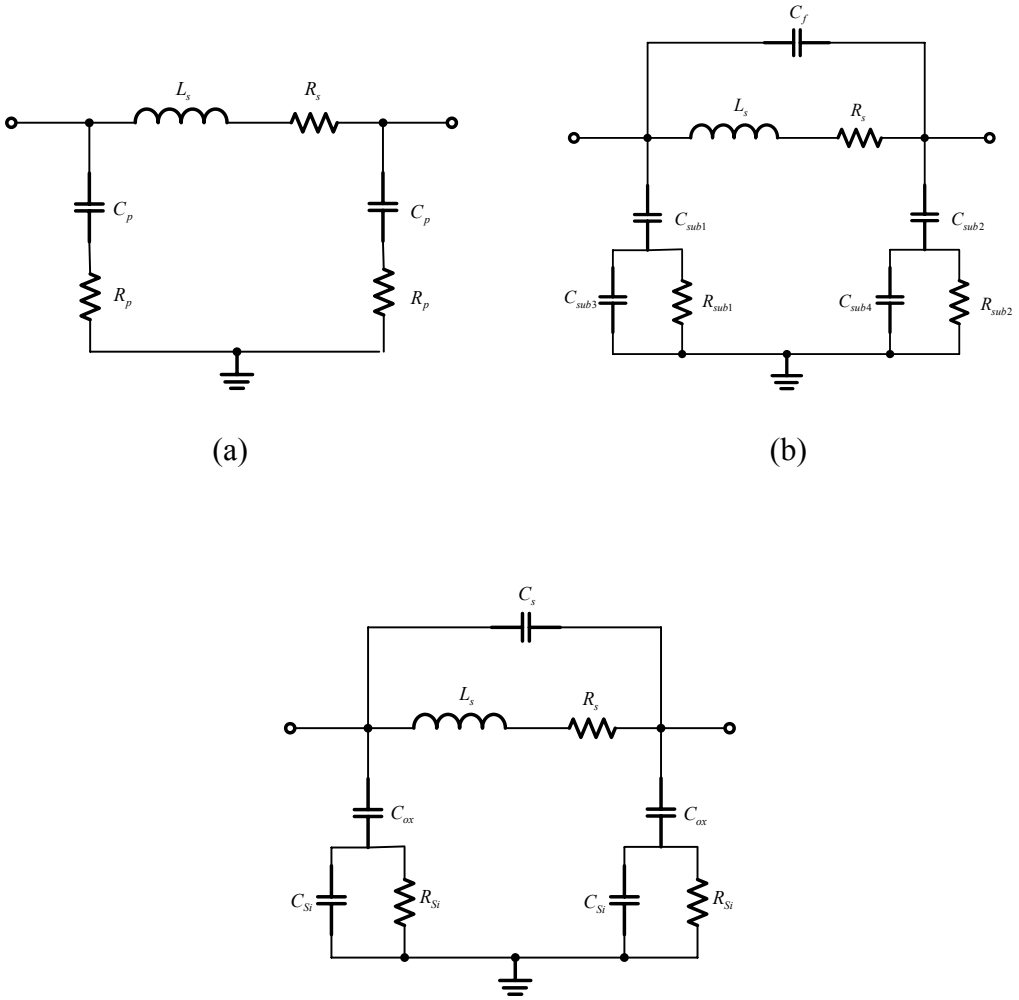


Figure 6 Lumped π models for spiral inductors developed by (a) Nguyen and Meyer [9]; (b) Ashby et al. [10]; and (c) Yue and Wong [11].

2.1.1 Series Inductance

It is quite obvious that the knowledge of series inductance is critical to engineers who develop and utilize on-chip inductors for RF IC's. The inductance represents the magnetic energy stored in the device, although parasitic components may store energy as well. Numerical simulators computing the electromagnetic field distribution can be used to calculate the inductance, but our focus here is to determine such a parameter through analytical means, as the latter is less complicated and provides more physical insights.

In 1946, Grover derived formulas for the inductance of various inductor structures [12]. Greenhouse later applied the formulas to calculate the inductance of a square shaped inductor [13]. He divided the inductor into straight-line segments, and calculated the inductance by summing the self inductance of the individual segment and mutual inductance between any two parallel segments. The model has the form of

$$L_S = L_0 + M_+ - M_- \tag{1}$$

where LS is the total series inductance, L0 is the sum of the self inductance of all the straight segments, M+ is the sum of the positive mutual inductances and M- is the sum of the negative mutual inductances. Self inductance L'0 of a particular segment can be expressed as

$$L'_0 = 2l\left(\ln\frac{2l}{w+t} + 0.5 + \frac{w+t}{3l}\right) \tag{2}$$

L'0 is the inductance in nH, l is the length of a segment in cm, w is the width of a segment in cm, and t is the metal thickness in cm. The mutual inductance between any two parallel wires can be calculated using

$$M = 2lQ' \tag{3}$$

where M is the mutual inductance in nH and Q' is the mutual inductance parameter

$$Q' = \ln\left[\frac{l}{GMD} + \sqrt{1+\left(\frac{l}{GMD}\right)^2}\right] - \sqrt{1+\left(\frac{l}{GMD}\right)^2} + \frac{l}{GMD} \tag{4}$$

GMD denotes the geometrical mean distance between the two wires. When two parallel wires are of the same width, GMD is reduced to

$$\ln GMD = \ln d - \frac{w^2}{12d^2} - \frac{w^4}{60d^4} - \frac{w^6}{168d^6} - \frac{w^8}{360d^8} - \frac{w^{10}}{660d^{10}} - \cdots \tag{5}$$

d is the pitch of the two wires. Note that the mutual inductance between two segments that are perpendicular to each other is neglected. As the number of segments increases, the calculation complexity is increased notably because it is proportional to (number of segments)^2. Another drawback of the model is its limitation to only square shaped inductors.

The above model could be simplified using an averaged distance for all segments rather than considering the segments individually [14]. Based on this approach, the self and mutual inductances are calculated directly as

$$L_0 = \frac{\mu_0}{4\pi} l \left(\ln \frac{l_T}{n(w+l)} - 0.2 \right) \tag{6}$$

$$M_- = \frac{\mu_0}{4\pi} l_T \frac{n}{214} \tag{7}$$

$$M_+ = \frac{\mu_0}{4\pi} l_T (n-1) \left[\ln \left(\sqrt{1+\left(\frac{l_T}{4nd}\right)^2} + \frac{l_T}{4nd} \right) - \sqrt{1+\left(\frac{4nd}{l_T}\right)^2} + \frac{4nd}{l_T} \right] \tag{8}$$

where μ_0 is the permeability of vacuum, l_T is the total inductor length, n is the number of turns, and d' is the averaged distance of all segments:

$$d' = (w+s) \left(\sum_{i=1}^{(n-i)>0} i(n-i) \Big/ \sum_{i=1}^{(n-i)>0} (n-i) \right) \tag{9}$$

Mohan developed another method which further simplifies the calculations based on the current sheet concept [15]. His method serves as an adequate approximation for geometries where the conductor thickness is dwarfed by the length and width, and has the advantage of easily extendable to other geometries (i.e., octagonal and circular).

The methods mentioned above offer various solutions to estimate the inductance of a square shaped inductor. Some empirical techniques based on curve fitting have also been reported in [16]-[18], however models derived in this way cannot be scaled to reflect changes in the inductor's layout or fabrication technology.

2.1.2 Resistances

Series resistance R_S (see Figure 6(c)) arises from the metal resistivity in the inductor and is closely related to the quality factor. As such, the series resistance is a key issue for inductor modeling. When the inductor operates at high frequencies, the metal line suffers from the skin and proximity effects, and R_S becomes a function of frequency [19]. As a first-order approximation, the current density decays exponentially away from the metal-SiO_2 interface, and R_S can be expressed as [11]:

$$R_S = \frac{\rho \cdot l_T}{w \cdot t_{eff}} \tag{10}$$

Where ρ is the resistivity of the wire, and t_{eff} is given by

$$t_{eff} = \delta \cdot \left(1 - e^{-t/\delta}\right) \tag{11}$$

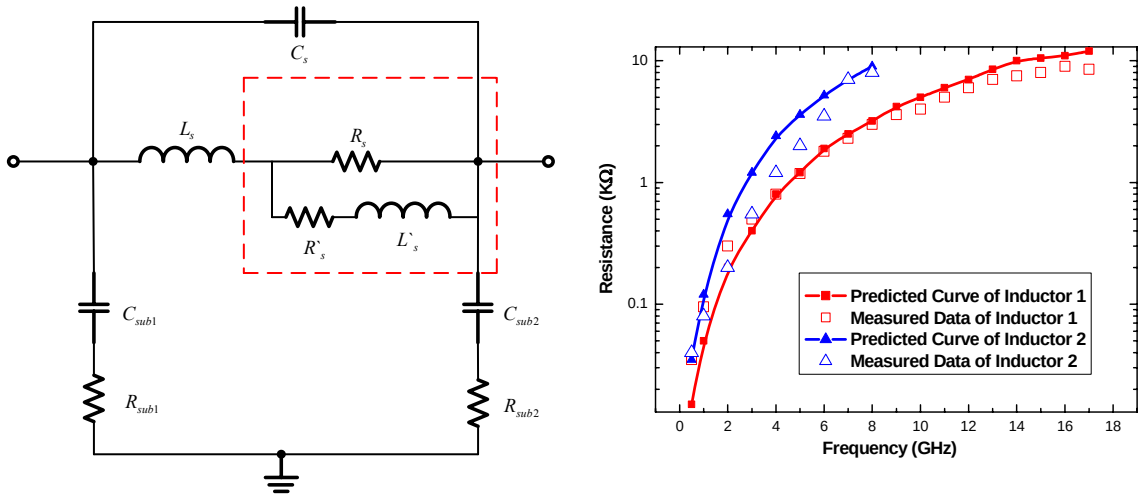
t is the physical thickness of the wire, and δ is the skin depth which is a function of the frequency:

$$\delta = \sqrt{\frac{\rho}{\pi \mu f}} \tag{12}$$

where μ is the permeability in H/m and f is the frequency in Hz.

The most severe drawback of a frequency-dependent component, such as R_S, in a model is that it cannot be directly implemented in a time domain simulator, such as Cadence Spectre. Researchers have proposed to use frequency-independent components to model frequency-dependent resistance [19]-[25]. Ooi et al. [21] replaced R_S with a network of 2 R's and 1 L, where R and L are frequency-independent components, in the inductor equivalent circuit, as shown in the dashed line box in Figure 7(a). The total equivalent resistance R_{total} of the box is

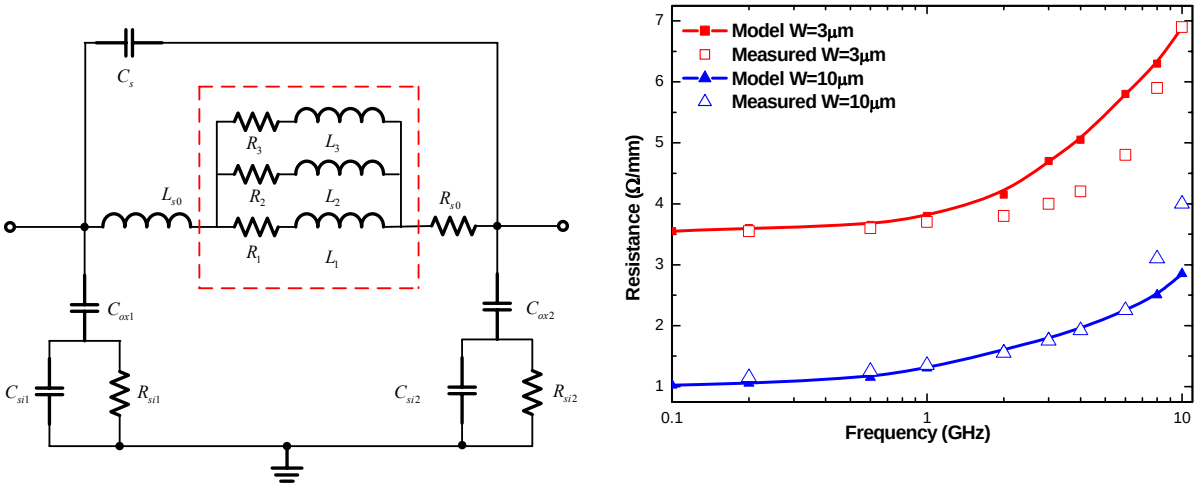
$$R_{total} = R_0\left[1+\frac{\omega^2\left(0.035\,\mathrm{w}^4 t^2\sigma^2\mu_0^2\right)}{P^2}\sum_{n=1}^{N}\left(\frac{n-M}{N-M}\right)^2\right] \qquad (13)$$



(a) (b)

Figure 7 (a) Model with improved series resistance (dashed line box) developed by Ooi et al. and (b) resistances measured and simulated for two different inductors (after [21]).

where R_0 is the steady-state series resistance, ω is the radian frequency, P is the turn pitch, t is the inductor thickness, w is the inductor width, σ is the conductivity, N is the total number of turns, and M is the turn number where the field falls to zero. This expression coincides with the approach based on the square-law relationship proposed in [22]. Figure 7(b) compares the measured and simulated series resistances of two different inductors. Another approach [23] used an R-L ladder to model the frequency-dependant resistor, which gives better flexibility and accuracy. Figs. 8(a) and (b) show the equivalent circuit of R-L ladder model and the series resistance results, respectively. Melendy et al. [24] used a series of R-L loops to represent the effect of series resistance, see Figs. 9(a) and (b). Another method is to average the different parameter values associated with R over the frequency [25].



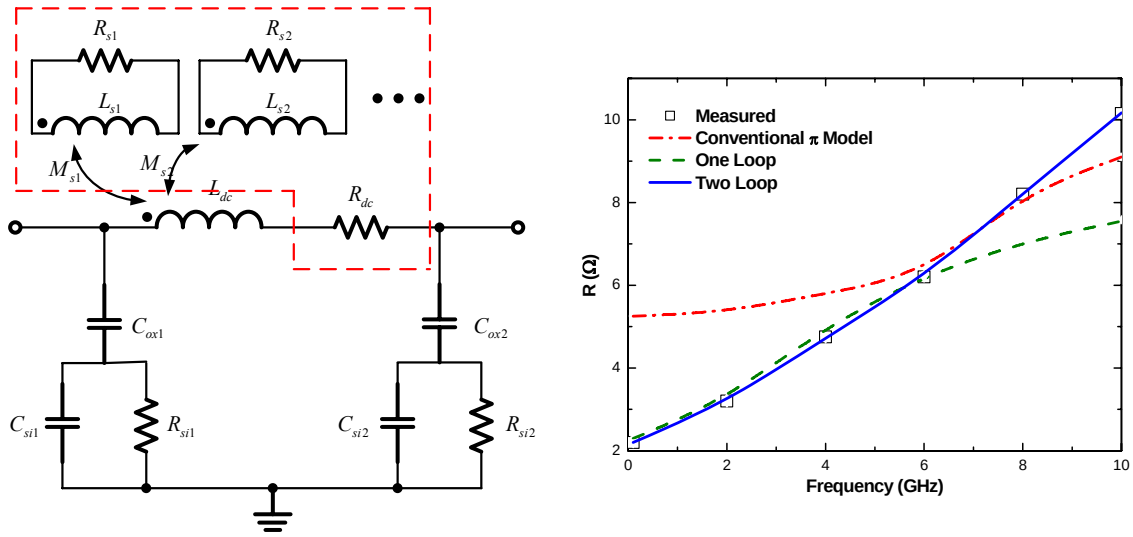
(a) (b)

Figure 8(a) Model with improved series resistance (dashed line box) developed by Rotella et al. and (b) resistances measured and simulated for two different inductors (after [23]).

Coupling resistance R_{Si} associated with the Si substrate (see Figure 6(c)) also degrades the inductor performance. A simple model to describe the substrate resistance is given by [11]

$$R_{Si} = \frac{2}{l \cdot \mathrm{w} \cdot G_{sub}} \tag{14}$$

where l is total length of all line segments, G_{sub} is the conductance per unit area of the substrate.



(a) (b)

Figure 9 (a) Model with improved series resistance (dashed line box) developed by Melendy et al. and (b) resistances measured and simulated from the conventional model and improved model with one and two R/L loops in the dashed line box (after [24]).

2.1.3 Capacitances

There are basically three types of capacitances in an on-chip inductor: the series capacitance C_S between metal lines, the oxide capacitance C_{OX} associated with the oxide layer, and the coupling capacitance C_{Si} associated with the Si substrate. Traditionally, they are modeled using the parallel-plate capacitance concept [11]:

$$C_s = n \cdot \mathrm{w}^2 \cdot \frac{\varepsilon_{ox}}{t_{oxM1-M2}} \tag{15}$$

$$C_{ox} = \frac{1}{2} \cdot l_T \cdot \mathrm{w} \cdot \frac{\varepsilon_{ox}}{t_{ox}} \tag{16}$$

$$C_{Si} = \frac{1}{2} \cdot l_T \cdot \mathrm{w} \cdot C_{sub} \tag{17}$$

where n is the number of overlaps, w is the spiral line width, C_{sub} is the capacitance of the substrate, t_{ox} is the oxide thickness underneath the metal, and $t_{oxM1\text{-}M2}$ is the oxide thickness between the spiral. An improved method [26], which evaluates the voltage and energy stored in each turn, leads to the equivalent capacitances of C_p and C_{sub}, as shown in Figure 10. Compared to the model in Figure 6(c), C_p and $\mathrm{C_{sub}}$ in this model are equivalent to C_S and the combination of C_{ox} and C_{Si}, respectively,

$$C_p = \sum_{k=1}^{n-1} \frac{1}{4} C_{mm} l_k \left[d(k+1) - d(k-1) \right]^2 \tag{18}$$

$$C_{sub} = \sum_{k=1}^{n} \frac{1}{4} C_{ms} A_k \left[2 - d(k-1) - d(k) \right]^2 \tag{19}$$

$$d(k) \equiv h_1 + h_2 + \cdots h_{k-1} + h_k \tag{20}$$

$$h_k = (l_k / l_T) \tag{21}$$

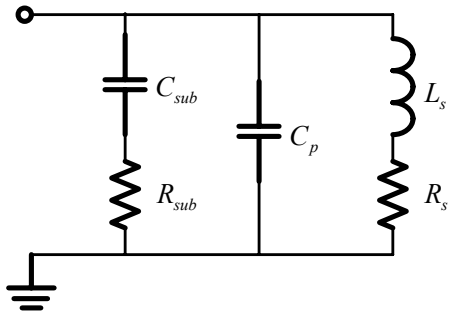


Figure 10 Equivalent circuit of spiral inductor developed by Wu et al. [26].

where C_{ms} represents the capacitance per unit area between the m^{th} metal layer and the substrate, C_{mm} represents the capacitance per unit length between adjacent metal tracks, A_k is the track area of k^{th} turn and l_k is the length of kth turn. The model also implies that C_S is a function of the index difference of each adjacent segment pair. This means that the larger the index difference between the two adjacent lines, the higher the capacitance [27]. This concept can be used to improve the inductor structure to be discussed in Section III.

2.1.4 Q Factor and Substrate Loss

The quality factor Q is an extremely important figure of merit for the inductor at high frequencies. For an inductor, only the energy stored in the magnetic field is of interest, and the quality factor is defined as [28]

$$Q = 2\pi \cdot \left(\frac{Peak\ Magnetic\ Energy - Peak\ Electric\ Energy}{Energy\ Loss\ in\ One\ Oscillation\ Cycle} \right) \tag{22}$$

Basically, it describes how good an inductor can work as an energy-storage element. In the ideal case, inductance is pure energy-storage element (Q approaches infinity), while in reality parasitic resistance and capacitance reduce Q. This is because the parasitic resistance consumes stored energy, and the parasitic capacitance reduces inductivity (the inductor can even become capacitive at high frequencies). Self-resonant frequency f_{SR} marks the point where the inductor turns to capacitive and, obviously, the larger the parasitic capacitance, the lower the f_{SR}.

If the inductor has one terminal grounded, as in typical applications, then the equivalent circuit of the inductor can be reduced to that shown in Figure 11. From such a model, the quality factor Q of the inductor can be derived as [28]:

$$\begin{aligned} Q &= \frac{\omega L_s}{R_s} \cdot \frac{R_p}{R_p + \left[\left(\omega L_s / R_s \right)^2 + 1 \right] R_s} \cdot \left[1 - \frac{R_s^2 \left(C_s + C_p \right)}{L_s} - \omega^2 L_s \left(C_s + C_p \right) \right] \\ &= \frac{\omega L_s}{R_s} \cdot Substrate\ Loss\ Factor \cdot Self\ Resonance\ Factor \end{aligned} \tag{23}$$

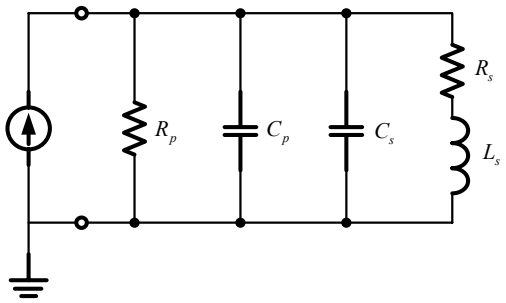


Figure 11 Equivalent circuit of one terminal grounded inductor for modeling the Q factor.

where ω is the radian frequency, L_S is the series inductance, R_S is the series resistance, R_P is the coupling resistance, and C_P is the coupling capacitance. R_P and C_P in Figure 11 are related to R_{Si}, C_{Si}, and C_{OX} in the model in Figure 6(c) as

$$C_p = C_{ox} \cdot \frac{1+\omega^2\left(C_{ox}+C_{Si}\right)C_{Si}R_{Si}^2}{1+\omega^2\left(C_{ox}+C_{Si}\right)^2 R_{Si}^2} \tag{25}$$

Note that Q increases with increasing L_S and with decreasing R_S. Moreover, it appears from (23) that Q should increase monotonically with the frequency. This is not the case, however, as the substrate loss becomes a dominant factor for Q at high frequencies. The last two terms on the right-hand side of (23) denote the substrate loss factor and self-resonant factor. On-chip inductors are normally built on a conductive Si substrate, and the substrate loss is due mainly to the capacitive and inductive coupling [7]. The capacitive coupling (represented by C_P in the model in Figure 11) from the metal layer to the substrate changes the substrate potential and induces the displacement current. The inductive coupling is formed due to time-varying magnetic fields

penetrating the substrate, and such a coupling induces the eddy current flow in the substrate. Both the displacement and eddy currents give rise to the substrate loss and thereby degrade the inductor performance. Figure 12 illustrates schematically the eddy and displacement currents in the substrate induced magnetically and electrically, respectively, by the current flow in the inductor spiral.

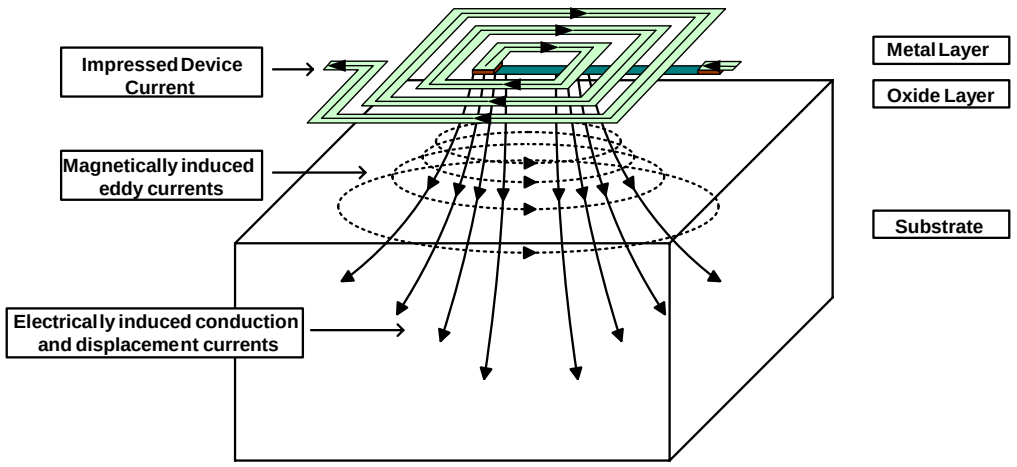
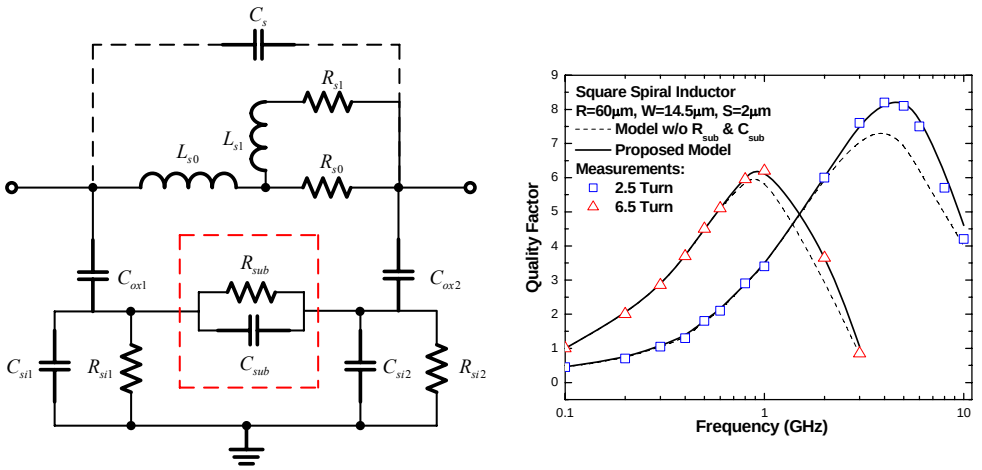


Figure 12 Eddy and displacement currents in the substrate induced by the current flow in inductor spiral.

An important conclusion can be drawn from (23), that is when R_P approaches infinity, the substrate loss factor approaches unity. Since R_P approaches infinity when R_{Si} goes to zero or infinity, Q can be improved by making the silicon substrate either a short or an open [28].

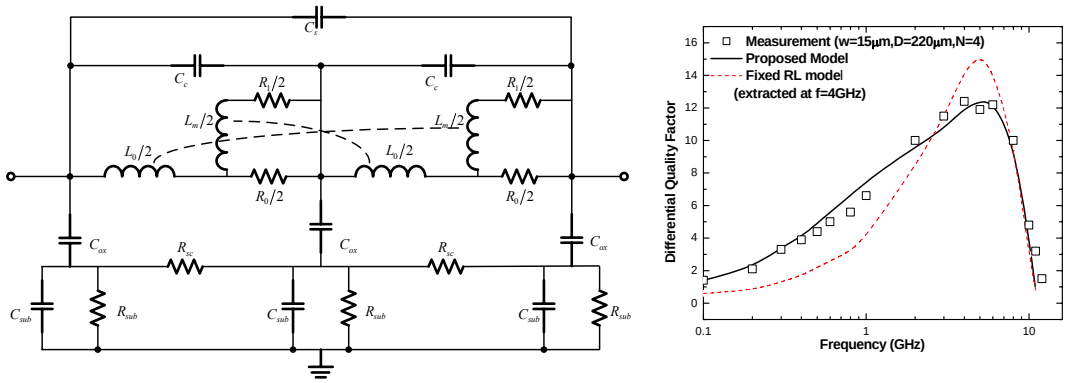
2.1.5 Modified π Models

Some studies have been conducted to improve the accuracy of the simple lumped models shown in Figure 6. Gil and Shin [29] modified the simple π model by adding the horizontally coupled substrate resistor and capacitor, and the equivalent circuit and results of Q factor are given in Figures. 13(a) and (b). Cao et al. [19] proposed a double π model to account for the frequency-dependant resistance and inductance, in which the frequency-independent resistance components follow the square-law relationship suggested in [21]-[22] and the frequency-independent inductance components are derived based on mutual inductances and calculated from empirical equations. The equivalent circuit and model results are given in Figures. 14(a) and (b). Lakdawala et al. [30], on the other hand, used an RLC laddered network to describe the frequency-dependent resistance and inductance, as shown in Figure 15(a). The measured and calculated Q factors of conventional and micromachined inductors are given in Figure 15(b). The models in Figures. 8(a) and Figure 9(a) could also yield good predictions for Q, and the results are shown in Figures. 16(a) and (b), respectively.



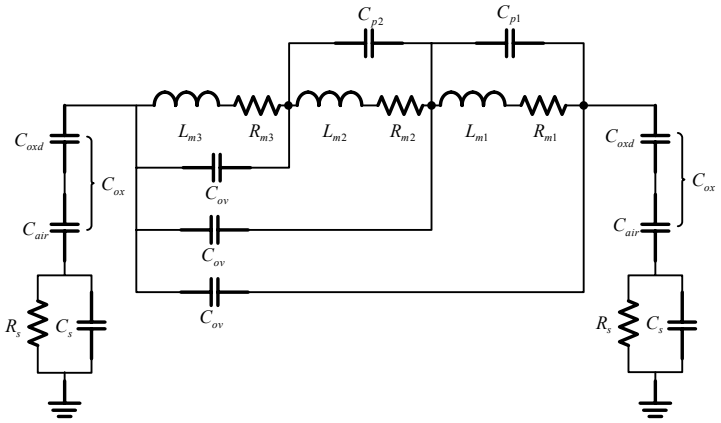
(a) (b)

Figure 13(a) Improved inductor model with horizontally coupled resistance and capacitance (R_{sub} and C_{sub}) and (b) Q factors measured and simulated with and without R_{sub} and C_{sub} (after [29]).

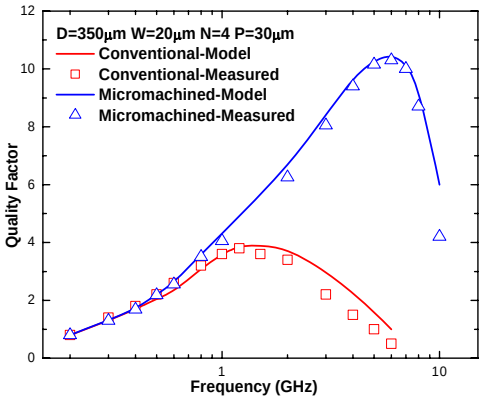


(a) (b)

Figure 14(a) Improved double π model to more accurately account for the frequency-dependent series resistance and inductance and (b) Q factors measured and simulated from the conventional and improved models (after [19]).

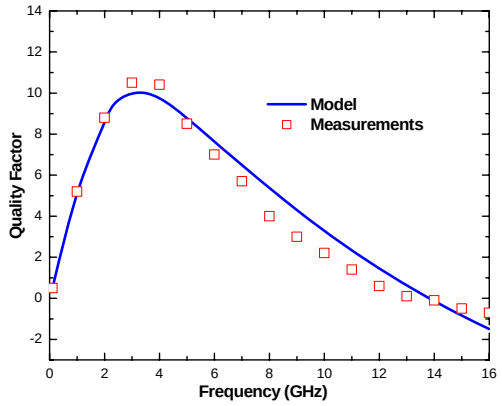


(a)

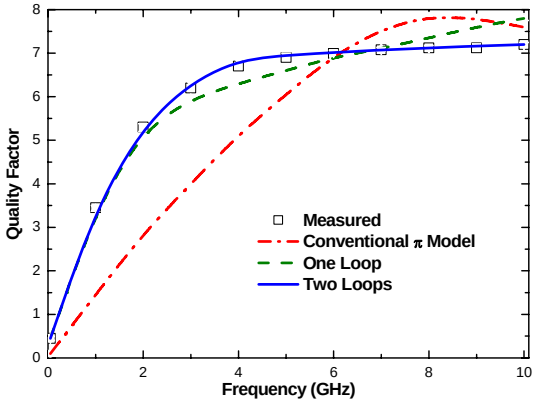


(b)

Figure 15(a) Modified π model with RLC laddered network and (b) Q factors measured and calculated from the modified model (after [30]).



(a)



(b)

Figure 16(a) Quality factors measured and calculated from model in Figure 7(a); (b) Inductances and quality factors measured and calculated from model in Figure 8(a).

2.2 Advanced Structures

The preceding section has addressed the design concept and modeling of a typical square shaped spiral inductor. The performance of such an inductor can be improved with the following advanced structures.

2.2.1 Structures to Reduce Substrate Loss

(a) Ground Shield

As mentioned earlier, the substrate loss can be reduced with decreasing the substrate resistance R_{Si}. To achieve this, one can insert a metal or ploy-Si layer between the inductor and substrate, and connect this layer to the ground. This approach, called the ground shielding, reduces the effective distance between the spiral metal and ground and thereby reduces the substrate coupling resistance. Another purpose of the shield is that it can truncate the electric field in the substrate and thus reduce the noise. For a solid ground shield (SGS), however, the varying electromagnetic field in the inductor could induce the eddy current with the presence of ground plane, and the reflected image in the ground plane serves as a counteractive inductor [31]. Hence, it's necessary to pattern the shield to cut the eddy current loop [28], [32]. It has been found that poly-Si is a good material for the patterned ground shield (PGS). Chen et al. [33] reported the use of an n^+-diffusion Si patterned ground shield to improve the quality factor. Since the substrate current mainly concentrates at the Si-SiO_2 surface due to the proximity effect, the n^+-diffusion Si PGS can effectively break the current loop and thus eliminate the eddy current effect [34]. Figs. 17(a) and

(b) show a typical PGS and the results of quality factor Q with SGS and PGS. Clearly, the presence of PGS improves Q considerably.

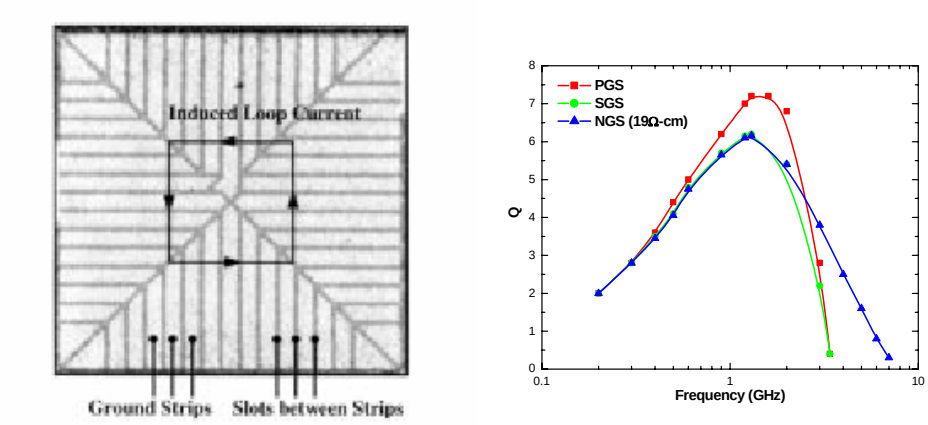


Figure 17(a) Schematic of patterned ground shield (PGS) and (b) quality factors of solid ground shield (SGS), PGS, and no ground shield (NGS) (after [28]).

The most significant drawback of ground shielding is the fact that it reduces the distance between inductor and ground and thereby introduces additional capacitance. This effect may sometimes adversely decrease the quality factor of ground-shielding inductors [35].

(b) Substrate Removal

Another way to enhance Q is to increase the substrate resistance. In order to elevate R_{Si} to approaching infinity, one idea is to use insulator as substrate. Quartz or glass shows better Q and higher self-resonant frequency than Si [35]. For Si technology, however, it is not possible to use a high resistive substrate as an effective RF ground, and via contacts through the chip to define RF

grounds on both the chip front side and back side is usually not available. In other words, for CMOS-based on-chip inductors, we cannot avoid using a low resistive Si substrate. Nonetheless, instead of building the whole circuit on a low resistive substrate, we can make a region with high resistivity for placing the inductor [36]. This can be accomplished by using the proton implantation, and Chan et al. [36] achieved a 7% higher self-resonant frequency and 61% higher Q through this approach.

Researchers have come up with other novel ideas to keep the inductor away from substrate so that substrate coupling and loss can be greatly reduced. Using an advanced micromachinary process, an inductor can be built above the silicon surface [30], [37]-[38], as shown in Figs. 18 and 19, or the silicon underneath the inductor can be removed using the deep-trench technology [39], as shown in Figure 20.

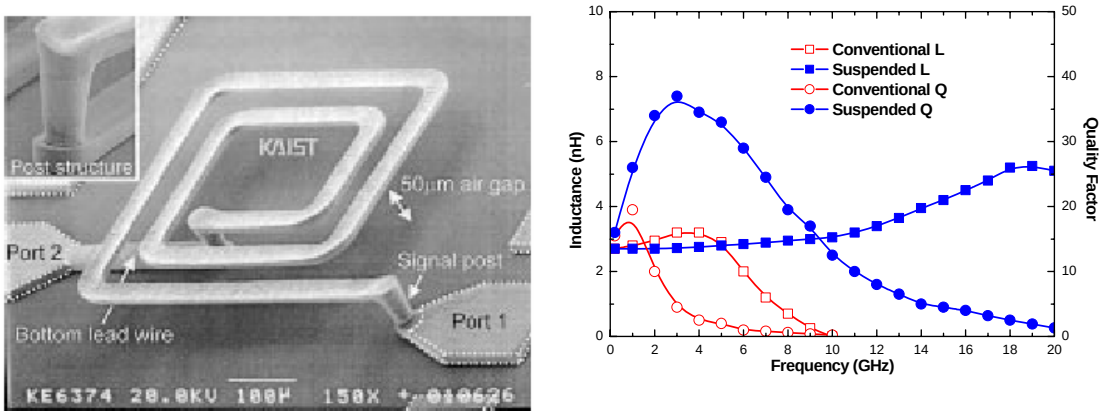


Figure 18(a) Topology of the suspended inductor and (b) comparison of inductances and Q factors of conventional and suspended inductors (after [37]).

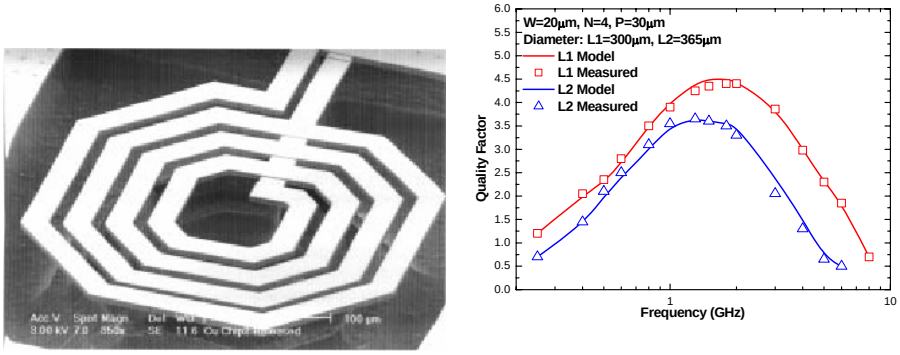


Figure 19(a) Topology of the micromachined inductor and (b) Q factors of such an inductor with two different diameters (after [30]).

(c) Horizontal Inductors

An alternative way to reduce magnetic field coupling to substrate is to have the magnetic field parallel to the substrate. To this end, research works have been done to fabricate horizontal inductors with multilayer of interconnects [40]-[41]. Using this layout, the magnetic field is parallel to the substrate surface and the magnetic coupling to the substrate is minimal. This structure nevertheless gives rise to an increased in the coupling capacitance. Since a large metal is needed for the bottom layer of the horizontal inductor, the inductor-substrate capacitance increases tremendously if the inductor is on silicon. Again, researchers tried to use high resistive substrate [41], suspend the inductor in air [42], or even rectify the inductor with the so-called plastic deformation magnetic assembly (PDMA) [43]. Figs. 21(a) and (b) show the topology and performance of a horizontal inductor using the PDMA.

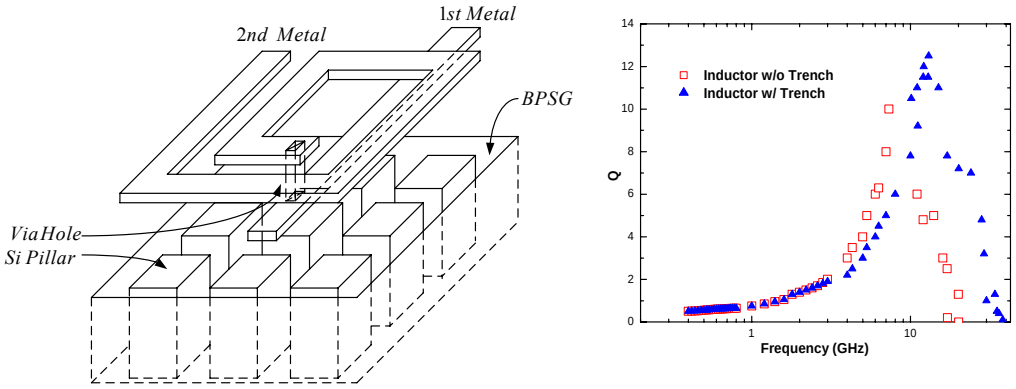


Figure 20(a) Inductor with substrate removed by a deep trench technology and (b) Q factors of conventional and trenched inductors (after [39]).

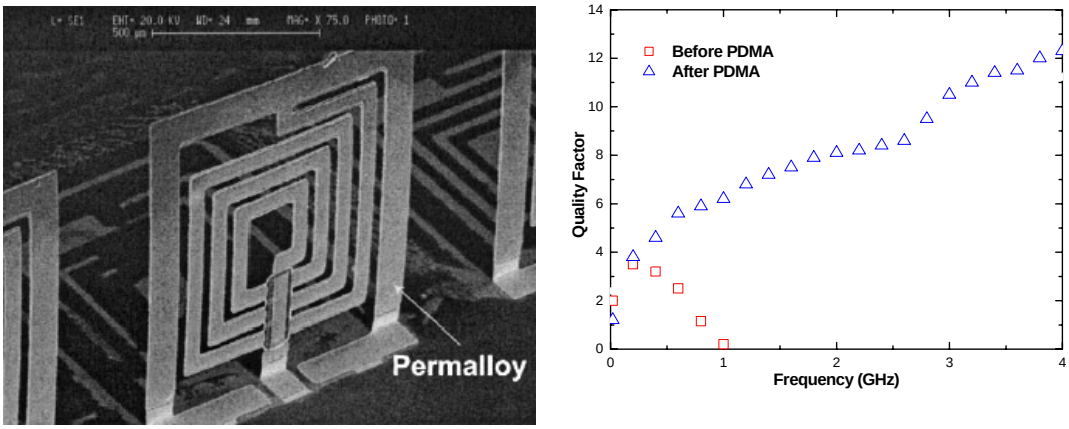


Figure 21(a) Topology of the horizontal inductor based on the PDMA process and (b) Q factors of conventional and horizontal inductors (after [43]).

2.2.2 Structures to Reduce Series Resistance

Metal resistivity gives rise to the series resistance R_S, and it is always desired to reduce the resistance in order to improve the quality factor. One simple idea is to increase the line width. This method may work at low frequencies where the current density in a wire is uniform; however, as the frequency increases, the skin effect pushes the more current to the outer cross section of the metal wire and the so-called skin depth (i.e., the depth in which the current flows) is reduced with increasing frequency (see Eq. (12)). Thus, the skin effect increases the series resistance at high frequencies, and the approach of increasing the line width would not be effective. According to an earlier study, the larger the cross section, the lower the onset frequency at which the skin effect dominates the series resistance. Furthermore, a wider metal line would occupy more area, which increases the fabrication cost. Several possible solutions to this problem are given below.

(a) Vertical Shunt

In this approach, the inductor is made of multiple metal layers and the neighboring metal layers are shunted through via arrays, so the effective thickness of the spiral inductor is increased, the skin effect is weakened, and the series resistance is reduced. A detailed study and comparison on the multilayer inductors are presented in [44]. The inductors are fabricated with multiple metal layers (M1 to M4), and these layers can be shunted through via arrays, as shown in Figure 22(a) for the case of shunting M2, M3 and M4. The results in Figure 22(b) show a reduced series resistance and thus an improved *Q* as the number of shunts is increased (i.e., the case of M3 has no vertical shunt). The performance of the inductor is therefore optimized with the increment of total metal thickness without occupying more area. One important aspect the inductor in Figure 22 did not address is

that the inductor may experience a lower self-resonant frequency with the utilization of lower metal layers. This is because 1) the reduction of metal-substrate distance could cause a significant increase in C_{ox}, and 2) the capacitance among the metal lines would also increase.

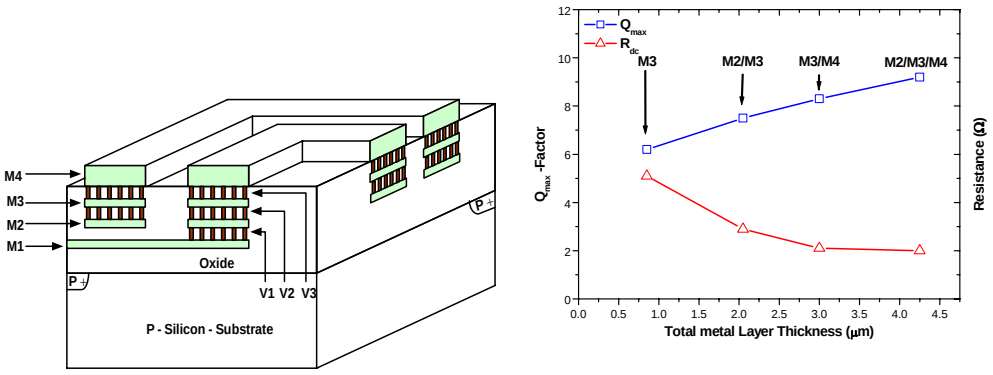


Figure 22(a) Inductor with multiple metal layers and vertical shunt and (b) maximum Q factors and resistances for the inductor having different numbers of vertical shunt (after [44]).

(b) Horizontal Shunt

Instead of shunting vertically, the spiral inductor can be split into several shunting current paths, each with an identical resistance and inductance. This approach, called the horizontal shunt, can suppress the current crowding and increase the Q factor [45]. Figs. 23(a) and (b) show such an inductor and its Q factor, respectively. It is shown that for the same line width, the Q factor increases with increasing number of splits.

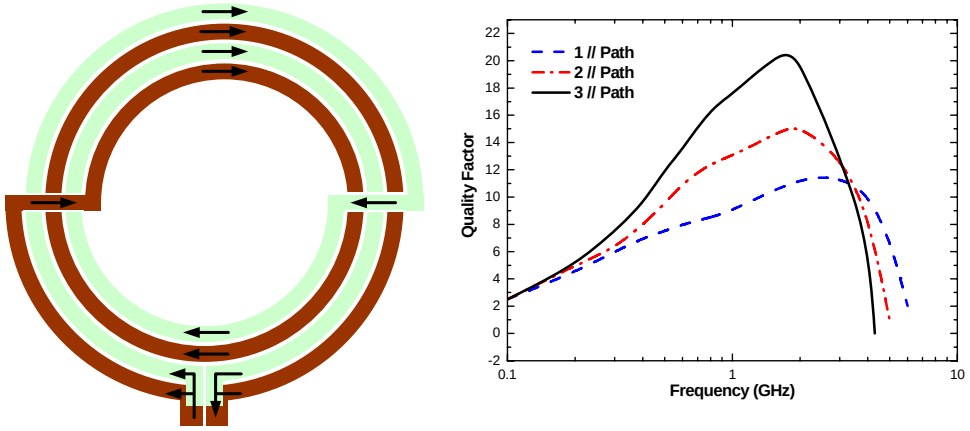


Figure 23(a) Inductor with metal line split into shunt current paths and (b) Q factors of horizontally shunt inductor with one, two, and three splits in the metal line (after [45]).

(c) Line Width Optimization

For inductors fabricated with a constant line width, the influence of magnetically induced losses is much more significant in the inner turns of the spiral, where the magnetic field reaches its maximum. To avoid this effect, one method is to employ the so-called tapered inductor, in which the line width decreases toward the center of the spiral [46], as shown in Figure 24(a). A reduced series resistance can also be achieved from this approach. Detailed study was performed in [47] regarding the optimization of line width in order to enhance the RF performance. The frequency- and position-dependent optimum width W_{opt} is given by:

$$W_{opt,n} = \sqrt[3]{\frac{r_s(f)}{2 \cdot C \cdot g_n^2 \cdot f^2}} \qquad (26)$$

where $r_s(f)$ is the sheet resistance of the metal strip, f is the frequency, C is a fitting constant, and g_n is a geometric dependent parameter. As can be seen in Figure 24(b), the Q factor of a spiral inductor is much improved when the line width is not uniform and is optimized.

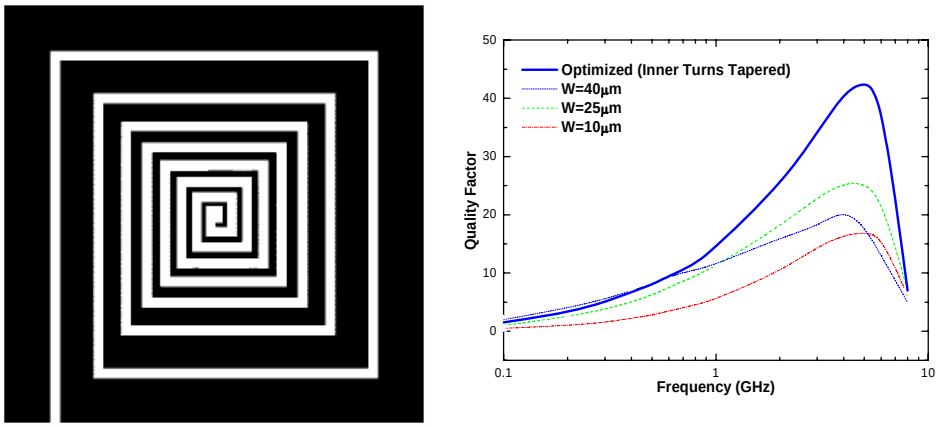


Figure 24(a) Topology of a tapered inductor and (b) Q factors of a tapered inductor and three non-tapered inductors (after [47]).

2.2.3 Structures to Increase Inductance

Since the quality factor is directly proportional to the series inductance, approaches to increase the inductance have also been suggested for on-chip inductor performance enhancement.

(a) Stacked Inductor

A stacked inductor is a set of series inductors made from different metal layers, as illustrated in the schematic in Figure 25(a). This method maximizes the inductance per unit area. It has been reported that a 10 nH inductor can be achieved with an area of 22 μm × 23 μm, as opposed to several hundreds μm by several hundreds μm for regular inductors [48]. This is the main advantage

that this technology can offer. Shortcomings are relatively low Q factor and self-resonant frequency, due to the increased substrate capacitance and line to line coupling capacitance. The Q factor and inductance of such an inductor are illustrated in Figure 25(b).

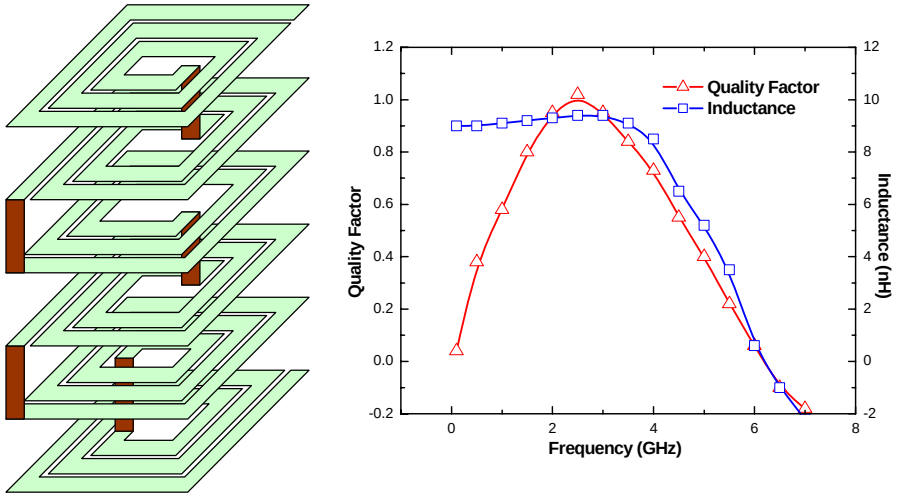


Figure 25(a) Stacked inductor with six metal layers and (b) Q factor and inductance of the stacked inductor (after [48]).

(b) Miniature 3-D Inductor

A high-performance stack-like inductor, called the miniature 3-D inductor, was proposed in [49]. Figure 26(a) shows such an inductor, which consists of at least two or more stacked inductors by series connections, and every stacked inductor has only one turn in every metal layer. The miniature inductor, while quite complicated, possesses a minimal coupling capacitance. This leads to a much higher self-resonant frequency and a wider frequency range for high quality factor.

Comparisons of capacitances and Q factors obtained from this inductor and a typical stacked inductor are given in Figs. 26(b) and (c), respectively.

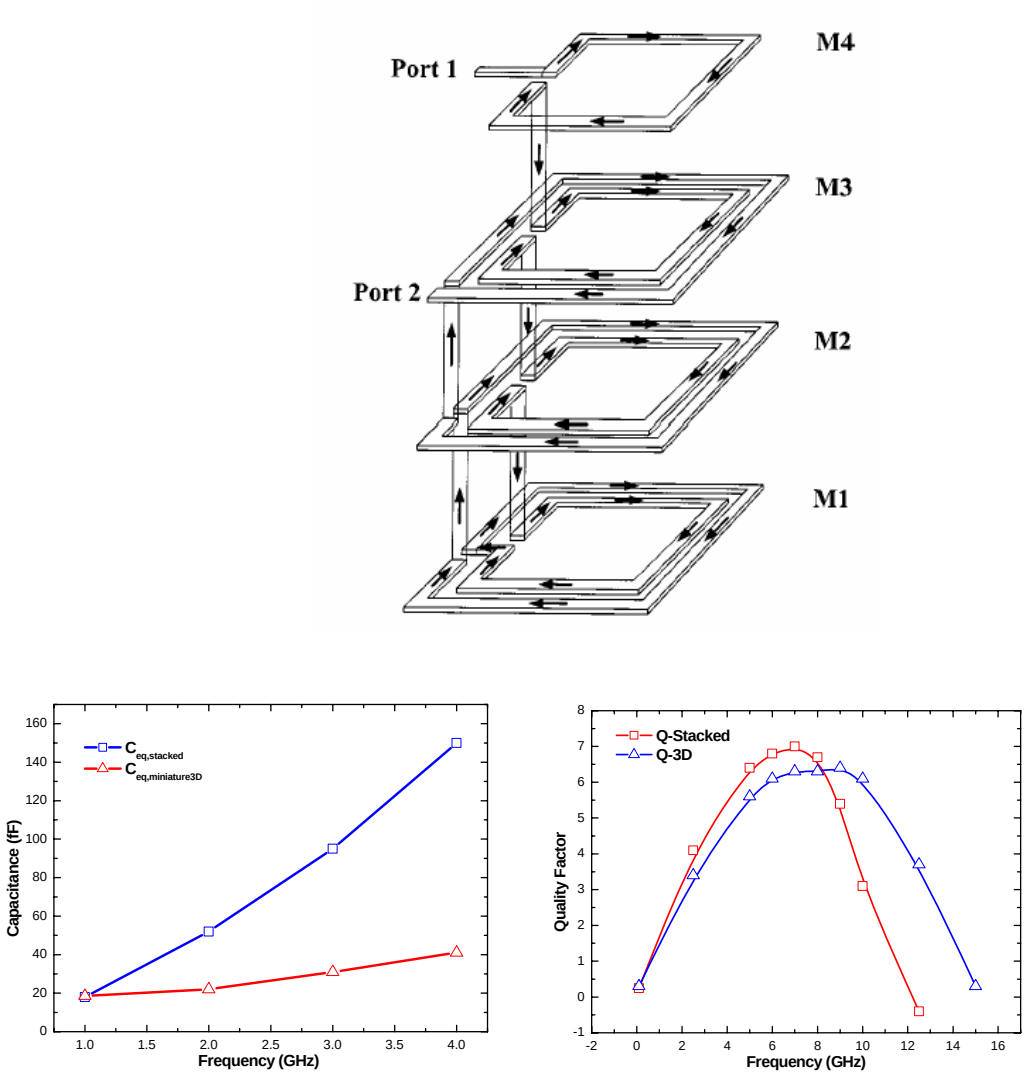


Figure 26(a) Structure of the miniature 3-D inductor, (b) capacitances of typical stacked and 3-D inductors, and (c) Q factors of typical stacked and 3-D inductors (after [49]).

2.2.4 Symmetrical Inductor

Traditionally, the winding of an inductor spiral starts from the outer turn to inner turn and then goes back out through an underpass. This is called the non-symmetrical inductor, as shown in Figure 27(a). An improved structure with a symmetrical winding, called the symmetrical inductor shown in Figure 27(b), will yield better performances [50]. This is because in the symmetrical inductor the geometric center of the symmetrical inductor is exactly the magnetic and electric center, which increases the mutual inductance and consequently the total inductance. Performances of the symmetrical and non-symmetrical inductors are illustrated in Figs. 28(a), (b) and (c). While the Q factor and series resistance of the symmetrical inductor are improved, the self-resonant frequency (i.e., frequency at which the inductance is zero) of such an inductor is reduced. This is due to an increased ac potential difference between the neighboring turns in the symmetrical inductor, a mechanism that increases the coupling capacitance and degrades the self-resonant frequency [26].

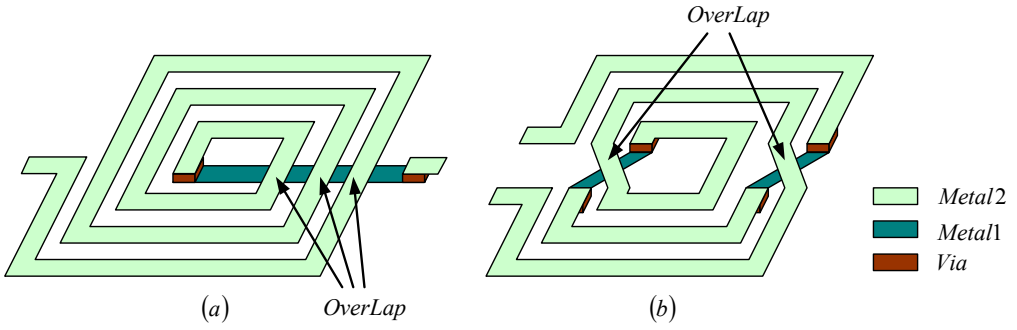


Figure 27 Spiral pattern of (a) non-symmetrical inductor and (b) symmetrical inductor.

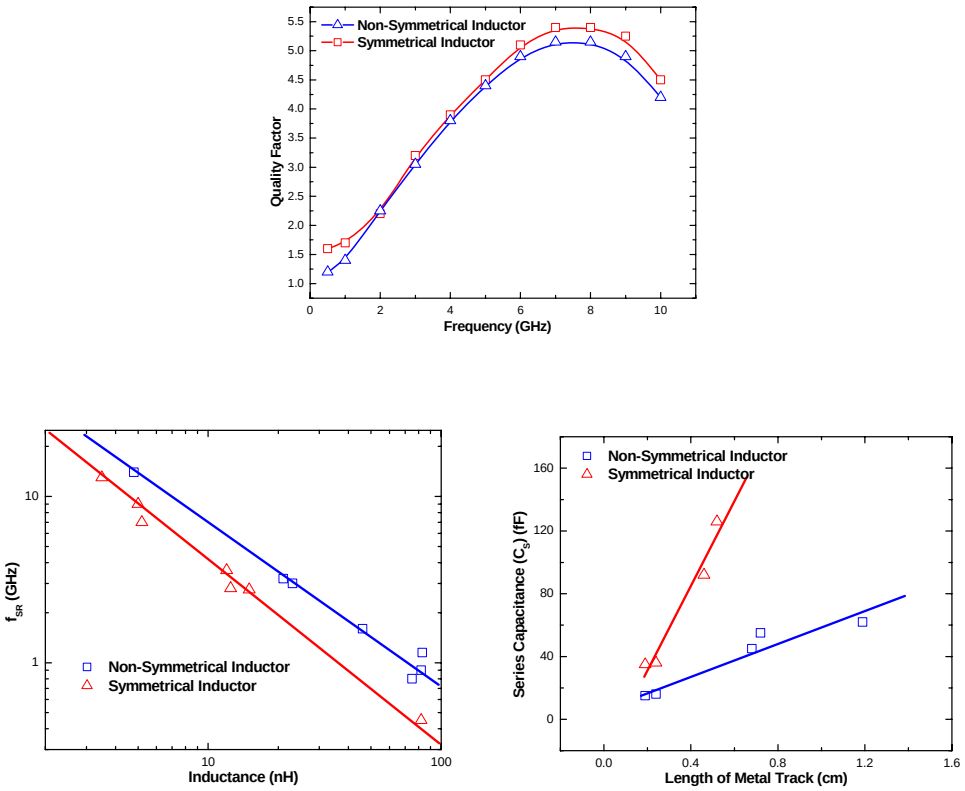
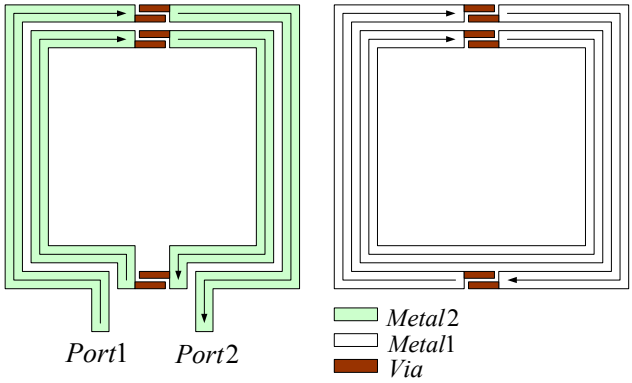
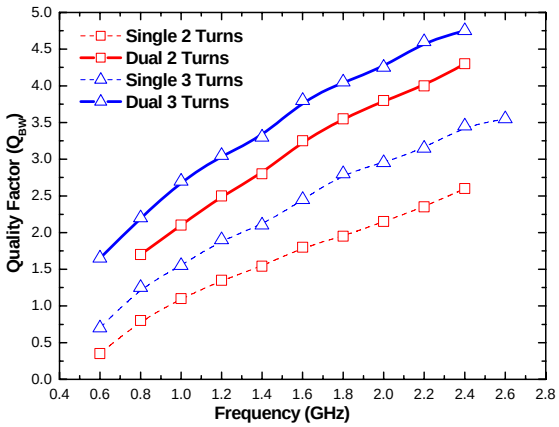


Figure 28 Comparison of (a) Q factor [50], (b) self-resonant frequency [27], and (c) capacitance [27] of non-symmetrical and symmetrical inductors.

The symmetrical inductor can be further enhanced with a dual-layer structure, as shown in Figure 29(a) [51]. The results in Figure 29(b) suggest that this structure possesses a much higher Q factor over its single-layer counterpart.



(a)



(b)

Figure 29(a) Structure of the dual-layer symmetrical inductor and (b) Q factors of single and dual-layer symmetrical inductors (after [51]).

2.2.5 Alternative Patterns

The preceding discussions have focused mainly on square shaped spiral inductors. As mentioned earlier, while the circular shaped inductor yields better performance, such a pattern is more difficult to realize than its square counterpart. On the other hand, alternatives like the hexagonal and octagonal patterns are more feasible and good compromises. For these inductors, as the number of sides is increased, less metal length is needed to achieve the same number of turns. Thus series resistance is compressed and Q factor improved. On the other hand, the square shaped inductor is more area efficient. For example, for a square area on the wafer, square shape utilizes 100% of the area, whereas hexagonal, octagonal and circular shapes use 65%, 82.8% and 78.5%, respectively. As a result, square inductor can accommodate more metal line, thus yielding a larger inductance, within the same square area.

Selection of the pattern shape is a compromise between quality factor and area. Mohan [15] studied inductors with different shapes having a fixed inductance of 5 nH. As shown in Figure 30, the quality factor is improved with increasing number of sides (note that circular pattern can be considered as having infinite number of sides). The study further suggested that an octagonal spiral inductor suffers a 3~5% lower Q factor but achieves a 3~5% smaller effective chip area than the circular spiral inductor [15].

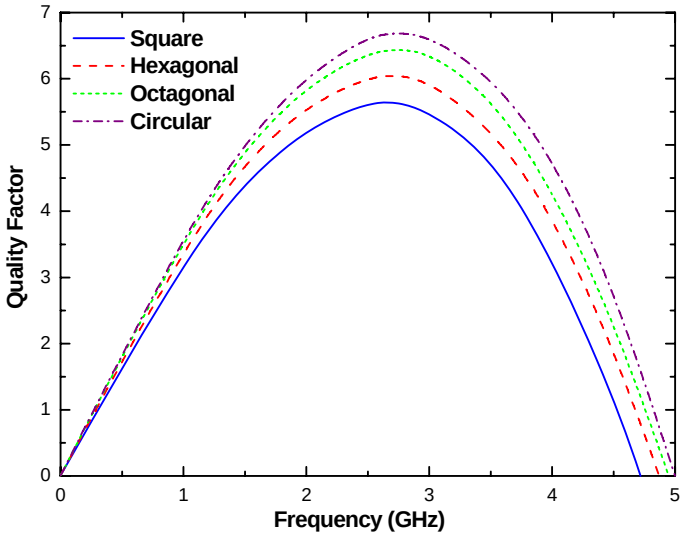


Figure 30 Q factors of different shaped inductors with a fixed inductance of 5 nH (after [15]).

The quality factor and inductance of square and octagonal shaped inductors having the same inner diameter are compared in Figs. 31(a) and (b) [52]. The square inductor possesses a higher peak inductance but a lower self-resonant frequency. This is because the longer metal line of square inductor induces a larger metal to substrate coupling capacitance, which reduces the inductance at high frequencies. For low frequencies, the inductor performance depends mainly on the length of the spiral wire, and the square pattern possesses a larger inductance in this region. Experiments of other research works also indicated an up to 10% resistance reduction of circular and octagonal inductor over the square inductor with the same inductance [8], as illustrated in Figure 32.

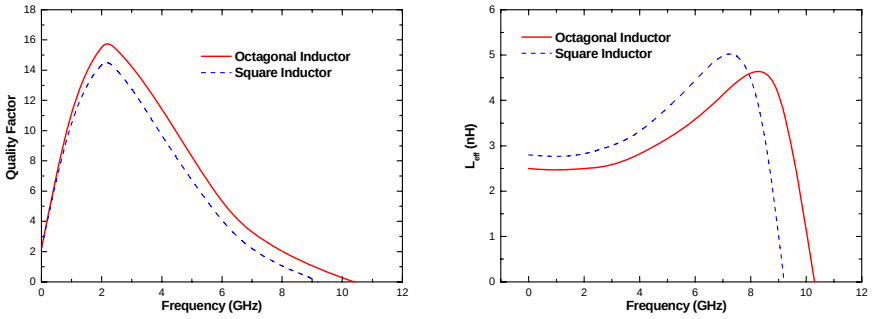


Figure 31(a) Q factor and (b) inductance of octagonal and square inductors having the same inner-diameter of 100 μm, number of turns of 3.5, and line width of 6 μm (after [52]).

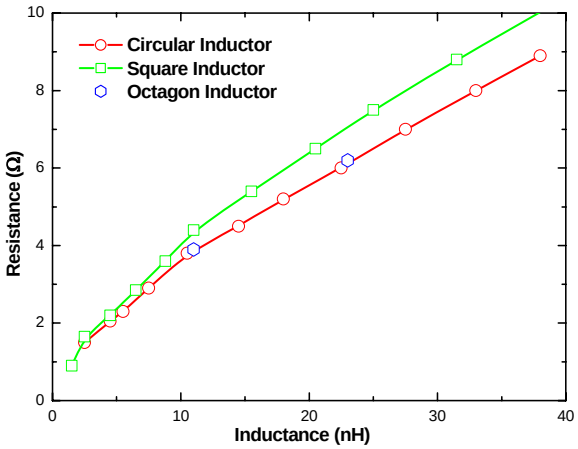


Figure 32 Resistance comparison on square, octagon and circular inductors

The dynamic growth in RF electronics has demanded and vitalized the need of high-performance on-chip passive components. One of these components, the on-chip spiral inductor, has been considered and reviewed in this chapter. Many aspects of the design and modeling of the on-chip inductor have been presented, and their impacts on RF performance addressed. It is demonstrated that while it is cost effective and technology reliable to fabricate such devices on Si substrate, the conductive nature of Si material gives rise to a large substrate loss and consequently relatively poor RF performance. The spiral pattern and geometry can also be optimized to enhance the quality factor, but these alternatives often come with trade-offs or compromises. This work should provide a useful and sufficient breath to researchers and engineers who are interested in the design and development of RF IC's involving passive components.

CHAPTER THREE: MODELING METHODOLOGY

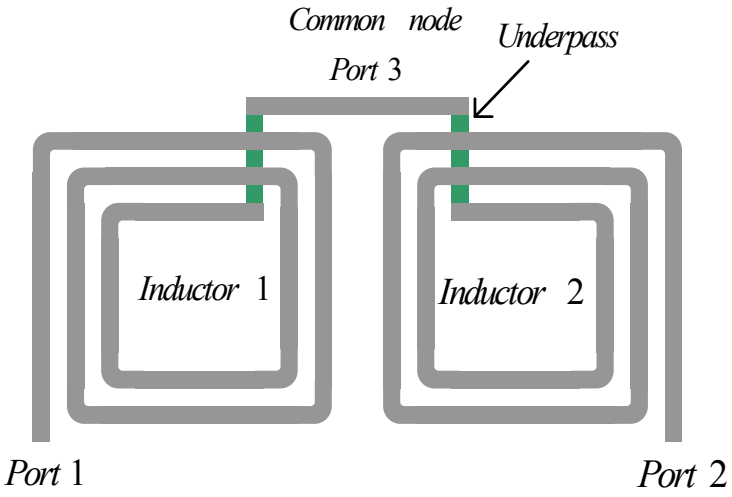
Recent growth in RF applications has increased the use of spiral inductors and thus demanded a more accurate model for such devices. In this dissertation, we focus on the model development of spiral inductors with symmetrical and asymmetrical terminals. Relevant and important physics such as the current crowding in metal line, frequency-dependent permittivity in oxide, and overlap parasitics are accounted for. Experimental data and results calculated from the existing inductor models are included in support of the model development.

3.1 Introduction

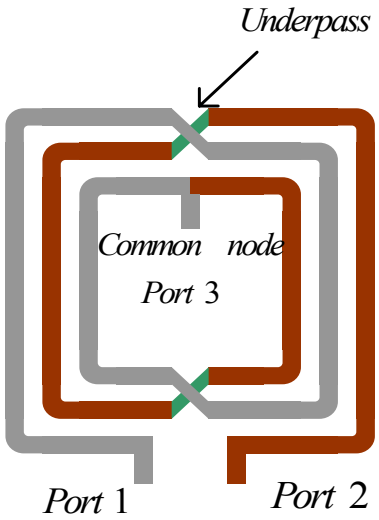
Wireless communications is already part of our daily life. To reduce the cost of monolithic microwave integrated circuits (MMICs), passive devices are frequently integrated with active components on the same chip. Spiral inductors are particularly important and widely used in MMICs such as low-noise amplifiers, oscillators, and mixers [8].

Spiral inductors with asymmetrical and symmetrical terminals have been used in RF IC's, and their configurations for the widely used differential driven applications are shown in Figs. 1(a) and (b), respectively. For such applications, the symmetrical inductor yields better performance [53]. This is due to the presence of a shorter underpass metal line and smaller number of overlaps in the symmetrical inductor, which decrease the capacitance and consequently improve the quality factor

(Q factor) of the inductor [50]. In addition, the symmetrical inductor occupies a smaller chip area than its asymmetrical counterpart [53].



(a)



(b)

Figure 33 Schematic of (a) asymmetrical inductor and (b) symmetrical inductor with a square pattern for differential driven applications

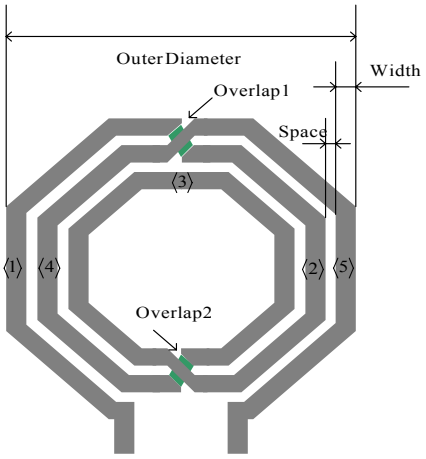
Many spiral inductors models have been reported in the literature [15][9][11], and all these models were developed intended for asymmetrical inductors but nonetheless sometimes used for symmetrical inductors. To the best of our knowledge, an accurate and compact symmetrical inductor model is not yet available and urgently needed. Empirical technique based on curve fitting for symmetrical inductors has been reported in [16], but models derived this way cannot be scaled to reflect changes in the inductor's layout or fabrication technology and cannot be implemented into a circuit simulator. Commercial electromagnetic field solver may also be used to predict the inductor's performance accurately, but the computation time can be too extensive to be practical.

In this paper, a physics-based model applicable for both symmetrical and asymmetrical inductors will be developed. Model development and the proposed equivalent circuit for symmetrical inductors will first be given in Section II. This is followed by the model development of asymmetrical inductors in Section III. In Section IV, results obtained from the present model, existing models, and measurements are compared. Finally, conclusions are given in Section V.

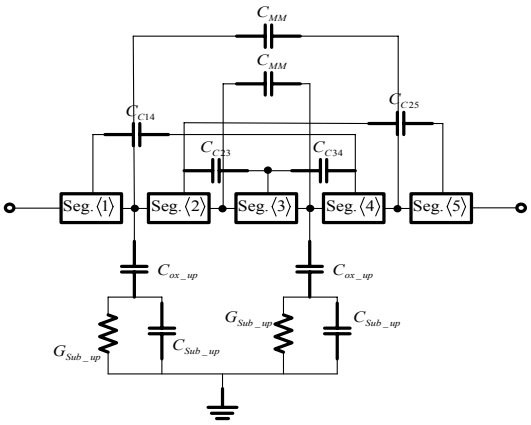
3.2 Model Development of Symmetrical Inductor

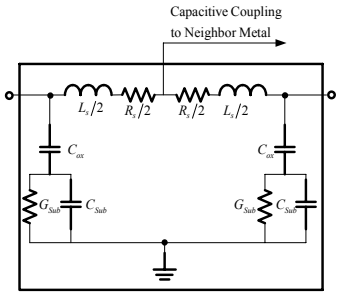
Our model development will first focus on symmetrical inductors. In addition, an octagonal spiral pattern will be considered, but the approach applies generally to other non-circular patterns. It has been suggested that the octagonal spiral provides a higher Q factor and lower series resistance than

the square pattern [8] and is more area efficient and easier realized than the circular spiral [15]. The consideration of the octagonal in fact makes the model more comprehensive than most existing models which consider only square or hexagonal patterns.



(a)





(b) (c)

Figure 34 (a) Schematic of an octagon symmetrical inductor with 3 turns, (b) overall equivalent circuit for the inductor including segmental and overlap components, and (c) equivalent circuit for the segment in (b).

Figure 34(a) shows a symmetrical, octagon spiral inductor with 3 turns. For such an inductor, the metal track can be divided into 5 segments and 2 overlaps (see Figure 34(a)), and the improved equivalent circuit for the inductor is given in Figure 34(b). In Figure 34(b), each segment box is represented by a lumped model shown in Figure 34(c). In addition, coupling capacitances between the metal lines and parasitics associated with the overlaps need to be considered. These are accounted for with all the other components besides the segment boxes in Figure 34(b), where $C_{C,ij}$ is the coupling capacitance between two particular metal lines i and j, C_{mm} represents the capacitance associated with the overlap, C_{ox_up} and C_{sub_up} model the capacitances associated with the oxide and substrate of the underpass metal, respectively, and G_{sub_up} models the substrate conductance of the underpass metal. Note that there are two sets of the overlap parasitic components, and the subscripts 1 and 2 denote the components pertinent to overlaps 1 and 2, respectively. It is worth mentioning that the lumped equivalent circuit in Figure 34(c) is the sole framework used in the conventional modeling of spiral inductors. The improved version suggested in Figure 34(b) allows for the inclusion of the distributed nature of the spiral inductor and thus an increase in the model accuracy.

We want to point out that horizontal coupling in the substrate (horizontal coupling underneath the adjacent metal lines in the substrate) may affect the inductor performance, but such an effect is rarely included in the inductor compact modeling because of the complexity associated with its distributed nature. To the best of our knowledge, only the work by Gil and Shin [29] included the horizontal substrate coupling, but the model considered only the lump components for the horizontal substrate coupling, and all the model parameters were obtained from fitting schemes. To keep the present model compact and the parameters physics-based, this coupling effect will not

be considered. The eddy current is another mechanism for substrate loss. However, a recent work [19] has suggested that the loss due to eddy current is negligible in a relatively low conductive substrate with a resistivity larger than 10 Ω-cm. Because all the inductors considered in our work have a substrate resistivity of larger than 15 Ω-cm, such an effect will be neglected in this work.

3.2.1 Nonuniform Current Distribution in Metal Lines

A difficult issue in modeling the spiral inductor is the fact that the current distribution in a metal line is not uniform and is a strong function of its location and operating frequency. Such a nonuniform current distribution is an important mechanism affecting the inductor performance. Traditionally, the current density in a metal line is considered to be governed by the skin and proximity effects [19]. It is more realistic, however, to consider the subject metal line lies in midst of electromagnetic field generated by all the other metal lines. According to the partial-element-equivalent-circuit (PEEC) simulation [54] and 3-D electromagnetic simulation [55], the current distribution in a metal line in general exhibits an exponential decay from the inner edge (side of metal line closer to the center of spiral) to the outer edge (side of metal line farther away from the center of spiral). Furthermore, this exponential-decay distribution is more prominent in the inner turns (i.e., segments 2, 3, and 4) and as the frequency is increased. Figure 35 shows the current density distributions in segments 1, 4, and 3 (circled in Figure 35) simulated from an EM simulator. The frequency and location dependencies of the current distribution in the metal lines are clearly illustrated.

We now introduce the concept of the effective line width W_{eff} in which the majority of the current density exists (the region where the first exponent of current density exists). Once W_{eff} is in place, then the nonuniform current distribution effect can be accounted for by replacing the physical line width in the model parameters with W_{eff}. The following expressions are proposed to describe the effective line width as a function of the frequency and the segment number:

$$w_{eff} = W_{0,i}\left(1-\exp\left(-\frac{w}{W_{0,i}}\right)\right) \tag{1}$$

$$W_{0,i} = c1\cdot c2^{i-1}\sqrt{\frac{1}{f}} \tag{2}$$

where w is the physical width of metal line, f is frequency in Hz, i is turn index (i.e., for segments 1 and 5, i=1; segments 2 and 4, i=2; segments 3, i=3), and $c1$ and $c2$ are fitting parameters to make the inductance and resistance match with measurements. A systematic method to determine the values of $c1$ and $c2$ will be developed and discussed later.

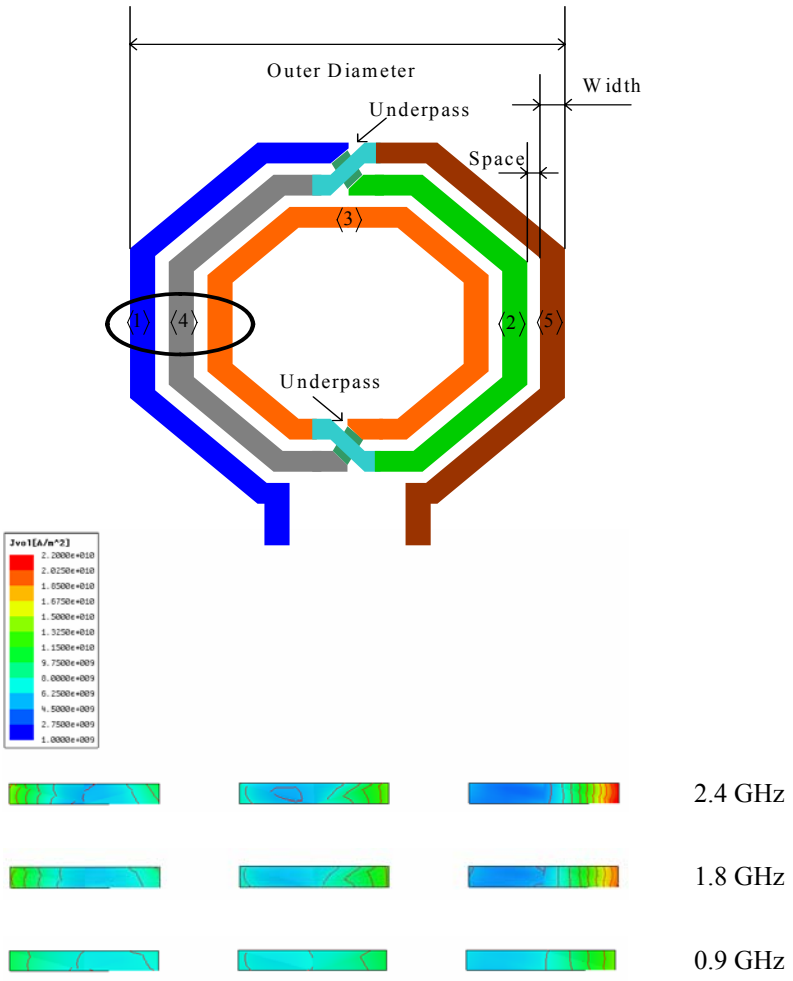


Figure 35 Current density contours in the three metal lines at three different frequencies simulated from an EM simulator.

Figure 36 shows the normalized current distributions in segments 3, 2, and 5 (see Figure 36) obtained from an EM simulator and the effective line width model. The model results were calculated by first integrating the current distribution simulated from the EM simulator over the physical line width, normalizing it with the current integrated over the effective line width, and then using it as the peak value followed by an exponential decay function. The good agreement

demonstrates the soundness of using the effective line width for modeling the frequency- and location-dependent natures of the spiral inductors.

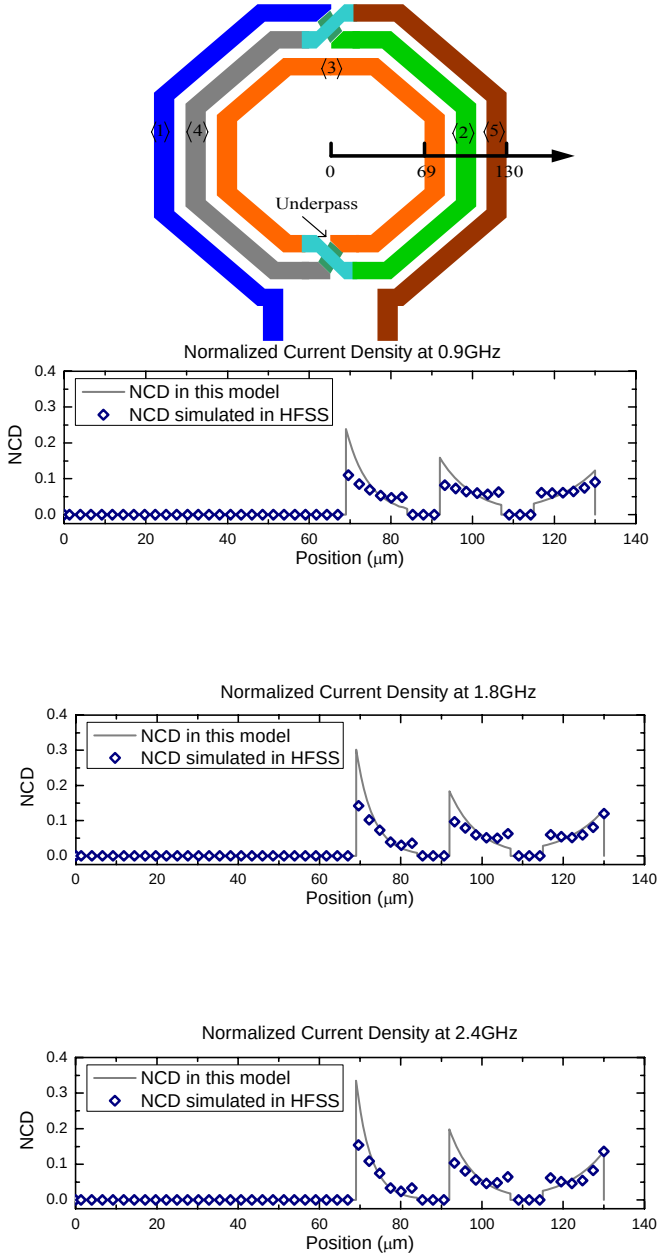


Figure 36 Comparison of current density distributions in the three metal lines calculated from the present model (lines) and obtained from EM simulations (symbols).

3.2.2 Modeling the Segment Box

We will now first discuss the modeling of the components in the segment box (see Figure 34(c)), and later discuss the modeling of the overlap components in Figure 34(b). As shown in Figure 34(c), the model components in the segment box include the series inductance L_S, series resistance R_S, and substrate parasitics.

(a) Series Inductance

The metal track in each segment can be further divided into several straight metal lines (for example, 5 straight metal lines for segment 4, see Figure 34(a)), so that the inductance L_{S_lines} of each straight metal line can be expressed as the self inductance L_{line_self} plus the mutual inductance M from all other metal lines [13]:

$$L_{S\_line} = L_{line\_self} + \sum M \tag{3}$$

The self inductance of a straight metal line can be written as [12]:

$$L_{line\_self} = 2l\left(\ln \frac{2l}{w_{eff} + t} - 0.5 \right) \tag{4}$$

where l is the length of the straight line, and t is the line thickness. Note that the current crowding effect has been accounted for and the self inductance is frequency dependent because of the introduction of w_{eff} in (4).

At low frequencies where the current distribution in a metal line is fairly uniform, mutual inductance of two parallel metal lines can be calculated using the geometric mean distance (GMD) [12]. This approach becomes questionable for high frequencies because of the highly non-uniform current distribution. In this work, the line separation is more accurately determined by the distance d between the centers of the two effective line widths. Based on this concept, the mutual inductance M_p for two parallel filaments of equal length (see Figure 37(a)) is expressed as

$$M_p(l) = 2l\left[\ln\left(\frac{l}{d}+\sqrt{1+\frac{l^2}{d^2}}\right)-\sqrt{1+\frac{d^2}{l^2}}+\frac{d}{l}\right] \tag{5}$$

For unequal parallel filaments (see Figure 37(b)), the mutual inductance M'_P is

$$2M'_p = \left[M_p(l+m+\delta)+M(\delta)\right]-\left[M(l+\delta)+M(m+\delta)\right] \tag{6}$$

Here, m is the length of the second line, and δ is the misalignment of the two lines and δ becomes negative when two filaments overlap. For filaments incline with an angle between them (see Figure 37(c)), the mutual inductance M_i is

$$M_i(m,l) = \cos(\alpha)\cdot\left[l\cdot\ln\left(\frac{l+m+R}{l-m+R}\right)+m\cdot\ln\left(\frac{l+m+R}{m-l+R}\right)\right] \tag{7}$$

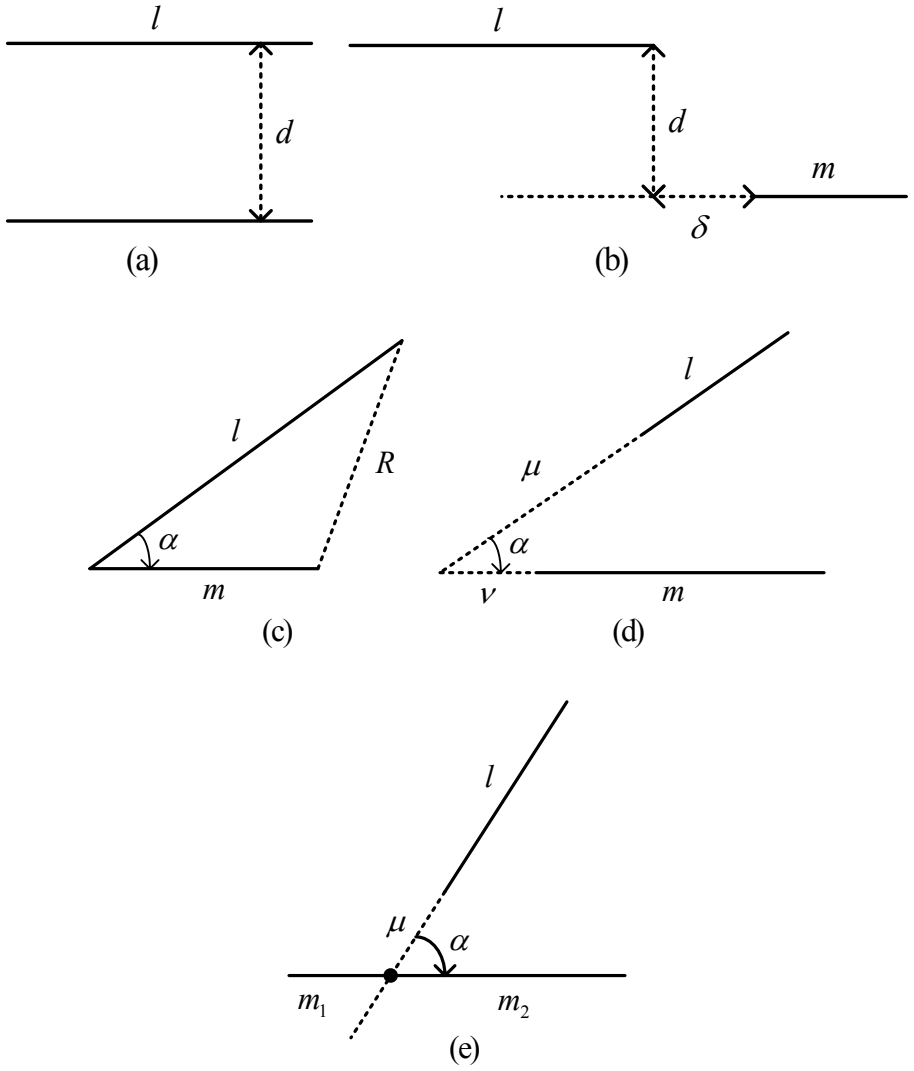


Figure 37 Different possible filament alignments for the mutual inductance calculations.

For the other possible configurations shown in Figure 37(d) and (e), the mutual inductances M'_i and M''_i can be modeled as

$$M'_i = \left[M_i(\mu + l, \nu + m) + M_i(\mu, \nu)\right] - \left[M_i(\mu + l, \nu) + M_i(\nu + m, \mu)\right] \quad (8)$$

$$M''_i = \left[M_i(m_1, \mu + l) + M_i(m_2, \mu + l)\right] - \left[M_i(m_1, \mu) + M_i(m_2, \mu)\right] \quad (9)$$

The total series inductance of a segment is the sum of all the straight-line series inductances, including the self and mutual inductances, within the segment.

Note that because of the need of a terminal taken in the middle of the segment box to connect the coupling capacitance to the neighboring segment box, the series inductance is split into two, each with $L_S/2$ and located on both sides of the terminal (see Figure 34(c)). The same applies to the series resistance.

(b) Series Resistance

Ohmic loss (I^2R) caused by the series resistance in the metal line is a factor limiting the inductor performance. At low frequencies, where the current density in the metal line is uniform, the series resistance can be easily found from the metal line resistivity and geometry. For spiral inductors operating at high frequencies, the series resistance of a straight line is frequency dependent and can be modeled using the concept of the effective metal width:

$$R_{line}(f) = \frac{\rho \cdot l}{w_{eff} \cdot t_m} \quad (10)$$

where ρ represents the resistivity in Ω-cm and t_m is the metal thickness. The total series resistance of a segment is the sum of all straight line resistances.

(c) Substrate Parasitics

Substrate parasitics result from the electrical coupling between the metal track and substrate, as the metal track of a spiral inductor can be considered as a microstrip on substrate with waves passing through it. Three elements, C_{ox}, G_{sub}, and C_{sub}, are used to model the substrate parasitics (see Figure 34(c)).

The frequency-dependent permittivity $\varepsilon_{eff}(f)$ is needed to model the frequency-dependent capacitance. It can be written as [56]:

$$\varepsilon_{eff}(f) = \varepsilon_{ox} - \frac{\varepsilon_{ox} - \varepsilon'}{1 + (f/f_c)^2} \tag{11}$$

$$\varepsilon' = \frac{\varepsilon_{ox} + 1}{2} + \frac{\varepsilon_{ox} - 1}{2(1 + 10 t_{ox}/w_{eff})} \tag{12}$$

Here, t_{ox} is the thickness of oxide under the metal line, ε_{ox} is the relative permittivity of oxide, and the critical frequency f_C is given by

$$f_C = \frac{c^2 \varepsilon_0 Z_0 \varepsilon_{ox}^{1/2}}{2 t_{ox} \varepsilon'^{1/2}} \tag{13}$$

$$Z_0 = \frac{120\pi \cdot F\left(w_{eff}, t_{ox}\right)}{\varepsilon'^{1/2}} \tag{14}$$

with

$$F\left(w_{eff}, t\right) = \begin{cases} \dfrac{1}{2\pi} \ln\left(\dfrac{8t}{w_{eff}} + \dfrac{w_{eff}}{4t}\right) & \text{for } t/w_{eff} > 1 \\ \dfrac{1}{w_{eff}/t + 2.42 - 0.44 t/w_{eff} + \left(1 - t/w_{eff}\right)^6} & \text{for } t/w_{eff} < 1 \end{cases} \tag{15}$$

Using the frequency-dependent permittivity, the oxide capacitance and substrate conductance can be expressed as

$$C_{ox}\left(f\right) = \frac{\varepsilon_0 \varepsilon_{eff}\left(f\right)}{2F\left(w_{eff}, t_{ox}\right)} \cdot l \tag{16}$$

$$G_{sub} = \frac{\sigma_{sub}\left[1 + \left(1 + 10\, t_{sub}/w_{eff}\right)^{-1/2}\right]}{2F\left(w_{eff}, t_{sub}\right)} \cdot l \tag{17}$$

where ε_0 is the permittivity of free space, σ_{sub} is the silicon substrate conductivity, and t_{sub} is the thickness of substrate. The substrate capacitance can be expressed using (16) with t_{ox} replaced by t_{sub}.

3.2.3. Modeling Components Outside Segment Box

Two types of components are located outside the segment boxes in Figure 34(b): the coupling capacitances between the metal lines and parasitics associated with the overlaps.

(a) Coupling Capacitance Between Metal Lines

$C_{C,ij}$ in Figure 34(b) describes the coupling capacitance between segments *i* and *j*. Such a capacitance can be modeled using the method stated in [57]. For a conductor of width *w* centered at *b*, the even-symmetric potential at any point $z = x + jy$ in the complex plane is given by

$$\phi_e(z,b,w) = q\left[\frac{1}{\varepsilon_0} H_e(z,b,w)\right] \tag{18}$$

where

$$H_e = \left(\frac{1}{2\pi}\right)\mathrm{Im}\left(\arcsin\left(\frac{z-b}{w/2}\right)\right) \tag{19}$$

On the other hand, the odd-symmetric potential at any z is

$$\phi_o = g\left[\frac{1}{\varepsilon_0} H_o(z,w,b)\right] \tag{20}$$

where

$$H_o = \mathrm{Re}\left[(z-b) - \mathrm{sign}(\mathrm{Re}(z-b)) \cdot \sqrt{(z-b)^2 - (w/2)^2}\right] \tag{21}$$

q and g in the above expressions are constants. Therefore, the potential of a two conductors centered at b and $-b$ can be written as

$$\phi(z) = Q \cdot h_e(z) + G \cdot h_o(z) \tag{22}$$

Q and G are the normalized charge and amplitude, respectively, and

$$h_e = H_e(z,b,w) - H_e(z,-b,w) \tag{23}$$

Forcing the potential $\phi(z) = V$ at the two match points z_1 and z_2 yields

$$z_1 = b - r \cdot w/2 \tag{25}$$

$$z_2 = b + r \cdot w/2 \tag{26}$$

These constraints, together with the assumption that the metal lines are relatively thin, lead to the following simplified expressions [57]

$$\begin{bmatrix} h_e(z_1) & h_o(z_1) \\ h_e(z_2) & h_o(z_2) \end{bmatrix} \cdot \begin{bmatrix} Q \\ G \end{bmatrix} = \begin{bmatrix} V \\ V \end{bmatrix} \tag{27}$$

Solving for the charge Q in (27), and the coupling capacitance C_C per unit length between the two metal strips can be calculated from [57]

$$C = \varepsilon_0 Q / 2V \tag{28}$$

To include the nonuniform current distribution effect discussed in Sec. 3.2.1, the metal line width w in the above equations should be replaced with w_{eff}.

(b) Overlap Parasitics

Because the length of overlap between the top and underpass is normally much shorter than that of the whole metal line, the resistance and inductance of the overlap can be omitted, and only the overlap capacitances are considered. There are two set of parasitic components denoted by subscripts 1 and 2 due to two different overlaps (see Figure 34(b)). The analysis below applies generally to both sets of the components.

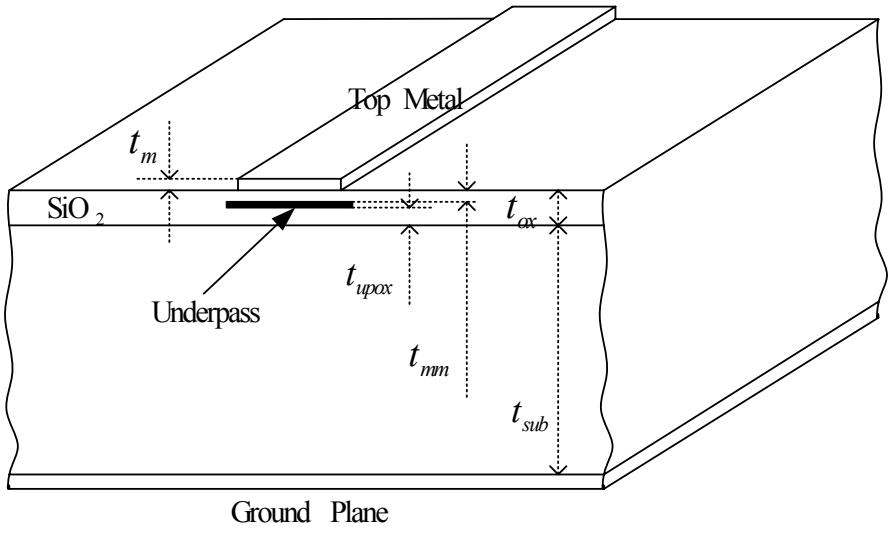


Figure 38 Cross-section showing the different thicknesses associated with the overlap parasitics modeling.

Figure 38 shows the structure of the overlap and three pertinent thicknesses: t_{upox}, t_{sub}, and t_{mm}. All the underpass capacitances can be modeled using the same approach as in Sec. 2.1. The oxide dielectric permittivity can be assumed frequency-independent because the underpass metal is relatively short. Thus,

$$C_{ox\_up} = \frac{\varepsilon_0 \varepsilon_{ox} (\text{underpass area})}{t_{upox}} \tag{29}$$

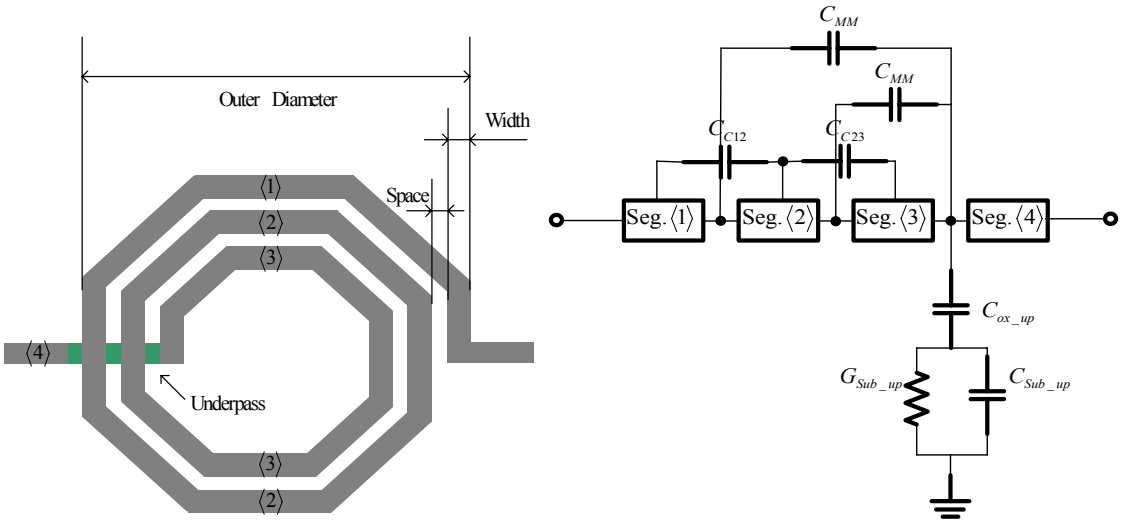
$$C_{sub\_up} = \frac{\varepsilon_0 \varepsilon_{ox} (\text{underpass area})}{t_{sub}} \tag{30}$$

$$C_{mm} = \frac{\varepsilon_0 \varepsilon_{ox} (\text{overlap area})}{t_{mm}} \tag{31}$$

$$G_{sub\_up} = \frac{\text{underpass area}}{\rho_{sub} \cdot t_{sub}} \tag{32}$$

3.3 Model Development of Asymmetrical Inductor

The concept of modeling the asymmetrical inductor, shown in Figure 39(a), is analogous to that of the symmetrical inductor given in Section II. For this inductor having 2.5 turns and octagonal pattern, the metal track can be divided into 4 segments and 1 overlap. Another difference between this and the symmetrical inductor in Figure 34(a) is the different location of the underpass. The equivalent circuit of the asymmetrical inductor is given in Figure 39(b).



(a) (b)

Figure 39 (a) Schematic of an octagon, 2.5-turn asymmetrical inductor and (b) overall equivalent circuit for the inductor including segment, capacitive coupling, and overlap components.

3.4 Model Verification

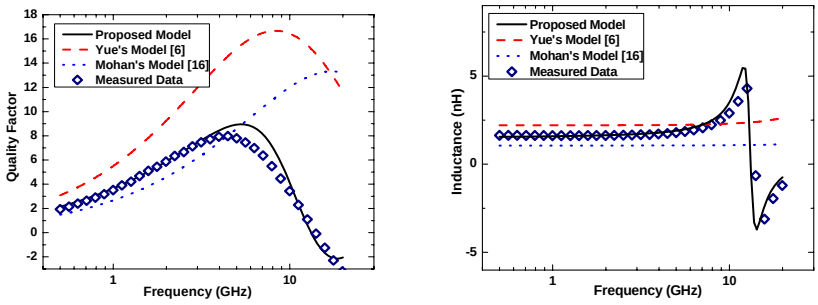
A symmetrical, octagon inductor fabricated with the 0.35μm CMOS technology was first considered and measured to verify the model developed. The inductor was built on a 9.59μm oxide and 500μm silicon substrate. The inductor has 3 turns, metal width of 15μm, metal thickness of 2μm, and metal line spacing of 8μm. Two-port parameters were measured, and the inductance, resistance and quality factor of the inductor were extracted. In addition to the present model, two existing inductor models [11],[58] intended for the asymmetrical inductors were considered. Note that the models of Yue and Wong [11] and Mohan et al. [58] employed a simple π equivalent circuit, and the results of their models were simulated based on the equivalent circuit with the components calculated from the expressions given in the papers.

A systematic method to determine the values of the fitting parameters ($c1$ and $c2$) in equations (2) is needed. To this end, the following function is developed:

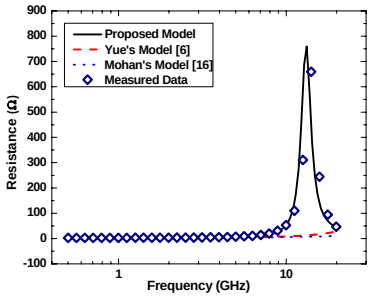
$$D = \sqrt{\sum_l \left(\frac{Q_{measure}(f_l) - Q_{model}(f_l)}{Q_{measure}(f_l)} \right)^2 + \sum_l \left(\frac{L_{measure}(f_l) - L_{model}(f_l)}{L_{measure}(f_l)} \right)^2} \qquad (33)$$

where D describes the averaged error associated with fitting the model to the measured Q factor and inductance using different fitting parameter values at several different frequencies. The parameter value that yields the smallest D is the one to use, and $c1 = 0.653$ and $c2 = 0.53$ (also listed in Table 1) were obtained from this approach for the spiral inductor considered and compared.

Figure 40(a)-(c) show the quality factor, inductance, and resistance, respectively, calculated from the present model, calculated from the two existing models, and obtained from measurements. The present model demonstrates a better accuracy over the existing models for a wide range of operating frequencies. Thus, our results suggested that it is erroneous and impractical to use the inductor model developed intended for asymmetrical inductors for predicting the characteristics of symmetrical inductors. The magnitude and phase of S_{21} parameter calculated from the models and obtained from measurements are compared in Figure 41(a) and (b), respectively.

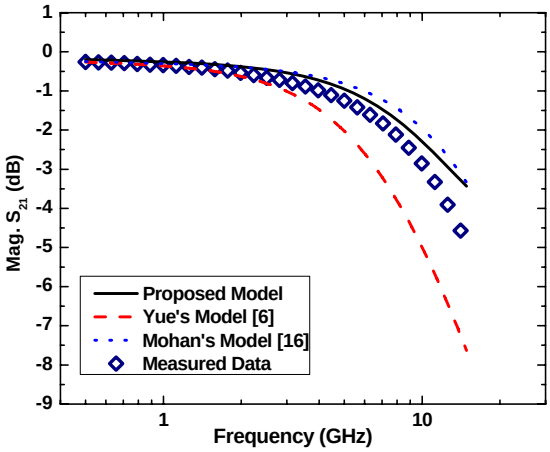


(a) (b)

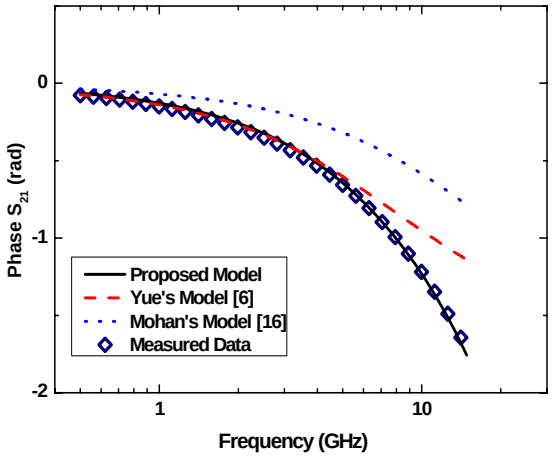


(c)

Figure 40 Comparisons of the present model, existing models, and measurements of (a) quality factor (b) inductance and (c) series resistance for the 3-turn symmetrical inductor.



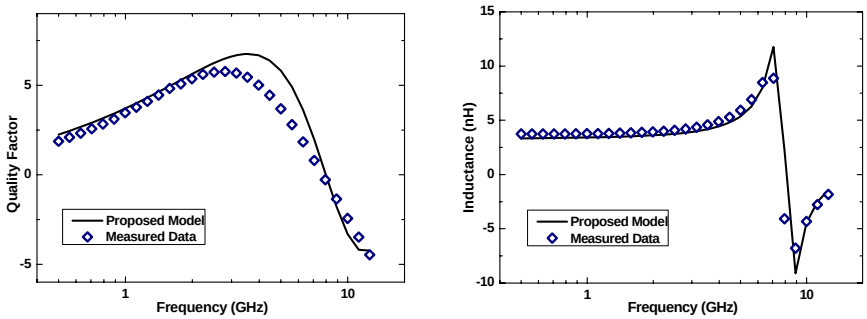
(a)



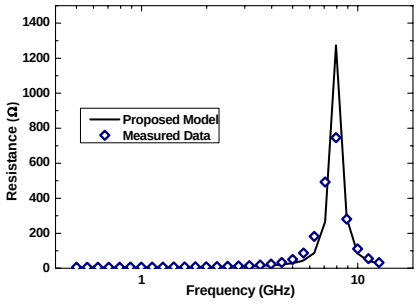
(b)

Figure 41 Comparisons of the present model, existing models, and measurements of (a) magnitude and (b) phase of S_{21} for the 3-turn symmetrical inductor.

To further verify the model developed, we compare the model calculations with data measured from another spiral inductor having an octagonal, 5-turn, and symmetrical structure, and the Q factor, inductance, and resistance results are given in Figure 42(a)-(c). The values of fitting parameters $c1$ and $c2$ for this inductor are listed in Table 1. Again, a good agreement between the model and measurements is found.



(a) (b)



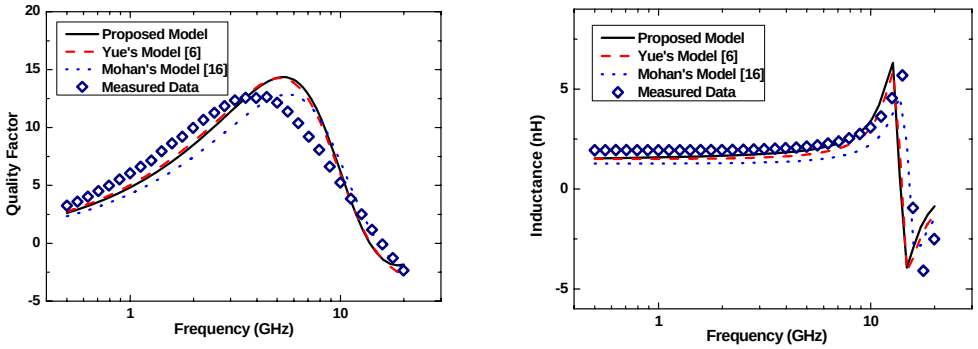
(c)

Figure 42 Comparisons of the present model and measurements of (a) quality factor (b) inductance and (c) series resistance for the 5-turn symmetrical inductor.

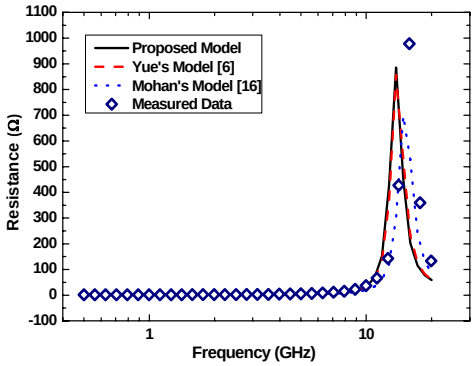
Table 1 Values of Fitting Parameters for the Three Inductors Considered

	c1	*c2*
3-turn symmetrical inductor	0.653	0.53
5-turn symmetrical inductor	0.669	0.56
2.5-turn asymmetrical inductor	0.816	0.75

One would expect that the existing models [11],[58] would be more accurate for asymmetrical inductors because they were developed intended for such devices. This is indeed the case, as shown in the results of the Q factor, inductance, and resistance given in Figure 43(a)-(c). The asymmetrical inductor considered has 2.5 turns, metal width of 16μm and spacing is 10μm, and the values of $c1$ and $c2$ for modeling this inductor are again given in Table 1. In fact, while the model predictions vary slightly at different frequencies, all three models possess very similar overall accuracy when compared to the experimental data. S-parameter results given in Figure 44 (a) and (b) yield similar conclusions.

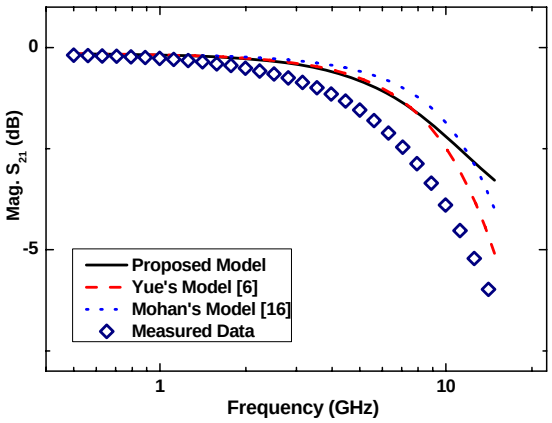


(a) (b)

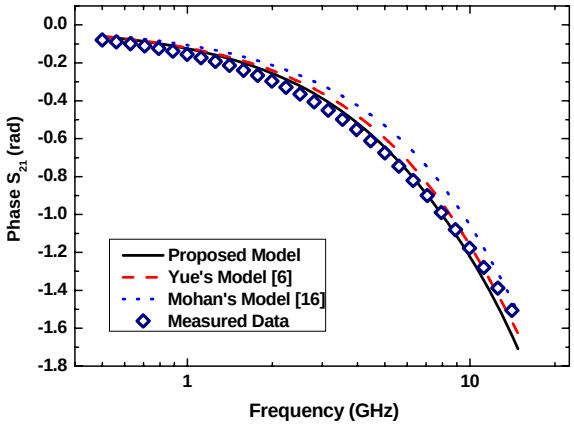


(c)

Figure 43 Comparisons of the present model, existing models, and measurements of (a) quality factor (b) inductance and (c) series resistance for the 2.5-turn asymmetrical inductor.



(a)



(b)

Figure 44 Comparisons of the present model, existing models, and measurements of (a) magnitude and (b) phase of S_{21} for the 2.5-turn asymmetrical inductor.

3.5 Conclusions

A compact and accurate model for spiral inductors has been developed. Unlike the existing inductor models which were developed intended only for asymmetrical inductors, the present model is shown capable of predicting accurately both the symmetrical and asymmetrical inductors. The concept of the effective line width was introduced to account for the effect of nonuniform current distribution in the metal lines, and overlap parasitics and geometry factors have also been included. Comparisons among the present model, existing models, and measured data were presented to illustrate the usefulness of this work.

Acknowledgements—Authors are grateful to Dr. Yun Yue at Conexant Systems for useful discussions on the inductor modeling and providing experimental data.

CHAPTER FOUR: APPLICATION IN DIFFERENTIAL INDUCTORS AND BALUNS

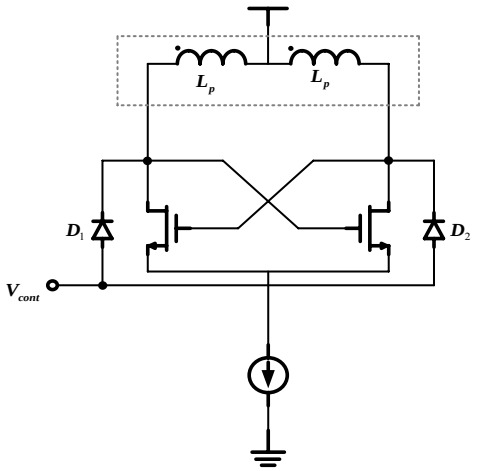
On-chip differential inductors and transformers have been used widely in RF ICs, and a compact and accurate model for these devices is not yet available in the literature. In this dissertation, such a model is developed based on the concept of the effective metal line width to account for the frequency- and location-dependent current distribution effect. Results obtained from model calculation and measured data for a differential and transformer are included in support of the model development.

4.1 Introduction

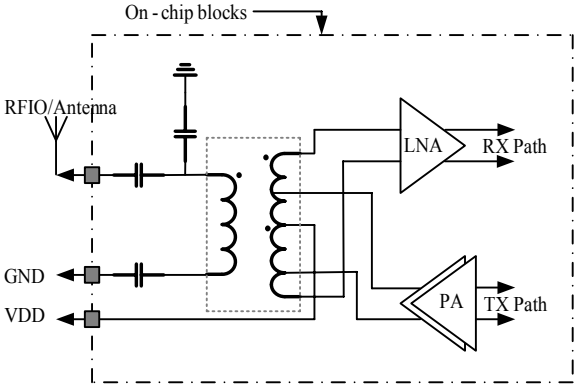
On-chip spiral inductor is no doubt a key component for modern radio frequency integrated circuits (RFIC's), and it is required in the design and realization of many RFIC's such as the low noise amplifier (LNA) and oscillator. In particular, differential inductors and transformers (or baluns), which are built based on the spiral inductors, have broad applications in RF circuits involving with differential signals. Figure 45(a) and (b) show RF circuits using a differential inductor and transformer, respectively.

Despite the importance of these devices, modeling of the differential inductor and transformer is largely overlooked and not yet well established. Some efforts have been reported in the literature [15][9][11][16], but the focus has been placed on the less complex two-terminal inductors, rather than the three-terminal differential inductors and 4-terminal transformers. In addition, relevant

physical mechanism, such as nonuniform current distribution in the metal line, was not fully incorporated in the models. Recently, we introduced the concept of effective metal line width to account for the current crowding effect, and based on this concept a compact model for the two-terminal spiral inductor was developed [60]. In this dissertation, we will extend the approach developed in [60] to the modeling of differential inductors and transformers.



(a)



(b)

Figure 45 Examples of differential inductor and transformer applications: (a) voltage control oscillator (VCO) with a differential inductor, (b) RF front-end circuit with a transformer for Bluetooth applications.

In section II, models of differential inductor and transformer/balun will be developed. Discussions and model verifications against measured data will be presented in section III. Finally, conclusions are given in section IV.

4.2 Model Development

In this section, the physics of nonuniform current distribution in the metal line of spiral inductor, and the concept of the effective metal line width, will first be reviewed. This is followed by the development of model for the different inductors and transformers.

4.2.1 Nonuniform Current Distribution

Traditionally, the current distribution in a metal line is considered to be governed by the skin and proximity effects [57][19]. This is true for a simple conductor, where the metal line is subject to the magnetic field of its own. For the case of spiral inductors and transformers, such a simple environment does not exist, since each metal line lies in the midst of all the electromagnetic fields generated by many other metal lines. According to the observations of partial-element-equivalent-circuit (PEEC) simulation [54] and 3-D electromagnetic simulation [55], the current distribution in a metal line in general exhibits an exponential decay from the inner edge (side of metal line close to the center of spiral) to the outer edge (side of metal line away from

the center of spiral). Furthermore, this exponential-decay distribution is more prominent in the inner turns and as the frequency is increased.

The nonuniform current distribution effect was accounted for effectively and accurately using the concept of the effective line width W_{eff} [60]. It is defined as the length of the region in which the first exponent of current density exists, and W_{eff} is then used to replace the physical metal line width to accurately model the frequency-dependent behavior of the spiral inductor. The following expressions were developed for the effective line width as a function of the frequency and the line segment index [60]:

$$w_{eff} = W_{0,i}\left(1-\exp\left(-\frac{w}{W_{0,i}}\right)\right) \tag{1}$$

$$W_{0,i} = c1\cdot c2^{i-1}\sqrt{\frac{1}{f}} \tag{2}$$

where w is the physical metal line width, f is frequency in Hz, i is index of the spiral line segment divided based on the location of the underpasses, and $c1$ and $c2$ are parameters for matching the model with measurements. The method to determine the values of $c1$ and $c2$ is discussed briefly below. The following function was developed [60]:

$$D = \sqrt{\sum_l\left(\frac{R_{measure}(f_l)-R_{model}(f_l)}{R_{measure}(f_l)}\right)^2+\sum_l\left(\frac{L_{measure}(f_l)-L_{model}(f_l)}{L_{measure}(f_l)}\right)^2} \tag{3}$$

where *D* describes the averaged error associated with fitting the model to the measured resistance and inductance using different fitting parameter *c*1 and *c*2 values at several different frequencies. The values that result in the smallest D are then chosen for the inductor modeling.

4.2.2. Differential Inductor

We now focus on the model development for a differential inductor. A three-turn square differential inductor is considered and shown in Figure 46. With the center tap floating, this structure can be used as a single-ended inductor. When it is driven by a differential signal, the center tap is often connected to an ac ground, and the structure is called the differential inductor. Following the approach developed in [60], the spiral is first divided into six segments, as labeled in Figure 46, by underpasses and center tap. Then each segment is represented by a single π equivalent circuit as shown in Figure 47. Thus, the complete equivalent circuit for the entire differential inductor is shown in Figure 48. Note that each numbered box in Figure 48 represents the single π equivalent circuit for each numbered segment. Information on the single π equivalent circuit for each segment and the construction of the complete equivalent circuit for the spiral inductor has been discussed in detailed in [60].

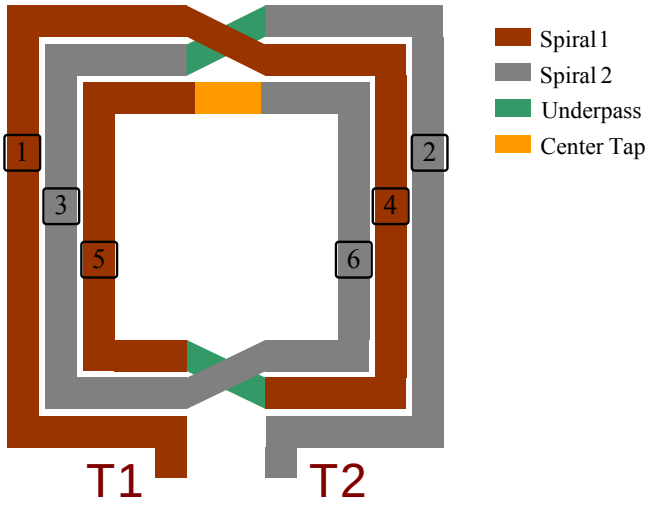


Figure 46 Pattern of a three-turn square differential inductor, with six metal-line segments divided by the underpasses and center tap.

The series inductance L_s in Figure 47 consists of the self inductance L of a particular segment and the mutual inductance M between this and another segment are calculated as

$$L_i^{seg} = \sum_m L_m^{line} \tag{4}$$

$$M_{i,j}^{seg} = \sum_m \sum_n M_{m,n}^{line} \tag{5}$$

where i and j are the index numbers of two different segments, and m and n are the index numbers of metal lines in a segment. A segmental inductance matrix is formed after all the self and mutual inductances are known.

Other components in the equivalent circuit in Figure 47 include the series resistance R_s, oxide layer capacitance C_{ox}, and substrate coupling conductance G_{sub} and capacitance C_{sub}. Besides the segment box, other components in Figure 48 account the parasitic effect at the underpass region. They are C_{ox_up}, G_{sub_up} and C_{sub_up}, and C_{mm} is the capacitance from top metal to underpass. Expressions for these components can be found in [60].

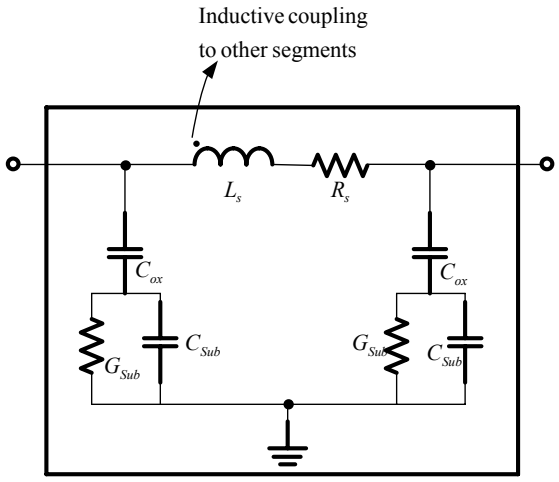


Figure 47 Equivalent circuit of each segment in Figure 46.

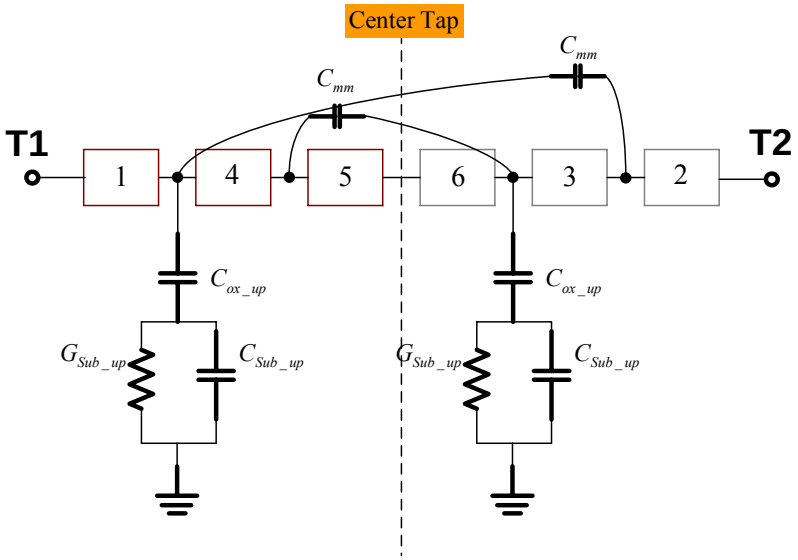


Figure 48 Complete equivalent circuit for the differential inductor in

4.2.3. Transformer/Balun

A transformer/balun, which has two terminals, can be viewed as two differential inductors inter-winding together. Figure 49 shows the transformer/balun structure considered in this study. When the two center taps are both floating, the structure is called the transformer, and when inductor1's center tap is grounded and inductor2's center tap is floating, or vise versa, the structure is called the balun. The equivalent circuit for the transformer/balun, as given in Figure 50, can be constructed based on the same concept used in Sec. 2.2.

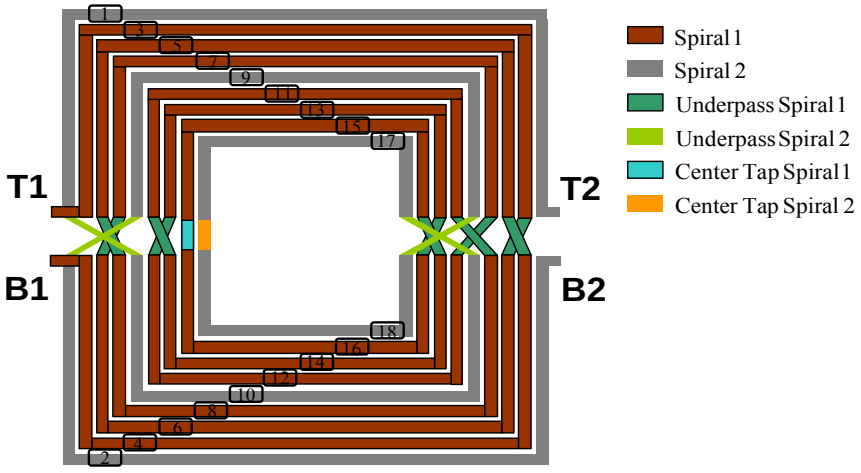


Figure 49 Pattern of a nine-turn square transformer/balun.

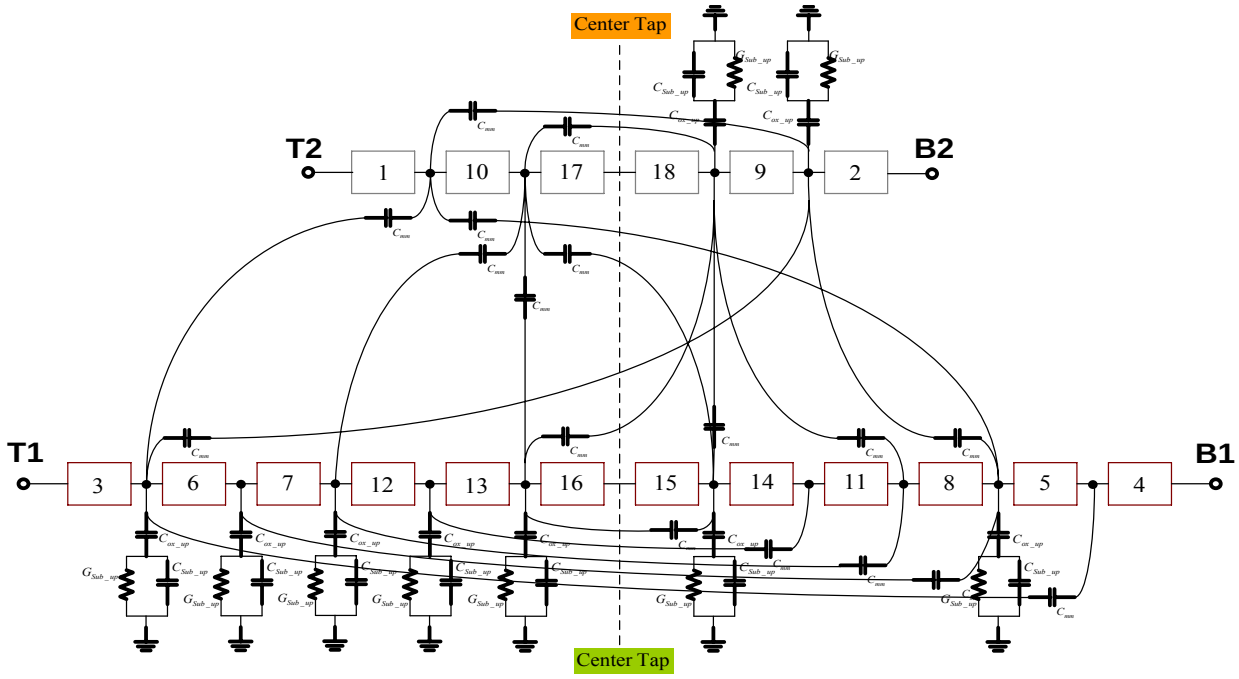


Figure 50 Complete equivalent circuit for the transformer/balun in Figure 49.

4.3 Model Verification and Discussions

A 3-turn differential inductor and a 9-turn transformer were fabricated using the 0.18 μm CMOS technology and measured to verify the model developed. The spiral inductor was built on an 11.31 μm oxide and 330 μm silicon substrate. Other parameters for the structures are listed in Table.1.

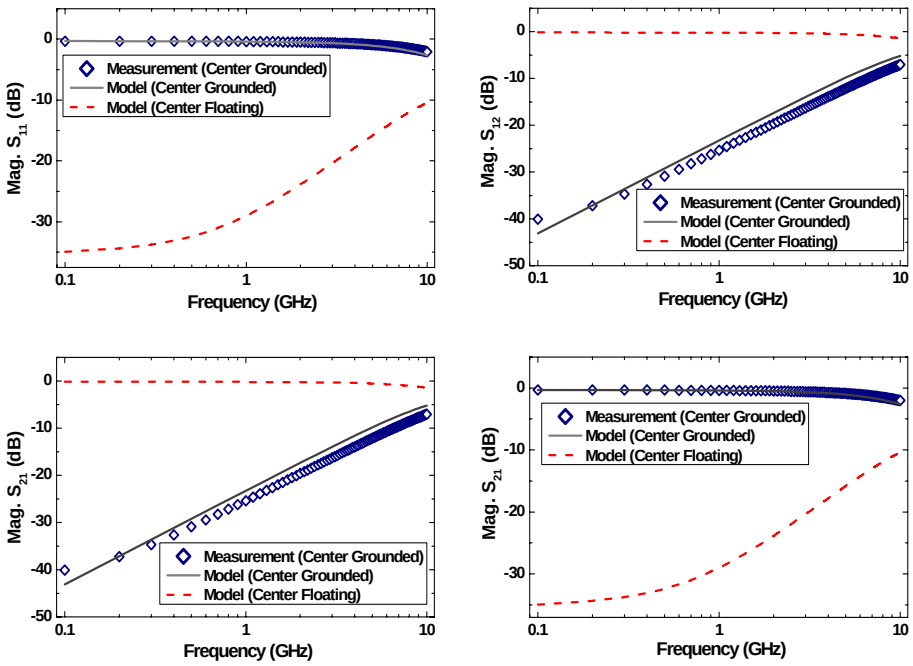


Figure 51 Magnitude of two-port S-parameters for the inductor shown in

Figure 51 and Figure 52 show the magnitude and phase of four S parameters calculated from our model (solid lines) and obtained from measurements (symbols). In addition, the results for the two-terminal inductor (center tap floating) are also included (dashed lines). Figure 53 compares the differential inductance, resistance and quality factor calculated from the model and obtained from measurements.

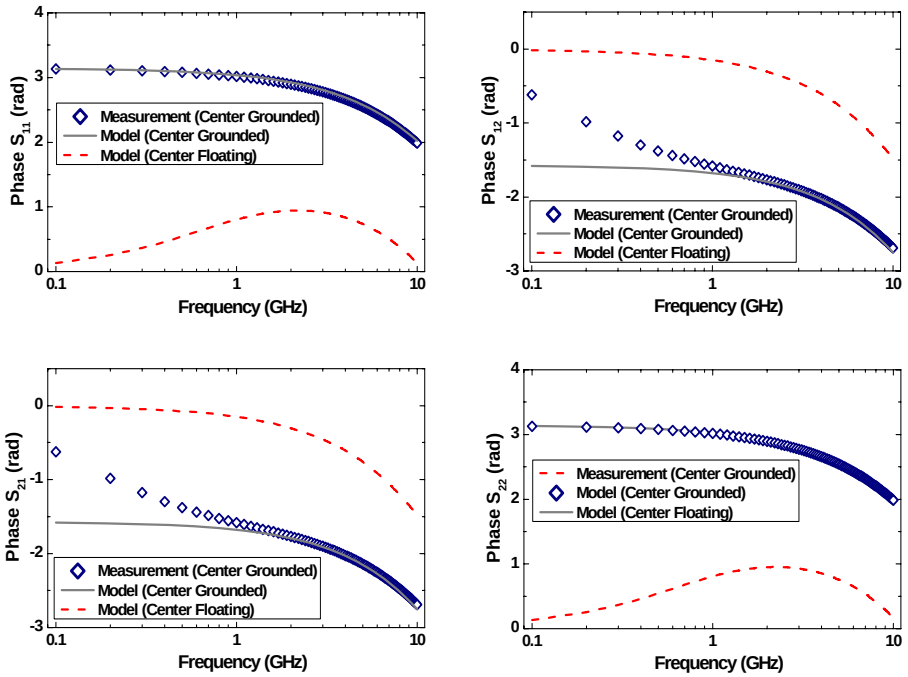


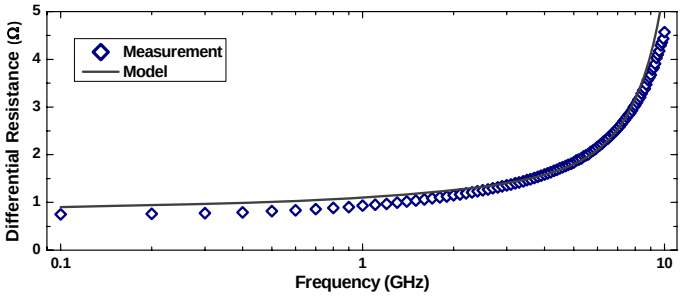
Figure 52 Phase of two-port S-parameters for the inductor shown in

Figure 46

Table 2 Parameters for the inductors considered and fabricated

	Nt	*Od*	*Wi*	*Sp*	*c1*	*c2*
Differential Inductor	3	180μm	12.5μm	3μm	1.225	0.55
Transformer/Balun	9	180μm	5μm	2μm	0.572	0.85

Nt=number of turns, Od= outer diameter, Wi=width, Sp=spacing



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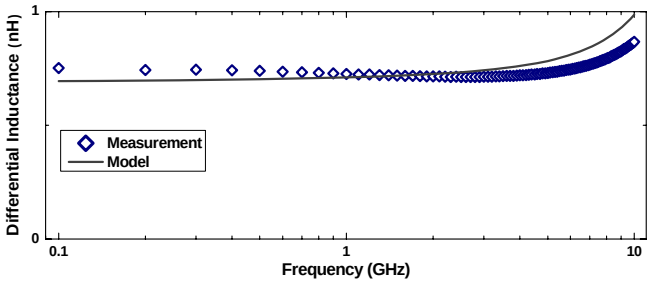
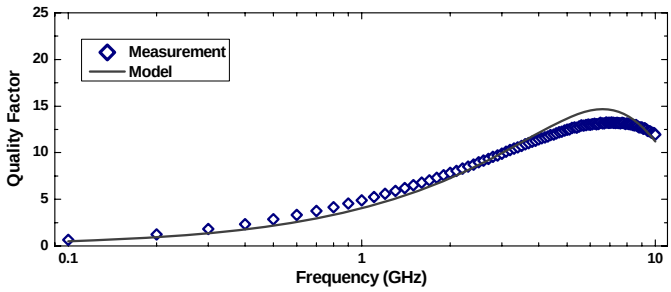


(b)



(c)

Figure 53 (a) Inductance, (b) resistance, and (c) quality factor for the inductor shown in Figure 46

Calculated and measured magnitude and phase of four S parameters for the transformer are plotted in Figure 54 and Figure 55. In addition, the model results for the balun from port1 to port2 (inductor1's center tap grounded) and the balun from port2 to port1 (inductor2's center tap grounded) are also given to demonstrate of the capability of our model. For the case of both ports matched, which yields the best available RF performance, Figure 56 and Figure 57 illustrate the transducer gain (insertion loss) and the resistance/inductance of the transformer, respectively. All these model results compare favorably with measured data.

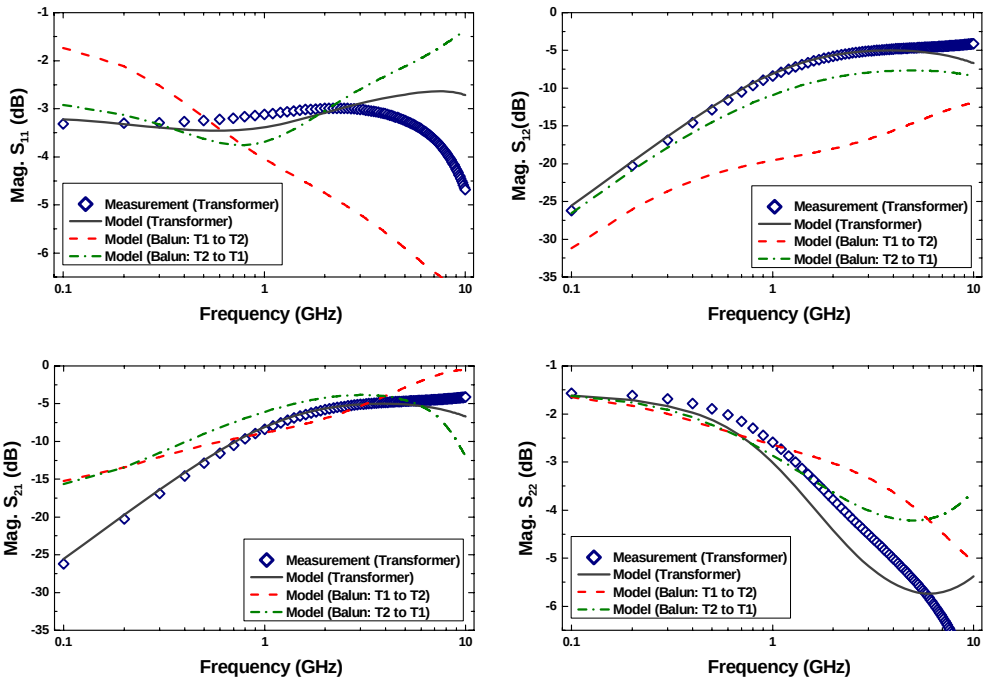


Figure 54 Magnitude of two-port S-parameters for the transformer/balun shown in Figure 49

It is worth pointing out that no comparison to other compact models was made in the above figures, as to the best of our knowledge no such models are available in the literature.

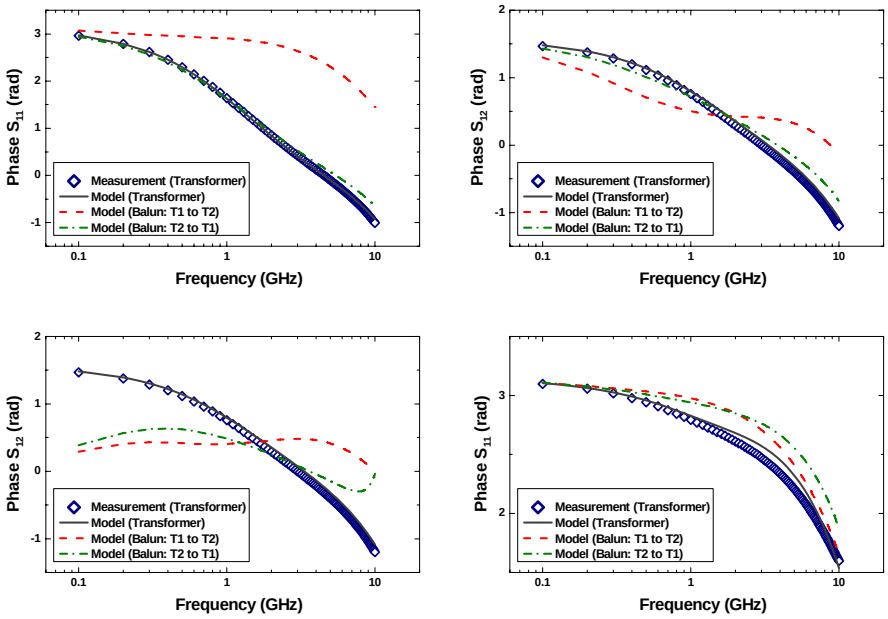


Figure 55 Phase of two-port S-parameters for the transformer/balun shown in Figure 49

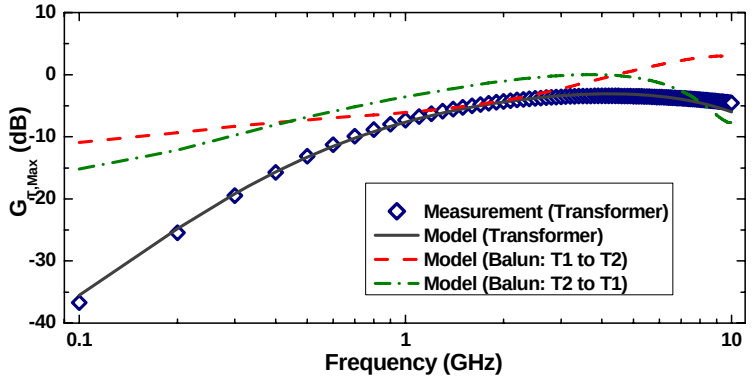


Figure 56 Best available (with both ports matched) transducer gain (insertion loss) for the transformer/balun shown in Figure 49

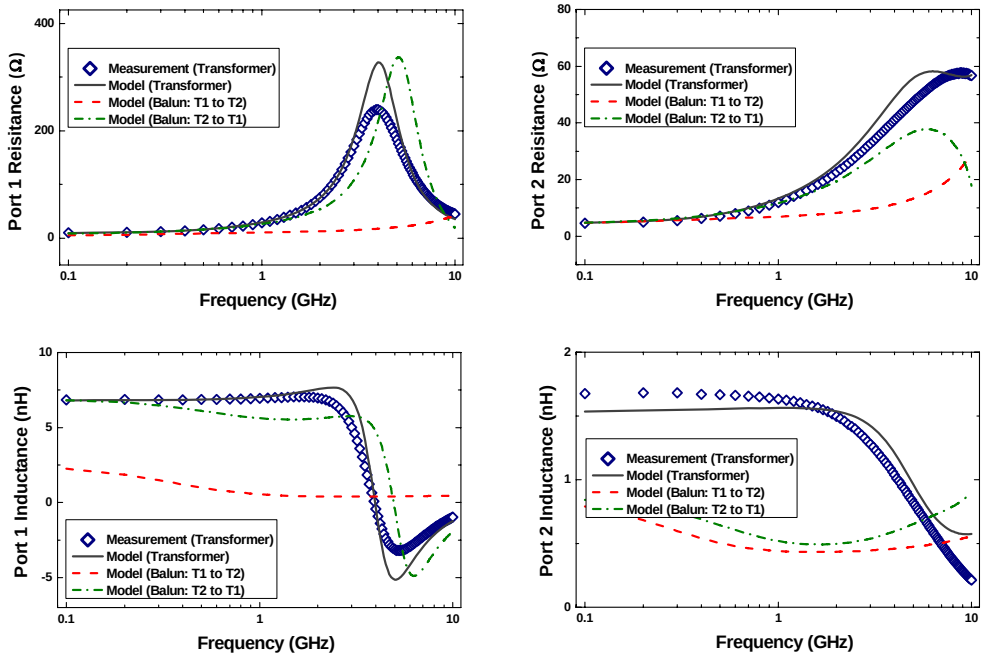


Figure 57 Resistance and inductance of the transformer with both ports matched

4.4 Conclusions

A physics-based and compact model for differential inductors and transformers/baluns has been developed in this work. Included in the model framework are the equivalent circuit, concept of the effective metal width to account for the nonuniform current distribution, and method to determine the values of two fitting parameters involved in the model. RF performance calculated from the present model show good agreement with experimental data measured from a 3-turn differential inductor and 9-turn transformer. The model developed should provide a useful and practical CAD tool for the design and fabrication of spiral inductors for RF applications.

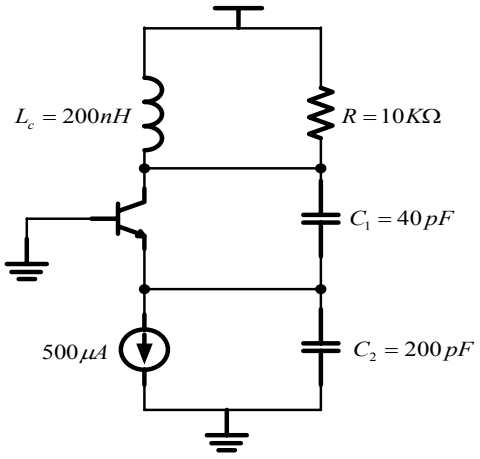
CHAPTER FIVE: APPLICATION IN METAL WIDTH OPTIMIZATION

It is always desirable to know the performance limit of an existing technology without expensive option and long term development. Inductor, as a key passive device in radio frequency circuit today, has it performance highly depend on layout technique. Whereas the performance of active devices is decided by material and doping profiles, there is some room for inductor to improve. This chapter is to propose some new angles to view the parameters of on-chip spiral inductor, and optimize them. The results are verified with measurement.

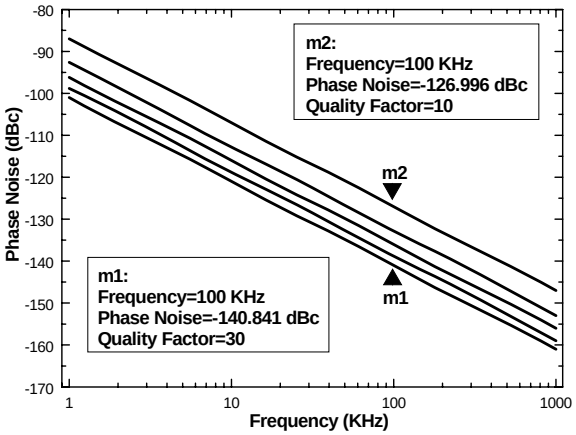
5.1 Introduction

Modern radio frequency (RF) technology becomes one of the fast growing sectors in the semiconductor industry, as we can easily experience the daily convenience provided by the cell-phone, GPS, bluetooth, wireless LAN, etc. To realize these RF electronics, the RF front-end module is inevitable the first and critical block to process RF signals. Design and optimization of the on-chip inductor, a key passive component for the RF front-end circuits such as the voltage controlled oscillator (VCO) and low noise amplifier (LNA), has drawn a great deal of attention recently. For example, high performance (i.e., high quality factor or Q factor) inductors are needed in the VCO to suppress its phase noise, which is an important spec for all RF communication chips. Any failure in meeting the phase noise requirement will result in compromising the RF functionality of the entire chip. For example, the Q factor in an LC tank is inversely proportional to the phase noise of an oscillator circuit shown in Figure 58, in which the capacitor/varactor Q is

typically fixed at 50. The quality factor of the inductor then decides the overall performance of the circuit. As a result, the design of high performance RF IC's is often a careful selection of the correct and suitable inductor technology [6].



(a)



(b)

Figure 58 (a) An RF oscillator circuit, and (b) simulated phase noises of the circuit with the inductor's Q factor increasing from 10 to 30.

It is always desirable to know the performance limit of an existing technology without expensive fabrication and long development cycle. Unlike active devices whose performance is decided predominantly by the material property and doping profile, the behavior of the on-chip inductor depends heavily on the layout technique [37][30][39][43]. With the limitation of the existing CMOS technology, the most viable way to optimize the on-chip inductor performance is the manipulation of the inductor's layout [15][52][50]. In this aspect, inductor's shape is frequently an important factor, and it is well known that the octagonal or circular shape can enhance the inductor's Q factor. But this enhancement always comes at the expense of decreased inductance. This is because it is impossible to vary the shape while keep all other parameters (i.e., area, metal width, spacing, total metal length, etc.) intact. For impedance matching in LNA and LC tank resonance in VCO, a specific inductance, in addition to a high Q factor, is needed. So it is important to develop a method that can optimize the layout of an inductor while maintaining a desirable inductance.

In this paper, a generalized frame work to optimize the Q factor for a specific inductance will be proposed. The optimization approach will be presented in section II, and the experimental verification of the inductor optimization will be demonstrated in section III. Finally, conclusions will be given in section IV.

5.2 Optimization Approach Development

Conventionally, the on-chip spiral inductor optimization focuses on a few layout parameters. For a single-ended square inductor, the most often used layout parameters are the outer diameter, metal width, spacing and number of turns. The work in [47] proposed a good scheme to minimize the serial resistance in order to meet the goal of achieving the highest quality factor. But as the inductance at the frequency of interest is shifted after the optimization, this approach has little use in the practical design of spiral inductors. Furthermore, for the frequency range of several GHz, the current nonuniform effect in the inductor is always quite prominent [60], and such an effect can influence the inductor's performance significantly. Thus, an effective and accurate design and optimization must account for the current nonuniform effect, but such an inclusion will further complicate the optimization procedure.

At a given frequency, it has been shown that the current nonuniformity is fairly constant within a specific turn [60]. As such, the optimization will be carried out first in a specific turn, and the width of the metal line in the turn will be set as a variable to optimize. The spacing between the two adjacent metal tracks affects the mutual inductance and capacitive coupling. Since the capacitive coupling among the different turns is of minor importance to the overall inductance performance, the spacing can be fixed at the minimum value decided by the ground rule to maximize the mutual inductance in order to obtain a high Q factor. The outer diameter can also be fixed based on the maximum die size allowed, so that a high area efficient is achieved. Thus, for a given inductor shape (i.e., square, octagonal, etc.), the variables to be optimized are the metal line width of each

turn and number of turns. Note that the optimization requires a model which accounts for various physical effects and is valid for an arbitrary inductor. The model reported in [60] meets such requirements and will be used as the backbone for the optimization method.

A few commercial software tools, such as Matlab, are available for finding the maximum Q factor in an inductor, but only the local optimum (i.e., one parameter optimized while others are fixed) can be obtained from these tools. A more generalized way is to consider multiple applicable variables mentioned above in the range of interest, and the results will be a multi-dimensional plot of inductance and Q factor. This allows for a true optimization of the spiral inductor to meet specific design criteria.

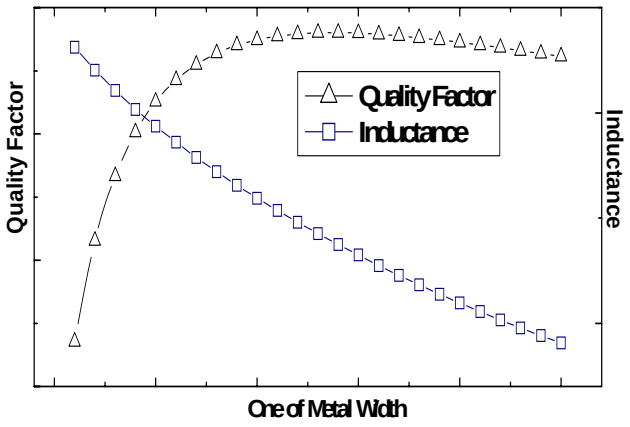


Figure 59 Typical variation of inductance and quality factor with sweep of metal line width.

Obviously, an importance issue is the range of inductance of interest. An initial observation of this can be obtained by changing one of the metal widths while holding all other parameters constant. Using this approach, the inductance vs. metal line width characteristics of a typical inductor are illustrated in Figure 59. The inductance decreases with increasing metal line width, while the Q factors increases quickly; it reaches the peak value and drops slowly afterward. From these results, one can determine the lower and upper bounds of the metal line width for the inductance of interest.

We propose the following procedure to optimize the metal line widths at the different turns of a spiral inductor:

1. Set outer diameter and spacing (depend on technology and maximum die side allowed) and choose an initial guess for the number of turns;
2. Decide the minimum and maximum values of the width of the first turn (Turn 1) as illustrated in Figure 59;
3. Using the inductor model in [60], together with the two metal line width values in step 2, calculate the inductance at the frequency of interest. If the inductance of interested is within the calculated inductance values, then start to sweep the width of Turn 1; if not, change number of turns, and go back to step 2;
4. Record the calculated Q factors vs. metal line width results and select the line width that yields the maximum Q factor;
5. Repeat steps 2-4 for other turns (i.e., Turn 2, Turn 3, etc.); and
6. Repeat steps 2-5 until all possible metal line width/number of turns combinations have been considered and calculated.

After this optimization procedure, we will have a list of the Q factor as a function of the metal width and number of turns for the inductances of interest. The optimum Q factor can be picked from these results. The optimization procedure is summarized in the flowchart in Figure 60.

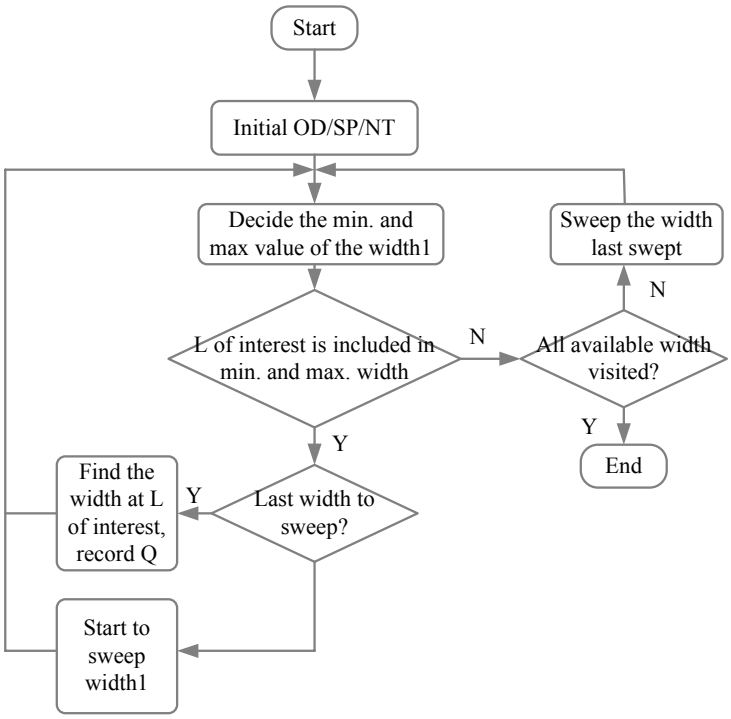


Figure 60 Optimization flow graph

5.3. Experimental Verification

The model report in [60] has been used to calculate the inductance and Q as a function of the inductor layout and frequency. The fitting parameters needed in the model were first obtained from a structure of similar outer diameter and occupation ratio (inner diameter divided by outer diameter). The optimization target is the highest possible Q factor for a square shape, single-ended inductor with a 180 μm outer diameter, an inductance of 1.7 nH, and operates at a frequency of 1 GHz. The task is challenging because of the low inductance required and limited outer diameter. The optimization procedure outlined in section II was carried out, and optimized layout obtained

from this procedure is designated as Inductor 2 in Table 3. For comparison purposes, the layout of a non-optimized inductor, designated as Inductor 1, is also given in the table.

Table 3 Layouts of optimized and non-optimized inductors

	description	*Nt*	*Od*	*W1*	*W2*	*W3*	*W4*	*Sp*
Inductor1	Square Single-ended	3	180	14	14	14	-	2.6
Inductor2	Square Single-ended (opt)	3	180	13.96	11.47	10.4	-	2.6
Inductor3	Octagonal Single-ended	3	180	11	11	11	-	2.6
Inductor4	Octagonal Single-ended (opt)	3	180	7.73	9.91	15.56	-	2.6
Inductor5	Octagonal Differential	3	280	9	9	9	-	2.6
Inductor6	Octagonal Differential (opt)	3	280	8.32	7.865	17.26	-	2.6
Inductor7	Square Single-ended	4	250	14.5	14.5	14.5	14.5	2.6
Inductor8	Square Single-ended (opt)	4	250	11.82	18.07	13.19	12.7	2.6

Inductors 1 and 2 were then fabricated following the layouts listed in Table 3 using a 2 μm thick metal placed on 5.07 μm oxide and 350 μm substrate, and the topology of the inductors are shown in Figure 61(a) and (b), respectively. Since the dielectric material between the spiral and substrate has many layers, the effective dielectric constant Er_{eff} is calculated as

$$Er_{eff} = \sum_i d_i \cdot \left(\sum_i \frac{d_i}{Er_i} \right)^{-1} \qquad (1)$$

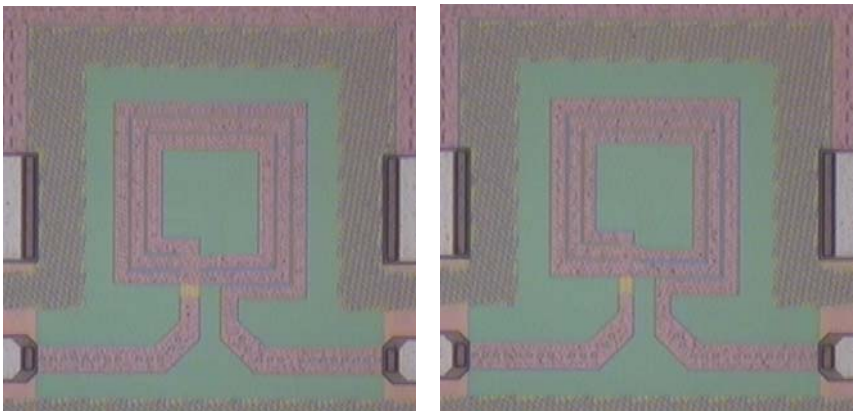


Figure 61 Layout topology of (a) Inductor 1 (b) Inductor 2

where d_i is the thickness of *ith* layer, and Er_i is the dielectric constant of the *ith* layer. The inductors were measured using the Agilent network analyzer and properly de-embedded. Figure 62 compares the measured inductances and Q factors of Inductors 1 and 2. Note that the peak Q factors for Inductors 1 and 2 are 12.5 and 14.5, respectively, confirming that the present approach can be used to obtain an optimal layout for the spiral inductors.

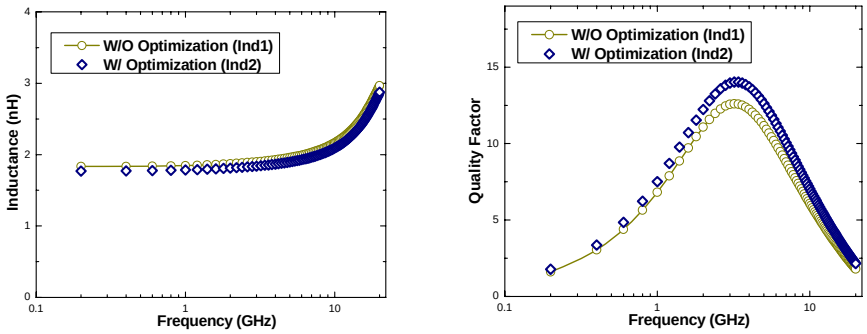


Figure 62 (a) The inductance and (b) quality factor of Inductors 1 and 2

The optimization procedure developed is applicable to other types of inductors as well. Layouts of optimized 3-turn octagonal single-ended and differential inductors, designated as Inductors 4 and

6, respectively, are listed in Table 3. The layouts of their non-optimized counterparts, designated as Inductors 3 and 5, are also given in Table 3. Figure 63 and Figure 64 illustrated the measured inductances and Q factors for Inductors 3 and 4 and Inductors 5 and 6, respectively. Inductors with a 4-turn and 250 μm outer diameter layout were also considered, and the non-optimized and optimized layouts designated as Inductors 7 and 8 are listed in Table I and their performances are shown in Figure 65. These results again indicate clearly that the Q factor improved after inductor's layout is optimized with the present approach.

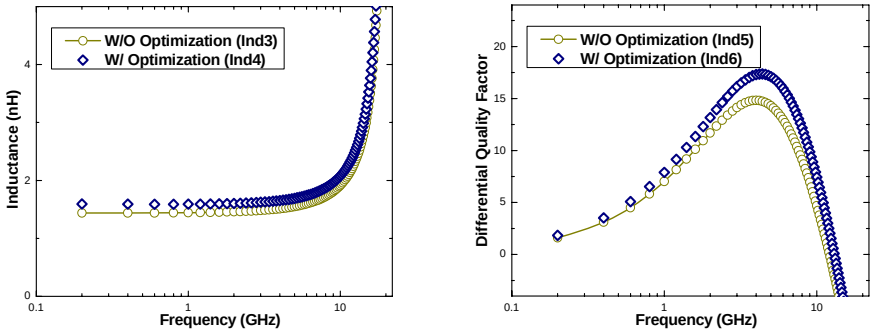


Figure 63 (a) The inductance (b) and quality factor of Inductors 3 and 4

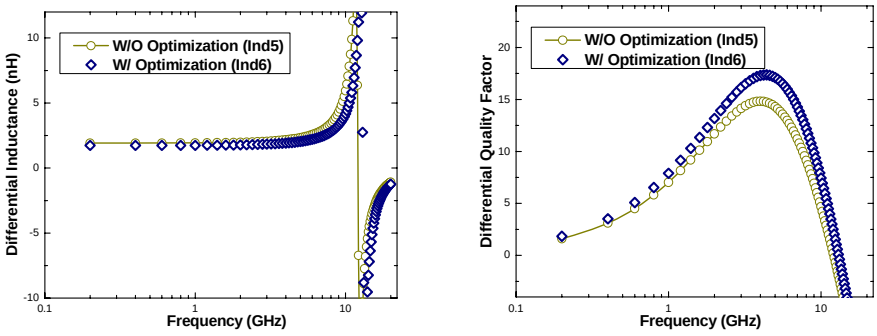


Figure 64 (a) The inductance and (b) quality factor of Inductors 5 and 6

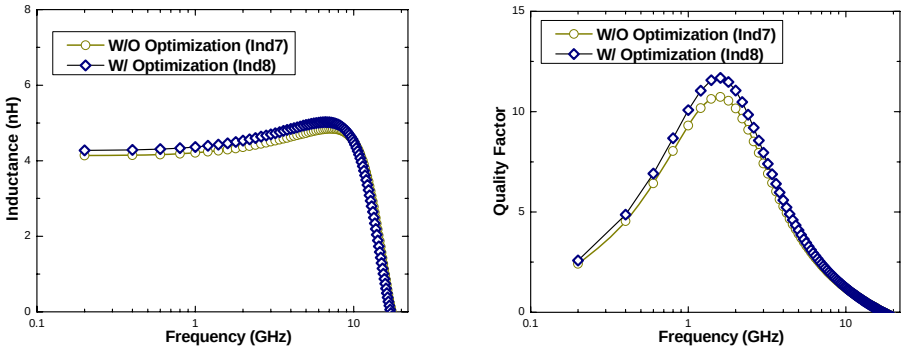


Figure 65 (a) The inductance and (b) quality factor of Inductors 7 and 8

5.4. Conclusion

An optimization procedure for the spiral inductor has been developed and verified with measurements. A previously developed inductor model was used as the backbone for the optimization calculations, and a procedure was established to carry out the optimization of the layout of the inductors. The approach developed can reduce the design cycle significantly and thus decrease greatly the cost of RF IC's development.

CHAPTER SIX: SUMMARY AND FUTURE WORK

6.1 Summary

This dissertation reviews existing articles about on-chip inductor, and describes the in-sufficiency of skin effect and proximity effect in terms of addressing the current crowding. It also presents new modeling technique of inductor and balun with new explanation of current crowding of on-chip inductor. An optimization procedure is proposed as well.

In chapter 1 and chapter 2, author elaborately collected references from over 200 existing articles that focus on inductor design, modeling and advanced technology. The chapters start with the basic structure and modeling technique. They later lead to more advanced technology to improve the performance, which includes the techniques using existing technology (metal paralleling, metal width optimization) and special technologies (deep trench, MEMS). Their improvement and limitations are also introduced. The modeling regarding to each component (mostly series resistance and inductance) is embodied as well.

In chapter 3 and chapter 4, author conceptual and experimentally explained the caused of current crowding in inductor is the magnetic field generated by the whole inductor. On the other hand, traditionally believed skin effect and proximity effect are suitable for only single conductor and conductor pair. Current distribution in the metal crosssection is neither at the surface (skin effect) nor at the inner side (proximity effect). A model was proposed to account this new discovered current crowding phenomenon, and it is also applied to differential driven inductor and balun. Model simulation results are plotted against measured data, and a good agreement can be found.

Traditionally, the inductor optimization needs to parameterize the inductor with four parameters: outer diameter, metal width, spacing and number of turns. Many complex mathematic methods are used to accelerate the optimization procedure. The potential problem is that they can not guarantee the convergence and the result is initial-value-dependent. Thus the result may not the real optimized one. Chapter 5 proposed a simple method based on sweeping all possible parameter combinations with skipping the un-usable region. The scheme is robust and efficient. The optimization parameters are not limited by the four mentioned above. The chapter proposed to introduce one width parameter for each turn. Optimization result is improved by 7~10% comparing with the uniform width inductor.

The purpose of this dissertation is to discover new design guidance to achieve best inductor with given technology and silicon area and new model for time domain simulation. Both of them are of significance in modern semiconductor industry.

6.2 Future Work

As stated above, the two tasks are efficient inductor design and accurate inductor modeling. Author would like to suggest possible future development based on his point of view.

The model proposed in this dissertation fulfilled the idea of current crowding. But the current crowding model needs two fitting parameters, which restricts its application. It is encouraged to

derive physical expressions for the fitting parameters, thus the model become fully physical and predictive. Furthermore, components in model are frequency dependent, which prevent it become a candidate for time domain simulator (SPICE, SPECTRE).

An accurate predictive model is critical for parameter optimization. Without the model, the optimization result is meaningless. 2.5 D numerical EM simulator could be a good candidate before reliable model is available. Normally, with mesh reduction and neglect the radiation, a simulation takes about one minute. This is acceptable with low volume of request on IC chip. And, with the development of digital calculation power, the EM solution will become more popular.

LIST OF REFERENCES

[1] T. H. Lee and S. S. Wong, *CMOS RF integrated circuits at 5 GHz and beyond*, Proc. IEEE, Vol. 88, pp. 1560-1571, Oct. 2000.

[2] T. H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*, Cambridge University Press, 2002.

[3] Ali M. Niknejad and Robert G. Meyer, *Design, Simulation and Applications of Inductors and Transformers for Si RF ICs*, Kluwer Academic Publishers, 2000

[4] C. Patrick Yue, *On-Chip Spiral Inductors for Silicon-Based Radio-Frequency Integrated Circuits*, Doctoral Dissertation, Stanford University, 1998

[5] Ken Boak, *An introduction to telephone line interfacing using the PIC microcontroller*, http://puggy.symonds.net/~catalyticideas/rat_ring/index.

[6] Seung-Min Oh, Chang-Wan Kim, and Sang-Gug Lee, *A 74%, 1.56 ~2.71 GHz, wide-tunable LC-tuned VCO in 0.35 μm CMOS technology*, Microwave and Optical Technology Letters, Vol. 37, pp. 98-100, April 2003.

[7] Tsui Chiu, *Integrated On-Chip Inductors For Radio Frequency CMOS Circuits*, Master Dissertation, The Hong Kong Polytechnic University, 2003.

[8] S. Chaki, S. Aono, N. Anodoh, Y. Sasaki, N. Tanino, and O. Ishihara, *Experimental study on spiral inductors*, Digest of IEEE International Microwave Theory and Techniques Symposium, 1995.

[9] N. M. Nguyen and R. G. Meyer, *Si IC-compatible inductors and LC passive filters*, IEEE Journal of Solid-State Circuits, Vol. 25, Pages 1028-1031, Aug. 1990.

[10] K. B. Ashby, W. C. Finley, J. J. Bastek, S. Moinian, and I. A. Koullias, *High Q inductors for wireless applications in a complementary silicon bipolar process*, Proc. Bipolar/BiCMOS Circuits and Technology Meeting, Pages 179–182, 1994.

[11] C. Patrick Yue and S. Simon Wong, *Physical modeling of spiral inductors on silicon, IEEE Transactions on Electron Devices*, Vol. 47, March 2000.

[12] Frederick W. Grover, *Inductance Calculations*, New York, D. Van Nostrand Company, Inc. 1946.

[13] H. M. Greenhouse, *Design of planar rectangular microelectronic inductors*, IEEE Transactions on Parts, Hybrids, and Packaging, Vol. 10, Pages 101-109, 1974.

[14] S. Jenei; B. K. J. C. Nauwelaers, and S. Decoutere, *Physics-based closed-form inductance expression for compact modeling of integrated spiral inductors*, IEEE Journal of Solid-State Circuits, Vol. 37, Pages 77-80, Jan. 2002.

[15] Sunderarajan S. Mohan, *The Design, Modeling And Optimization Of On-Chip Inductor And Transformer Circuit*, Doctoral dissertation, Stanford University, 1999.

[16] J. Crols, P. Kinget, J. Craninckx, and M. Steyeart, *An analytical model of planar inductors on lowly doped silicon substrates for analog design up to 3GHz*, Digest of VLSI Circuits, pp. 28-29, 1996.

[17] J. O. Voorman, *Continuous-time analog integrated filters*, IEEE Press, 1993.

[18] H. E. Bryan, *Printed inductors and capacitors*, Tele-tech and Electronic Industries, December 1955.

[19] Yu Cao, R. A. Groves, N. D. Zamdmer, J. O. Plouchart, R. A. Wachnik, Xuejue Huang, T. J. King, and Chenming Hu, *Frequency-independent equivalent circuit model for on-chip spiral inductors*, Proc. IEEE Custom Integrated Circuits Conference, pp. 217–220, 2002.

[20] T. Kamgaing, T. Myers, M. Petras, and M. Miller, *Modeling of frequency dependent losses in two-port and three-port inductors on silicon*, IEEE Radio Frequency Integrated Circuits Symposium, Pages 307–310, 2002.

[21] Ban-Leong Ooi, Dao-Xian Xu, Pang-Shyan Kooi, and Fu-Jiang Lin, *An improved prediction of series resistance in spiral inductor modeling with eddy-current effect*, IEEE Trans. Microwave Theory and Techniques, Vol. 50, Pages 2202-2206, Sept. 2002.

[22] W. B. Kuhn and N. M. Ibrahim, *Approximate analytical modeling of current crowding effects in multi-turn spiral inductors*, Digest of Microwave Symposium, Pages 405-408, June 2002.

[23] F. M. Rotella, V. Blaschke, and D. Howard, *A broad-band scalable lumped-element inductor model using analytic expressions to incorporate skin effect, substrate loss, and proximity effect*, Digest of IEEE International Electron Device Meeting, Pages 471–474, Dec. 2002.

[24] D. Melendy, P. Francis, C. Pichler, Hwang Kyuwoon, G. Srinivasan, and A. Weisshaar, *Wide-band compact modeling of spiral inductors in RFICs*, Digest of Microwave Symposium, Pages 717–720, June 2002.

[25] X. Z. Xiong, V. F. Fusco, and B. Toner, *Optimized design of spiral inductors for Si RF IC's*, High Frequency Postgraduate Student Colloquium, Pages 51–58, Sept. 2002.

[26] Chia-Hsin Wu, Chih-Chun Tang, and Shen-Iuan Liu, *Analysis of on-chip spiral inductors using the distributed capacitance model*, IEEE Journal of Solid-St. Circuits, Vol. 38, Pages 1040–1044, June 2003.

[27] H. B. Erzgraber, M. Pierschel, G. G. Fischer, T. Grabolla, and A. Wolff, *High performance integrated spiral inductors based on a minimum AC difference voltage principle*,Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems, Pages 71-74, April 2000.

[28] C. P. Yue and S. S. Wong, *On-chip spiral inductors with patterned ground shields for Si-based RF ICs*, IEEE Journal of Solid-State Circuits, Vol. 33, Pages 743–752, May 1998.

[29] Joonho Gil and Hyungcheol Shin, *Simple wide-band on-chip inductor model for silicon-based RF ICs*, International Conference on Simulation of Semiconductor Processes and Devices, Pages 35–38, Sept. 2003.

[30] H. Lakdawala, X. Zhu, H. Luo, S. Santhanam, L. R. Carley, and G. K. Fedder, *Micromachined high-Q inductors in a 0.18-μm copper interconnect low-k dielectric CMOS process*, IEEE Journal of Solid-State Circuits, Vol. 37, Pages 394–403, Mar. 2002.

[31] D. M. Krafcsik and D. E. Dawson, *A Closed-Form Expression for Representing the Distributed Nature of the Spiral Inductor*, Microwave and Millimeter-Wave Monolithic Circuits, Vol. 86, Pages 87–92, June 1986.

[32] K. Murata, T. Hosaka, and Y. Sugimoto, *Effect of a ground shield of a silicon on-chip spiral inductor*, Asia-Pacific Microwave Conference, Pages 177-180, Dec. 2002.

[33] Y. E. Chen, D. Bien, D. Heo, and J. Laskar, *Q-enhancement of spiral inductor with N+-diffusion patterned ground shields*, Digest of IEEE International Microwave Symposium, Vol. 2, Pages 1289-1292, May 2001.

[34] R. Mernyei, R. Darrer, M. Pardoen, and A. Sibrai, *Reducing the substrate losses of RF integrated inductors*, IEEE Microwave and Guided Wave Letters, Vol. 8, Pages 300–301, Sept. 1998.

[35] J. N. Burghartz, *Progress in RF Inductors on Silicon-Understanding Substrate Losses*, Digest of IEEE International Electron Devices Meeting, Pages 523-526, Dec. 1998.

[36] K. T. Chan, C. H. Huang, A. Chin, M. F. Li, Dim-Lee Kwong, S. P. McAlister, D. S. Duh, and W. J. Lin, Large *Q-factor improvement for spiral inductors on silicon using proton implantation*, IEEE Microwave and Wireless Components Letters, Vol. 13, Pages 460–462, Nov. 2003.

[37] Jun-Bo Yoon, Yun-Seok Choi, Byeong-Il Kim, Yunseong Eo, and Euisik Yoon, *CMOS-compatible surface-micromachined suspended-spiral inductors for multi-GHz silicon RF ICs*, IEEE Electron Device Letters, Vol. 23, Pages 591–593, Oct. 2002.

[38] Liang-Hung Lu, G. E. Ponchak, P. Bhattacharya and L. P. B. Katehi, High-Q X-band and *K-band Micromachined Spiral Inductors for Use in Si-based Integrated Circuits*, Digest of Silicon Monolithic Integrated Circuits in RF Systems, Pages 108-112, April 2002.

[39] H. Yoshida, H. Suzuki, Y. Kinoshita, H. Fujii, and T. Yamazaki, *An RF BiCMOS process using high f_{SR} spiral inductor with premetal deep trenches and a dual recessed bipolar collector sink*, IEEE International Electron Devices Meeting, Pages 213–216, Dec. 1998.

[40] Ju-Ho Son, Sun-Hong Kim, Seok-Woo Choi, Do-Hwan Rho, and Dong-Yong Kim, *Multilevel monolithic 3D inductors on silicon*, Proc. IEEE Midwest Circuits and Systems Symposium, Vol. 2, Pages 854-857, Aug. 2001.

[41] D. C. Edelstein and J. N. Burghartz, *Spiral and solenoidal inductor structures on silicon using Cu-damascene interconnects*, Proc. IEEE Interconnect Technology Conference, Pages 18–20, June 1998.

[42] Young-Jun Kim and M. G. Allen, *Integrated solenoid-type inductors for high frequency applications and their characteristics*, IEEE Electronic Components and Technology Conference, Pages 1247–1252, May 1998.

[43] Jun Zou, Chang Liu, D.R. Trainor, J. Chen, J. E. Schutt-Aine, and P.L. Chapman, *Development of three-dimensional inductors using plastic deformation magnetic assembly (PDMA)*, IEEE Trans. Microwave Theory and Techniques, Vol. 51, Pages 1067-1075, 2003.

[44] J. N. Burghartz, M. Soyuer, and K. A. Jenkins, *Microwave inductors and capacitors in standard multilevel interconnect silicon technology*, IEEE Trans. Microwave Theory and Techniques, Vol. 44, Pages 100–104, 1996.

[45] L. F. Tiemeijer, D. Leenaerts, N. Pavlovic, and R. J. Havens, *Record Q spiral inductors in standard CMOS*, IEEE International Electron Devices Meeting, Pages 40.7.1-40.7.3, Dec. 2001.

[46] John R. Long and Miles A. Copeland, *The Modeling, Characterization, and Design of Monolithic Inductors for Silicon RF IC's*, IEEE Journal of Solid-State Circuits, Vol. 32, March 1997

[47] Jose M. Lopez-Villegas, Josep Samitier, Charles Cane, Pere Losantos, and Joan Bausells, *Improvement of the quality factor of RF integrated Inductors by Layout Optimization*, IEEE Transactions on Microwave Theory and Techniques, Vol. 48, January 2000.

[48] H. Feng, G. Jelodin, K. Gong, R. Zhan, Q. Wu, C. Chen, and A. Wang, *Super compact RFIC inductors in 0.18 μm CMOS with copper interconnects*, IEEE Radio Frequency Integrated Circuits Symposium, Pages 443–446, June 2002.

[49] Chih-Chun Tang, Chia-Hsin Wu, and Shen-Iuan Liu, *Miniature 3-D inductors in standard CMOS process*, IEEE Journal of Solid-State Circuits, Vol. 37, Pages 471–480, 2002.

[50] Ban-Leong Ooi, Dao-Xian Xu, and Pang-Shyan Kooi, *A comprehensive explanation on the high quality characteristics of symmetrical octagonal spiral inductor*, IEEE Radio Frequency Integrated Circuits Symposium, Pages 259–262, June 2003.

[51] Sang-Gug Lee, Gook-Ju Ihm, and Won-Chul Son, *Design and analysis of symmetric dual-layer spiral inductors for RF integrated circuits*, IEEE Asia Pacific Conference, Pages 5–8, 1999.

[52] Feng Ling, Jiming Song, Telesphor Kamgaing, Yingying Yang, William Blood, Michael Petras, and Thomas Myers, *Systematic analysis of inductors on silicon using EM simulations*, Electronic Components and Technology Conference, 2002.

[53] Mina Danesh and John R. Long, *Differentially Driven Symmetric Microstrip Inductors*, IEEE Trans. Microwave Theory and Techniques, vol. 50, Jan. 2002.

[54] A. Niknejad, *Analysis and Simulation of Spiral Inductors and Transformers for ICs* (ASITIC), http://rfic.eecs.berkeley.edu/~niknejad/asitic.html

[55] Ansoft Corporation, HFSS, http://www.ansoft.com/products/hf/hfss/

[56] J. S. Yuan, W. R. Eisenstadt, and J. J. Liou, *A novel lossy and dispersive interconnect model for integrated circuit simulation,* IEEE Trans. Components, Hybrids, and Manufacturing Technology, vol. 13, pp. 275-280, June 1990.

[57] G.L Matthaei,. G.C Chinn, C.H Plott, N Dagli, *A simplified means for computation for interconnect distributed capacitances and inductances*, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 11, pp. 513-524, April 1992.

[58] Sunderarajan S. Mohan, Mari del Mar Hershenson, Stephen P. Boyd, and Thomas H. Lee, *Simple Accurate Expressions for Planar Spiral Inductances*, IEEE J. Solid-State Circuits, vol. 34, Oct. 1999.

[59] Haitao Gan, *On-Chip Transformer Modeling, Characterization, and Applications in Power AND Low Noise Amplifiers,* Doctoral dissertation, Department of Electrical Engineering, Stanford University, March 2006.

[60] Ji Chen and Juin J. Liou, *Improved and Physics-Based Model for Symmetrical Spiral Inductors*, IEEE Transactions on Electron Devices, VOL.53,NO.6, June 2006