EMC and the Printed Circuit Board: Design, Theory, and Layout Made Simple. Mark I. Montrose
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Signal Integrity and Crosstalk

7.1 NEED FOR SIGNAL INTEGRITY

Every year, clocks and system speeds become faster. Clocks in computer systems that now operate at frequencies above 300 MHz will rise into the GHz range in the near future. Processors currently in development will reach new levels of high-speed performance. Computer systems, local-area networks, wide-area networks, and cellular and optical-fiber systems are becoming more common every day.

As the demand for more and faster computer chips increases, the chip vendors are also struggling to increase the yield and decrease the cost of the individual die obtained from each raw wafer. One method for simultaneously achieving all of these goals is to make more die on each silicon wafer using a process known as "die shrink." In die shrink, the photolithographic manufacturing steps are adjusted in order to reduce the size of each transistor gate without having to redesign the individual transistor components or their metallic interconnects. When the distances between individual gates on a die decrease, the time it takes for electrons to propagate between the gates also decreases. In addition, as the transistors are made smaller, the transistors switch faster. As a result, the component becomes faster with the same functional performance, all at practically zero additional cost per semiconductor wafer.

Today's chip manufacturing processes commonly use transistors and interconnects with submicron dimensions. Components made in the 1980s used fabrication technologies with 2- to 5-micron line widths. With 5-micron technologies, edge transition rates were in the 20-ns range. With 0.12- to 0.25-micron process technologies, speeds in the low picoseconds are now possible and will become the standard for most semiconductor products in the near future.

Chip manufacturing equipment is very expensive. Major new semiconductor fabrication facilities typically cost from $1 billion to $2 billion. The time it takes to incorpo-

rate a manufacturing process for a new silicon wafer is typically six to eight weeks. As a result, chip manufacturers are constantly changing their process steps in order to accommodate a smaller component and to achieve a higher and more uniform throughput of semiconductor die. It is much less expensive for a chip manufacturer to die shrink a standard CMOS logic component by 50% and label it with a slower speed rating than it is to redesign or retool the manufacturing process. The shrunken chip will still operate as desired; however, the "new" chip edge rate transitions are much faster than the "old" ones.

TTL logic is becoming obsolete with high-technology products; hence, newer logic families with higher frequency components are being developed. The component will operate as desired, but the "real" edge rate transitions are much faster. Recall that EMI spectral profiles are dominated by the edge rate transition times and their related harmonic frequency components. The process of marking chip components with a slower speed rating explains why a second source of components for the same function may result in significant EMI concerns that are not encountered with the original part. If a product once complied with EMI regulatory requirements for emissions and immunity, and the product now fails, it could be that the vendor took the device through the die shrink process without the customer knowing it. A typical logic designer will usually accept a manufacturer's faster component without considering EMI or signal integrity issues.

When components operate at high frequencies, signal edge rates become faster to accommodate the smaller clock pulse intervals. As a result, RF spectral distribution increases. When this level of technology is reached, signal integrity CAD tools (circuit simulation programs with high-frequency models) must be used to determine the effects of fast edge rates, long trace lengths, and parasitic capacitance and inductance of circuit elements. This includes the behavioral characteristics of the source and load devices, the conductor impedances, the physical and electrical parameters of the PCB materials, and numerous other parameters that become a prime concern for the designer during the circuit simulation and layout cycle.

To define high-speed design characteristics, a simple driver-receiver circuit is used to illustrate signal integrity problem, shown in Fig. 7.1 [5]. As long as the interconnects are "short" and the clock rates are "low," the receivers act as loads for the driver. This loading can affect the receiver's output waveform. The effect of loading the traces is counted as lumped capacitance to ground in addition to the capacitance provided by the receiver loads.

When the trace length becomes electrically "long,"—that is, when the edge transition time of the signal is less than the time it takes for the signal to travel from source to load and return from load to source—signal integrity concerns increasingly arise. Within the time period that the signal's transition occurs between the high and low state, the impedance of the trace becomes the actual load for the driver. This load is in addition to the input impedance of the receivers. Transmission line effects such as reflections, overshoot, undershoot, and crosstalk will distort the transmitted signal. Classical lumped circuit theory no longer applies under these conditions, and a distributed circuit model must be used in the circuit simulation design program [13].

To better describe this signal integrity concern, we reexamine why edge rate, and not clock frequency, is of primary concern. For example, a relatively low-frequency 1-MHz clock with a rise time of 1 ns has transmission line effects only during the transition time as the periodicity of the waveform is long. The signal will eventually attain steady state. Because of the fast edge rate, if the transmission line length is long, the sig-

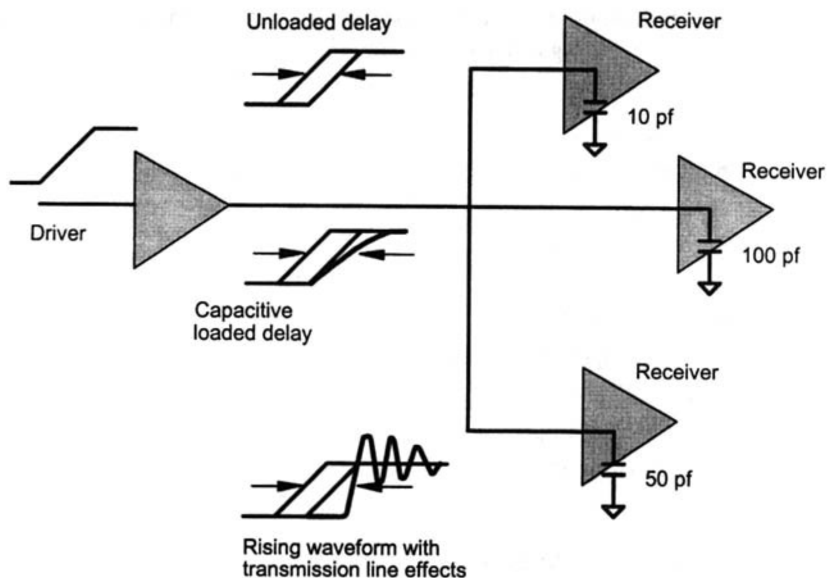


Figure 7.1 Transmission line effects in a trace.

nal may falsely trigger circuits, for the threshold voltage will vary at different portions of the timing cycle. Ringing and reflections may also exist.

A trapezoidal signal with a finite rise and fall time has a spectral distribution based on the Fourier component of the signal. The fundamental RF frequency is that of the clock itself. The magnitude of the spectral distribution decreases at the rate of 20 dB per decade up to the frequency that corresponds to the rise time. For example, a 5V, 100 MHz clock with a 50% duty cycle and a 1-ns edge rate has a fundamental RF frequency with an amplitude of approximately 3V. The 1-GHz component of this clock will have an amplitude of approximately 0.3V. Depending on the application of the circuit, undesired effects may occur along with switching noise and ground bounce. In mixed logic designs, this is a concern, especially if a 0.3V noise margin requirement exists. As a rule of thumb, the trace length should be between 20 and 25% of the signal rise and fall time.

For example, all logic and analog components have some sensitivity to changes in power supply voltages. This sensitivity may be reflected in changes in the output levels or in the switching thresholds at the input pins. The amount of performance degradation as a function of power supply voltage must be determined during the design cycle. A tradeoff between power supply accumulation and noise erosion needs to be performed, taking into consideration all other components and their unique noise margin requirements.

Lack of an optimal 0V reference structure is common in high-speed networks and designs. Inductance will always be present between the virtual and actual ground because of interconnect (trace) and lead inductance. If many clock drivers switch simultaneously, a voltage proportional to the rate of change of current with time is induced in the trace. This simultaneous switching may cause false switching of devices on victim traces. Vias, bond wires, and package connector pins also contribute to this inductive effect, which is also known as ground bounce or delta I noise. Component packages with *no* internal ground planes are the worst offender!

The following are potential sources of noise that may cause signal functionality concerns or make a logic signal unusable.

- Reflections
- Ground bounce
- Crosstalk
- Reference accuracy
- Thermal offsets
- Ground offsets
- Power supply variations
- Trace IR drop
- Ground IR drop
- Terminator noise

7.2 REFLECTIONS AND RINGING

Reflections are an unwanted byproduct in digital logic designs. Ringing within a transmission line contains both overshoot and undershoot before stabilizing to a quiescent level and is a manifestation of the same effect. *Overshoot* is the effect of excessive voltage above the power rail or below the ground reference. Excessive voltage levels below ground reference is not undershoot. Undershoot is a condition where the voltage level does not reach the desired amplitude for both maximum and minimum transition levels. Components must have a sufficient tolerance rating for voltage margin requirements. Both overshoot and undershoot can be controlled by proper terminations and proper PCB and IC package design. Overshoot and undershoot, if severe enough, can overstress devices and cause damage or even failure.

For an unterminated transmission line, ringing and reflected noise are one and the same. This can be observed with measurement equipment at the frequency associated as a quarter wave length of the transmission line, as is most apparent in an unterminated, point-to-point trace. The driven end of the line is commonly tied to AC ground with a low-impedance (5–20 ohms) load. This transmission line closely approximates a quarter wavelength resonator (stub shorted on one end, open on the other). Ringing is the resonance of that stub.

As signal edges become faster, consideration must be given to propagation and reflection delays of the routed trace. If the propagation time and reflection within the trace are longer than the edge transition time from source to load, an *electrically long trace* will exist. This electrically long trace can cause signal integrity problems depending on the type and nature of the signal. These problems include crosstalk, ringing, and reflections. EMI concerns are usually secondary to signal quality when referenced to electrically long lines. Although long traces can exhibit resonances, other suppression and containment measures implemented within the product may mask the EMI energy created. As a result, the device may cease to function properly if impedance mismatches exist in the system between source and load. Reflections are frequently both a signal quality and an EMI issue when the edge time of the signals constitutes a significant percentage of the propa-

gation time between the device load intervals. Solutions to reflection problems may require extending the edge time (slowing the edge rate) or decreasing the distance between load device intervals.

Reflections from signals on a trace are one source of RF noise within a network. Reflections are observed when impedance discontinuities exist. These discontinuities consist of

- Changes in trace width
- Improperly matched termination networks
- Lack of terminations
- T-stubs or bifurcated traces[1]
- Vias between routing layers
- Varying loads and logic families
- Large power plane discontinuities
- Connector transitions
- Changes in impedance of the trace

When a signal propagates down a transmission line, a fraction of the source voltage will initially propagate down the trace. This source voltage is a function of frequency, edge rate, and amplitude. Ideally, all traces should be treated as a transmission line. Transmission lines are described by their characteristic impedance, Z_o, and propagation delay, t_{pd}. These parameters are dependent on the inductance and capacitance per unit length of the trace, the actual interconnect component, the physical dimensions of the interconnect, the RF return path, and the permittivity of the insulator between them. Propagation delay is also a function of the length of the trace and dielectric constant of the material. When the load impedance at the end of the interconnect equals that of the characteristic impedance of the trace, no signal is reflected.

A typical transmission line is shown in Fig. 7.2. Here we notice that

- Maximum energy transfer occurs when $Z_{out} = Z_o = Z_{load}$.
- Minimum reflections will occur when $Z_{out} = Z_o$ and $Z_o = Z_{load}$.

If the load is not matched to the transmission line, a voltage waveform will be reflected back toward the source. The value of this reflected voltage is

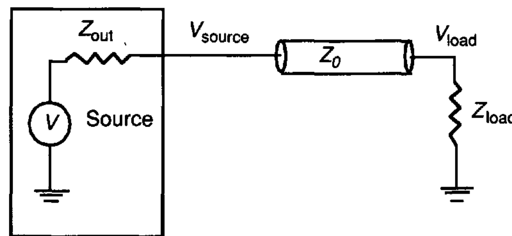


Figure 7.2 Typical transmission line system.

[1]A bifurcated trace is a single trace that is broken up into two traces routed to different locations.

$$V_r = V_o\left(\frac{Z_L - Z_o}{Z_L + Z_o}\right) \tag{7.1}$$

where V_r = reflected voltage
V_o = source voltage
Z_L = load resistance
Z_o = characteristic impedance of the transmission path

When Z_{out} is less than Z_o, a negative reflected wave will be created. If Z_L is greater than Z_o, a positive wave is observed. The wave will repeat itself at the source driver if the impedance is different from the line impedance, Z_o.

Equation (7.1) relates the reflected signal in terms of voltage. When a portion of the propagating signal reflects from the far end, this component of energy will travel back to the source. As it reflects back, the reflected signal may cross over the tail of the incoming signal. At this point, both signals will propagate simultaneously in opposite directions, neither interfering with each other.

We can derive an equation for the reflected wave. The reflection equation, Eq. (7.2), is for the fraction of the propagating signal that is reflected back toward the source.

$$\%\ \text{reflection} = \left(\frac{Z_L - Z_o}{Z_L + Z_o}\right) \times 100 \tag{7.2}$$

This equation applies to any impedance mismatch, regardless of voltage levels. Use Z_o for the signal source of the mismatch and Z_L for the load. To improve the noise margin budget and requirements for logic devices, positive reflections are acceptable as long as they do not exceed V_{Hmax} of the receive component.

A forward-traveling wave is initiated at the source in the same manner as the incoming backward-traveling wave, which is the original pulse returned back to the source by the load. The corresponding points in the incoming wave are reduced by the percentage of the reflection on the line. The process of repeated reflections can continue as re-reflections at both the source and load. At any point in time, the total voltage (or current) becomes the *sum* of all the individual voltage (or current) sources present. It is for this reason that we may observe a 7V signal on the output of a source driver while the power supply is operating at 5V. The term *ringback* is the effect of the rising edge of a logic transition that meets or exceeds the logic level required for functionality, and then re-crosses the threshold level before settling down. Ringback can be caused by a mismatch of logic drivers and receivers, poor termination techniques, and impedance mismatches of the network [14].

Sharp transitions in a trace may be observed through use of a Time Domain Reflectometer (TDR). Multiple reflections caused by impedance mismatches are observed by a sharp jump in the signal voltage level. These abrupt transitions usually have rise and fall times that can be comparable to the edge of the original pulse. The time delay from the original pulse to the occurrence of the first reflection can be used to determine the location of the mismatch. A TDR determines discontinuities within a transmission line structure. An oscilloscope observes reflections. Both types of discontinuities are shown in Fig. 7.3. Although several impedance discontinuities are shown, only one reflection is illustrated [16].

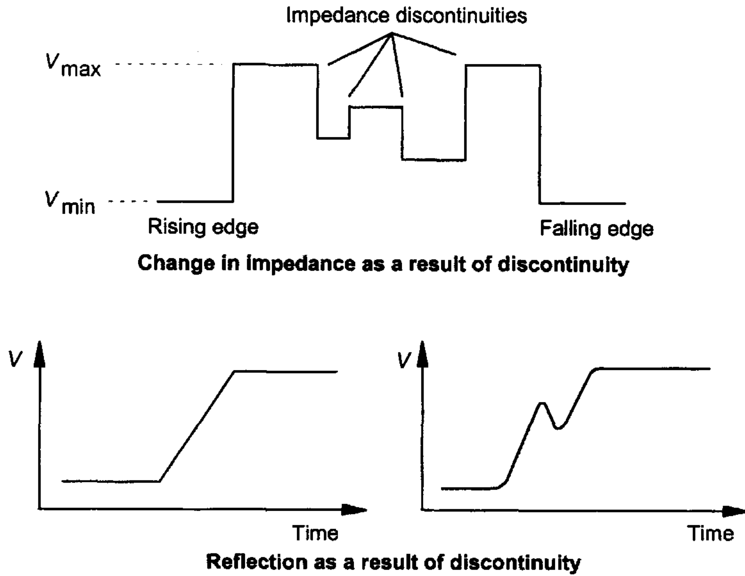


Figure 7.3 Discontinuities in a transmission line.

7.2.1 Identification of Signal Distortion

The shape of signal distortion can indicate the type of signal quality problem. When a signal deviates from its desired shape, the waveform will indicate the specific problem. The distortion on the leading or trailing edge of a pulse is often referred to as a *glitch*. Usually, little attention is paid to the detailed shape of the glitch. We examine two common waveforms that indicate signal quality problems in Fig. 7.4.

Ringing is caused by reflections with significant impedance mismatch (a result of resonant effects) in the trace and will corrupt signal quality and cause possible nonfunctionality of the circuit. Ringing within a trace also indicates that excessive inductance may be present in the network. The signal that is ringing will either add or subtract (voltage phasing of the signal). Depending on the net result of phasing, the signal may be degraded

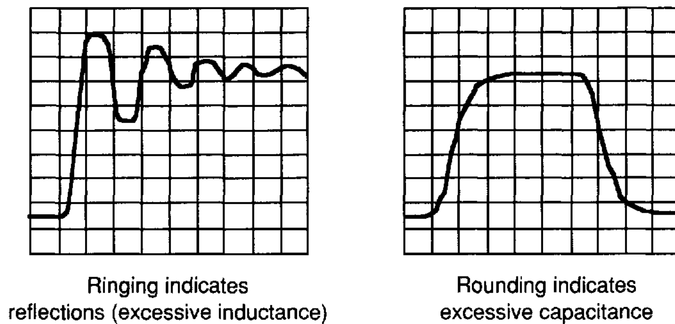


Figure 7.4 Ringing and rounding of a signal within a trace (identifying distortion).

to the point where it becomes an invalid or metastable logic state. Knowledge and proper use of transmission line theory allow signals to travel between the source and load without creating a functionality concern.

An *underdamped* circuit with excessive trace inductance can cause the edges of a signal pulse to ring. Ringing is a damped sinusoidal oscillation or resonance. For a circuit to ring or oscillate, there must be capacitance. *Capacitance* is a necessary part of the circuit load and will always be present. Excessive wiring inductance is also a cause of ringing. Ringing may be minimized by adding series resistance or providing proper termination.

Rounding indicates excessive capacitance. When the pulse edge is rounded, the circuit is *overdamped*. Shunt capacitance always exists in both the trace and the input to the load. The parallel combination of these two capacitors (trace and load) determines total shunt capacitance. Excessive series resistance in the signal source may also cause rounding due to the time constant $\tau = RC$. The impedance ratios between source, line, and load are an important requirement for circuit design parameters.

7.2.2 Conditions That Create Ringing

Figure 7.5 illustrates a typical circuit using lumped components. A source driver with internal series resistance, R_s, is shown along with inductance of the trace, L (which includes component lead wires), and distributed capacitance from trace to ground, X_c. This is in addition to the internal capacitance of the receiver. Within this circuit, additional resistance, inductance, and capacitance may also exist but is not included in this simple example.

Assume there is capacitive reactance of the trace plus load ($X_c = 1/\omega C$) which is much less than the load resistance (R_L) at high frequency. When a trace is physically short, the semiconductor package and decoupling capacitor lead-length inductance become the dominant cause of ringing. This is analyzed in terms of lumped circuitry where the damping of a simple RLC series circuit applies. The condition for ringing (underdamped) is

$$\text{Ringing} = R^2X_c/4 > 1 \tag{7.3}$$

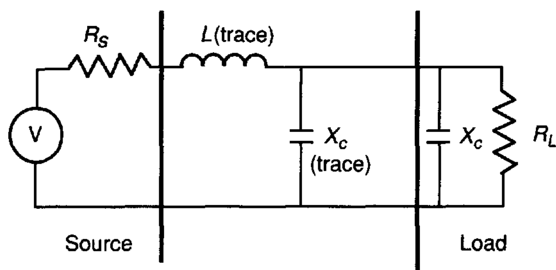


Figure 7.5 Equivalent circuit for ringing or rounding.

For rounding (overdamped)

$$\text{Rounding} = X_c > 4L/R^2 \tag{7.4}$$

The inductance that causes ringing is often very small. Sometime 0.5 nH is more than enough to cause signal functionality concerns. A 1-inch trace, located directly above a ground plane, could easily exceed this inductance value.

Figure 7.6 shows what occurs in a typical PCB layout as it relates to signal integrity: reflections and ringing. Notice the overshoot of up to 7V at the load and possible false triggering of a low logic state at 3.5V. At the source, the reflected signal also has an overshoot of −1.0V and ringing at 3V. False trigger can occur with 3V ringing for certain logic families. For a trapezoidal waveform, the ringing illustrated in Fig. 7.6 distorts the spectra, emphasizing the frequency of the ringing or the spectra of the complex waveform.

Figure 7.6, plot A, shows that if a properly terminated transmission line is present, a smooth signal pulse will be propagated down the trace from source to load. Ringing, which always exists in some manner, is usually minor compared to what can happen when a transmission line is not matched or has impedance discontinuities. Active components always exhibit some ringing generated by the output switching transistors. These transistors are generally nonideal or have nonperfect drive characteristics. These nonideal or nonperfect characteristics are due to the manufacturing process and design of the circuit. The behavioral models used for signal integrity analysis usually are considered as being ideal. In actual usage, behavioral models often may not illustrate real, important transmission line effects.

Figure 7.6, plot B, shows an active load circuit with an electrically long trace. Ringing (overshoot and undershoot) is present. Ringback, if severe enough, can falsely trigger the load into believing that a logic 0 state is present. This false triggering can cause im-

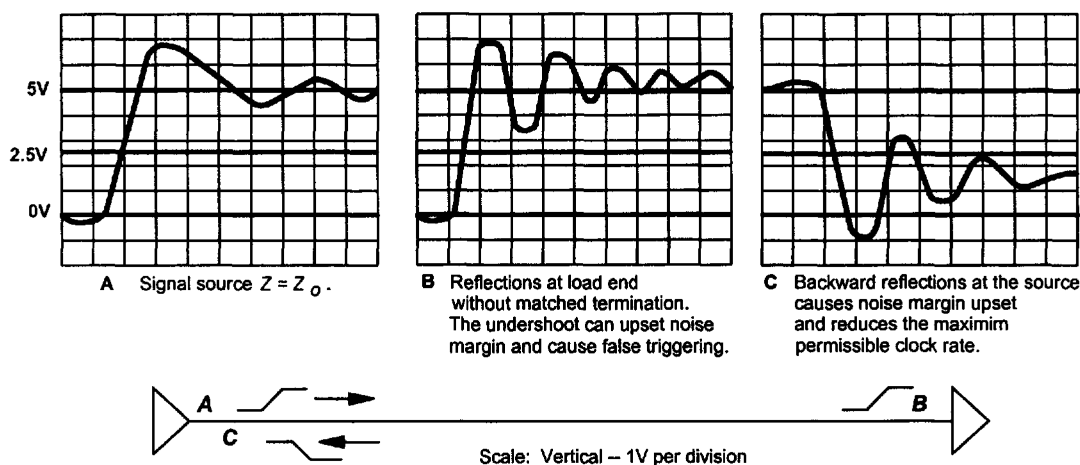


Figure 7.6 Ringing on traces.

proper operation of the circuit. If the length of the trace is very long with respect to the propagation delay of the signal (source-to-load and load-to-source) or if there are long intervals between devices, reflections will be created and bounced back and forth between these end points.

Figure 7.6, plot C, indicates what happens back at the source driver of an unterminated transmission line. Backward reflections can cause noise margin upset and will corrupt the quality of the desired signal if another clock transition occurs when the reflected pulse reaches the driver at the wrong point in time. These reflections are also created by an electrically long signal trace (or long loading intervals) as described for Fig. 7.6, plot B. When backward reflections occur, the edge rate desired for proper operation is reduced to a slower time period. This signal degradation may be sufficient to prevent other sections of the PCB from functioning at the intended speed of operation. Hence, performance is degraded, or the circuit may become nonfunctional.

The relationship between PCB line length and logic families is illustrated in Table 7.1. Details on how this table is created are presented later in this chapter.

TABLE 7.1 Logic Families and Important Characteristic Parameters

Logic Family (Sample List)	Rise/Fall Time (Approx.) T_r/T_f	Maximum Non-transmission Line Trace Length (Microstrip) $L_{max} = 9 * T_r$	Maximum Non-transmission Line Trace Length (Stripline) $L_{max} = 7 * T_r$
74L xxx	31–35 ns	279 cm (110″)	217 cm (85.4″)
74C xxx	25–60 ns	225 cm (88.5″)	175 cm (69″)
74HC xxx	13–15 ns	117 cm (46″)	91 cm (36″)
74 xxx	10–12 ns	90 cm (35.5″)	70 cm (27.5″)
(flip-flop)	15–22 ns	135 cm (53″)	105 cm (41″)
74LS xxx	9.5 ns	85.5 cm (34″)	66.5 cm (26″)
(flip-flop)	13–15 ns	117 cm (46″)	91 cm (36″)
74H xxx	4–6 ns	36 cm (14.2″)	28 cm (11″)
74S xxx	3–4 ns	27 cm (10.6″)	21 cm (8.3″)
74HCT xxx	5–15 ns	45 cm (18″)	35 cm (14″)
74ALS xxx	2–10 ns	18 cm (7″)	10 cm (4″)
74ACT xxx	2–5 ns	18 cm (7″)	10 cm (4″)
74F xxx	1.5–1.6 ns	10.5 cm (4″)	10.5 cm (4″)
ECL 10K	1.5 ns	10.5 cm (4″)	10.5 cm (4″)
ECL 100K	0.75 ns	6 cm (2.4″)	5.25 cm (2″)
BTL	1.0	9 cm (3.5″)	7 cm (2.8″)
LVDS	0.3*	2.7 cm (1.1″)	2.1 cm (0.8″)
GTL+	0.3*	2.7 cm (1.1″)	2.1 cm (0.8″)
GaAs	0.3*	2.7 cm (1.1″)	2.1 cm (0.8″)

Assume 1.7 ns/ft (0.14 ns/in. or 0.36 ns/cm) for microstrip. Propagation delay for FR-4, $\varepsilon_r = 4.6$.
Assume 2.2 ns/ft (0.18 ns/in. or 0.47 ns/cm) for stripline. Propagation delay for FR-4, $\varepsilon_r = 4.6$.
T_r and T_f depends greatly on load capacitance, supply voltage, and IC complexity.
Note: T_r and T_f will differ between device manufacturers because of the fabrication process used.
*These are the fastest edge rate values.

7.3 CALCULATING TRACE LENGTHS (ELECTRICALLY LONG TRACES)

When designing a transmission line, PCB designers need a method that allows quick determination if a trace routed on a PCB can be considered electrically long during component placement. A simple calculation is available that determines whether the approximate length of a routed trace is electrically long under typical conditions. When determining whether a trace is electrically long, we must think in the *time domain.* The equations provided below are best used when doing preliminary component placement on a PCB. For extremely fast edge rates, detailed calculations are required based on the actual dielectric constant value of the core and prepreg material. Chapter 6 provides equations if more accuracy is required.

Assuming a typical velocity of propagation that is 60% the speed of light, we can calculate the maximum permissible unterminated line length per Eq. (7.5). This equation is valid when the two-way propagation delay (source-load-source) equals the signal rise time.

$$l_{max} = \frac{t_r}{2\, t'_{pd}} \tag{7.5}$$

where t_r is edge rate (ns)
t'_{pd} is propagation delay (ns)
l_{max} maximum routed track length (cm)

Figure 7.7 illustrates this equation for quick reference with a dielectric constant of 4.6.

To simplify Eq. (7.5), we use the real value of propagation delay (actual dielectric constant based on frequency of interest; see Chapter 6) from FR-4 material using microstrip and stripline impedance equations (factoring in propagation delay and constant). Equations (7.6) and (7.7) are presented for determining the maximum electrical line length before termination is required. This length is for round-trip distance. *The one-way length, from source to load is one-half the value of l_{max} calculated below.* The following calculations are for a dielectric constant of 4.6.

$$\begin{aligned} l_{max} &= 9 * t_r && \text{(for microstrip topology—in cm.)} \\ l_{max} &= 3.5 * t_r && \text{(for microstrip topology—in in.)} \end{aligned} \tag{7.6}$$

$$\begin{aligned} l_{max} &= 7 * t_r && \text{(for stripline topology—in cm.)} \\ l_{max} &= 2.75 * t_r && \text{(for stripline topology—in in.)} \end{aligned} \tag{7.7}$$

For example, if a signal edge is 2 ns, the maximum round-trip, unterminated trace length when routed on microstrip is

$$l_{max} = 9 * t_r = 18 \text{ cm } (7'')$$

When this same clock trace is routed on stripline, the maximum unterminated trace length of this 2-ns signal edge becomes

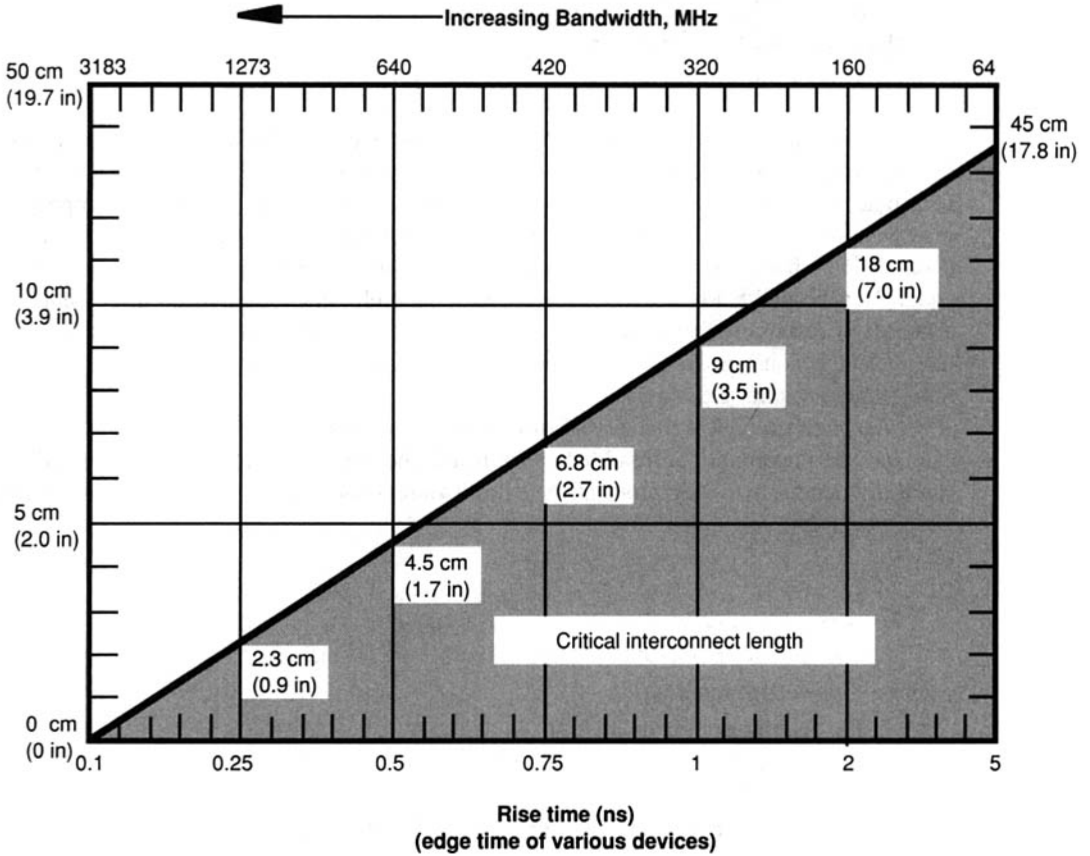


Figure 7.7 Maximum unterminated line length versus signal edge rate (FR-4 material).

$$l_{max} = 7 * t_r = 14 \text{ cm } (5.5'')$$

These equations are also useful when we are evaluating the propagational time between load intervals on a line with multiple loads.

To calculate the constant for l_{max}, use the following example, which is in inches.

EXAMPLE

$$l_{max} = x\left(\frac{1}{[t_{pd}/a]}\right) \quad \text{(cm)}$$

where $a = 30.5$ for cm, 12 for inches; $x = 0.5$, converts transmission line to one way path

$t_{pd} = 1.017\sqrt{0.475\,\varepsilon_r + 0.67}$ (for microstrip); $t_{pd} = 1.017\sqrt{\varepsilon_r}$ (for stripline)

example for $\varepsilon_r = 4.1$, $l_{max} = 8.9$ for microstrip (in cm) or 3.5 (in inches)

$l_{max} = 6.9$ for stripline (in cm) or 2.7 (in inches)

If a trace or interval is longer than l_{max}, then termination should be implemented, for signal reflections (ringing) may occur in this electrically long trace. Even with good termination, a finite amount of RF currents can still be in the trace. For example, use of a series resistor (source location) will achieve the following:

- Minimize RF currents within the trace.
- Absorb reflections (ringing).
- Match trace impedance.
- Minimize overshoot and undershoot.
- Reduce RF energy generated by slowing down the edge rate of the clock signal.

When placing PCB components during layout that use clocks or periodic waveform signals, these components must be located so that the signal traces are routed for the best straight-line path possible with minimal trace length and number of vias in the route. Each via will add inductance and discontinuities to the trace (approximately 1–3 nH each). Inductance in a trace may cause signal integrity concerns, impedance mismatches, and potential RF emissions. Inductance in a trace allows this wire to act as an antenna. The faster the edge rate of the clock signal, the more important this design rule becomes. If a periodic signal or clock trace must traverse from one routing plane to another, this transition should occur at a component lead (pin escape) and not anywhere else. If possible, additional inductance presented to the trace can be reduced from using two less vias.

Equation (7.8) is used to determine if a trace or loading interval is electrically long and requires termination.

$$l_d < l_{max} \tag{7.8}$$

where l_{max} is the calculated maximum trace length and l_d is the length of the trace route as measured in the actual board layout. Keep in mind that l_d is the round-trip length of the trace.

Ideally, trace impedance should be kept at ± 10%. In some cases, ±20–30% may be acceptable only after careful consideration has been given to performance. The width of the trace, its height above a reference plane, dielectric constant of the board material, plus other microstrip and stripline constants determine the impedance of the trace (see Eqs. 6.7 through 6.20). It is always best to maintain constant impedance control at all times for any dynamic signal condition.

An example used to determine whether it is necessary to terminate a signal trace using characteristic impedance, propagation delay, and capacitive loading is now presented.

MICROSTRIP EXAMPLE

A 5-ns edge rate device is provided on a 5-inch surface microstrip trace. Six loads (components) are distributed throughout the route. Each device has an input capacitance of 6 pF. Is termination required for this route?

Geometry

Trace width, W = 0.010 in.
Height above a plane, H = 0.012 in.

Trace thickness, $T = 0.002$ in.
Dielectric constant, $\varepsilon_r = 4.6$

A. Calculate characteristic impedance and propagation delay detailed in Chapter 6 [Eqs. (6.7) and (6.9)].

$$Z_o = \left(\frac{79}{\sqrt{\varepsilon_r + 1.41}}\right) Ln \left(\frac{5.98\,H}{0.8\,W + T}\right)$$

$$Z_o = \left(\frac{79}{\sqrt{4.6 + 1.41}}\right) Ln \left(\frac{5.98 \times 12}{0.8 \times 10 + 2}\right) = 63.5\ \Omega$$

$$t_{pd} = 1.017 * \sqrt{0.475\,\varepsilon_r + 0.67} = 1.72 \text{ ns / ft} \quad (0.143 \text{ ns/in.})$$

B. Analyze capacitive loading.

Calculate C_d, distributed capacitance (total normalized input capacitance divided by length).

$$C_d = 6 * C_d/\text{trace length} = (6 * 6 \text{ pF}) / 5 \text{ in.} = 7.2 \text{ pF/in.}$$

Calculate intrinsic capacitance of the trace—Eq. (6.24).

$$C_o = 1000\,(t_{pd}/Z_o) = 1000\,(1.72/63.5) \text{ ns/ft} = 27.0 \text{ pF/ft} = 2.26 \text{ pF /in.}$$

Calculate one-way propagation delay time from the source driver—Eq. (6.21).

$$t'_{pd} = t_{pd}\sqrt{1 + C_d/C_o}$$

$$t'_{pd} = 0.143\sqrt{1 + 7.2 / 2.26} = 0.29 \text{ ns/in. } (3.5 \text{ ns/ft})$$

C. Perform a transmission line analysis.

Ringing and reflections are masked during edge transitions if

$$(2*t'_{pd})*\text{trace length} \le t_r \text{ or } t_f$$

For this situation,

$$(2 * t'_{pd})* \text{ trace length} = (2*0.29 \text{ ns/in.}) * 5 \text{ in.} = 2.9 \text{ ns}$$

Given that the edge rate of the component is $t_r = t_f = 5$ ns and propagation delay is 2.9 ns, termination is not required. Sometimes the guideline of ($3 \times t'_{pd} \times$ trace length) is used as a margin of safety. For this case, propagation delay would be 4.35 ns; hence, termination would still not be needed.

Assume now that the trace is routed stripline. Is termination required?

From above:

$$t_{pd} = 1.017 \times \sqrt{\varepsilon_r} = 2.18 \text{ ns/ft} = 0.18 \text{ ns/in.}$$

$$C_o = t_{pd} / Z_o = 2.18 / 63.5 = 34.3 \text{ pf/ft } (2.86 \text{ pF/in.})$$

$$C_o = 1000\,(t_{pd}/Z_o) = 1000\,(2.18/63.5) = 34.3 \text{ pF/ft } (2.86 \text{ pF/in.})$$

C_d is the same as above (7.2 pF/in.)

$$t'_{pd} = t_{pd}\sqrt{1 + C_d/C_o} = 4.05 \text{ ns/ft } (0.34 \text{ ns/in.})$$

$$2 \times t'_{pd} \times \text{trace length} = 2 \times 0.34 \text{ ns/in.} \times 5 \text{ in.} = 3.4 \text{ ns}$$

Again, this trace would not require termination since 3.4 ns ≤ 5 ns. The propagation delay for stripline is 1.60 ns longer because t_{pd} (unloaded) is substantially greater than microstrip (0.65-ns margin). This factor helps prevent transmission line effects from being masked during edge rate changes.

STRIPLINE EXAMPLE

A 2-ns edge rate device on a 10-inch stripline trace is used. Five logic devices are distributed throughout the route. Each device has an input capacitance of 12 pF. Is termination required for this route?

Geometry

Trace width, $W = 0.006$ in.
Distance from a plane, $B = 0.020$ in.
Trace thickness, $T = 0.0014$ in.
Dielectric constant, $\varepsilon_r = 4.6$

A. Calculate characteristic impedance and propagation delay detailed in Chapter 6. [Use Eqs. (6.13) and (6.15).]

$$Z_o = \left(\frac{60}{\sqrt{\varepsilon_r}}\right) Ln\left(\frac{1.9\,B}{0.8W + T}\right)$$

$$Z_o = \left(\frac{60}{\sqrt{4.6}}\right) Ln\left(\frac{1.9 \times 20}{0.8(6) + 1.4}\right) = 50.7\ \Omega$$

$$t_{pd} = 1.017\sqrt{\varepsilon_r} = 2.18 \text{ ns/ft} \quad (0.182 \text{ ns/in.})$$

B. Analyze capacitive loading.

Calculate C_d, distributed capacitance (total input capacitance divided by length).

$$C_d = 6 * C_d / \text{trace length} = (6 * 12 \text{ pF}) / 10 \text{ in.} = 7.2 \text{ pF/in.}$$

Calculate intrinsic capacitance of the trace.

$$C_o = 1000\,(t_{pd} / Z_o) = 1000\,(0.182/50.7) = 3.58 \text{ pF/in.} \quad (43.0 \text{ pF/ft})$$

Calculate one-way propagation delay time from the source driver.

$$t'_{pd} = 0.182\sqrt{1 + 7.2 / 3.58} = 0.32 \text{ ns/in.} \ (3.79 \text{ ns/ft})$$

C. Perform transmission line analysis.

The important condition of interest is $(2 * t'_{pd}) *$ trace length $\leq t_r$ or t_f.

$$(2 * t'_{pd}) * \text{trace length} = (2 * 0.32 \text{ ns/in.}) * 10 \text{ in.} = 6.4 \text{ ns}$$

Since the edge rate of the component $t_r = t_f = 2$ ns, and propagation delay (6.4 ≥ 2), termination is required to absorb transmission line effects.

Assume the trace is routed microstrip. Is termination required?

From above:

$$t_{pd} = 1.017 \times \sqrt{0.475\,\varepsilon_r + 0.67} = 0.14 \text{ ns/in.} \ (1.72 \text{ ns/ft})$$

$$C_o = 1000\,(t_{pd}/Z_o) = 1000\,(0.14/50.7) = 2.76 \text{ pF/in.} \ (33 \text{ pF/ft})$$

C_d is the same as above (7.2 pF/in.)

$$t'_{pd} = t_{pd}\sqrt{1 + C_d / C_o} = 0.26 \text{ ns/in. } (3.19 \text{ ns/ft})$$

$$2 \times t'_{pd} \times \text{trace length} = 2 \times 0.26 \text{ ns/ft} \times 10 \text{ in.} = 5.20 \text{ ns}$$

Again, this trace would require termination since 5.20 ns ≥ 2 ns.

7.4 LOADING DUE TO DISCONTINUITIES

Depending on the routed configuration of a net along with component placement, the effects of a transmission line discontinuity must be examined. For a discontinuity to exist, a finite distance is required between source and load as well as the time of propagation across the distance interval with respect to edge times. This environment includes the difference between both a lumped and a distributed capacitive loaded transmission environment. This difference is dependent on the spacing at which the loads start to affect each other with a dependency of edge time of the signal [8]. The return path discontinuities also need to be considered. If a trace switches routing layers internal to the PCB, impedance control may be disrupted.

The load separation distance interval defines the point where reflections from one load on a transmission line starts to affect adjacent loads.

Within a PCB, logic input has an effective input capacitance associated with it. In a transmission line structure, a point discontinuity occurs whenever a capacitive load is provided. Each discontinuity will allow the propagated signal to pass down the line with a small portion of the signal reflected back toward the source. If the reflected signal is large, signal integrity concerns exist, including reflections and crosstalk. The width of the reflected pulse is a function of the edge transition of the incident pulse.

For a noticeable effect to be observed by point discontinuities, there must be a finite amount of distance separation. We identify this unit of separation as l_{sep} between adjacent loads. If the distance, l_{sep} (propagation time) is small with respect to edge times, the reflected pulses will not add together or combine into one large discontinuity, which may be measured with use of a TDR.

To calculate l_{sep} between two points, consider the reflected pulse width. This pulse width is directly equal to the propagation time between points A and B. Using knowledge of an electrically long trace which includes round-trip propagation delay (source-to-load and return path from load-to-source), use Eq. (7.9), based on Fig. 7.8 [8].

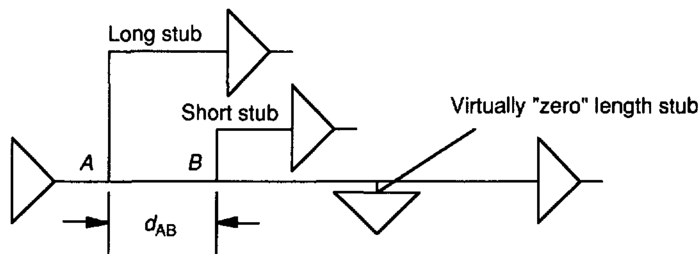


Figure 7.8 Point discontinuities and distance separation.

$$\gamma = 2 * d_{AB} * t_{pd} = 1.7 * t_r \tag{7.9}$$

where γ = width of the reflected pulse from A
d_{AB} = distance between points A and B
t_{pd} = unloaded propagation delay of the transmission line
t_r = 10%–90% edge transition rate (rise time)

Solving for d_{AB}, calculate minimum distance separation before a point discontinuity is observed.

$$d_{AB} = (1.7 * t_r)/(2 * t_{pd}) = 0.85\ t_r/t_{pd} \tag{7.10}$$

Assume an edge transition time of 0.8 ns (typical of a high-speed edge rate component) and FR-4 material. If a trace is routed stripline, with a dielectric constant 4.2, ($t_{pd} = 1.017\sqrt{4.2} = 2.08$ ns/ft or 0.17 ns/in.). The distance between two points acceptable before point discontinuity affects the signal is

$$d_{AB} = (1.7 * 0.8\text{ns}) / (2 * 0.17\ \text{ns/in.}) = 4.0\ \text{in.}\ (10.2\ \text{cm}) \tag{7.11}$$

The above example illustrates that if there are to be no point discontinuities, or a reflected pulse, the distance separation between points A and B must be less than 4.0 in., actual routed length.

What is meant by the term *reflected pulse?* A reflected pulse is a combination of two pulses as shown in Fig. 7.9. When there is a combination of multiple reflected signals, a single pulse effect will be observed within the circuit. If two pulses are allowed to overlap each other within the minimum distance separation, the maximum overlap of the two pulses will be less than the maximum amplitude of either pulse. This occurs when the pulse reaches a maximum amplitude and width. One-half of the pulse overlaps with another identical pulse at its halfway point. With this situation, distance separation can be reduced without affecting signal content.

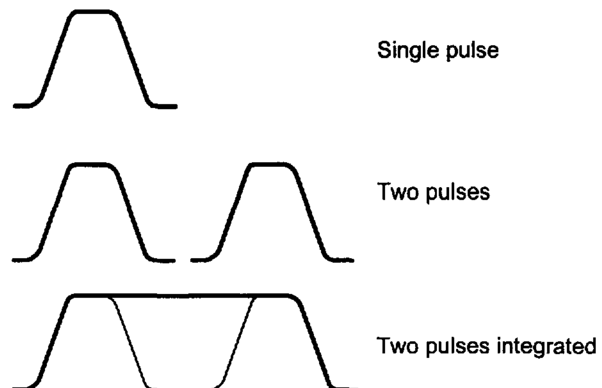


Figure 7.9 Reflected pulses from point discontinuities.

7.5 RF CURRENT DISTRIBUTION

A 0V reference plane allows RF current to return to its source from a load. This 0V plane completes the closed-loop circuit requirements discussed in Chapter 2. Current distribution along microstrip traces tends to spread out within the ground plane structure as illustrated in Fig. 7.10. This distribution will always exist in both the forward direction and the return path. This current distribution will share a common impedance between the trace and plane (or trace-to-trace), which results in mutual coupling due to the current spread. The peak current density lies directly beneath the trace and falls off sharply from each side of the trace into the ground plane structure.

When the distance spacing is far apart between trace and plane, the loop area between the forward and return path increases. This return path increase raises the inductance of the circuit where inductance is proportional to loop area. Equation (7.12) describes the current distribution that is optimum for minimizing total loop inductance for both the forward and return current path. The current that is described in Eq. (7.12) also minimizes the total amount of energy stored in the magnetic field surrounding the signal trace [3].

$$I(d) = \frac{I_o}{\pi H} \cdot \frac{1}{1 + \left(\frac{D}{H}\right)^2} \tag{7.12}$$

where $i(d)$ = signal current density (A/in.)
I_o = total current (A)
H = height of the trace above the ground plane (inches)
D = perpendicular distance from the centerline of the trace (inches)

The mutual coupling factor is highly dependent on frequency of operation and the skin depth effect of the ground plane impedance. As the skin depth increases, the resistive component of the ground plane impedance will also increase. This increase will be observed with proportionality at relatively high frequencies [2, 14].

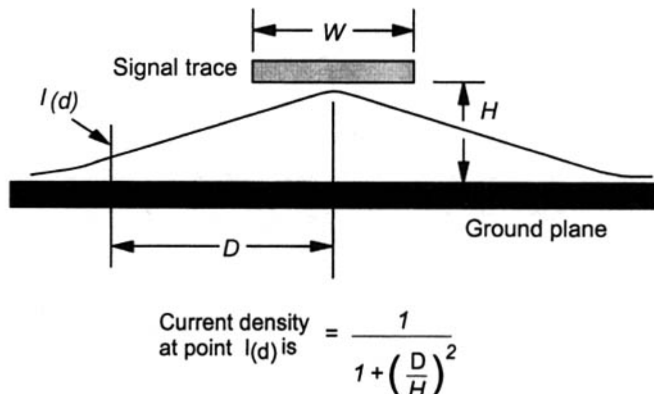


Figure 7.10 Current density distribution from trace to reference plane.

7.6 CROSSTALK

Crosstalk is one of several important aspects of a PCB design that must be considered during any design cycle. *Crosstalk* refers to the unintended electromagnetic coupling between traces, wires, trace-to-wire, cable assemblies, components, and any other electrical component subject to electromagnetic field disturbance. Crosstalk is caused by currents and voltages in a network and is similar to antenna coupling. When coupling occurs, near-field effects are observed.

Crosstalk between wires, cables, and traces affects intrasystem performance [2]. Intrasystem refers to both source and receptor being located within the same system or assembly. A product must be designed to be self-compatible. Hence, crosstalk may be identified as EMI internal to a system that must be minimized or eliminated. Crosstalk is an undesirable feature usually associated not only with clock or periodic signals, but also with data, address, control, and I/O traces.

Crosstalk is generally considered to be a functionality concern (signal quality) by causing a disturbance between traces. In reality, crosstalk can be a major contributor in the propagation of EMI. High-speed traces, analog circuits, and other high-threat signals may be corrupted by crosstalk induced from external sources. These EMI sensitive circuits may, however, also unintentionally couple their RF energy to the I/O section. This I/O coupling can result in radiated or conducted EMI that may be present within the enclosure or cause functionality problems between circuits and subsystems.

For crosstalk to occur, typically three or more conductors are required. These three conductors are identified in Fig. 7.11. Two lines carry the signal of interest, and the third line is a reference conductor which gives the circuits the ability to talk (communicate) to each other by capacitive or inductive coupling. If a two-wire system is provided, one wire pair is usually at a reference potential, while the other is differential, which prevents crosstalk from naturally occurring [2].

Figure 7.11 illustrates coupling between two circuits due to the result of a nonzero impedance in the mutual ground reference structure. This impedance is a prime reason why it is important to keep a low impedance between connecting points at 0V reference or ground.

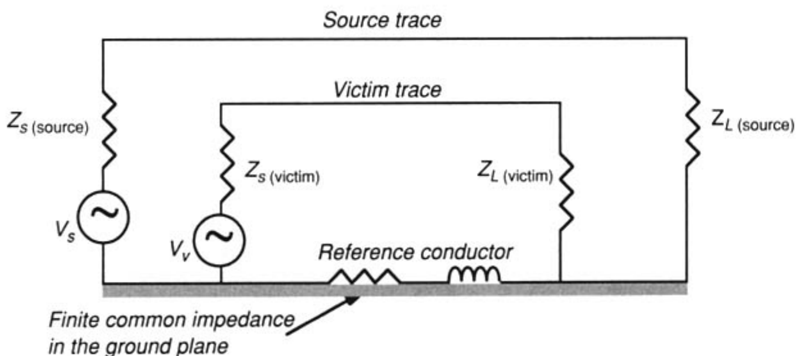
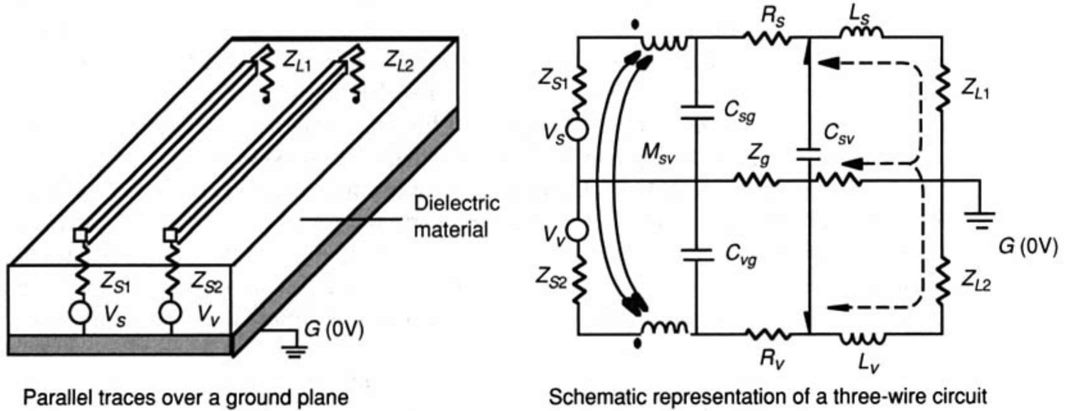


Figure 7.11 Three-conductor representation of a transmission line illustrating crosstalk.

Another visual representation of trace-to-trace coupling with capacitive and inductive components within a PCB trace is shown in Fig. 7.12. This is a detailed schematic of what occurs in a three-wire configuration. There are two parallel traces with mutual coupling mechanisms. The coupling on the source trace occurs through the common ground impedance, Z_g, the mutual capacitance between the traces, C_{sv}, and the mutual inductance M_{sv} between traces. Capacitive coupling between a trace and a reference plane is identified as C_{sg} (source-ground) and C_{vg} (victim-ground).

Crosstalk evaluation requires frequency domain analysis. What occurs in a logic circuit is both capacitive and inductive coupling of an electromagnetic field that interacts with other circuits. In Fig. 7.11, V_s is the source that generates an electromagnetic field that interacts between source and victim circuit, or trace. This interaction induces current and voltages at the input terminals of the termination point Z_s and Z_L. This termination is attached to the source and load ends of the circuit, respectively. The designer's responsibility is to determine if the crosstalk is near end (Z_s) or far end (Z_L). Near end refers to the



C_{sv} = Capacitance between source trace and victim trace
C_{vg} = Capacitance between victim trace and ground
C_{sg} = Capacitance between source trace and ground

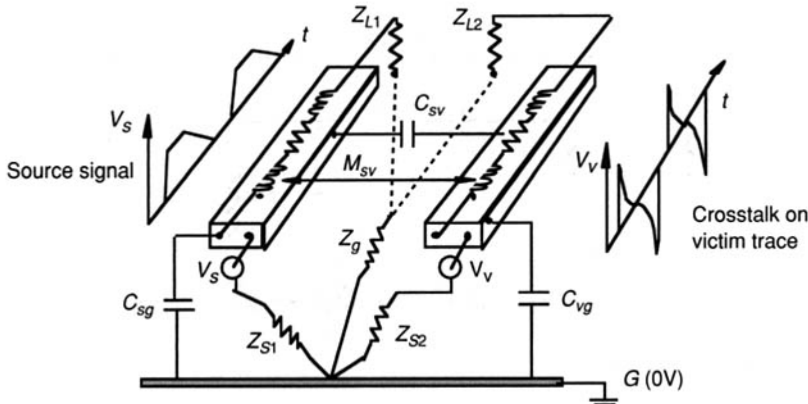


Figure 7.12 Trace-to-trace coupling within a PCB structure.

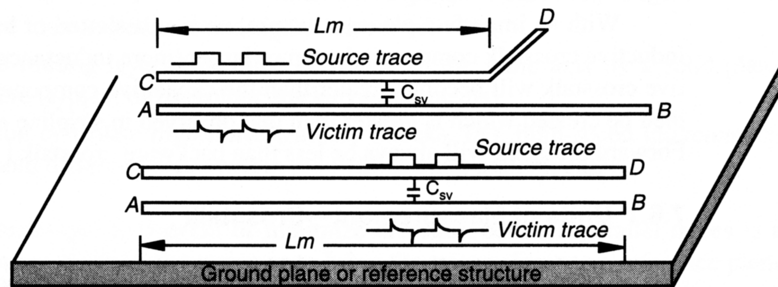
point of the circuit that is identified as source. Far end is the point identified as the load side of the circuit.

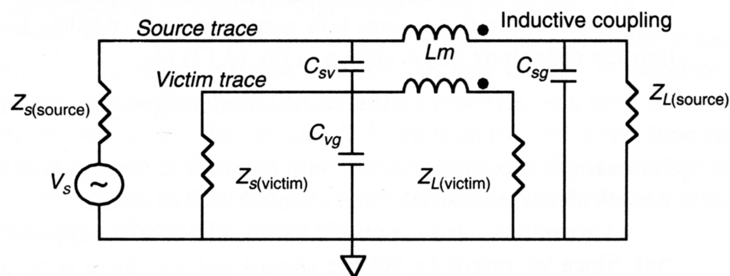
Time domain crosstalk analysis determines the time form of the receptor's terminal voltages, whereas frequency domain crosstalk analysis determines the magnitude and phase of the receptor voltages for a sinusoidal source voltage (electromagnetic field) [2]. This discussion examines only frequency domain analysis.

Crosstalk involves capacitive and inductive coupling. Capacitive coupling usually results from traces lying one on top of the other or above a reference plane. This coupling is a direct function of the distance spacing between the trace and an overlap area. The discussion on RF current distribution in the previous section illustrates the field density that occurs between a trace and reference plane. Coupled signals may exceed design limits with a very short trace route. This coupling may also be so severe that overlapping parallelism should be avoided at all times.

Inductive crosstalk involves traces that are physically located in close proximity to each other. With parallel routed traces, two forms of crosstalk will be observed, forward and backward. In a PCB, backward crosstalk is considered to be a greater concern than forward crosstalk. The high impedance in the circuit between source and victim trace will produce a high level of crosstalk. The preferred method for preventing crosstalk must be implemented during routing of the traces, or their physical location relative to a cable, I/O interconnect, and similar circuits subject to corruption. Inductive crosstalk can be controlled by increasing trace edge-to-edge separation between offending transmission lines or wires, or by minimizing the height separation distance of the trace above the reference plane.

Capacitive and inductive coupling are shown in Fig. 7.13. If a signal is sent from source-to-load, trace *C-D*, the signal will capacitively couple to the adjacent line, trace





$$Z_v = \frac{Z_s(v) \times Z_L(v)}{Z_s(v) + Z_L(v)}$$

C_{sv} = Capacitance between source trace and victim trace
C_{vg} = Capacitance between victim trace and ground
C_{sg} = Capacitance between source trace and ground

Figure 7.13 Fundamental representation of crosstalk.

A-B, only if the two lines are parallel to each other and in close proximity. The larger the capacitance between the two traces (mutual capacitance), the tighter the coupling that occurs with crosstalk energy transferred between the two. The coupled voltage on the victim trace, *A-B*, causes a current to flow from the "coupling point" toward both ends of the trace. The current going back toward the source, *A*, is backward crosstalk, whereas the signal traveling to the load, *B*, is forward crosstalk. The two traces also have mutual inductance between them, causing inductive coupling, L_m, of the current in the direction of backward crosstalk. If the output impedance of the driver, *A*, is normally low compared to the transmission line impedance, most of the backward crosstalk is reflected back toward the driver, *A*. Because a capacitor conducts RF energy (current) efficiently at high frequencies, the faster the edge rate, the greater the crosstalk.

The polarities for mutual capacitive coupling are positive for forward and negative for backward. This is the only difference in behavior from that of inductive interference spikes; otherwise, both coupling modes are essentially identical. This coupling spreads out over a period of $2t_p$ where t_p is the time period for signal transmission round-trip.

Backward crosstalk increases linearly with the coupled length. If the coupled length is electrically long, with respect to propagation delay of the round-trip signal, backward crosstalk will show a saturated value and not increase as the coupled length increases.

Under typical operating conditions when a contiguous ground plane is provided, both inductive and capacitive crosstalk coupling voltages approximate the same result. Forward crosstalk cancels while backward crosstalk reinforces. Stripline topology provides a balance between both inductive and capacitive coupling since forward-coupling coefficients are small. Microstrip allows the electric fields generated to partially radiate through free space instead of only through the dielectric material of the PCB. Although less capacitive coupling exists, this coupling can still be present which leads to a small negative forward coupling coefficient.

With an imperfect planar structure, such as a slotted or hashed reference plane, the inductive crosstalk component becomes larger (more inductance in the plane). This inductive crosstalk will become greater than the capacitive component. Forward crosstalk will then be created which is greater than that observed in stripline and is negative in polarity. Forward crosstalk will always be less than backward crosstalk [14].

7.6.1 Units of Measurement—Crosstalk

Crosstalk is measured in units of dB because the reference level is not an absolute power level. The reference is 90 dB loss from the interfering circuit to the victim circuit. As a result, this unit measures how much crosstalk coupling loss is above 90 dB. The relationship describing this is shown in Eq. (7.13) [4].

$$\text{dB} = 90\text{-(crosstalk coupling loss in dB)} \tag{7.13}$$

For example, circuit A couples with circuit B. Circuit A is at a 58 dB lower power level. We calculate the crosstalk from circuit A to B as 32 dB.

Crosstalk is also expressed by Eq. (7.14) when applied to a source and victim circuit. Since we reference voltage against voltage, there is no unit of measurement except that of the basic dB.

$$X_{\text{talk(dB)}} = 20 \log \frac{V_{\text{victim}}}{V_{\text{source}}} \tag{7.14}$$

7.6.2 Design Techniques to Prevent Crosstalk

To prevent crosstalk within a PCB, design and layout techniques listed here are useful within a PCB.

Crosstalk will sometimes increase with a wider trace width. This is not true if the separation distance is held constant as a result of the ratio of self and mutual capacitance being held at a fixed ratio value. If the ratio is not fixed, mutual capacitance, C_m, will increase. With parallel traces, the longer the trace, the greater the mutual inductance, L_m. An increase in impedance, along with mutual capacitance, will increase with faster rise times of a signal transition, thus exacerbating crosstalk. The design and layout techniques are as follows.

1. Group logic families according to functionality. Keep the bus structure tightly controlled.
2. Minimize physical distance between components.
3. Minimize parallel routed trace lengths.
4. Locate components away from I/O interconnects and other areas susceptible to data corruption and coupling.
5. Provide proper terminations on impedance-controlled traces, or traces rich in harmonic energy.
6. Avoid routing of traces parallel to each other. Provide sufficient separation between traces to minimize inductive coupling.
7. Route adjacent layers (microstrip or stripline) orthogonally. This prevents capacitive coupling between the planes.
8. Reduce signal-to-ground reference distance separation.
9. Reduce trace impedance and signal drive level.
10. Isolate routing layers that must be routed in the same axis by a solid planar structure (typical of backplane stackup assignments).
11. Partition or isolate high noise emitters (clocks, I/O, high-speed interconnects, etc.) onto different layers within the PCB stackup assignment.

The best technique to prevent or minimize crosstalk between parallel traces is to maximize separation between the traces or to bring the traces closer to a reference plane. These techniques are preferred for long clock signals and high-speed parallel bus structures. An illustration of various crosstalk configuration is shown in Fig. 7.14.

Because of the current density distribution described in Eq. (7.12), the associated local magnetic field strength drops off with distance. An easy method to calculate trace separation is to use Eq. (7.15). This equation expresses crosstalk as a ratio of measured noise voltage to the driving signal. The constant K depends on the circuit rise time and the length of the interfering traces. This value is always less than one. For most approximations, the value of one is generally used. This equation clearly shows that to minimize crosstalk, we must minimize H and maximize D [3].

$$\text{Crosstalk} \approx \frac{K}{1 + \left(\dfrac{D}{H}\right)^2} = \frac{K(H)^2}{H^2 + D^2} \tag{7.15}$$

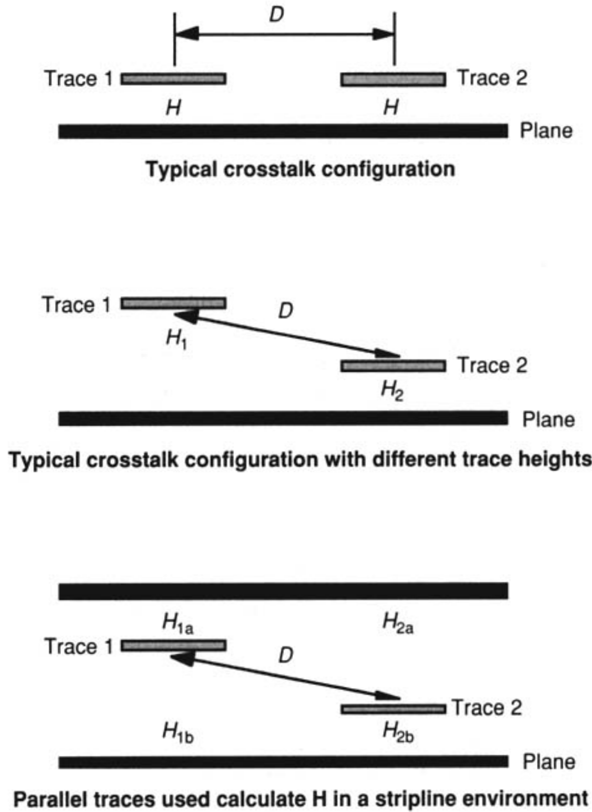


Figure 7.14 Calculating crosstalk separation.

For embedded microstrip, if the parallel traces are at different heights, the H^2 term becomes the product of the two heights as shown in Fig. 7.14 and Eq. (7.16). The dimension D becomes the direct distance between the centerline of the traces [3].

$$\text{Crosstalk} \approx \frac{1}{1 + \left(\dfrac{D}{H1 * H2}\right)} \tag{7.16}$$

If the traces are routed stripline between two reference planes, determine H using a parallel combination of heights to each plane, detailed in Eq. (7.17).

$$H_{\text{total}} = \frac{Hna * Hnb}{Hna + Hnb} \tag{7.17}$$

We can also determine the distance spacing for microstrip traces for eliminating crosstalk by using Table 7.2. When using Table 7.2, special notes are required.

1. PCB trace: $Z_L = 50\ \Omega$ (Z_s & $Z_L = 100\ \Omega$ in parallel) and 1-cm length.
2. Z_s and Z_L are real, not complex values.

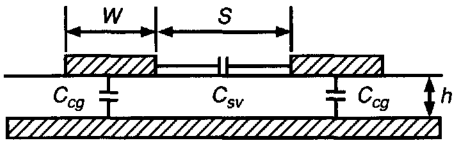


TABLE 7.2 Capacitive Crosstalk Coupling Distance Spacing

	$W/h = 3$ ($C_{cg} \approx 1.2$ pF/cm) $Z_o = 50\ \Omega$				$W/h = 1$ ($C_{cg} \approx 0.5$ pF/cm) $Z_o = 90\ \Omega$				$W/h = 0.3$ ($C_{cg} \approx 0.1$ pF/cm) $Z_o = 120\ \Omega$			
S/W (C_{sv}, pF/cm)	10 (0.003)	3 (0.02)	1 (0.06)	0.3 (0.17)	10 (0.003)	3 (0.02)	1 (0.06)	0.3 (0.17)	10 (0.003)	3 (0.02)	1 (0.06)	0.3 (0.17)
$F(\omega) = 1$ kHz	−174	−158	−148	−140	−158	−148	−142	−136	−146	−134	−130	−122
3 kHz	−164	−148	−138	−130	−148	−138	−132	−126	−136	−124	−120	−112
10 kHz	−154	−138	−128	−120	−138	−128	−122	−116	−126	−114	−110	−102
30 kHz	−144	−128	−118	−110	−128	−118	−112	−106	−116	−104	−100	−92
100 kHz	−134	−118	−108	−100	−118	−108	−102	−96	−106	−94	−90	−82
300 kHz	−124	−108	−98	−90	−108	−98	−92	−86	−96	−84	−80	−72
1 MHz	−114	−98	−88	−80	−98	−88	−82	−76	−86	−74	−70	−62
3 MHz	−104	−88	−78	−70	−88	−78	−72	−66	−76	−64	−60	−52
10 MHz	−94	−78	−68	−60	−78	−68	−62	−56	−66	−54	−50	−42
30 MHz	−84	−68	−58	−50	−68	−58	−52	−46	−56	−44	−40	−32
100 MHz	−74	−58	−48	−40	−58	−48	−42	−36	−46	−34	−30	−22
300 MHz	−64	−48	−38	−30	−48	−38	−32	−26	−36	−24	−20	−12
1 GHz	−56	−40	−30	−22	−38	−30	−22	−18	−28	−18	−14	−8
3 GHz	−52	−36	−26	−20	−32	−24	−18	−14	−24	−14	−10	−4
10 GHz	−52	−36	−26	−18	−30	−22	−16	−10	−24	−14	−10	−4

$$\text{Crosstalk} = 20 \log \frac{R_v (C_{sv})\, \omega}{\sqrt{[R_{v\omega}(C_{cg} + C_{sv})]^2 + 1}}$$

where R_v = impedance of victim trace (table uses 100 Ω)
C_{sv} = capacitance between source and victim trace
C_{cg} = capacitance between trace and ground
ω = frequency

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3. Crosstalk given per cm of parallel trace run. For other lengths, an approximate correction of 20 log (f_{cm}) may be added, with f_{cm} as parallel trace length in cm. This correction is applicable for frequencies up to 1 GHz.
4. For other lengths and Z_v (impedance of the victim trace), apply the correction factor: $20 \log[(Z_v \bullet l)/100]$ where l is the length of the trace.
5. Clamp at –4 dB for no ground plane.
   –10 dB for $W/h = 1$
   +4 dB for buried traces
6. If Z_s and $Z_L <> 100\ \Omega$, add 20 log $(Z_v/50)$, with $Z_v = \dfrac{Z_s Z_L}{Z_s + Z_L}$.

7.7 THE 3-W RULE

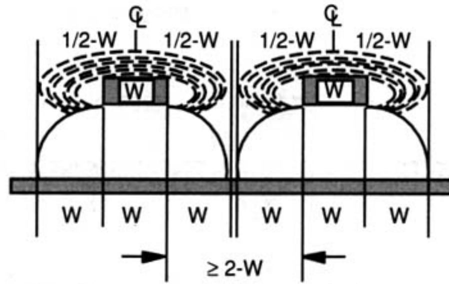
Crosstalk can exist between traces on a PCB. This undesirable effect is associated not only with clock or periodic signals, but also with other system critical nets. Data, address, control lines, and I/O all are affected by crosstalk and coupling. Clocks and periodic signals create the majority of problems and can cause functionality problems with other functional sections. Use of the *3-W* rule will allow a designer to comply with PCB layout criteria without having to implement other design techniques. This design technique takes up physical real estate and may make routing more difficult.

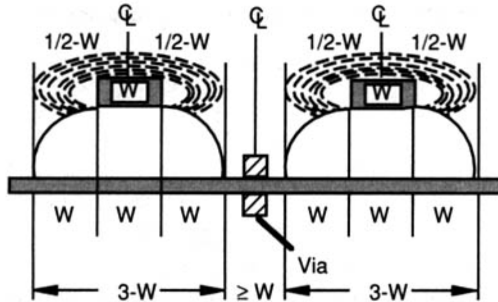
The basis for use of the *3-W* rule is to minimize coupling between traces. This rule states that *the distance separation between traces must be three times the width of a single trace, measured from centerline to centerline.* Otherwise stated, *the distance separation between two traces must be greater than two times the width of a single trace.* For example, a clock line is 6 mils wide. No other trace can be routed within a minimum of 2*6 mils of this trace, or 12 mils, edge-to-edge. As observed, much real estate is lost in areas where trace isolation occurs. An example of the *3-W* rule is shown in Fig. 7.15 [1].

Note that the *3-W* rule represents the approximate 70% flux boundary at logic currents. For the approximate 98% boundary, *10-W* should be used.

Use of the *3-W* rule is mandatory for *only* high-threat signals such as clock traces, differential pairs, video, audio, the reset line, or other system critical nets. Not all traces on a PCB have to conform to *3-W* routing. Using this design guideline, before routing the PCB, it is important to determine which traces must be routed *3-W*.

As shown in the middle drawing of Fig. 7.15, a via is located between two traces. This via is usually associated with a third routed net and may contain a signal that is susceptible to electromagnetic disruption. For example, the reset line, a video or audio trace, an analog level control trace, or an I/O interface may pick up electromagnetic energy, either inductively or capacitively. To minimize crosstalk corruption to the via, the distance spacing between adjacent traces must include the angular diameter and clearance of the via. The same requirement exists for this distance spacing between a routed trace rich in RF spectral energy that may couple a component's breakout pin (pin escape) to this routed trace.





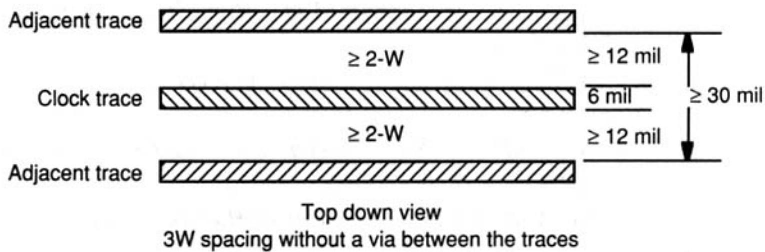


Figure 7.15 Designing with the 3-W rule.

Use of the *3-W* rule should not be restricted to only clock or periodic signal traces; differential pairs (balanced, ECL, and similar sensitive nets) are also prime candidates for *3-W*. The distance between paired traces must be *1-W* for differential traces. For differential traces, power plane noise and single-ended signals can capacitively (or inductively) couple into the paired traces. This can cause data corruption if those traces not associated with the differential pair are physically closer than *3-W*.

An example of routing differential pair traces within a PCB structure is shown in Fig. 7.16 [1].

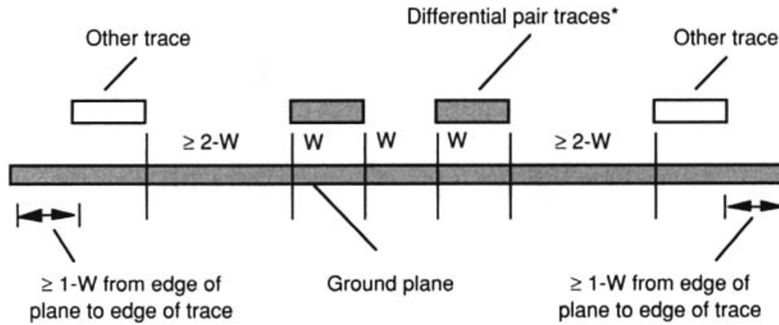


Figure 7.16 Parallel differential pair routing and the 3-W rule.

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